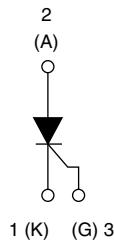
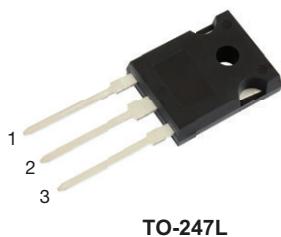


Thyristor High Voltage, Phase Control SCR, 50 A



PRODUCT SUMMARY	
Package	TO-247L
$I_T(AV)$	50 A
V_{DRM}/V_{RRM}	1200 V
V_T (typ.)	1.1 V
I_{GT} (typ.)	40 mA
T_J max.	150 °C
Diode variation	Single SCR

FEATURES

- Designed and qualified according to JEDEC®-JESD 47
- 150 °C maximum operating junction temperature
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

Typical usage is in input rectification crowbar (soft start) and AC switch motor control, UPS, welding, and battery charge.

DESCRIPTION

The VS-50TPS12 high voltage series of silicon controlled rectifiers are specifically designed for medium power switching, and phase control applications. The glass passivation technology used, has reliable operation up to 150 °C junction temperature.

MAJOR RATINGS AND CHARACTERISTICS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Peak repetitive reverse voltage	V_{RRM}/V_{DRM}		1200	V
On-state voltage	V_T	50 A, $T_J = 125$ °C	1.1	
Average rectified forward current	$I_T(AV)$		50	A
Maximum continuous RMS on-state current	I_{RMS}		79	
Non-repetitive peak surge current	I_{TSM}		630	
Maximum rate of rise	dV/dt		1000	V/μs
Operating junction and storage temperature range	T_J, T_{Stg}		-40 to +150	°C

VOLTAGE RATINGS			
PART NUMBER	V_{RRM}/V_{DRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM}/I_{DRM} AT 125 °C mA
VS-50TPS12L-M3	1200	1300	10

ABSOLUTE MAXIMUM RATINGS									
PARAMETER	SYMBOL	TEST CONDITIONS			TYP.	MAX.	UNITS		
Maximum average on-state current	$I_{T(AV)}$	$T_J = 112^\circ\text{C}$, 180° conduction half sine wave			-	50	A		
Maximum continuous RMS on-state current as AC switch	$I_{T(RMS)}$				-	79			
Peak, one-cycle non-repetitive surge current	I_{TSM}	10 ms sine pulse, rated V_{RRM} applied		Initial $T_J = T_J$ maximum		530	A		
		10 ms sine pulse, no voltage reapplied				630			
I^2t for fusing	I^2t	10 ms sine pulse, rated V_{RRM} applied				1405	A^2s		
		10 ms sine pulse, no voltage reapplied				1986			
$I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	$t = 0.1 \text{ ms to } 10 \text{ ms}$, no voltage reapplied, $T_J = 125^\circ\text{C}$			-	19 850	$\text{A}^2\sqrt{\text{s}}$		
Low level value of threshold voltage	$V_{T(TO)1}$	$T_J = 125^\circ\text{C}$			-	0.83	V		
High level value of threshold voltage	$V_{T(TO)2}$				-	0.95			
Low level value of on-state slope resistance	r_{t1}				-	0.58	$\text{m}\Omega$		
High level value of on-state slope resistance	r_{t2}				-	0.51			
On-state voltage	V_T	$50 \text{ A}, T_J = 25^\circ\text{C}$			1.2	1.32	V		
		$100 \text{ A}, T_J = 25^\circ\text{C}$			1.4	1.6			
Rate of rise of turned-on current	dI/dt	$T_J = 25^\circ\text{C}$			-	150	$\text{A}/\mu\text{s}$		
Holding current	I_H	Anode supply = 6 V, resistive load, $T_J = 25^\circ\text{C}$			-	300	mA		
Latching current	I_L				-	350			
Reverse and direct leakage current	I_{RRM}/I_{DRM}	$T_J = 25^\circ\text{C}$			-	0.05			
		$T_J = 125^\circ\text{C}$			-	10			
Rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to 80 % V_{DRM} , $R_g-k = \infty \Omega$			-	1000	$\text{V}/\mu\text{s}$		

TRIGGERING									
PARAMETER	SYMBOL	TEST CONDITIONS			TYP.	MAX.	UNITS		
Peak gate power	P_{GM}	10 ms sine pulse, no voltage reapplied			-	10	W		
Average gate power	$P_{G(AV)}$				-	2.5			
Peak gate current	I_{GM}				-	2.5	A		
Peak negative gate voltage	$-V_{GM}$				-	10	V		
Required DC gate voltage to trigger	V_{GT}	$T_J = -40^\circ\text{C}$		Anode supply = 6 V resistive load		1.6			
		$T_J = 25^\circ\text{C}$				1.5			
		$T_J = 150^\circ\text{C}$				1			
Required DC gate to trigger	I_{GT}	$T_J = -40^\circ\text{C}$		Anode supply = 6 V resistive load		160	mA		
		$T_J = 25^\circ\text{C}$				45			
		$T_J = 150^\circ\text{C}$				60			
DC gate voltage not to trigger	V_{GD}	$T_J = 150^\circ\text{C}$, V_{DRM} = rated value			-	0.2	V		
DC gate current not to trigger	I_{GD}				-	3	mA		

SWITCHING							
PARAMETER	SYMBOL	TEST CONDITIONS			TYP.	MAX.	UNITS
Turn-on time	t_{gt}	$I_T = 50 \text{ A}$, $V_D = 50\% V_{DRM}$, $I_{gt} = 300 \text{ mA}$, $T_J = 25^\circ\text{C}$			1.5	-	μs
Turn-off time	t_q				92	-	

THERMAL AND MECHANICAL SPECIFICATIONS							
PARAMETER	SYMBOL	TEST CONDITIONS			TYP.	MAX.	UNITS
Maximum junction and storage temperature range	T_J, T_{Stg}				-40	150	°C
Maximum thermal resistance, junction to case	R_{thJC}				-	0.35	°C/W
Maximum thermal resistance, junction to ambient	R_{thJA}				-	40	
Typical thermal resistance, case to heatsink	R_{thCS}	Mounting surface, smooth, and greased			0.2	-	kgf · cm (lbf · in)
Mounting torque	minimum				6 (5)	12 (10)	
	maximum				6 (5)	12 (10)	kgf · cm (lbf · in)
Marking device		Case style Super TO-247L			50TPS12L		

ΔR_{thJ-HS} CONDUCTION PER JUNCTION											
DEVICE	SINE HALF-WAVE CONDUCTION					RECTANGULAR WAVE CONDUCTION					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VS-50TPS12L-M3	0.143	0.166	0.208	0.299	0.490	0.099	0.168	0.223	0.311	0.494	°C/W

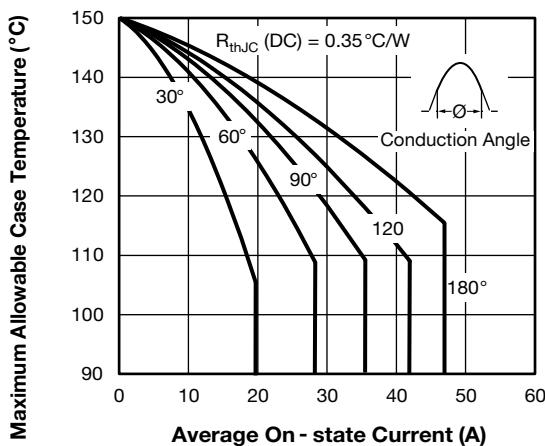


Fig. 1 - Current Rating Characteristics

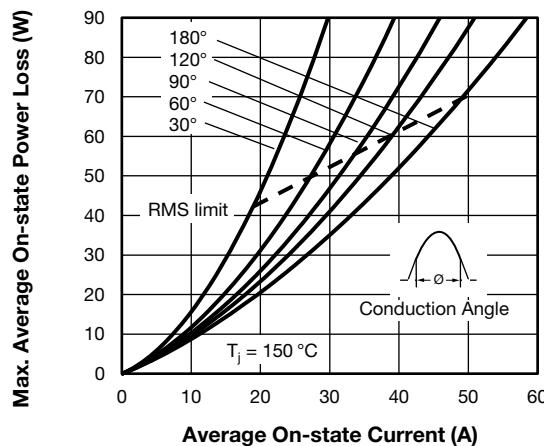


Fig. 3 - On-State Power Loss Characteristics

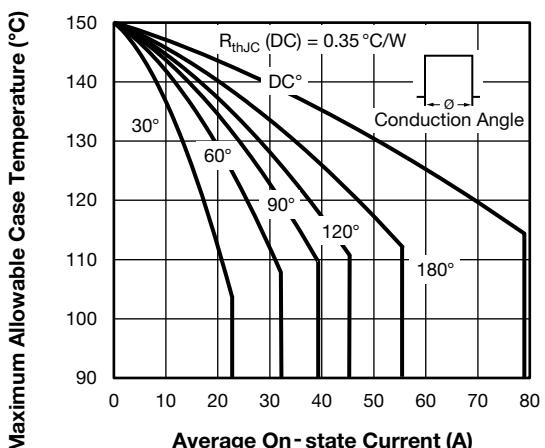


Fig. 2 - Current Rating Characteristics

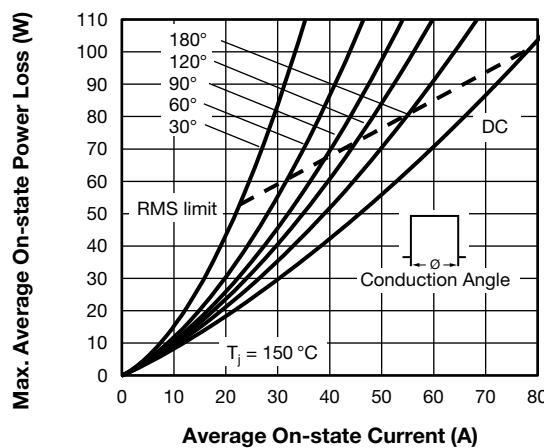


Fig. 4 - On-State Power Loss Characteristics

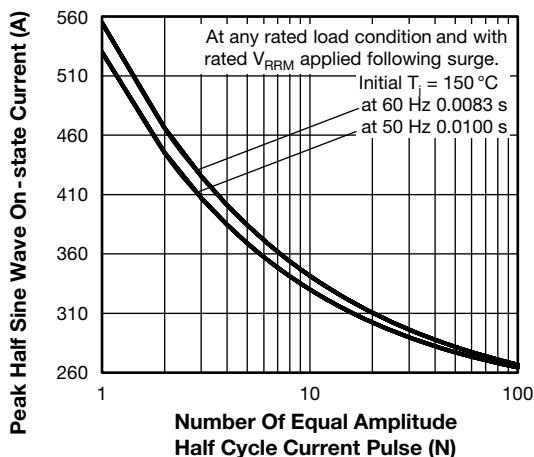


Fig. 5 - Maximum Non-Repetitive Surge Current

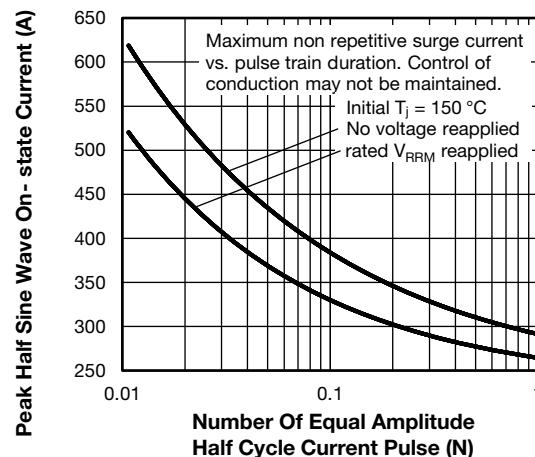


Fig. 6 - Maximum Non-Repetitive Surge Current

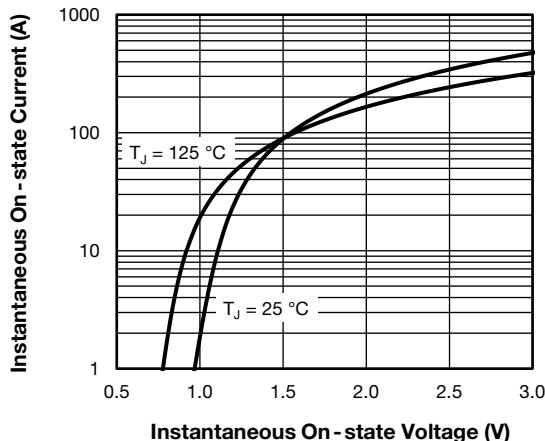


Fig. 7 - On-State Voltage Drop Characteristics

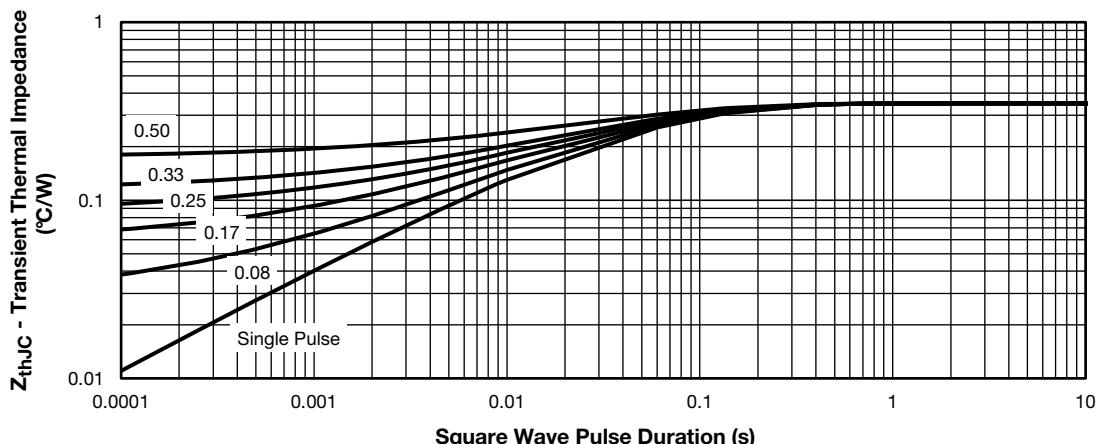
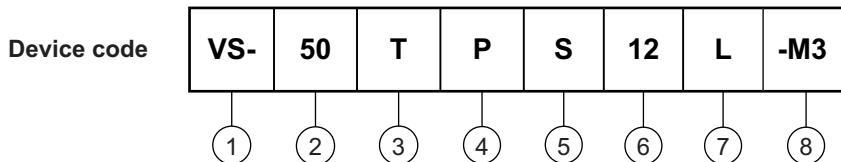


Fig. 8 - Gate Characteristics

ORDERING INFORMATION TABLE


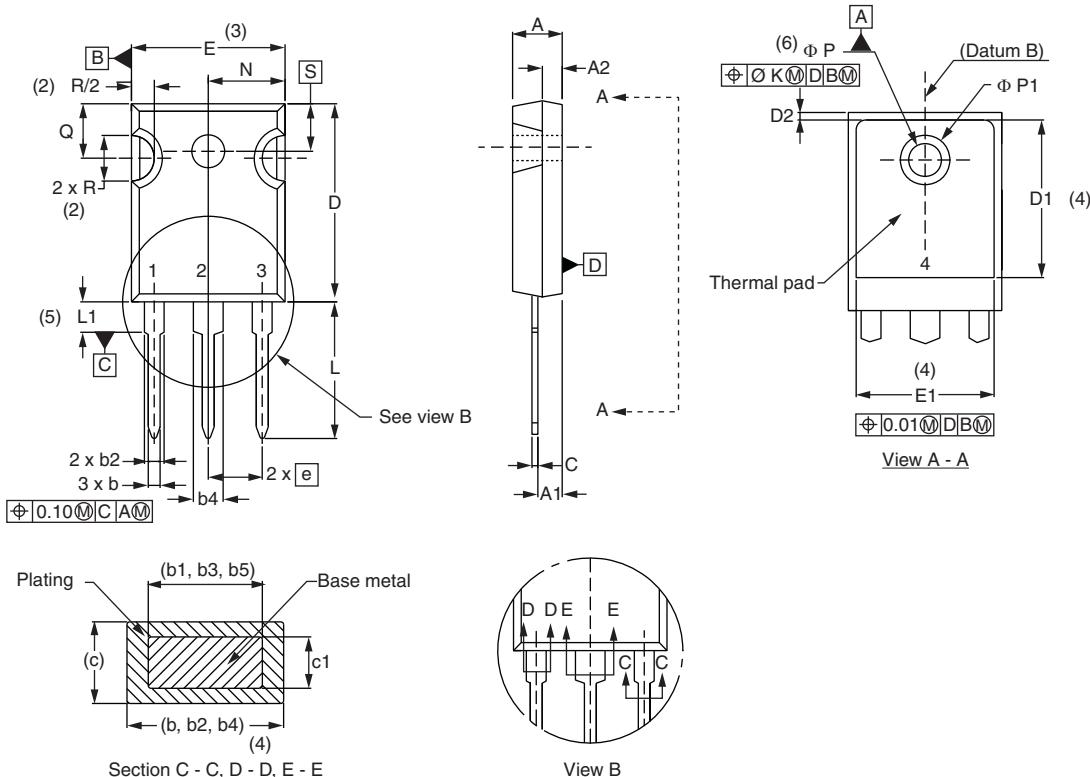
- (1)** - Vishay Semiconductors product
- (2)** - Current code (50 = 50 A)
- (3)** - Circuit configuration:
T = thyristor
- (4)** - P = TO-247 package
- (5)** - Type of silicon:
S = standard recovery rectifier
- (6)** - Voltage code (12 = 1200 V)
- (7)** - Package L = long lead
- (8)** - -M3 = halogen-free, RoHS-compliant, and terminations lead (Pb)-free

ORDERING INFORMATION (example)			
PREFERRED P/N	QUANTITY PER TUBE	MINIMUM ORDER QUANTITY	PACKAGING DESCRIPTION
VS-50TPS12L-M3	25	contact factory	Antistatic plastic tubes

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95626
Part marking information	www.vishay.com/doc?95007

TO-247L 3 Pins

DIMENSIONS in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES	View A-A	SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.				MIN.	MAX.	MIN.	MAX.	
A	4.65	5.31	0.183	0.209			D2	0.51	1.30	0.020	0.051	
A1	2.21	2.59	0.087	0.102			E	15.29	15.87	0.602	0.625	3
A2	1.50	2.49	0.059	0.098			E1	13.46	-	0.53	-	
b	0.99	1.40	0.039	0.055			e	5.46 BSC		0.215 BSC		
b1	0.99	1.35	0.039	0.053			Ø K	2.54		0.010		
b2	1.65	2.39	0.065	0.094			L	19.81	20.32	0.780	0.800	
b3	1.65	2.34	0.065	0.092			L1	3.71	4.29	0.146	0.169	
b4	2.59	3.43	0.102	0.135			N	7.62 BSC		0.3		
b5	2.59	3.38	0.102	0.133			Ø P	3.56	3.66	0.14	0.144	
c	0.38	0.89	0.015	0.035			Ø P1	-	6.98	-	0.275	
c1	0.38	0.84	0.015	0.033			Q	5.31	5.69	0.209	0.224	
D	19.71	20.70	0.776	0.815	3		R	4.52	5.49	0.178	0.216	
D1	13.08	-	0.515	-	4		S	5.51 BSC		0.217 BSC		

Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC® outline TO-247 with exception of dimension c and Q

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