W-LAN+Bluetooth Combo Module Data Sheet

Cypress Chipset CYW43012
for 802.11a/b/g/n,11ac-friendly + Bluetooth 5.0

Tentative P/N :LBEE59B1LV-TEMP

The revision history of the product specification

Revised No.	Revised Date	Note
-	2017.07.07	First Issue
A	2017.10.02	P4. Updated Block Diagram P6,8. Updated Pin Layout
B	2017.10.10	Cover. Added 11ac-friendly P4. Added 11ac-friendly on Scope
C	2018.04.04	P35. Added Reference circuit
D	2018.06.01	P10. Updated Supply voltage condition P25-31. Updated DC/RF characteristics
E	2018.08.02	P4. Updated Wright/MSL information P31-32. Updated BT output power spec P34 Updated Reference schematic(Added (*5)) P35 Added Tape and Reel packing information
F	2018.10.25	P4. Added “MAC/BD address are embedded P5. Updated Marking information P10. Updated VDDIO_SFL spec(8.OPERATING CONDITION) P13. Added digital I/O requirements BT/WL_REG_ON
G	2018.12.28	P33. Revised Reference circuit
H	2019.03.26	P5. Corrected Demotions(Added a5,c5)
I	2019.04.24	P40. Updated 18.PRECONDITION TO USE OUR PRODUCTS

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Please be aware that an important notice concerning availability, standard warranty and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.

1. SCOPE

This specification is applied to the IEEE802.11a/b/g/n,IEEE802.11ac-friendly*1) W-LAN + Bluetooth 5.0 combo module.

*1)IEEE 802.11ac full-compliance requires support for 40 MHz and 80 MHz channel bandwidths. CYW43012 only supports 20 MHz channel bandwidth however it supports 802.11ac's 256-QAM for the 20 MHz channels in the 5GHz band enabling it to offer higher throughput and lower energy per bit than 802.11n only products.

2. KEY FEATURE

- Cypress CYW43012 inside
- Compliant with IEEE802.11a/b/g/n, 11ac-friendly*1)
- Compliant with Bluetooth specification v5.0
- SDIO interface for W-LAN
- Interface support for Bluetooth is Host Controller Interface (HCI)
- Surface mount type 10.0 x 7.2 mm (Typical), H = 1.4 mm (Max)
- MAC/BD address are embedded
- Weight : 0.23g
- MSL : 3

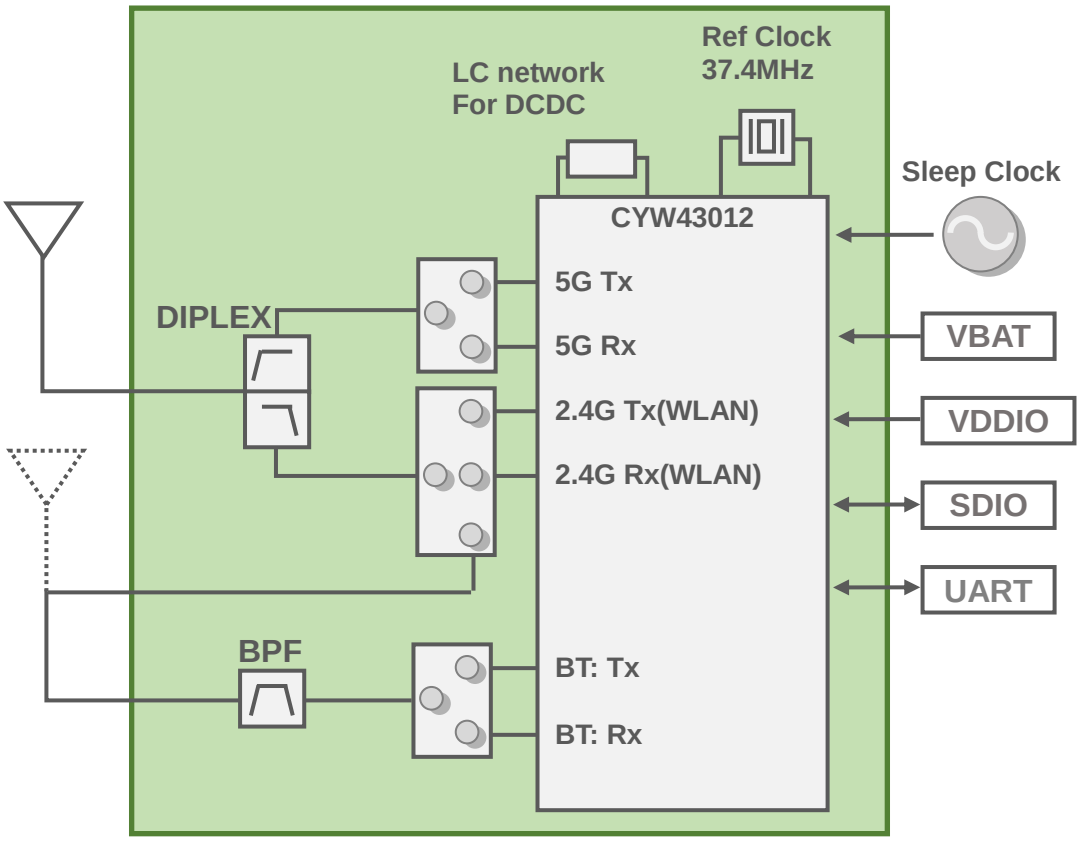
3. Part Number

Ordering Part Number	Description
LBEE59B1LV-TEMP	In case of sample order
LBEE59B1LV-TEMP-D	EVK

4. RoHS Compliance

This module is compliant with the RoHS directive.

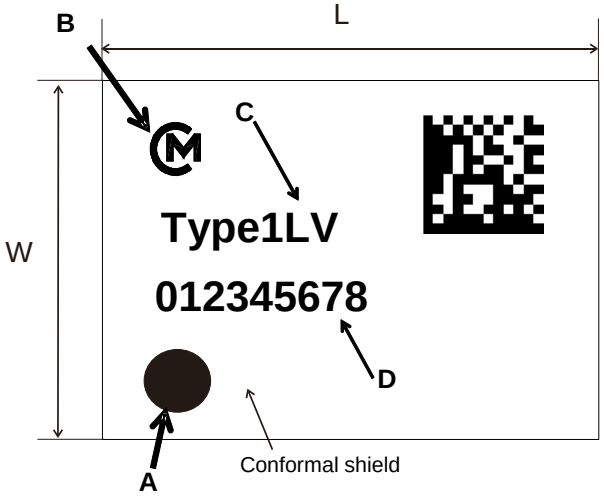
5. Block Diagram



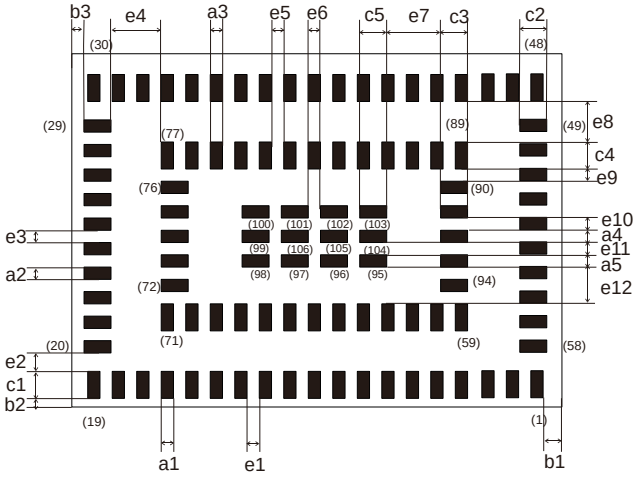
6. DIMENSIONS, MARKING AND TERMINAL CONFIGURATIONS

6.1. Dimensions

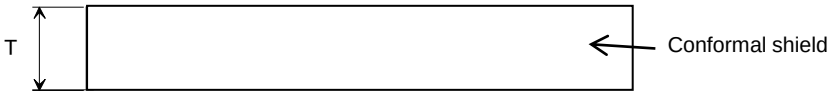
<TOP VIEW>



<BOTTOM VIEW>



<SIDE VIEW>

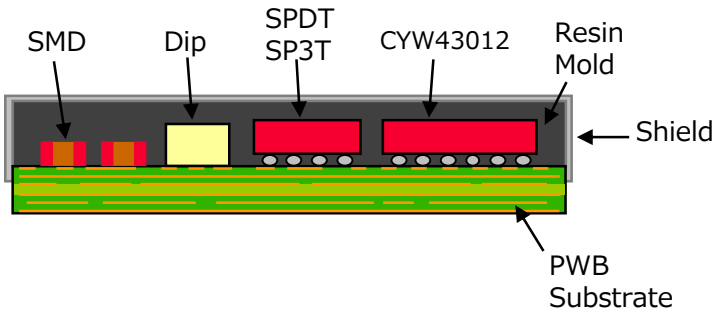


(unit : mm)

Mark	Dimensions	Mark	Dimensions	Mark	Dimensions
L	10.0 +/- 0.2	W	7.2 +/- 0.2	T	1.4max
a1	0.25+/- 0.1	a2	0.25 +/- 0.1	a3	0.25 +/- 0.1
a4	0.25 +/- 0.1	a5	0.25 +/- 0.1	b1	0.375 +/- 0.2
b2	0.30 +/- 0.2	b3	0.30 +/- 0.2	c1	0.55 +/- 0.1
c2	0.55 +/- 0.1	c3	0.55 +/- 0.1	c4	0.55 +/- 0.1
c5	0.55 +/- 0.1	e1	0.25 +/- 0.1	e2	0.375 +/- 0.1
e3	0.25 +/- 0.1	e4	1.025 +/- 0.1	e5	0.25 +/- 0.1
e6	0.25 +/- 0.1	e7	1.100 +/- 0.1	e8	0.825 +/- 0.1
e9	0.25 +/- 0.1	e10	0.25 +/- 0.1	e11	0.25 +/- 0.1

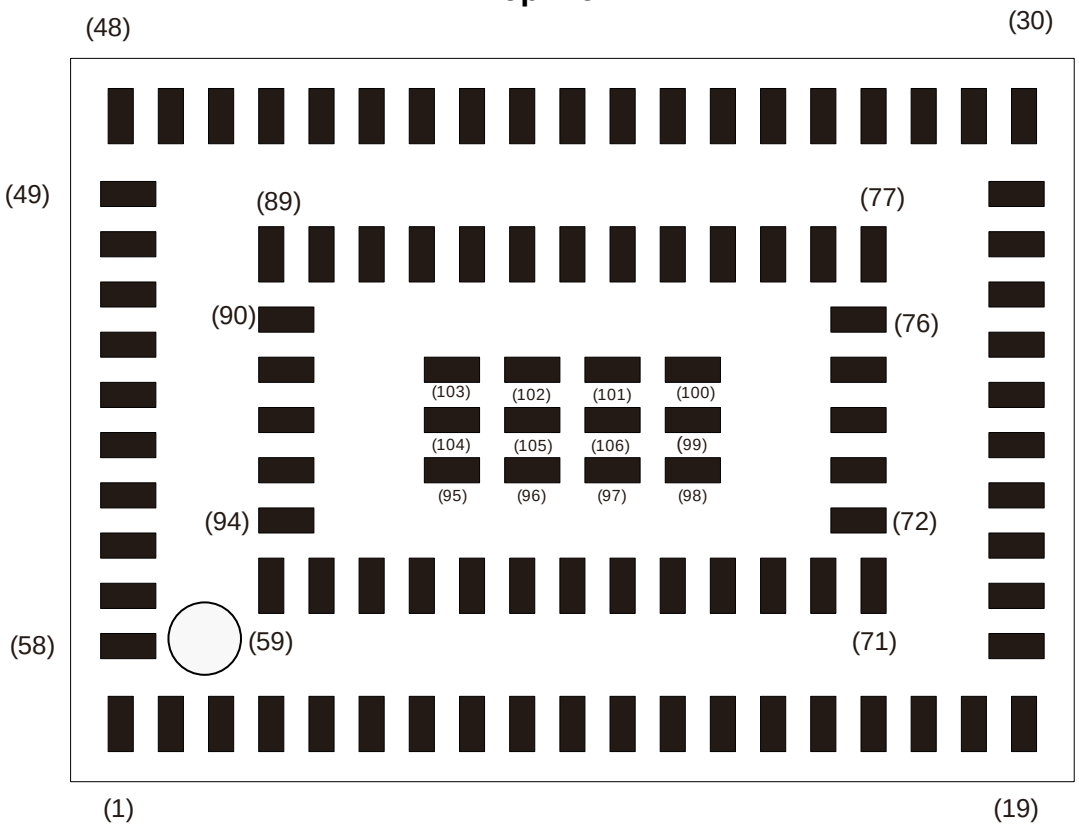
Marking	Meaning
A	Murata Logo
B	Inspection Number
C	Module Type
D	Pin 1 Marking

Structure



6.2. Pin Layout

Top View



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	GND	25	SDIO_DATA_3	49	BT_RF_OUT	73	GND
2	GND	26	SDIO_CMD	50	GND	74	SFL_IO0
3	GND	27	GND	51	BT_RF_IN	75	SFL_IO3
4	VDDIO_SFL	28	VDDOUT_VDDIO	52	GND	76	SFL_IO2
5	BT_HOST_WAKE	29	BT_DEV_WAKE	53	GND	77	SFL_CLK
6	GND	30	GND	54	RF_SW_CTRL_6	78	SFL_IO1
7	WL_HOST_WAKE	31	BT_UART_TXD	55	RF_SW_CTRL_10	79	SFL_CS
8	WL_DEV_WAKE	32	BT_UART_RXD	56	RF_SW_CTRL_5	80	EXT_LPO
9	BT_REG_ON	33	BT_UART_RTS	57	GND	81	CLK_REQ
10	WL_REG_ON	34	BT_UART_CTS	58	ANT0	82	BT_PCM_OUT
11	GND	35	VDDIO	59	GND	83	BT_PCM_SYNC
12	VOUT_3P3	36	GND	60	GND	84	BT_PCM_IN
13	VBAT	37	P9	61	WL_GPIO_15	85	BT_PCM_CLK
14	VBAT	38	P11	62	WL_UART_TX	86	BT_I2S_WS
15	GND	39	P13	63	WL_UART_RX	87	BT_I2S_CLK
16	RF_SW_CTRL_8	40	P5	64	WL_GPIO_14	88	BT_I2S_DI
17	RF_SW_CTRL_12	41	P6	65	GND	89	BT_I2S_DO
18	RF_SW_CTRL_11	42	P8	66	JTAG_TDO	90	BT_GPIO_2
19	GND	43	P7	67	JTAG_TDI	91	BT_GPIO_5
20	GND	44	P12	68	JTAG_TMS_SWD	92	BT_GPIO_4
21	SDIO_DATA_2	45	P0	69	JTAG_TCK_SWD	93	BT_GPIO_3
22	SDIO_DATA_1	46	P1	70	JTAG_SEL	94-106	GND
23	SDIO_DATA_0	47	GND	71	JTAG_TRS	-	-
24	SDIO_CLK	48	GND	72	GND	-	-

6.3. Module PIN Descriptions

No.	Pin name	Type	Connection to IC pin name	Description
1	GND	-	GND	Ground
2	GND	-	GND	Ground
3	GND	-	GND	Ground
4	VDDIO_SFL	I	VDDIO_SFL	DC supply voltage for SFLASH I/O
5	BT_HOST_WAKE	O	BT_HOST_WAKE	Bluetooth host wake
6	GND	-	GND	Ground
7	WL_HOST_WAKE	I/O	GPIO_0	WL_HOST_WAKE
8	WL_DEV_WAKE	I/O	GPIO_1	WL_DEV_WAKE
9	BT_REG_ON	I	BT_REG_ON	Used by the PMU to power-up or power-down the internal regulators used by the Bluetooth section
10	WL_REG_ON	I	WL_REG_ON	Used by the PMU to power up or power down the internal regulators used by the WLAN section
11	GND	-	GND	Ground
12	VOUT_3P3	O	VDDOUT_RF3P3 VDDIO_RF1	Output of 3.3V RF LDO
13	VBAT	I	SR_VDDBAT5 LDO_VDDBAT5 WRF_GENTRAL_VDD_V5P0 WRF_TX_VDD_V5P0 ET_LINREG_VDD_V5P0 ET_SWREG_VDD_V5P0	Power supply
14	VBAT			
15	GND	-	GND	Ground
16	RF_SW_CTRL_8	O	RF_SW_CTRL_8	Programmable RF switch-control lines
17	RF_SW_CTRL_12	O	RF_SW_CTRL_12	Programmable RF switch-control lines
18	RF_SW_CTRL_11	O	RF_SW_CTRL_11	Programmable RF switch-control lines
19	GND	-	GND	Ground
20	GND	-	GND	Ground
21	SDIO_DATA_2	I/O	SDIO_DATA_2	SDIO data line 2
22	SDIO_DATA_1	I/O	SDIO_DATA_1	SDIO data line 1
23	SDIO_DATA_0	I/O	SDIO_DATA_0	SDIO data line 0
24	SDIO_CLK	I	SDIO_CLK	SDIO clock
25	SDIO_DATA_3	I/O	SDIO_DATA_3	SDIO data line 3
26	SDIO_CMD	I/O	SDIO_CMD	SDIO command line
27	GND	-	GND	Ground
28	VDDOUT_VDDIO	O	VDDOUT_VDDIO OTP_VDD1P8 VDDP_RF1 VDDP_SFL	output for 1.8V power switch
29	BT_DEV_WAKE	I	BT_DEV_WAKE	Bluetooth device wake
30	GND	-	GND	Ground
31	BT_UART_TXD	O	BT_UART_TXD	UART serial output
32	BT_UART_RXD	I	BT_UART_RXD	UART serial input
33	BT_UART_RTS	O	BT_UART_RTS_N	UART request-to-send
34	BT_UART_CTS	I	BT_UART_CTS_N	UART clear-to-send

No.	Pin name	Type	Connection to IC pin name	Description
35	VDDIO	I	VDDIO PMU_VDDIOA PMU_VDDIOP STRAP_OFF_1P8 VDD18_FLL BT_VDDO BT_VDDO_HIB PAD_ADC_AVDDC	Power supply
36	GND	-	GND	Ground
37	P9	I/O	P9	Programmable LHL/HIB pads
38	P11	I/O	P11	Programmable LHL/HIB pads
39	P13	I/O	P13	Programmable LHL/HIB pads
40	P5	I/O	P5	Programmable LHL/HIB pads
41	P6	I/O	P6	Programmable LHL/HIB pads
42	P8	I/O	P8	Programmable LHL/HIB pads
43	P7	I/O	P7	Programmable LHL/HIB pads
44	P12	I/O	P12	Programmable LHL/HIB pads
45	P0	I/O	P0	Programmable LHL/HIB pads
46	P1	I/O	P1	Programmable LHL/HIB pads
47	GND	-	GND	Ground
48	GND	-	GND	Ground
49	BT_RF_OUT	I/O		Bluetooth Antenna
50	GND	-	GND	Ground
51	BT_RF_IN	I/O	(SP3T)	BT/WiFi one antenna: Routed to BT_RF_OUT Separate BT/WiFi antenna: connect to 50ohm terminal.
52	GND	-	GND	Ground
53	GND	-	GND	Ground
54	RF_SW_CTRL_6	O	RF_SW_CTRL_6	NC
55	RF_SW_CTRL_10	O	RF_SW_CTRL_10	Programmable RF switch-control lines
56	RF_SW_CTRL_5	O	RF_SW_CTRL_5	NC
57	GND	-	GND	Ground
58	ANT0	I/O		
59	GND	-	GND	Ground
60	GND	-	GND	Ground
61	WL_GPIO_15	I/O	GPIO_15	Programmable GPIO lines
62	WL_UART_TX	I/O	GPIO_13	This pin can programmed by S/W to be a GPIO, or Debug UART
63	WL_UART_RX	I/O	GPIO_12	This pin can programmed by S/W to be a GPIO, or Debug UART
64	WL_GPIO_14	I/O	GPIO_14	Programmable GPIO lines
65	GND	-	GND	Ground
66	JTAG_TDO	I/O	GPIO_5	Programmable GPIO lines, or JTAG_TDO(Pull-High JTAG SEL)
67	JTAG_TDI	I/O	GPIO_4	Programmable GPIO lines, or JTAG_TDI(Pull-High JTAG SEL)
68	JTAG_TMS_SWD	I/O	GPIO_3	Programmable GPIO lines, or JTAG_TMS_SWD(Pull-High JTAG SEL)
69	JTAG_TCK_SWD	I/O	GPIO_2	Programmable GPIO lines, or JTAG_TCK_SWD(Pull-High JTAG SEL)
70	JTAG_SEL	I	JTAG_SEL	JTAG select, pull-high to select the JTAG interface
71	JTAG_TRS	I/O	GPIO_6	Programmable GPIO lines, or JTAG_TRS(Pull-High JTAG SEL)
72	GND	-	GND	Ground
73	GND	-	GND	Ground
74	SFL_IO0	I/O	SFL_IO0	SFLASH data line 0
75	SFL_IO3	I/O	SFL_IO3	SFLASH data line 3
76	SFL_IO2	I/O	SFL_IO2	SFLASH data line 2
77	SFL_CLK	O	SFL_CLK	SFLASH clock
78	SFL_IO1	I/O	SFL_IO1	SFLASH data line 1
79	SFL_CS	O	SFL_CS	SFLASH chip select

No.	Pin name	Type	Connection to IC pin name	Description
81	CLK_REQ	I/O	CLK_REQ	Reference clock request
82	BT_PCM_OUT	O	BT_PCM_OUT	PCM data output
83	BT_PCM_SYNC	I/O	BT_PCM_SYNC	PCM sync, can be master (output) or slave (input)
84	BT_PCM_IN	I	BT_PCM_IN	PCM data input
85	BT_PCM_CLK	I/O	BT_PCM_CLK	PCM clock, can be master (output) or slave (input)
86	BT_I2S_WS	I/O	BT_I2S_WS	I2S serial word select
87	BT_I2S_CLK	I/O	BT_I2S_CLK	I2S serial clock
88	BT_I2S_DI	I	BT_I2S_DI	I2S serial data input
89	BT_I2S_DO	O	BT_I2S_DO	I2S serial data output
90	BT_GPIO_2	I/O	BT_GPIO_2	Bluetooth general-purpose I/Os
91	BT_GPIO_5	I/O	BT_GPIO_5	Bluetooth general-purpose I/Os
92	BT_GPIO_4	I/O	BT_GPIO_4	Bluetooth general-purpose I/Os
93	BT_GPIO_3	I/O	BT_GPIO_3	Bluetooth general-purpose I/Os
94-106	GND	-	GND	Ground

7. ABSOLUTE MAXIMUM RATINGS*2)

Parameter		min.	max.	Unit
Storage Temperature		-40	85	deg.C
Supply Voltage	VBAT	-0.5	5.0	V
	VDDIO	-0.5	2.2	V
	VDDIO_SFL	-0.5	4.1	V

*2) Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters are set within operating condition.

8. OPERATING CONDITION*3)

Parameter		min.	typ.	max.	unit
Operating Temperature		-20	25	+70	deg.C
Supply Voltage	VBAT	3.2	-	4.4	V
	VDDIO	1.62	1.8	1.98	V
	VDDIO_SFL	1.62/2.97	1.8/3.3	1.98/3.46	V

*3) Functionality is guaranteed but the specifications require the derating at over-temperatures, over-voltage condition.

9. External LPO Signal Requirement

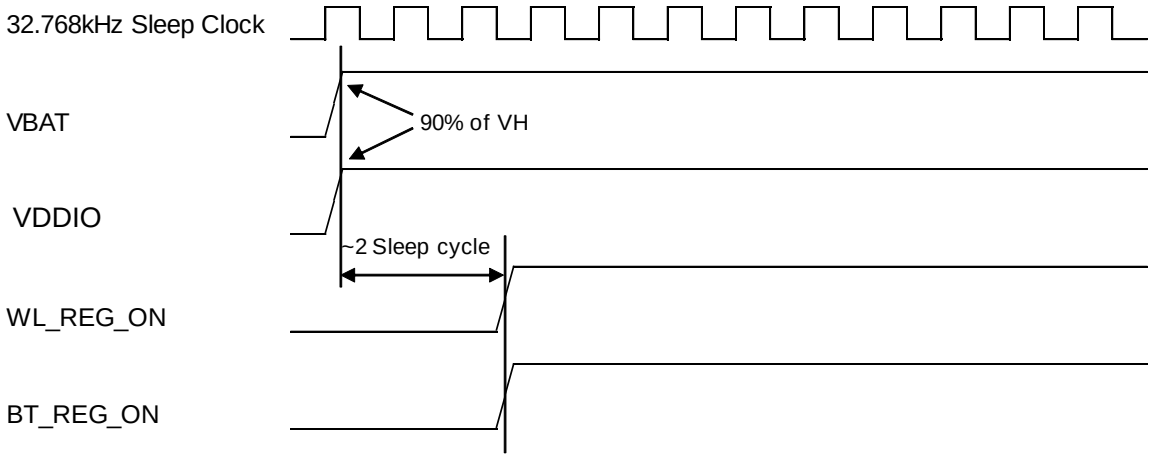
Parameter	External LPO Clock	Unit
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-250	ppm
Duty cycle	30-70	%
Input signal amplitude	500 – 1800	mVp-p
Signal type	Square-wave or sine-wave	-
Input impedance*4)	> 100k	ohm

*4) When power is applied or switch off

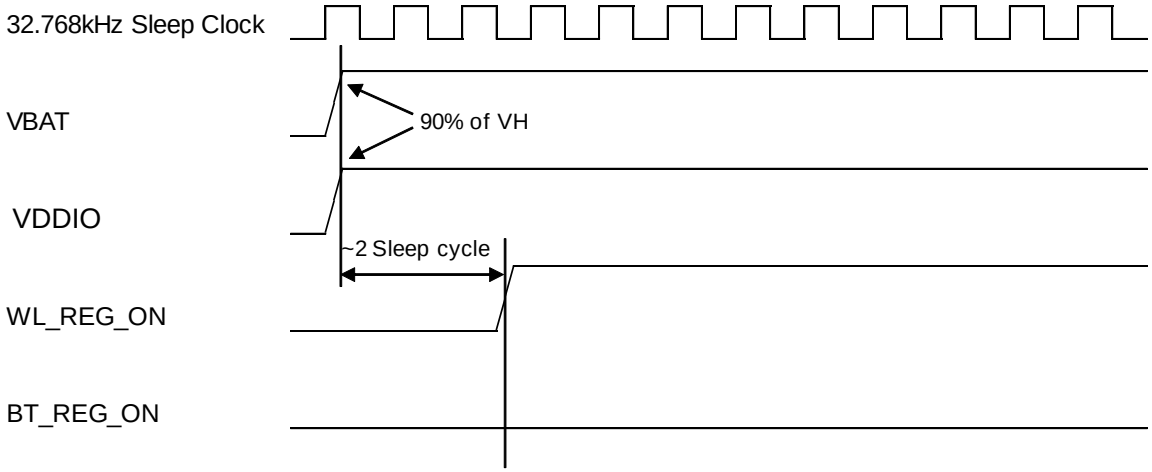
10. POWER ON SEQUENCE

-VBAT should not rise 10%-90%faster than 40 microsecond.
-VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

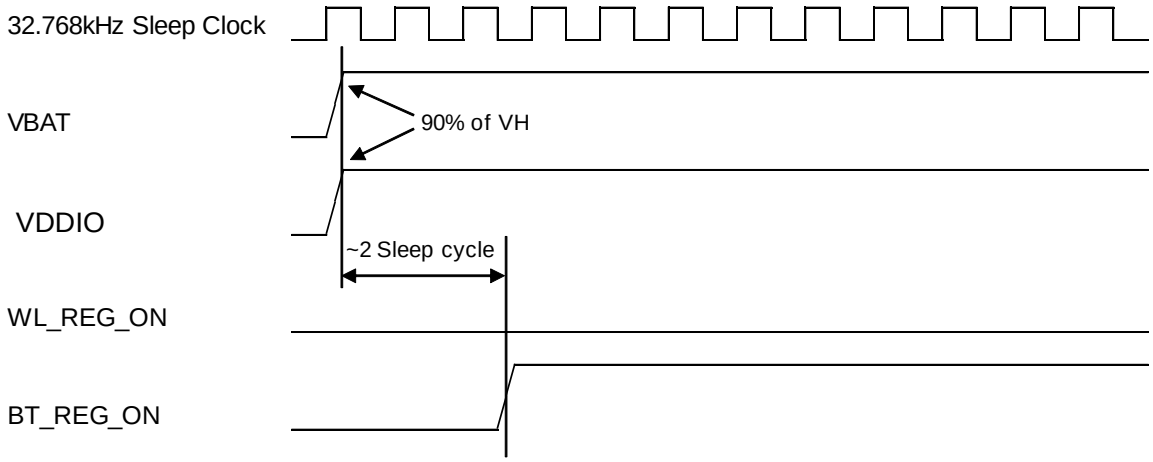
10.1. Power On Sequence for WLAN ON and BT ON



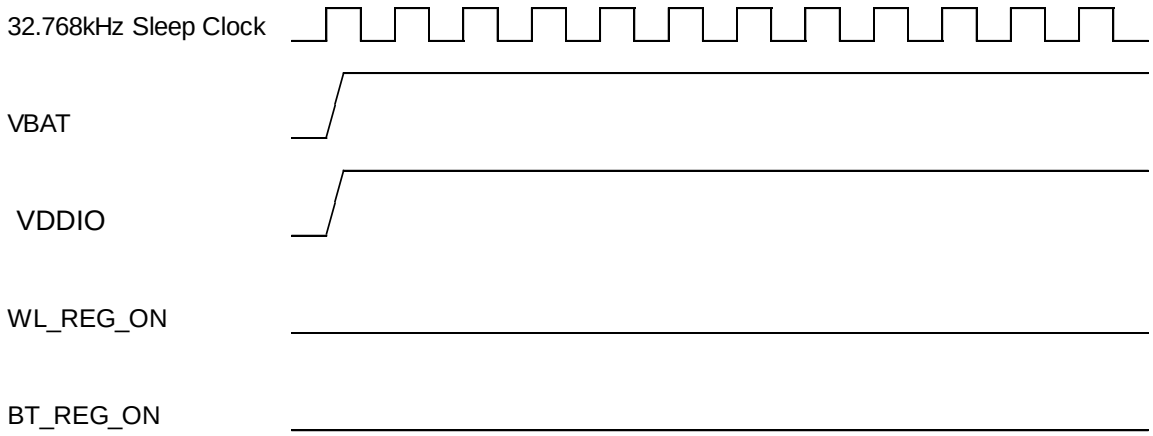
10.2. Power On Sequence for WLAN ON and BT Off



10.3. Power On Sequence for WLAN OFF and BT ON



10.4. Power On Sequence for WLAN OFF and BT OFF



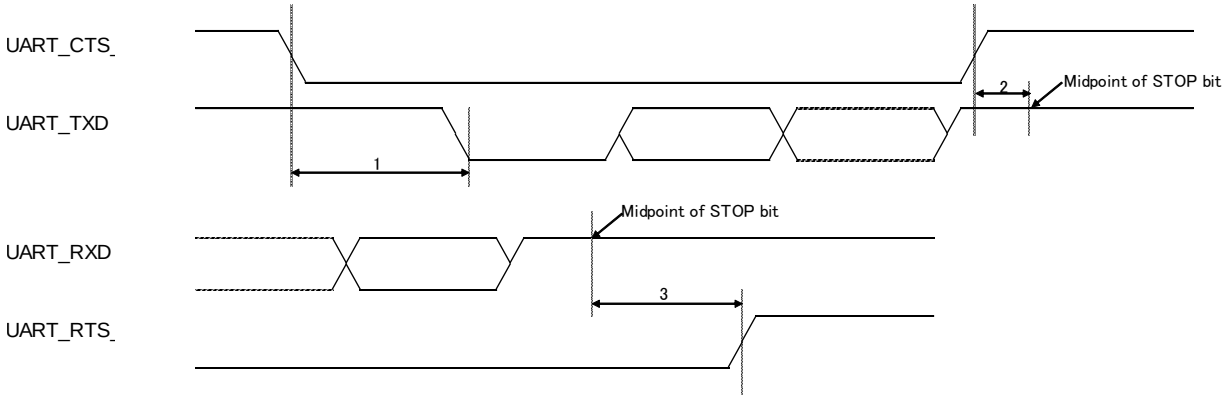
11. Digital I/O Requirements

Digital I/O Pins	Sym	min.	typ.	max.	unit
For VDDIO=1.8V:					
Input high voltage	VIH	0.65xVDDIO	-	-	V
Input low voltage	VIL	-	-	0.35xVDDIO	V
Output high voltage@2mA	VOH	VDDIO-0.45	-	-	V
Output low voltage@2mA	VOL	-	-	0.45	V

BT/WL_REG_ON	Sym	min.	typ.	max.	unit
Input high voltage	VIH	1	-	4.4	V
Input low voltage	VIL	VSS	-	0.3	V
Pull-down resistance(internal)	RPD	-	50	-	kΩ
Leakage discharged Current	ILEAK_DIS	-	28	-	nA
REG OFF time	TREG_OFF	2	-	-	ms

12. INTERFACE TIMING AND AC CHARACTERISTICS

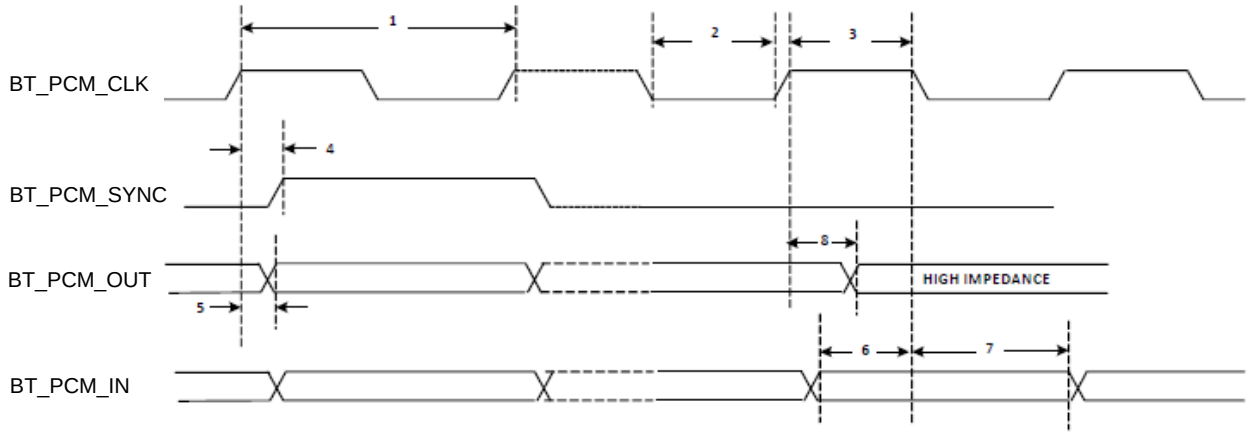
12.1. Bluetooth UART Timing



Reference	Description	Min	Typ	Max	Unit
1	Delay time, UART_CTS low to UART_TXD valid	-	-	1.5	Bit periods
2	Setup time, UART_CTS high before midpoint of stop bit	-	-	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS high	-	-	0.5	Bit periods

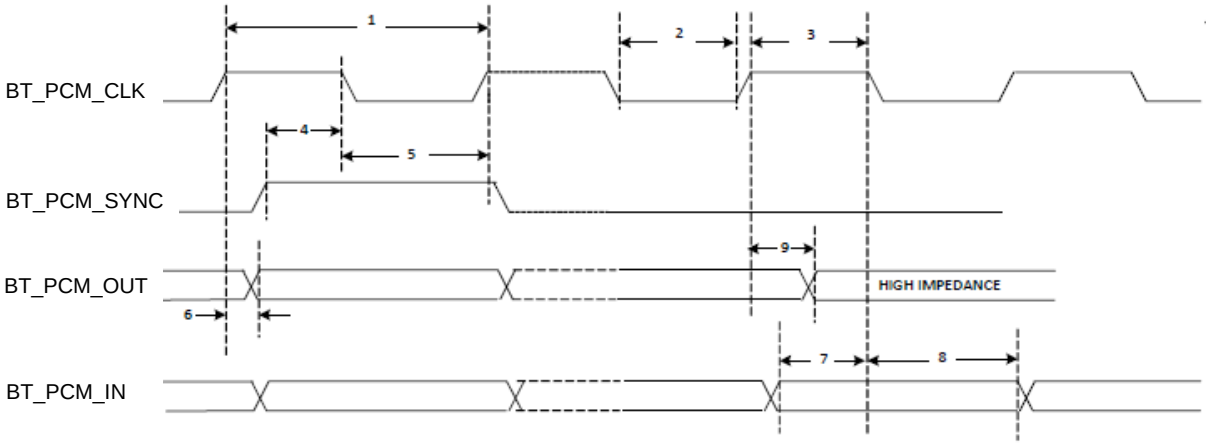
12.2. Bluetooth PCM Interface Timing

12.2.1. Short Frame Sync, Master Mode



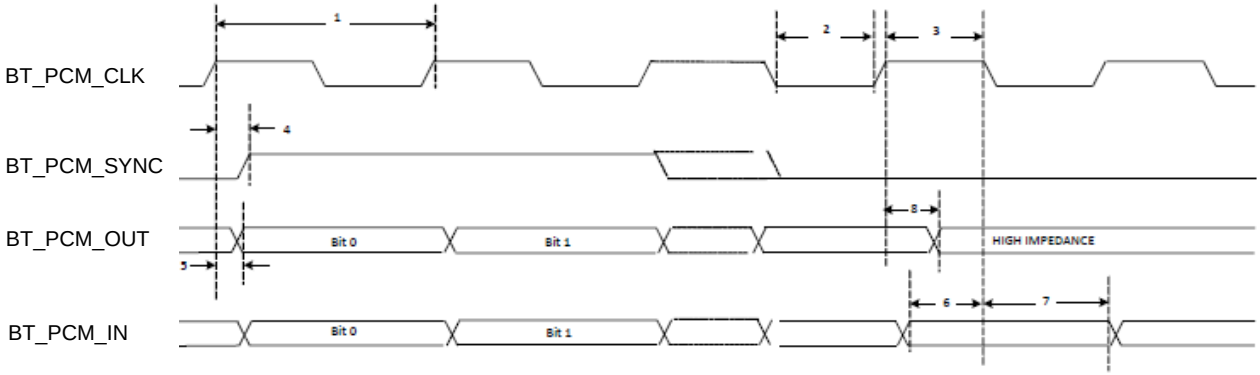
Reference	Description	Min	Typ	Max	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock High	41	-	-	ns
3	PCM bit clock Low	41	-	-	ns
4	BT_PCM_SYNC delay	0	-	25	ns
5	BT_PCM_OUT delay	0	-	25	ns
6	BT_PCM_IN setup	8	-	-	ns
7	BT_PCM_IN hold	8	-	-	ns
8	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance	0	-	25	ns

12.2.2. Short Frame Sync, Slave Mode



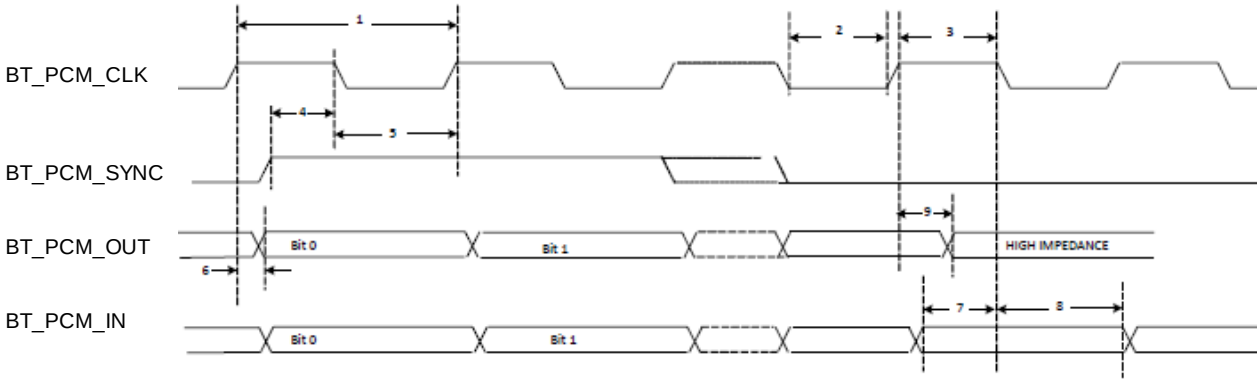
Reference	Description	Min	Typ	Max	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock High	41	-	-	ns
3	PCM bit clock Low	41	-	-	ns
4	BT_PCM_SYNC setup	8	-	-	ns
5	BT_PCM_SYNC hold	8	-	-	ns
6	BT_PCM_OUT delay	0	-	25	ns
7	BT_PCM_IN setup	8	-	-	ns
8	BT_PCM_IN hold	8	-	-	ns
9	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance	0	-	25	ns

12.2.3. Long Frame Sync, Master Mode



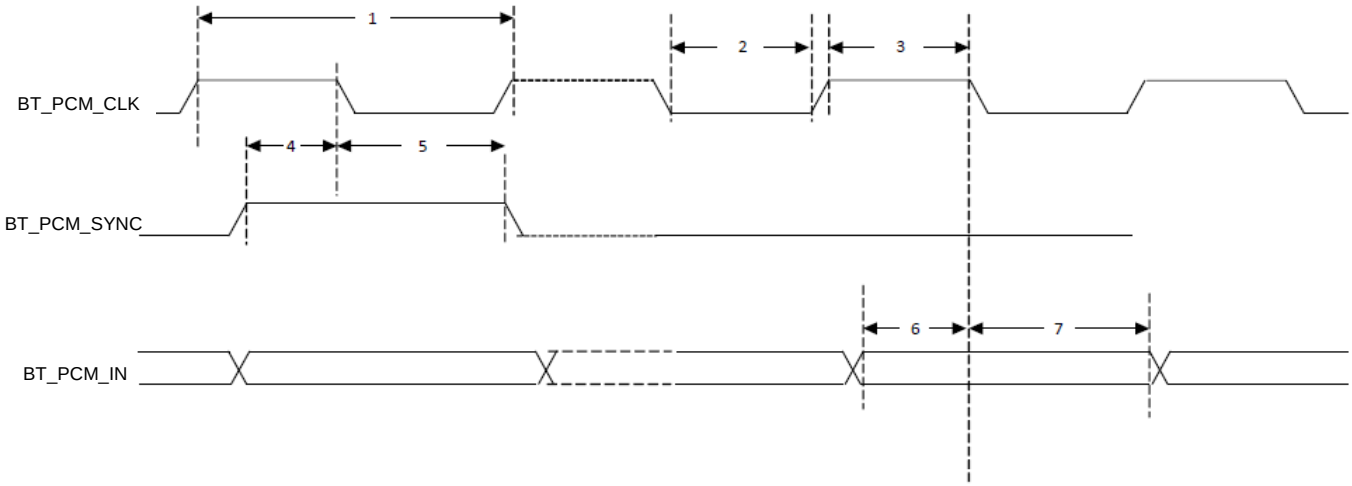
Reference	Description	Min	Typ	Max	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock High	41	-	-	ns
3	PCM bit clock Low	41	-	-	ns
4	BT_PCM_SYNC delay	0	-	25	ns
5	BT_PCM_OUT delay	0	-	25	ns
6	BT_PCM_IN setup	8	-	-	ns
7	BT_PCM_IN hold	8	-	-	ns
8	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance	0	-	25	ns

12.2.4. Long Frame Sync, Slave Mode



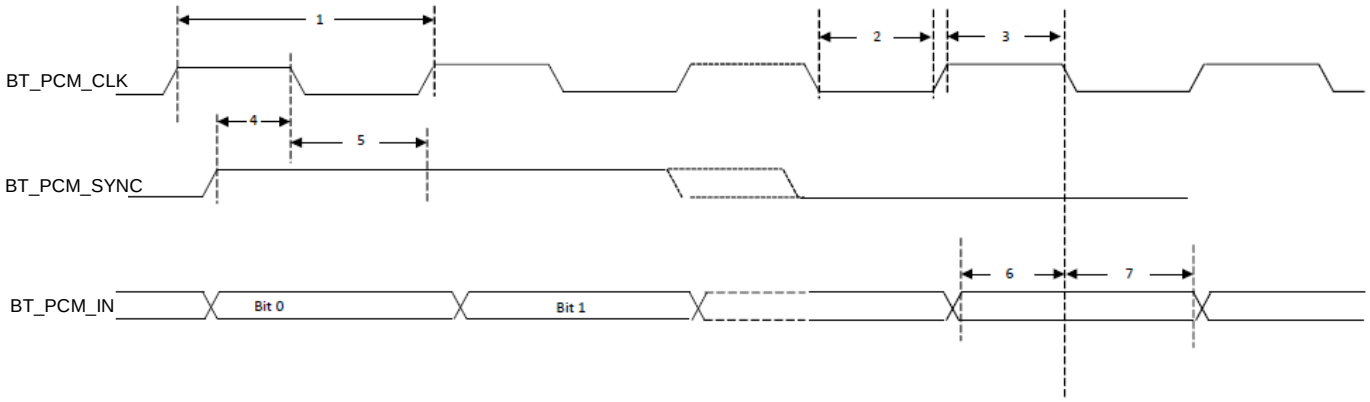
Reference	Description	Min	Typ	Max	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock High	41	-	-	ns
3	PCM bit clock Low	41	-	-	ns
4	BT_PCM_SYNC setup	8	-	-	ns
5	BT_PCM_SYNC hold	8	-	-	ns
6	BT_PCM_OUT delay	0	-	25	ns
7	BT_PCM_IN setup	8	-	-	ns
8	BT_PCM_IN hold	8	-	-	ns
9	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance	0	-	25	ns

12.2.5. Short Frame Sync, Burst Mode



Reference	Description	Min	Typ	Max	Unit
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock Low	20.8	-	-	ns
3	PCM bit clock High	20.8	-	-	ns
4	BT_PCM_SYNC setup	8	-	-	ns
5	BT_PCM_SYNC hold	8	-	-	ns
6	BT_PCM_IN setup	8	-	-	ns
7	BT_PCM_IN hold	8	-	-	ns

12.2.6. Long Frame Sync, Burst Mode



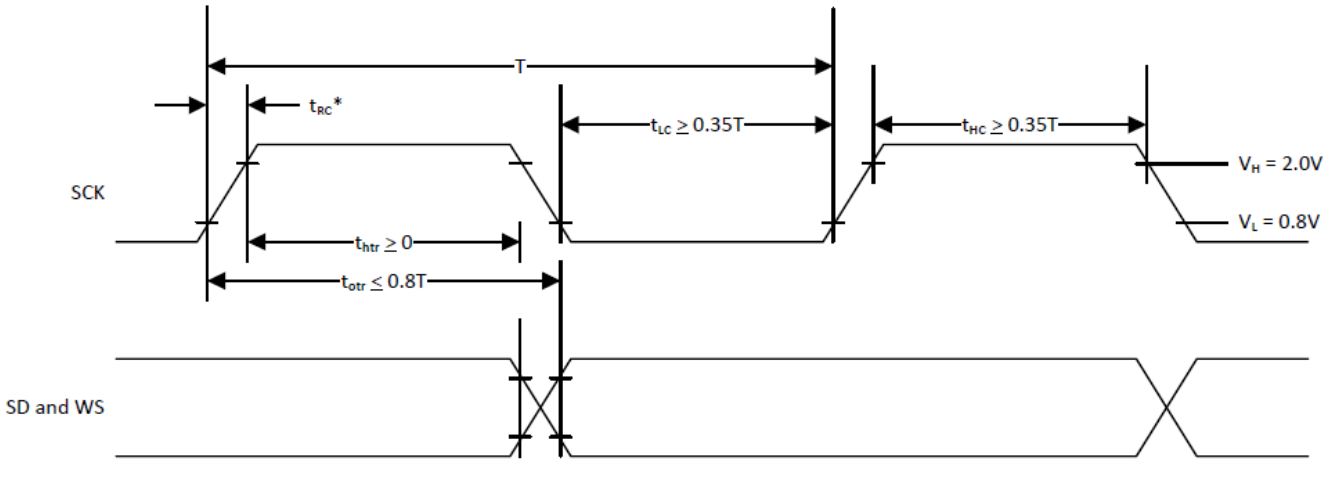
Reference	Description	Min	Typ	Max	Unit
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock Low	20.8	-	-	ns
3	PCM bit clock High	20.8	-	-	ns
4	BT_PCM_SYNC setup	8	-	-	ns
5	BT_PCM_SYNC hold	8	-	-	ns
6	BT_PCM_IN setup	8	-	-	ns
7	BT_PCM_IN hold	8	-	-	ns

12.3. I²S Timing

	Transmitter				Receiver				
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	Notes
Clock Period T	T_{tr}	-	-	-	T_{tr}	-	-	-	a
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	-	-	-	$0.35T_{tr}$	-	-	-	b
LOW t_{LC}	$0.35T_{tr}$	-	-	-	$0.35T_{tr}$	-	-	-	b
Slave Mode: Clock accepted by transmitter or receiver									
HIGH h_{TC}	-	$0.35T_{tr}$	-	-	-	$0.35T_{tr}$	-	-	c
LOW t_{LC}	-	$0.35T_{tr}$	-	-	-	$0.35T_{tr}$	-	-	c
Rise time t_{RC}	-	-	$0.15T_{tr}$	-	-	-	-	-	d
Transmitter									
Delay t_{dtr}	-	-	-	0.8T	-	-	-	-	e
Hold time t_{htr}	0	-	-	-	-	-	-	-	d
Receiver									
Setup time t_{sr}	-	-	-	-	-	$0.2T_r$	-	-	f
Hold time t_{hr}	-	-	-	-	-	0	-	-	f

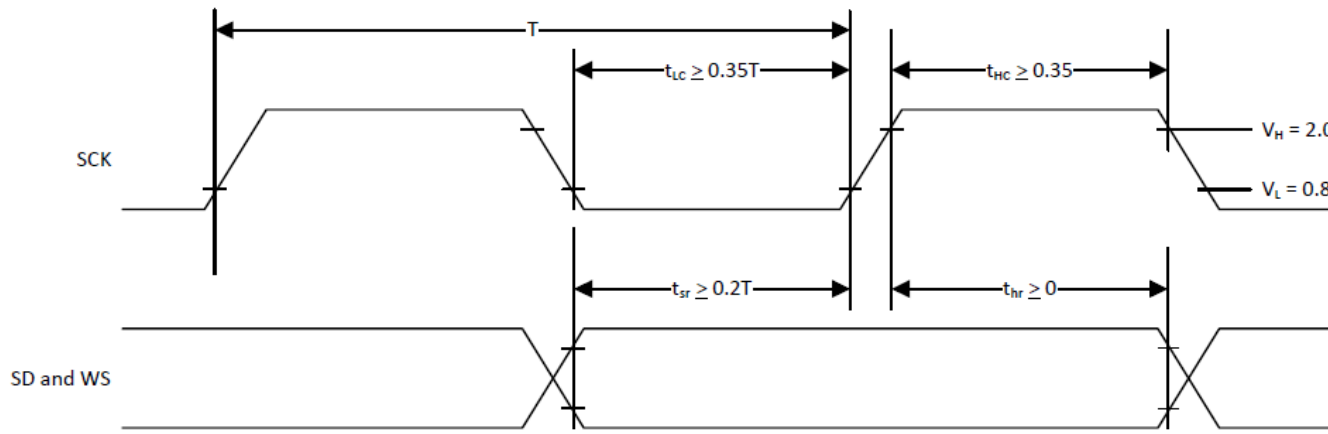
a. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
b. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
c. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
d. Because the delay(t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
e. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
f. The data setup and hold time must not be less than the specified receiver setup and hold time.

12.3.1. I²S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
T = T_{tr}
* t_{RC} is only relevant for transmitters in slave mode.

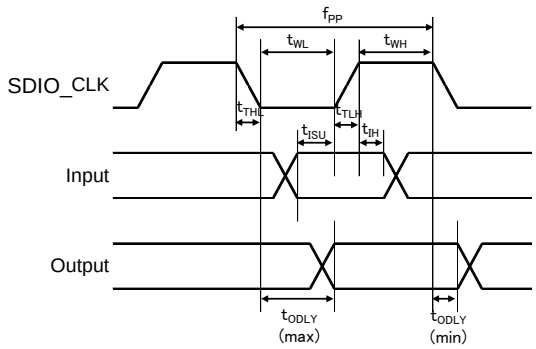
12.3.2. I²S Receiver Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
T > T_r

12.4. SDIO Timing

12.4.1. SDIO Default Mode Timing

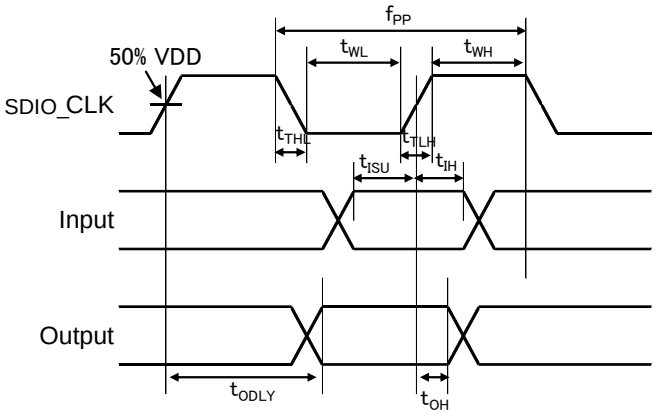


SDIO Bus Timing[a] parameters (default Mode)

Parameter	Symbol	Min	Typ	Max	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b]					
Frequency-Data Transfer Mode	fPP	0	-	25	MHz
Frequency-Identification Mode	fOD	0	-	400	kHz
Clock Low Time	tWL	10	-	-	ns
Clock High Time	tWH	10	-	-	ns
Clock Rise Time	tTLH	-	-	10	ns
Clock low Time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input Setup Time	tISU	5	-	-	ns
Input Hold Time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output Delay time-Data Transfer Mode	tODLY	0	-	14	ns
Output Delay time-Identification Mode	tODLY	0	-	50	ns

(a). Timing is based on CL ≤ 40pF load on CMD and Data.
(b). Min (Vih) = 0.7*VDDIO and max (Vil) = 0.2*VDDIO.

12.4.2. SDIO High-Speed Mode Timing



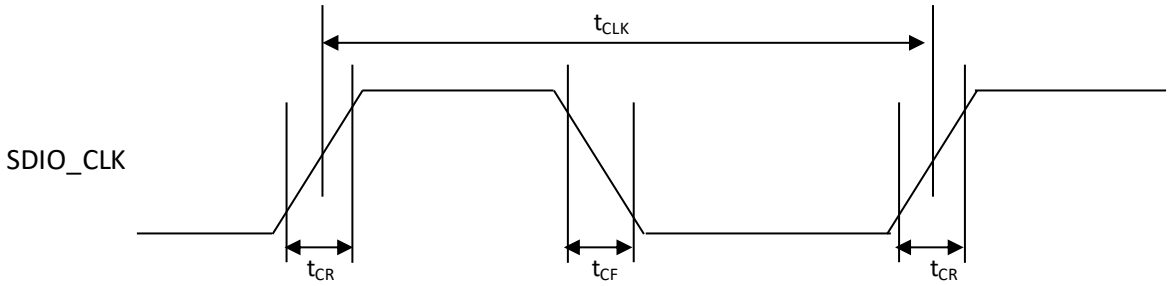
SDIO Bus Timing[a] parameters (High-Speed Mode)

Parameter	Symbol	Min	Typ	Max	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b]					
Frequency-Data Transfer Mode	fPP	0	-	50	MHz
Frequency-Identification Mode	fOD	0	-	400	kHz
Clock Low Time	tWL	7	-	-	ns
Clock High Time	tWH	7	-	-	ns
Clock Rise Time	tTLH	-	-	3	ns
Clock low Time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input Setup Time	tISU	6	-	-	ns
Input Hold Time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output Delay time-Data Transfer Mode	tODLY	-	-	14	ns
Output Hold time	tOH	2.5	-	-	ns
Total System Capacitance (each line)	CL	-	-	40	pF

(a). Timing is based on CL ≤ 40pF load on CMD and Data.
(b). Min (Vih) = 0.7*VDDIO and max (Vil) = 0.2*VDDIO

12.4.3. SDIO BUS Timing Specifications in SDR Modes

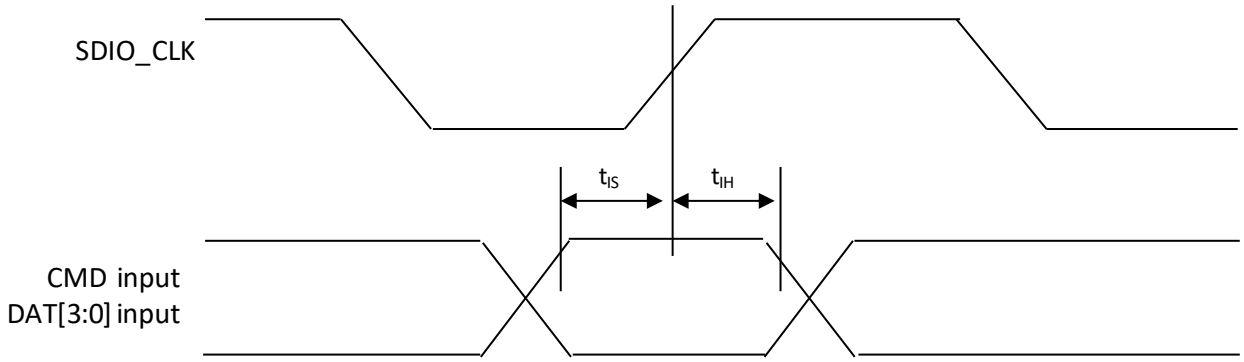
Clock Timing



SDIO Bus Clock Timing Parameters (SDR Modes)

Parameter	Symbol	Min	Max	Unit	Comments
-	tCLK	40	-	ns	SDR12 mode
		20	-	ns	SDR25 mode
-	tCR,tCF	-	0.2 x tCLK	ns	tCR,tCF<2.00ns(max)@100MHz,cCARD=10pF
Clock duty cycle	-	30	70	%	-

Card Input Timing

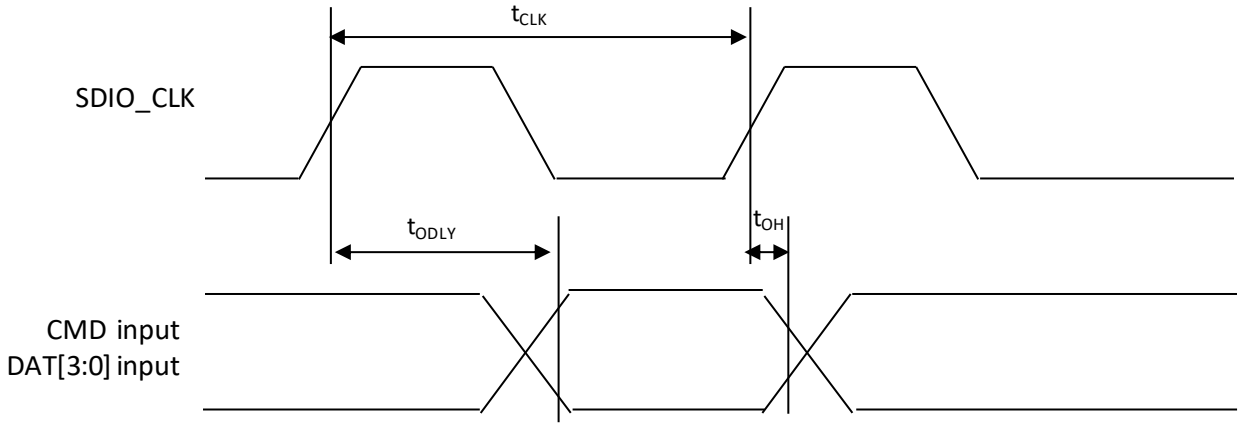


SDIO Bus Input Timing Parameters (SDR Modes)

Symbol	Min	Max	Unit	Comments
SDR50 Mode				
tIS	3.0	-	ns	cCARD = 10pF,VCT = 0.975V
tIH	0.8	-	ns	cCARD = 5pF,VCT = 0.975V

Card Output Timing

SDIO Bus Output Timing (SDR Modes up to 50MHz)



SDIO Bus Output Timing Parameters (SDR Modes up to 50MHz)

Symbol	Min	Max	Unit	Comments
tODLY	-	14.0	ns	tCLK ≧ 20ns CL = 40pF using for SDR12,SDR25
tOH	1.5	-	ns	Hold time at the tODLY(min) CL = 15pF

13. DC / RF Characteristics

13.1. DC/RF Characteristics for IEEE802.11b - 2.4GHz

Specification	IEEE802.11b
Mode	DSSS / CCK
Channel Frequency	2412 - 2472MHz
Data rate	1, 2, 5.5, 11Mbps

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 1.8V,
Output power setting=17dBm, 11Mbps mode unless otherwise specified.

Items	Contents			
- DC Characteristics -	min.	typ.	max.	unit
1. DC current				
1) Tx mode (1024byte, 20usec interval) *5)	-	200	-	mA
2) Rx mode	-	20	-	mA
- Tx Characteristics *5)-	min.	typ.	max.	unit
2. Output Power	15	17	19	dBm
3. Spectrum Mask margin				
1) 1st side lobes(-30dBr)	0	-	-	dB
2) 2nd side lobes(-50dBr)	0	-	-	dB
4. Power-on and Power-down ramp	-		2.0	µsec
5. RF Carrier Suppression	15	-	-	dB
6. Modulation Accuracy (EVM)	-	-	35	%
7.Frequency tolerance	-20		20	ppm
8. Out band Spurious Emissions				
1) 30-1000MHz	-	-	-36	dBm
2) 1000-12750MHz	-	-	-30	dBm
3) 1800-1900MHz			-47	dBm
4) 5150-5300MHz	-	-	-47	dBm
- Rx Characteristics -	min.	typ.	max.	unit
9. Minimum Input Level Sensitivity	-	-	-76	dBm
10. Adjacent Channel Rejection (FER ≦ 8%)	35	-	-	dB

*5): Defined when output power setting is 17dBm at Murata module antenna pad

13.2. DC/RF Characteristics for IEEE802.11g - 2.4GHz

Specification	IEEE802.11g
Mode	OFDM
Channel Frequency	2412 - 2472MHz
Data rate	6, 9, 12, 18, 24, 36, 48, 54Mbps

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 1.8V,
Output power setting=14dBm, 54Mbps mode unless otherwise specified.

Items	Contents			
- DC Characteristics -	min.	typ.	max.	unit
1. DC current				
1) Tx mode (1024byte, 20usec interval) *6)	-	150	-	mA
2) Rx mode	-	20	-	mA
- Tx Characteristics*6) -	min.	typ.	max.	unit
2. Output Power	12	14	16	dBm
3. Spectrum Mask margin				
1) 9MHz to 11MHz (0~ -20dBr)	0	-	-	dB
2) 11MHz to 20MHz (-20~ -28dBr)	0	-	-	dB
3) 20MHz to 30MHz (-28~ -40dBr)	0	-	-	dB
4) 30MHz to 33MHz (-40dBr)	0	-	-	dB
4. Constellation Error (EVM)	-	-	-25	dB
5.Frequency tolerance	-20		20	ppm
6. Out band Spurious Emissions				
1) 30-1000MHz	-	-	-36	dBm
2) 1000-12750MHz	-	-	-30	dBm
3) 1800-1900MHz			-47	dBm
4) 5150-5300MHz	-	-	-47	dBm
- Rx Characteristics -	min.	typ.	max.	unit
7. Minimum Input Level Sensitivity	-	-	-65	dBm
8. Adjacent Channel Rejection (PER ≦ 10%)	-1	-	-	dB

*6): Defined when output power setting is 14dBm at Murata module antenna pad

13.3. DC/RF Characteristics for IEEE802.11n – 2.4GHz

Specification	IEEE802.11n
Mode	OFDM
Channel Frequency	2412 - 2472MHz
Data rate	6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 1.8V,
Output power setting=13dBm, MCS7 unless otherwise specified.

- DC Characteristics -	min.	typ.	max.	unit
1. DC current				
1) Tx mode (1024byte, 20usec interval) *7)	-	140	-	mA
2) Rx mode	-	20	-	mA
- Tx Characteristics*7) -	min.	typ.	max.	unit
2. Output Power	11	13	15	dBm
3. Spectrum Mask				
1) 9MHz to 11MHz (0 ~ -20dBr)	0	-	-	dB
2) 11MHz to 20MHz (-20 ~ -28dBr)	0	-	-	dB
3) 20MHz to 30MHz (-28 ~ -45dBr)	0	-	-	dB
4) 30MHz to 33MHz (-45dBr)	0	-	-	dB
4. Constellation Error (EVM)	-	-	-27	dB
5.Frequency tolerance	-20		20	ppm
6. Out band Spurious Emissions				
1) 30-1000MHz	-	-	-36	dBm
2) 1000-12750MHz	-	-	-30	dBm
3) 1800-1900MHz			-47	dBm
4) 5150-5300MHz	-	-	-47	dBm
- Rx Characteristics -	min.	typ.	max.	unit
6. Minimum Input Level Sensitivity	-	-	-64	dBm
7. Adjacent Channel Rejection (PER ≦ 10%)	-2	-	-	dB

*7): Defined when output power setting is 13dBm at Murata module antenna pad

13.4. DC/RF Characteristics for IEEE802.11a - 5GHz

Specification	IEEE802.11a
Mode	OFDM
Channel Frequency	5180 - 5825MHz
Data rate	6, 9, 12, 18, 24, 36, 48, 54Mbps

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 1.8V,
Output power setting=13dBm, 54Mbps unless otherwise specified.

- DC Characteristics -	min.	typ.	max.	unit
1. DC current				
1) Tx mode (1024byte, 20usec interval) *8)	-	230	-	mA
2) Rx mode	-	20	-	mA
- Tx Characteristics*8) -	min.	typ.	max.	unit
2. Output Power	11	13	15	dBm
3. Spectrum Mask				
1) 9MHz to 11MHz (0~ -20dBr)	0	-	-	dB
2) 11MHz to 20MHz (-20~ -28dBr)	0	-	-	dB
3) 20MHz to 30MHz (-28~ -40dBr)	0	-	-	dB
4) 30MHz to 33MHz (-40dBr)	0	-	-	dB
4. Constellation Error (EVM)	-	-	-25	dB
5.Frequency tolerance	-20		20	ppm
- Rx Characteristics -	min.	typ.	max.	unit
6. Minimum Input Level Sensitivity	-	-	-65	dBm
7. Adjacent Channel Rejection (PER ≦ 10%)	-1	-	-	dB

*8): Defined when output power setting is 13dBm at Murata module antenna pad

13.5. DC/RF Characteristics for IEEE802.11n(HT20) - 5GHz

Specification	IEEE802.11n
Mode	OFDM
Channel Frequency	5180 - 5825MHz
Data rate	6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 1.8V,
Output power setting=12dBm, MCS7 unless otherwise specified.

- DC Characteristics -	min.	typ.	max.	unit
1. DC current				
1) Tx mode (1024byte, 20usec interval) *9)	-	210	-	mA
2) Rx mode	-	20	-	mA
- Tx Characteristics*9) -	min.	typ.	max.	unit
2. Output Power	10	12	14	dBm
3. Spectrum Mask margin				
1) 9MHz to 11MHz (0~ -20dBr)	0	-	-	dB
2) 11MHz to 20MHz (-20~ -28dBr)	0	-	-	dB
3) 20MHz to 30MHz (-28~ -45dBr)	0	-	-	dB
4) 30MHz to 33MHz (-45dBr)	0	-	-	dB
4. Constellation Error (EVM)	-	-	-27	dB
5.Frequency tolerance	-20		20	ppm
- Rx Characteristics -	min.	typ.	max.	unit
6. Minimum Input Level Sensitivity	-	-	-64	dBm
7. Adjacent Channel Rejection (PER ≦ 10%)	-2	-	-	dB

*9): Defined when output power setting is 12dBm at Murata module antenna pad

13.6. DC/RF Characteristics for IEEE802.11ac(VHT20) - 5GHz

Specification	IEEE802.11ac
Mode	OFDM
Channel Frequency	5180 - 5825MHz
Data rate	6.5, 13, 19.5, 26, 39, 52, 58.5, 65, 78Mbps

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 1.8V,
Output power setting=10dBm, MCS8 unless otherwise specified.

- DC Characteristics -	min.	typ.	max.	unit
1. DC current				
1) Tx mode (1024byte, 20usec interval) *10)	-	190	-	mA
2) Rx mode	-	20	-	mA
- Tx Characteristics*10) -	min.	typ.	max.	unit
2. Output Power	8	10	12	dBm
3. Spectrum Mask margin				
1) 9MHz to 11MHz (0~ -20dBr)	0	-	-	dB
2) 11MHz to 20MHz (-20~ -28dBr)	0	-	-	dB
3) 20MHz to 30MHz (-28~ -45dBr)	0	-	-	dB
4) 30MHz to 33MHz (-45dBr)	0	-	-	dB
4. Constellation Error (EVM)	-	-	-32	dB
5.Frequency tolerance	-20		20	ppm
- Rx Characteristics -	min.	typ.	max.	unit
6. Minimum Input Level Sensitivity	-	-	-59	dBm
7. Adjacent Channel Rejection (PER ≦ 10%)	-7	-	-	dB

*10): Defined when output power setting is 10dBm at Murata module antenna pad

13.7. DC/RF Characteristics for Bluetooth

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 1.8V

Items	Contents			
Bluetooth specification (power class)	Version 5.0 + EDR (Class1)			
Channel frequency (spacing)	2402 to 2480 MHz (1MHz)			
Current Consumption	Min.	Typ.	Max.	unit
(a) Tx=Rx=DH5 (fully occupied)	-	25	-	mA
(b) Tx=Rx=2DH5 (fully occupied)	-	22	-	mA
(c) Tx=Rx=3DH5 (fully occupied)	-	22	-	mA
Transmitter	Min.	Typ.	Max.	Unit
Output Power@DH5	6	-	13	dBm
Frequency range	2400	-	2483.5	MHz
20dB bandwidth	-		1	MHz
Adjacent Channel Power *11)				
(a) [M-N] =2	-	-	-20	dBm
(b) [M-N] ≥3	-	-	-40	dBm
Modulation characteristics				
(a) Modulation Δf1avg	140	-	175	kHz
(b) Modulation Δf2max	115		-	kHz
(c) Modulation Δf2avg / Δf1avg	0.8	-	-	
Carrier Frequency Drift				
(a) 1slot	-25	-	25	kHz
(b) 3slot / 5slot	-40	-	40	kHz
(c) Maximum drift rate		-	20	kHz/50us
EDR Relative Power	-4	-	1	dB
EDR Carrier Frequency Stability and Modulation Accuracy				
(a) ωi	-75	-	75	kHz
(b) ωi+ωo	-75	-	75	kHz
(c) ωo	-10	-	10	kHz
(d) RMS DEVM (DQPSK)	-	-	20	%
(e) Peak DEVM (DQPSK)	-	-	35	%
(f) 99% DEVM (DQPSK)	-	-	30	%
(g) RMS DEVM (8DPSK)	-	-	13	%
(h) Peak DEVM (8DPSK)	-	-	25	%
(i) 99% DEVM (8DPSK)	-	-	20	%
Spurious Emissions				
(a) 10MHz≦f<2387MHz	-	-	-36	dBm
(b) 2387MHz≦f<2400MHz	-	-	-30	dBm
(c) 2483.5MHz<f≦2496.5MHz			-47	dBm
(d) 2496.5MHz<f≦8GHz	-	-	-47	dBm
Receiver	Min.	Typ.	Max.	unit
BDR Sensitivity (BER≦0.1%)	-	-	-80	dBm
EDR Sensitivity (BER≦0.007%)@8DPSK	-	-	-77	dBm
C/I Performance (BER≦0.1%) *12)				
(a) co-channel	-	-	11	dB
(b) 1MHz	-	-	0	dB
(c) 2MHz	-	-	-30	dB
(d) 3MHz	-	-	-40	dB
(e) image (+4MHz)	-	-	-9	dB
(f) image +/- 1MHz	-	-	-20	dB
Maximum Input Level (BER≦0.1%)	-20	-	-	dBm

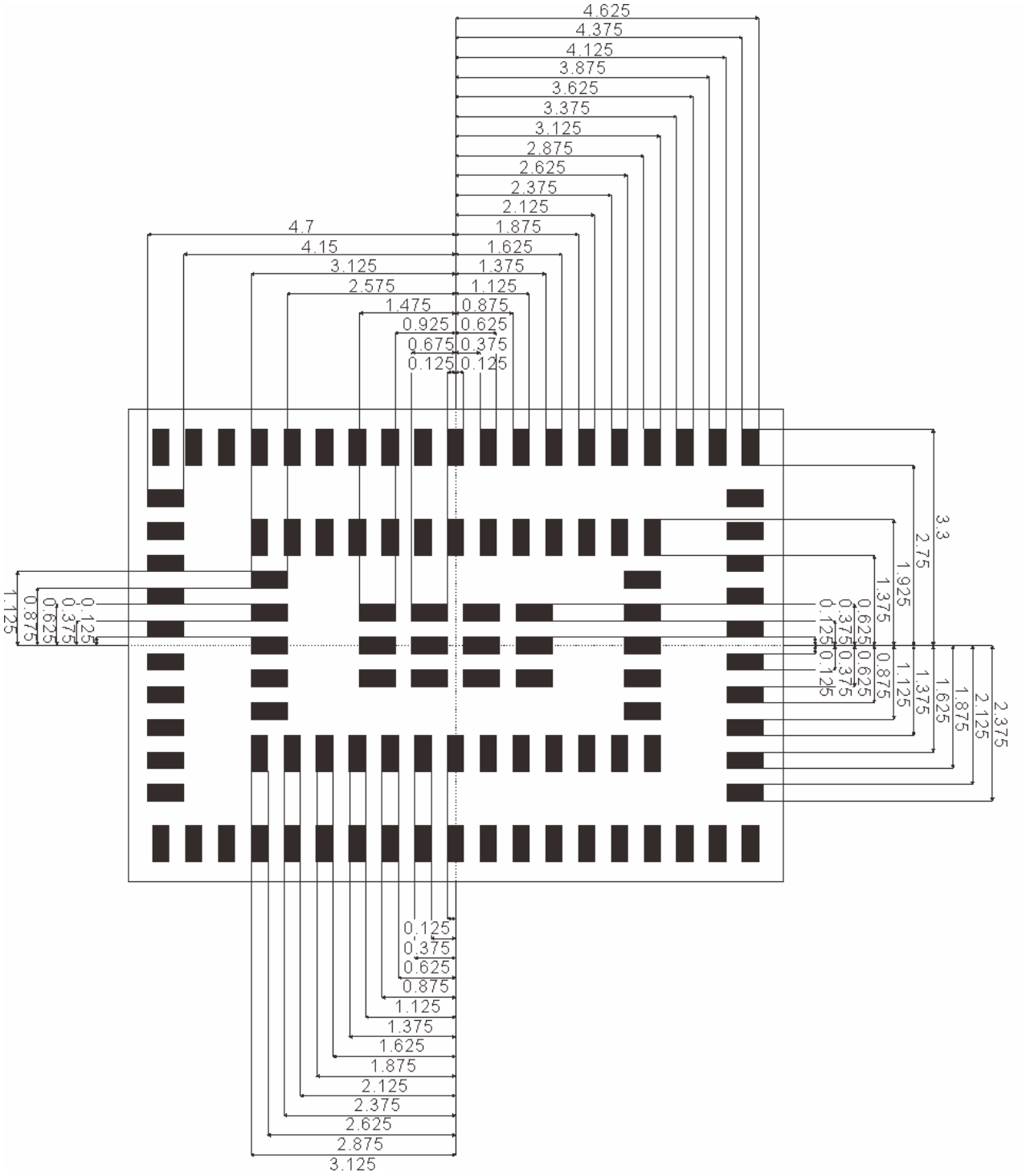
*11): Up to three spurious responses within Bluetooth limits are allowed.
*12): Up to five spurious responses within Bluetooth limits are allowed.

13.8. DC/RF Characteristics for Bluetooth (LE)

Conditions : 25deg.C, VBAT=3.3V, VDDIO= 1.8V

Items	Contents			
Bluetooth specification (power class)	Version 5.0(LE)			
Channel frequency (spacing)	2402 to 2480 MHz (2MHz)			
Number of RF Channel	40			
Item / Condition	**Min.**	**Typ.**	**Max.**	**Unit**
Center Frequency	2402	-	2480	MHz
Channel Spacing	-	2	-	MHz
Number of RF channel	-	40	-	-
Output power	2	-	9	dBm
Modulation Characteristics				
1) $\Delta f1_{avg}$	225	-	275	kHz
2) $\Delta f2_{max}$ (at 99.9%)	185	-	-	kHz
3) $\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8	-	-	-
Carrier frequency offset and drift				
1) Frequency offset	-	-	150	kHz
2) Frequency drift	-	-	50	kHz
3) Drift rate	-	-	20	kHz
Receiver sensitivity (PER < 30.8%)	-	-	-70	dBm
Maximum input signal level (PER < 30.8%)	-10	-	-	dBm
PER Report Integrity (-30dBm input)	50	-	65.4	%

14. LAND PATTERN (TOP VIEW)



* To avoid the short-circuit between the side shielding and a solder on the module land after the reflow, please locate the module land away from module outline as above figure.

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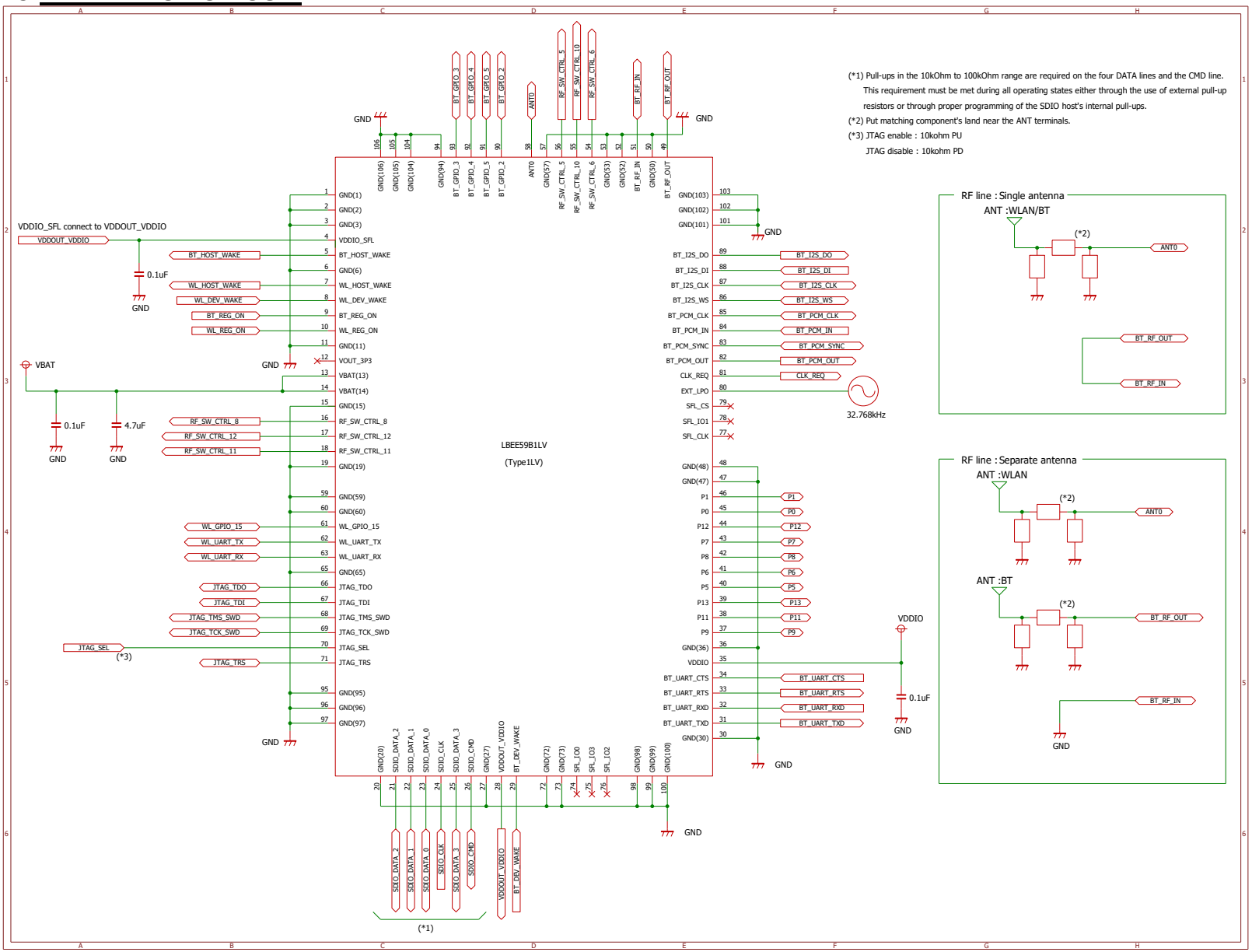
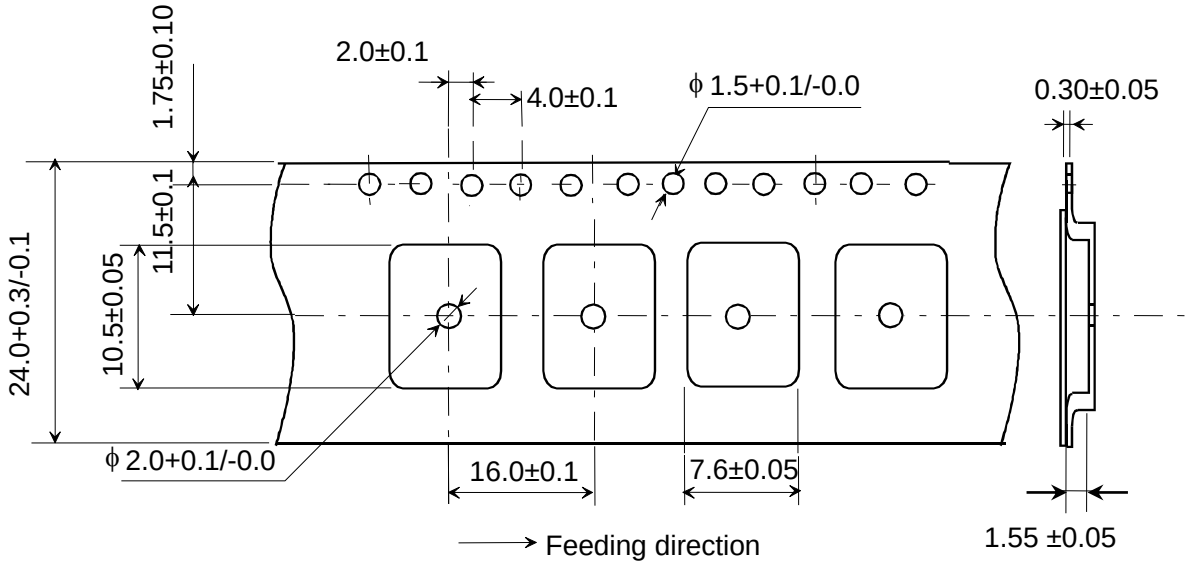
15. REFERENCE CIRCUIT

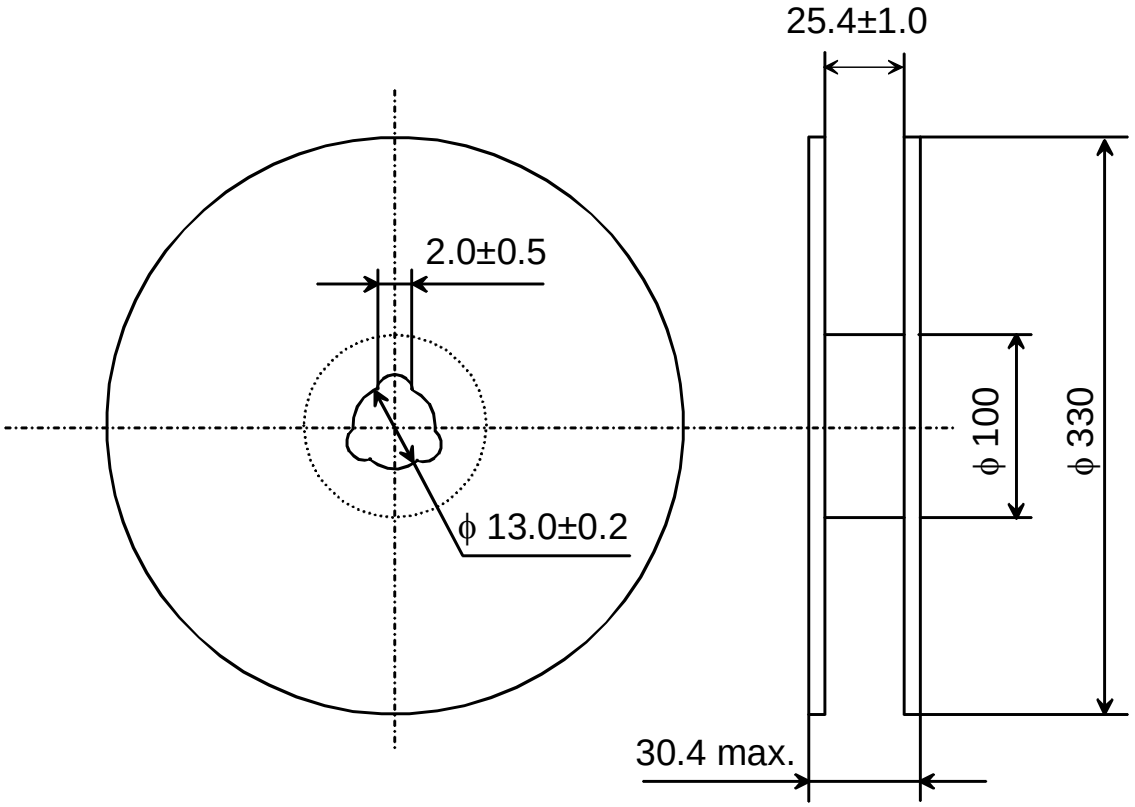


16. TAPE AND REEL PACKING

(1) Dimensions of Tape (Plastic tape)

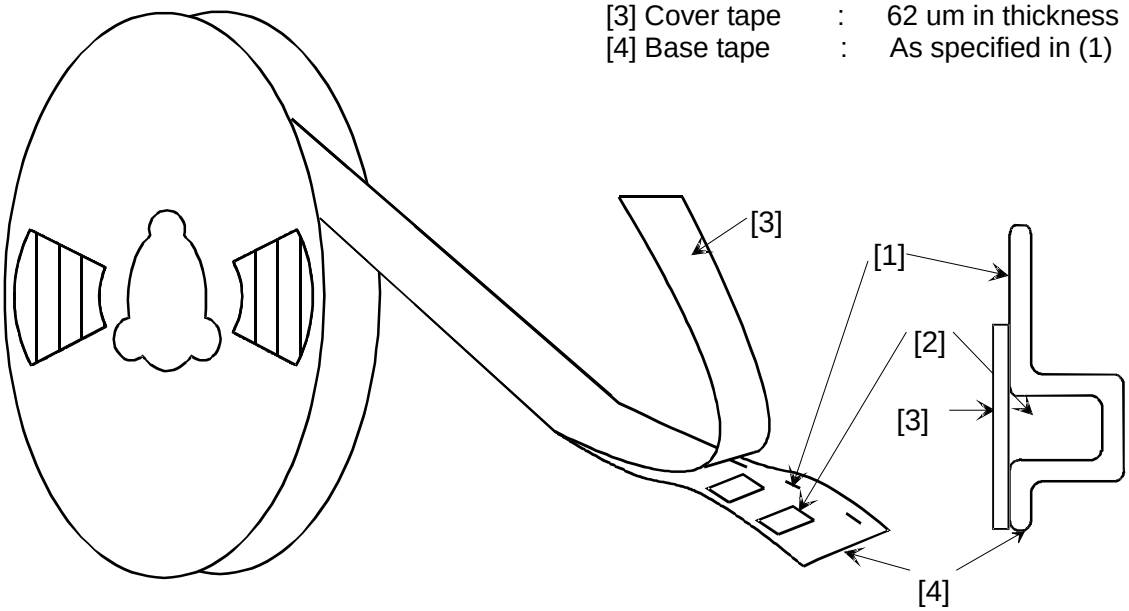


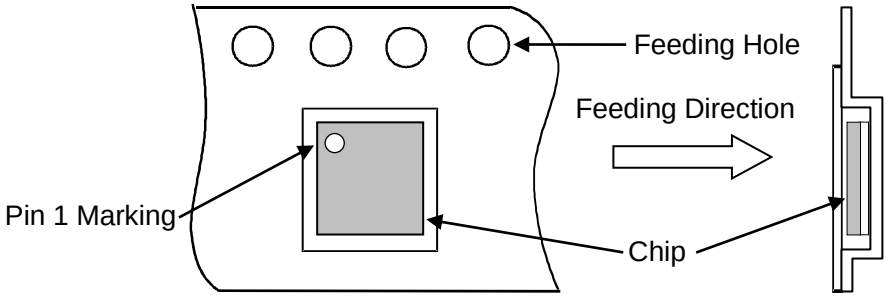
(2) Dimensions of Reel



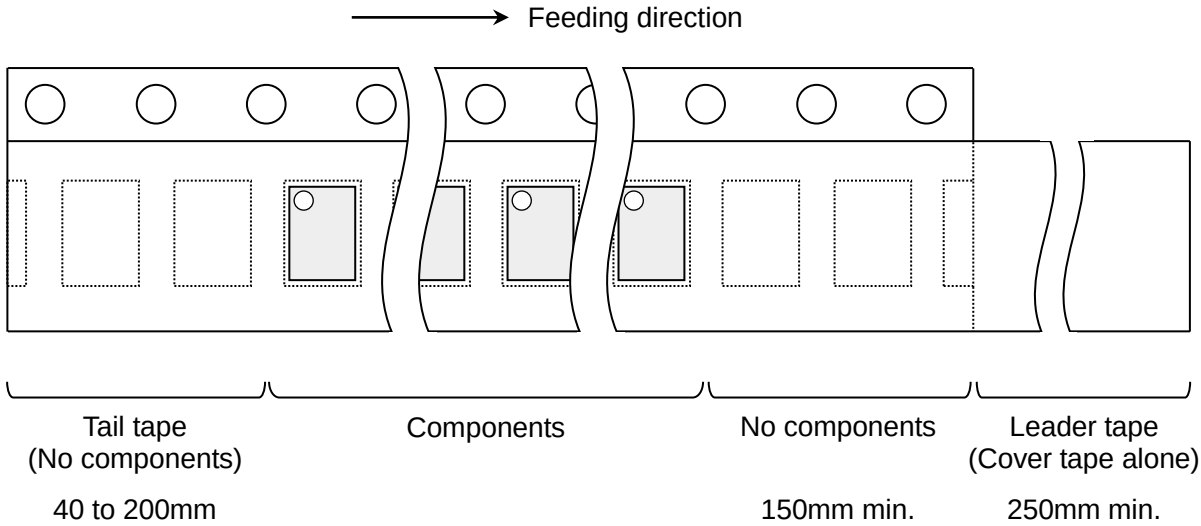
(3) Taping Diagrams

[1] Feeding Hole : As specified in (1)
[2] Hole for chip : As specified in (1)
[3] Cover tape : 62 um in thickness
[4] Base tape : As specified in (1)





(4) Leader and Tail tape



(5) The tape for chips are wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.

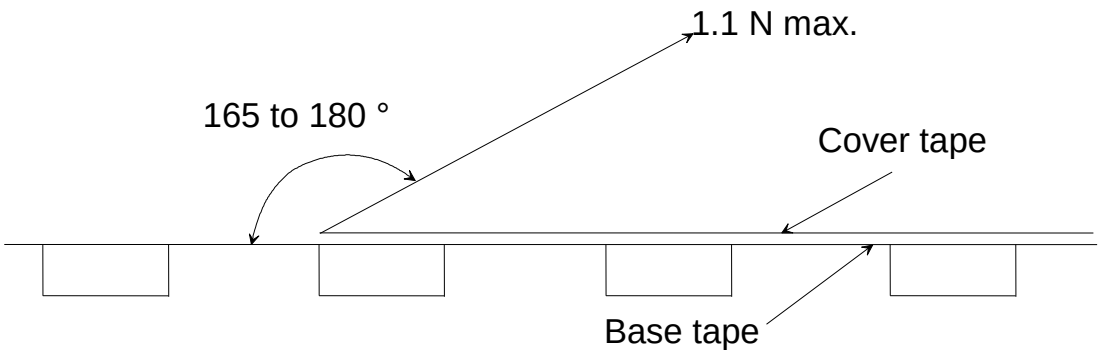
(6) The cover tape and base tape are not adhered at no components area for 250mm min.

(7) Tear off strength against pulling of cover tape: 5N min.

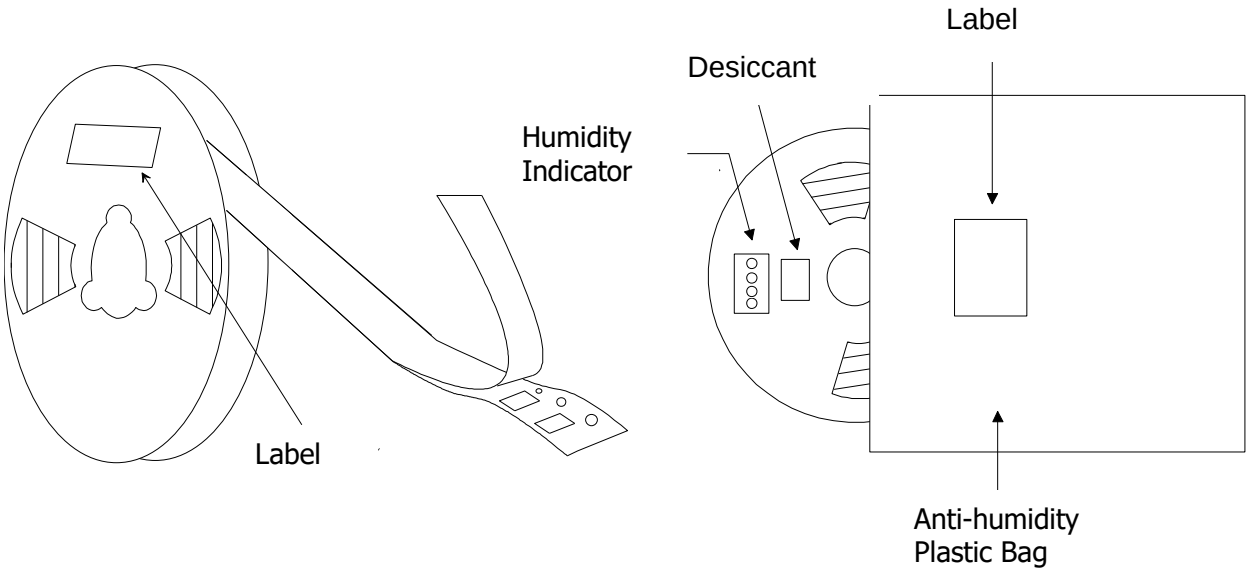
(8) Packaging unit : 1000pcs./ reel

(9) material - Base tape : Plastic
Real : Plastic
Cover tape, cavity tape and reel are made the anti-static processing.

(10) Peeling of force: 1.1N max. in the direction of peeling as shown below.



(11) PACKAGE (Humidity proof packing)



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

17. NOTICE

17.1. Storage Conditions:

Please use this product within 6month after receipt.
- The product shall be stored without opening the packing under the ambient temperature from 5 to 35deg.C and humidity from 20 to 70%RH.
(Packing materials, in particular, may be deformed at the temperature over 40deg.C.)
- The product left more than 6months after reception, it needs to be confirmed the solderbility before used.
- The product shall be stored in non corrosive gas (Cl_2, NH_3, SO_2, No_x, etc.).
- Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object and dropping the product, shall not be applied in order not to damage the packing materials.

This product is applicable to MSL3 (Based on JEDEC Standard J-STD-020)
- After the packing opened, the product shall be stored at ≦30deg.C / ≦60%RH and the product shall be used within 168hours.
- When the color of the indicator in the packing changed, the product shall be baked before soldering.

Baking condition: 125+5/-0deg.C, 24hours, 1time
The products shall be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) are not heat-resistant.

17.2. Handling Conditions:

Be careful in handling or transporting products because excessive stress or mechanical shock may break products.

Handle with care if products may have cracks or damages on their terminals, the characteristics of products may change. Do not touch products with bear hands that may result in poor solder ability and destroy by static electrical charge.

17.3. Standard PCB Design (Land Pattern and Dimensions):

All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.

The recommended land pattern and dimensions is as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

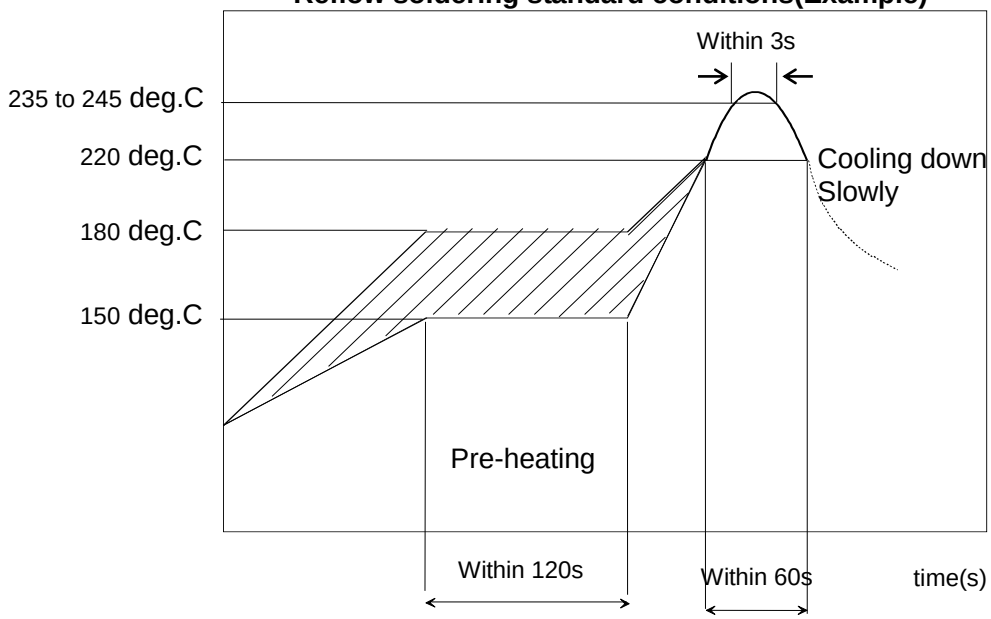
17.4. Notice for Chip Placer:

When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

17.5. Soldering Conditions:

The recommendation conditions of soldering are as in the following figure.
Soldering must be carried out by the above mentioned conditions to prevent products from damage. Set up the highest temperature of reflow within 260 °C. Contact Murata before use if concerning other soldering conditions.

Reflow soldering standard conditions(Example)



Please use the reflow within 2 times.
Use rosin type flux or weakly active flux with a chlorine content of 0.2 wt % or less.

17.6. Cleaning:

Since this Product is Moisture Sensitive, any cleaning is not recommended. If any cleaning process is done the customer is responsible for any issues or failures caused by the cleaning process.

17.7. Operational Environment Conditions:

Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity and pressure). Therefore, products have no problems to be used under the similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.

- In an atmosphere containing corrosive gas (Cl_2, NH_3, SO_x, NO_x etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.

If there are possibilities for products to be used under the preceding clause, consult with Murata before actual use.

As it might be a cause of degradation or destruction to apply static electricity to products, do not apply static electricity or excessive voltage while assembling and measuring.

17.8. Input Power Capacity:

Products shall be used in the input power capacity as specified in this specifications.
Inform Murata beforehand, in case that the components are used beyond such input power capacity range.

18. PRECONDITION TO USE OUR PRODUCTS

PLEASE READ THIS NOTICE BEFORE USING OUR PRODUCTS.

Please make sure that your product has been evaluated and confirmed from the aspect of the fitness for the specifications of our product when our product is mounted to your product.
All the items and parameters in this product specification/datasheet/catalog have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment specified in this specification. You are requested not to use our product deviating from the condition and the environment specified in this specification.
Please note that the only warranty that we provide regarding the products is its conformance to the specifications provided herein. Accordingly, we shall not be responsible for any defects in products or equipment incorporating such products, which are caused under the conditions other than those specified in this specification.
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The product shall not be used in any application listed below which requires especially high reliability for the prevention of such defect as may directly cause damage to the third party's life, body or property. You acknowledge and agree that, if you use our products in such applications, we will not be responsible for any failure to meet such requirements. Furthermore, YOU AGREE TO INDEMNIFY AND DEFEND US AND OUR AFFILIATES AGAINST ALL CLAIMS, DAMAGES, COSTS, AND EXPENSES THAT MAY BE INCURRED, INCLUDING WITHOUT LIMITATION, ATTORNEY FEES AND COSTS, DUE TO THE USE OF OUR PRODUCTS AND THE SOFTWARE IN SUCH APPLICATIONS.

- Aircraft equipment. - Aerospace equipment - Undersea equipment.
- Power plant control equipment - Medical equipment.
- Transportation equipment (vehicles, trains, ships, elevator, etc.).
- Traffic signal equipment. - Disaster prevention / crime prevention equipment.
- Burning / explosion control equipment
- Application of similar complexity and/ or reliability requirements to the applications listed in the above.

We expressly prohibit you from analyzing, breaking, reverse-engineering, remodeling altering, and reproducing our product. Our product cannot be used for the product which is prohibited from being manufactured, used, and sold by the regulations and laws in the world.
We do not warrant or represent that any license, either express or implied, is granted under any our patent right, copyright, mask work right, or our other intellectual property right relating to any combination, machine, or process in which our products or services are used. Information provided by us regarding third-party products or services does not constitute a license from us to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from us under our patents or other intellectual property.
Please do not use our products, our technical information and other data provided by us for the purpose of developing of mass-destruction weapons and the purpose of military use.
Moreover, you must comply with "foreign exchange and foreign trade law", the "U.S. export administration regulations", etc.
Please note that we may discontinue the manufacture of our products, due to reasons such as end of supply of materials and/or components from our suppliers.
By signing on specification sheet or approval sheet, you acknowledge that you are the legal representative for your company and that you understand and accept the validity of the contents herein. When you are not able to return the signed version of specification sheet or approval sheet within 30 days from receiving date of specification sheet or approval sheet, it shall be deemed to be your consent on the content of specification sheet or approval sheet. Customer acknowledges that engineering samples may deviate from specifications and may contain defects due to their development status. We reject any liability or product warranty for engineering samples. In particular we disclaim liability for damages caused by
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