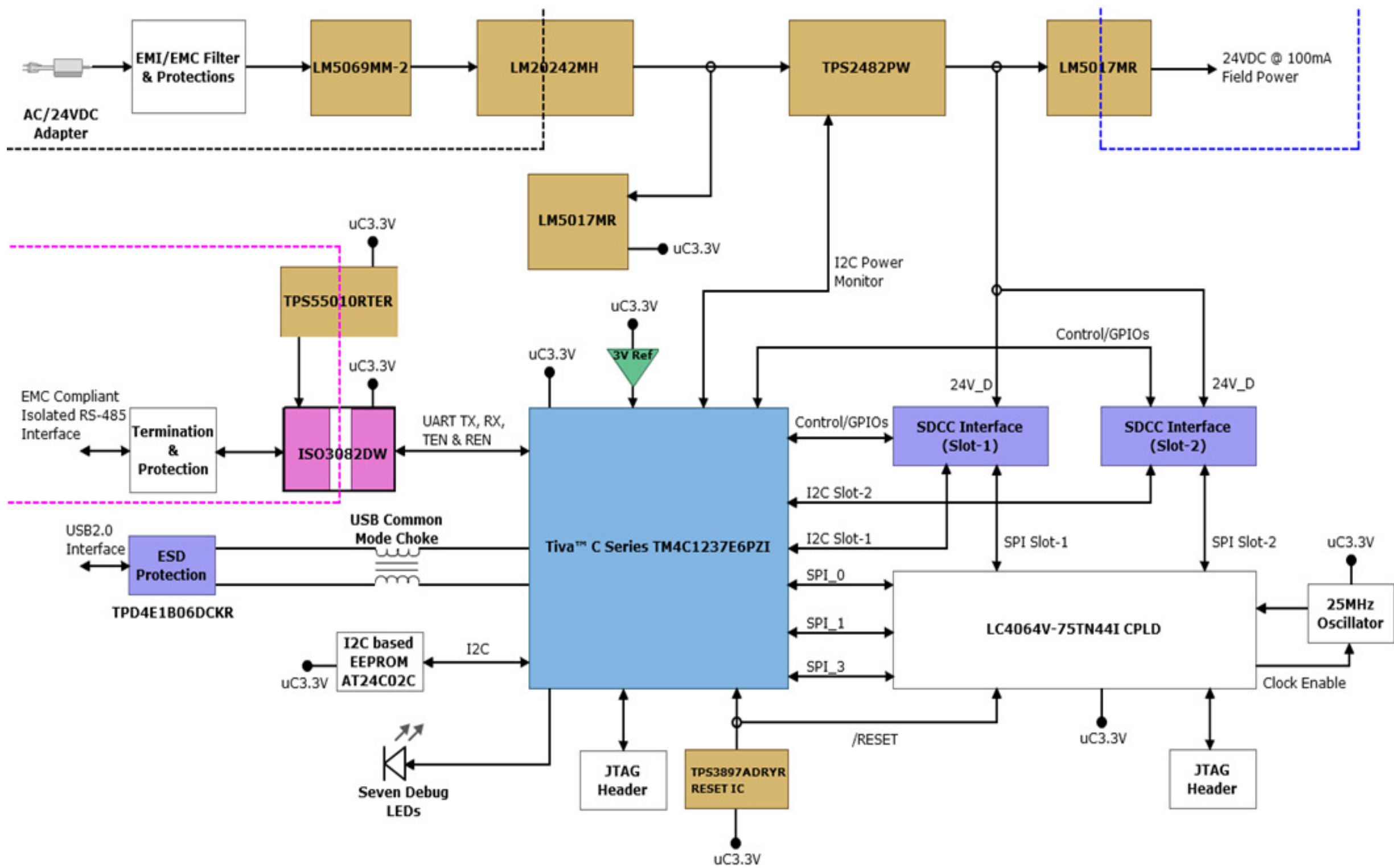
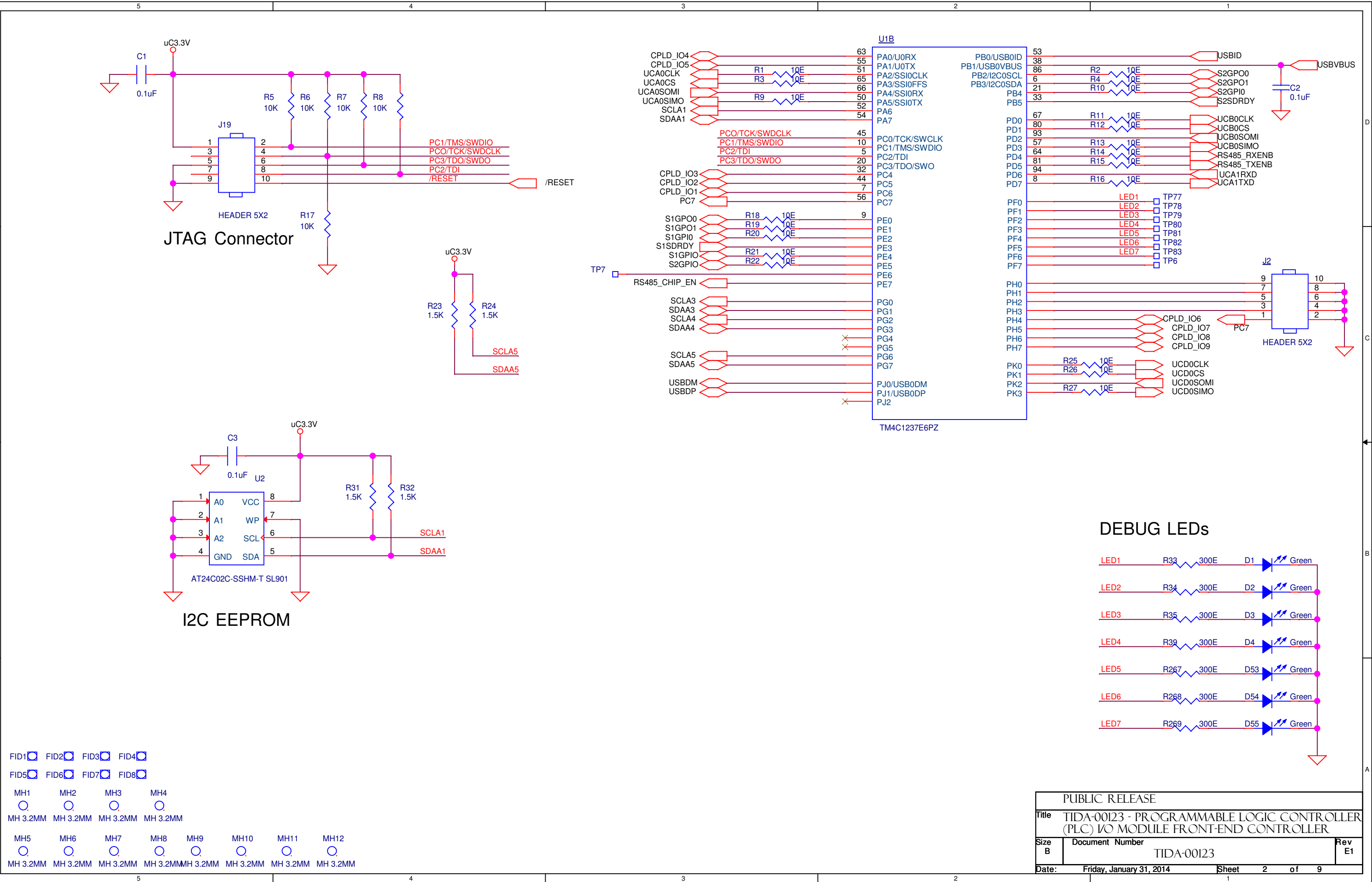


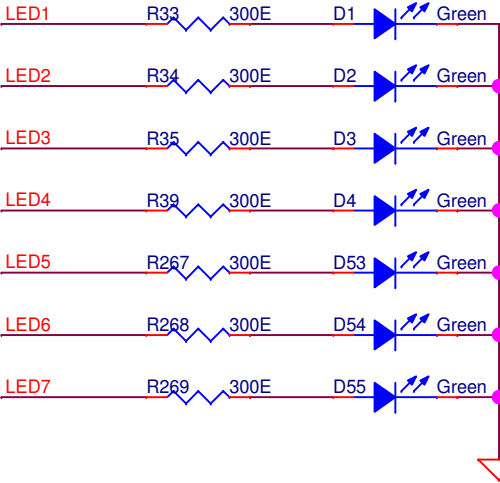
BLOCK DIAGRAM:



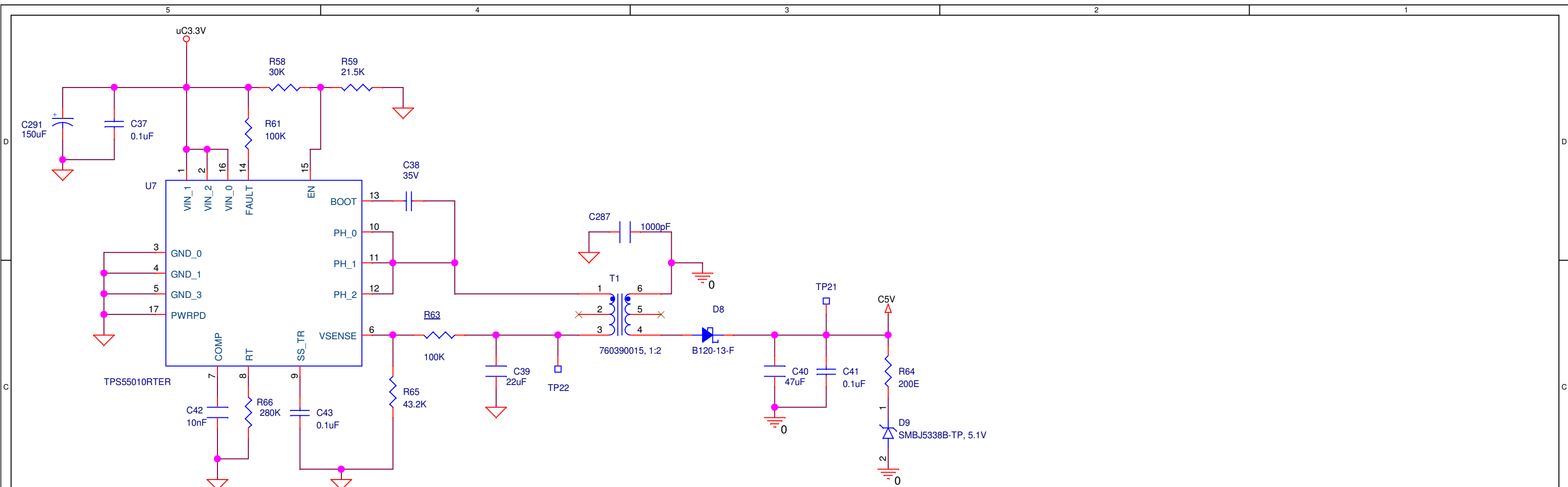
PUBLIC RELEASE		
Title	TIDA-00123 - PROGRAMMABLE LOGIC CONTROLLER (PLC) I/O MODULE FRONT-END CONTROLLER	
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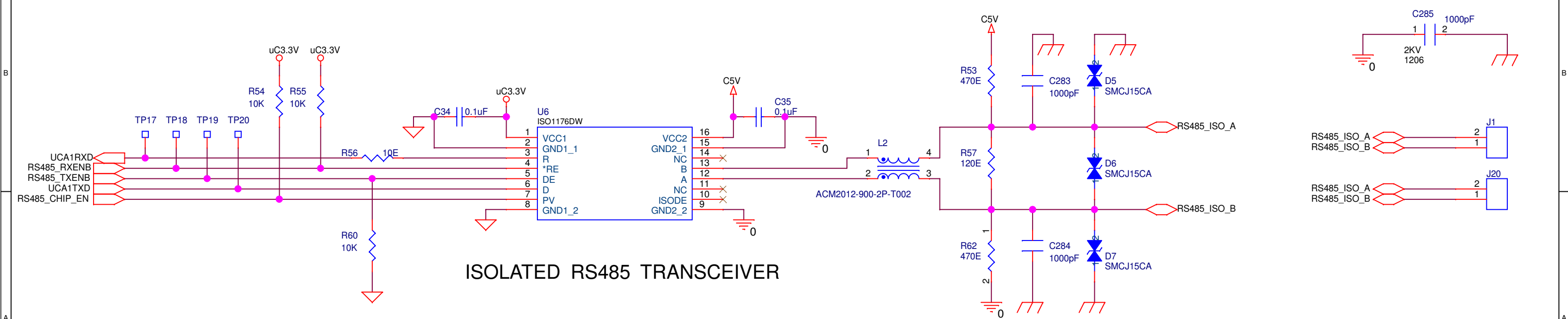
DEBUG LEDs



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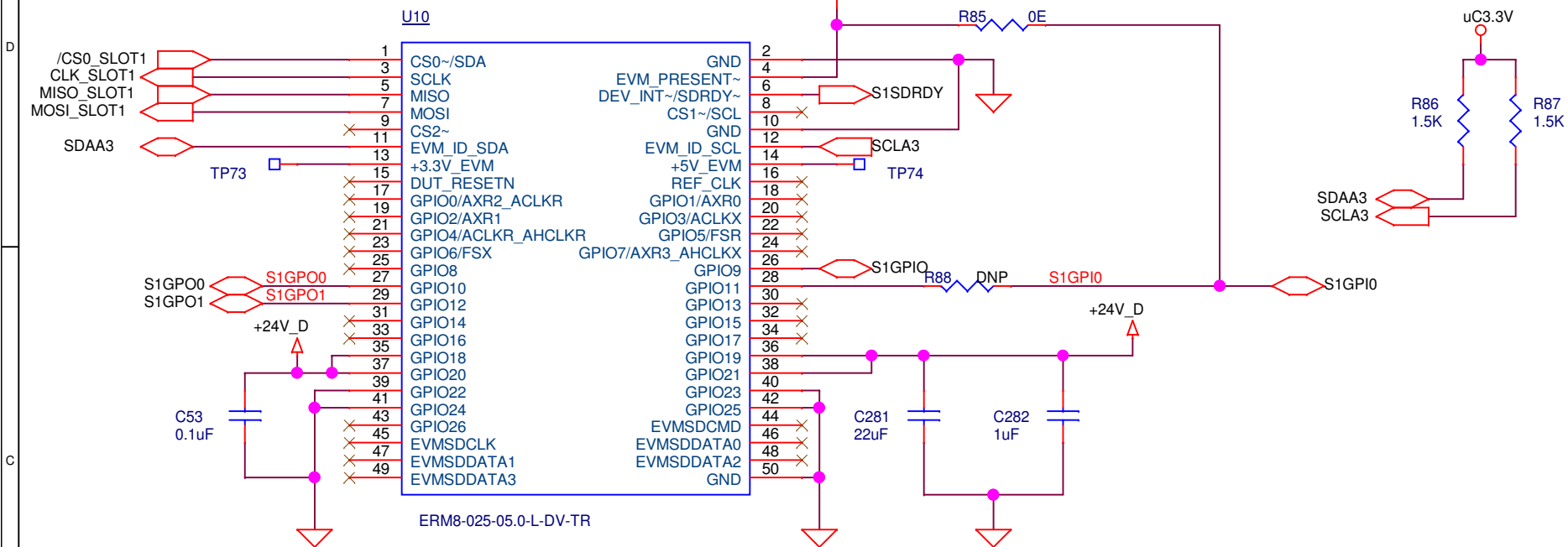
ISOLATED DC/DC CONVERTER FOR RS485



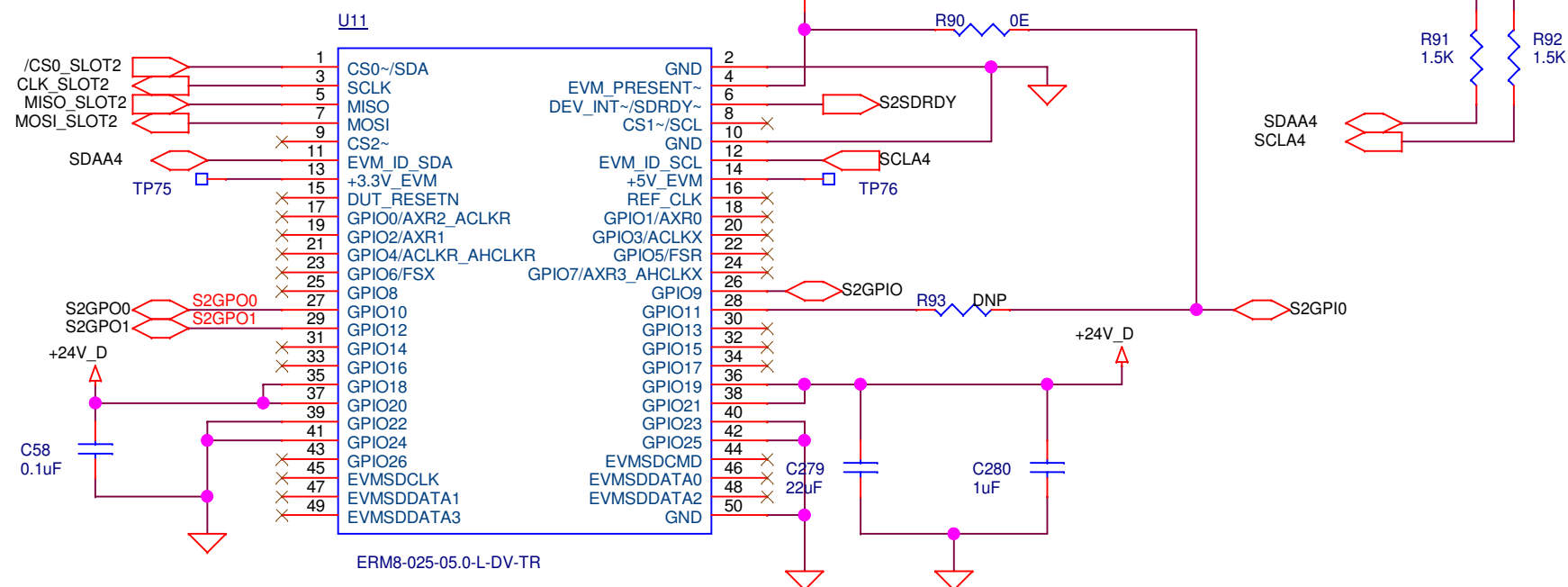
ISOLATED RS485 TRANSCEIVER

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SmartIO Interface Slot#1



SmartIO Interface Slot#2



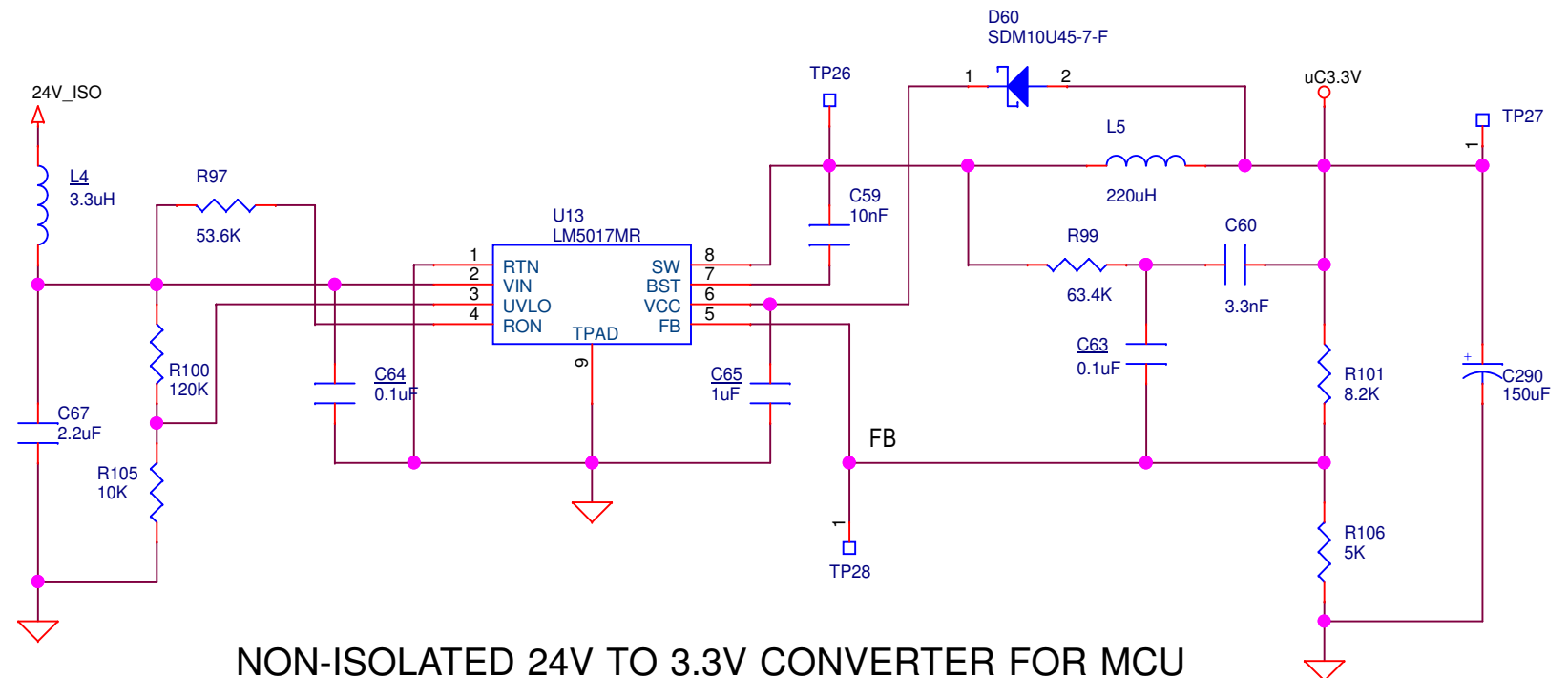
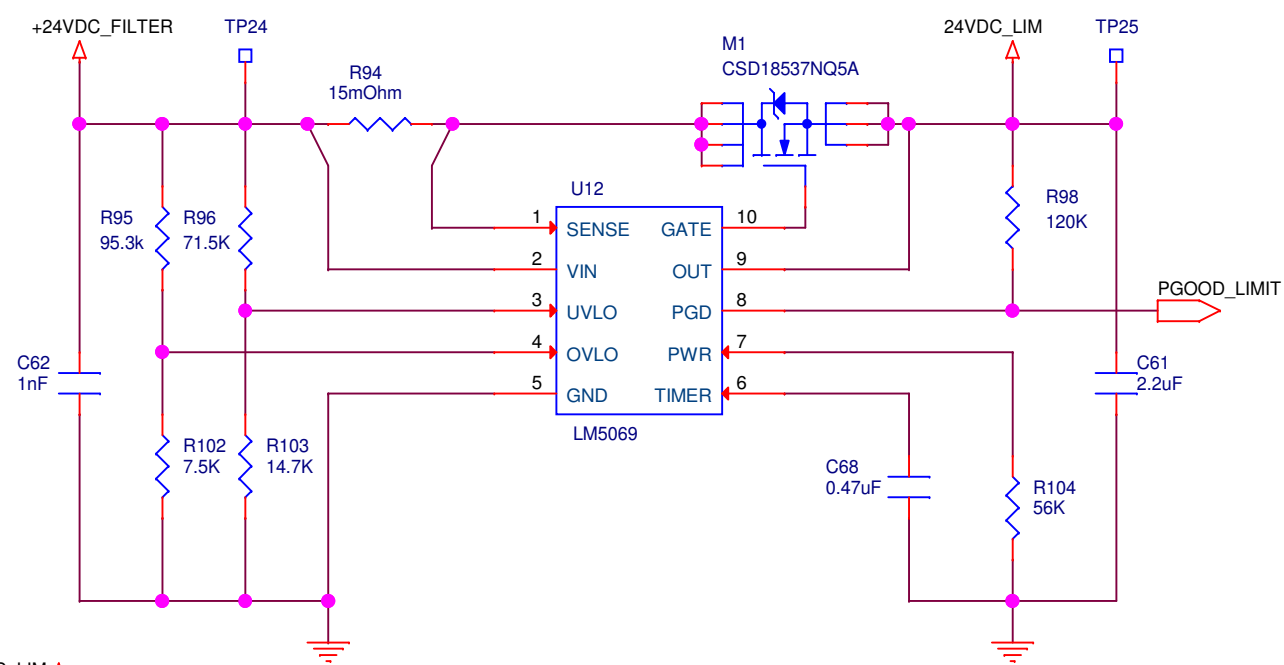
PUBLIC RELEASE

Title TIDA-00123 - PROGRAMMABLE LOGIC CONTROLLER (PLC) I/O MODULE FRONT-END CONTROLLER

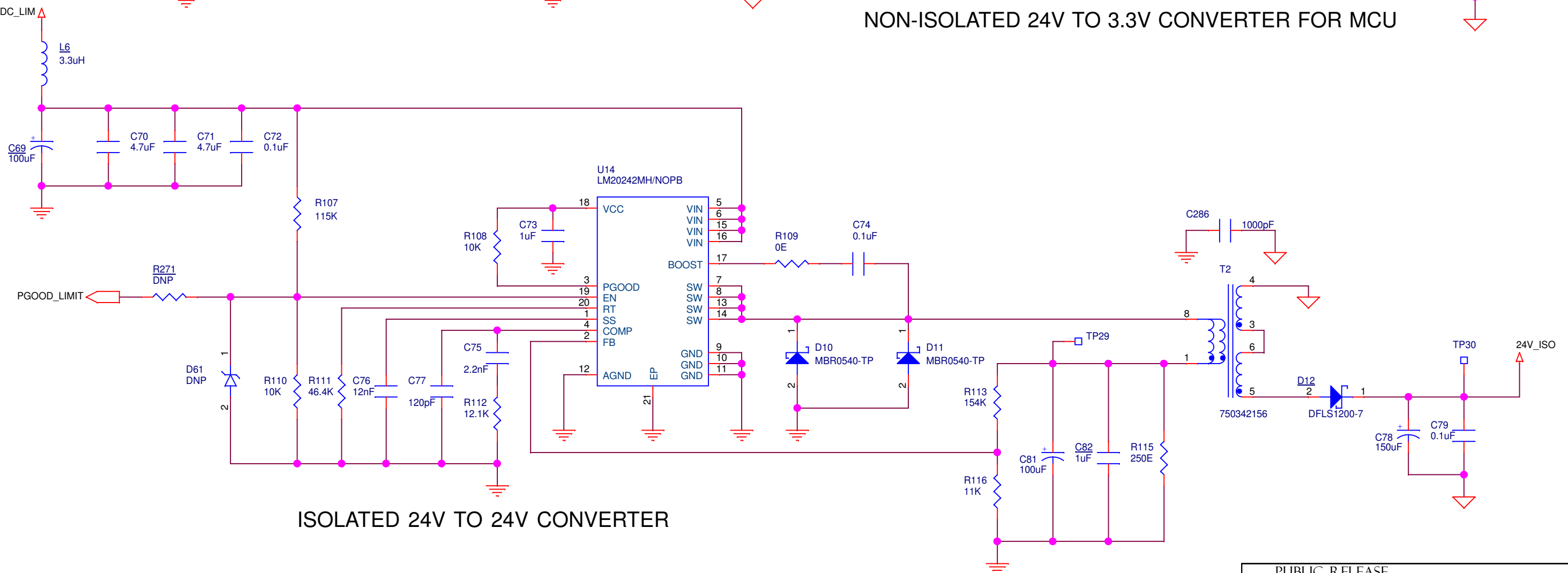
Size B Document Number TIDA-00123 Rev E1

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CURRENT LIMIT & HOT SWAP



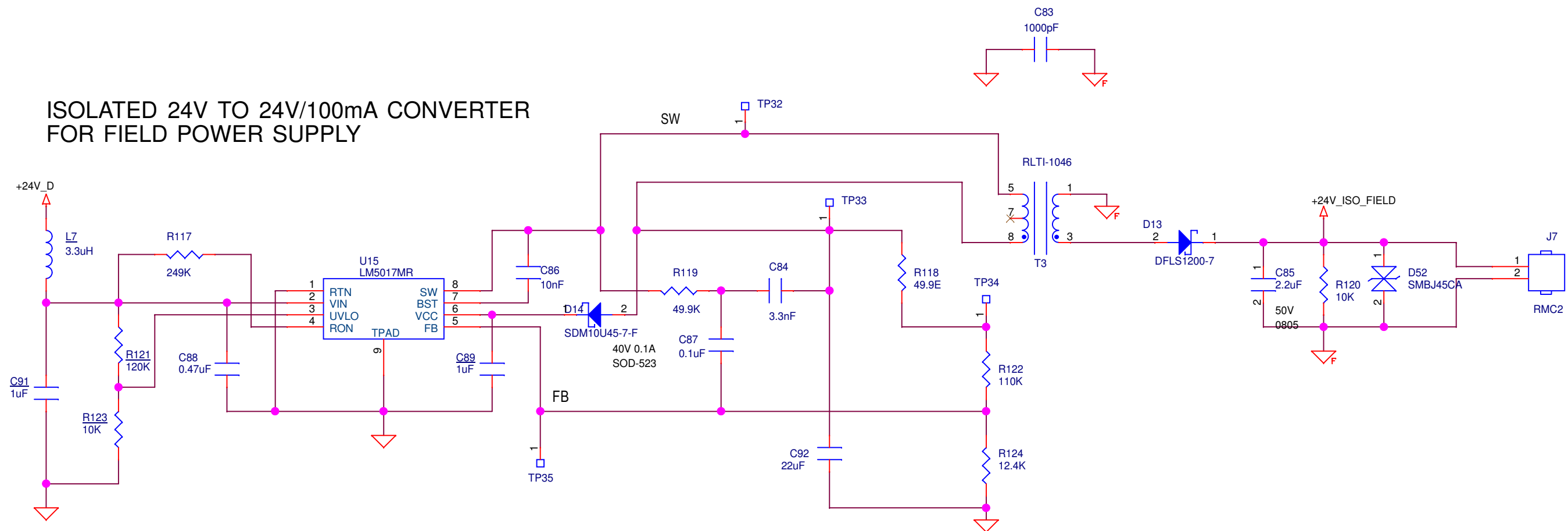
NON-ISOLATED 24V TO 3.3V CONVERTER FOR MCU



ISOLATED 24V TO 24V CONVERTER

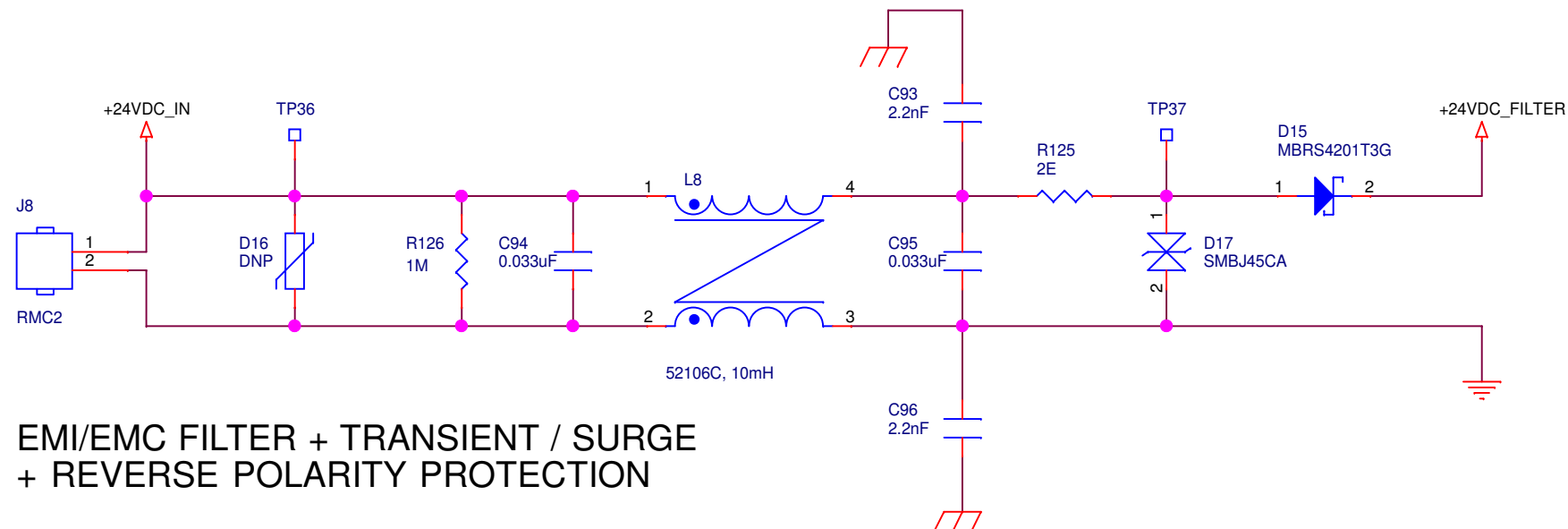
PUBLIC RELEASE			
Title	TIDA-00123 - PROGRAMMABLE LOGIC CONTROLLER (PLC) I/O MODULE FRONT-END CONTROLLER		
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ISOLATED 24V TO 24V/100mA CONVERTER FOR FIELD POWER SUPPLY



J18
RMC2
Protective Earth
or Chassis

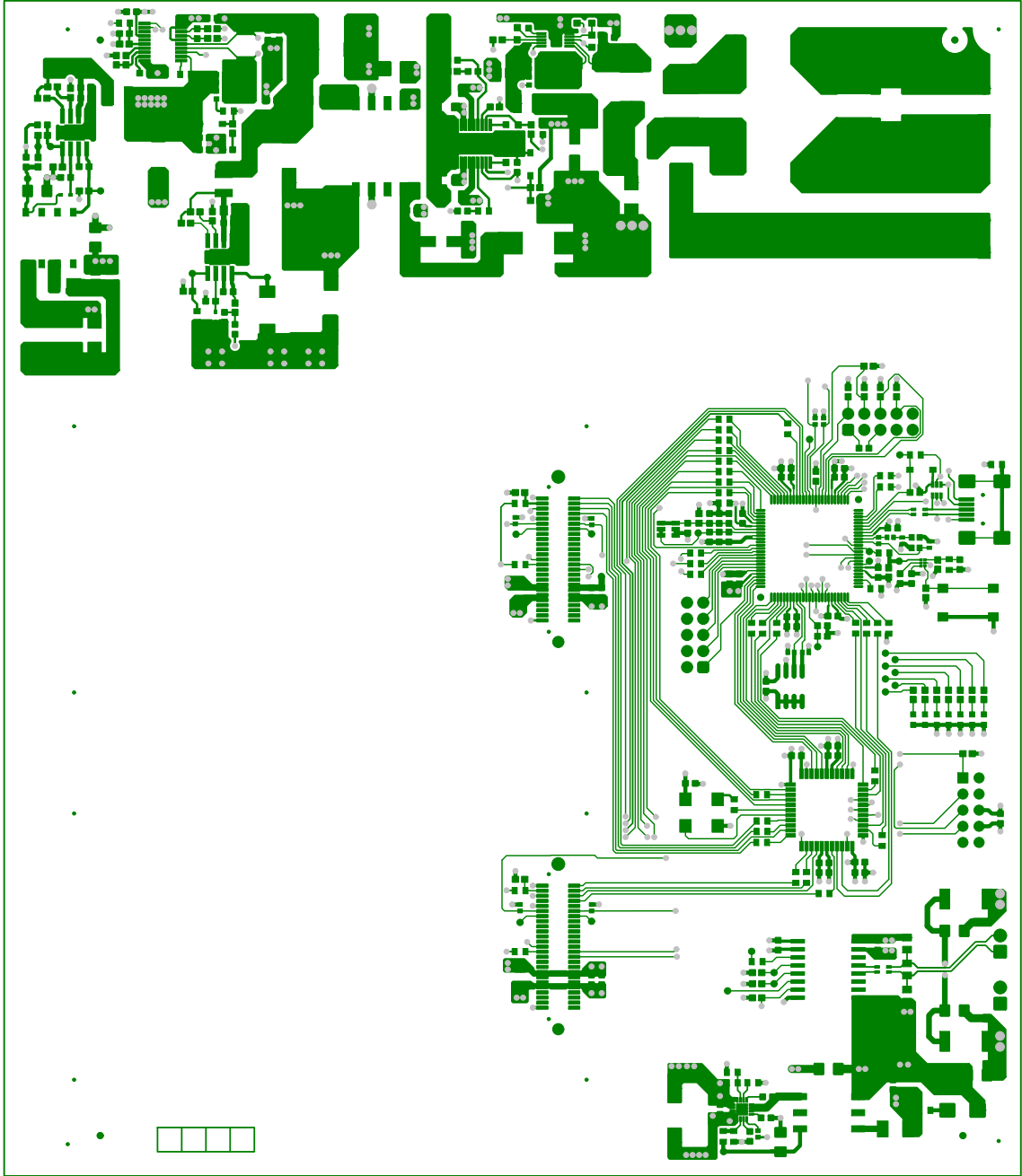
EMI/EMC FILTER + TRANSIENT / SURGE + REVERSE POLARITY PROTECTION



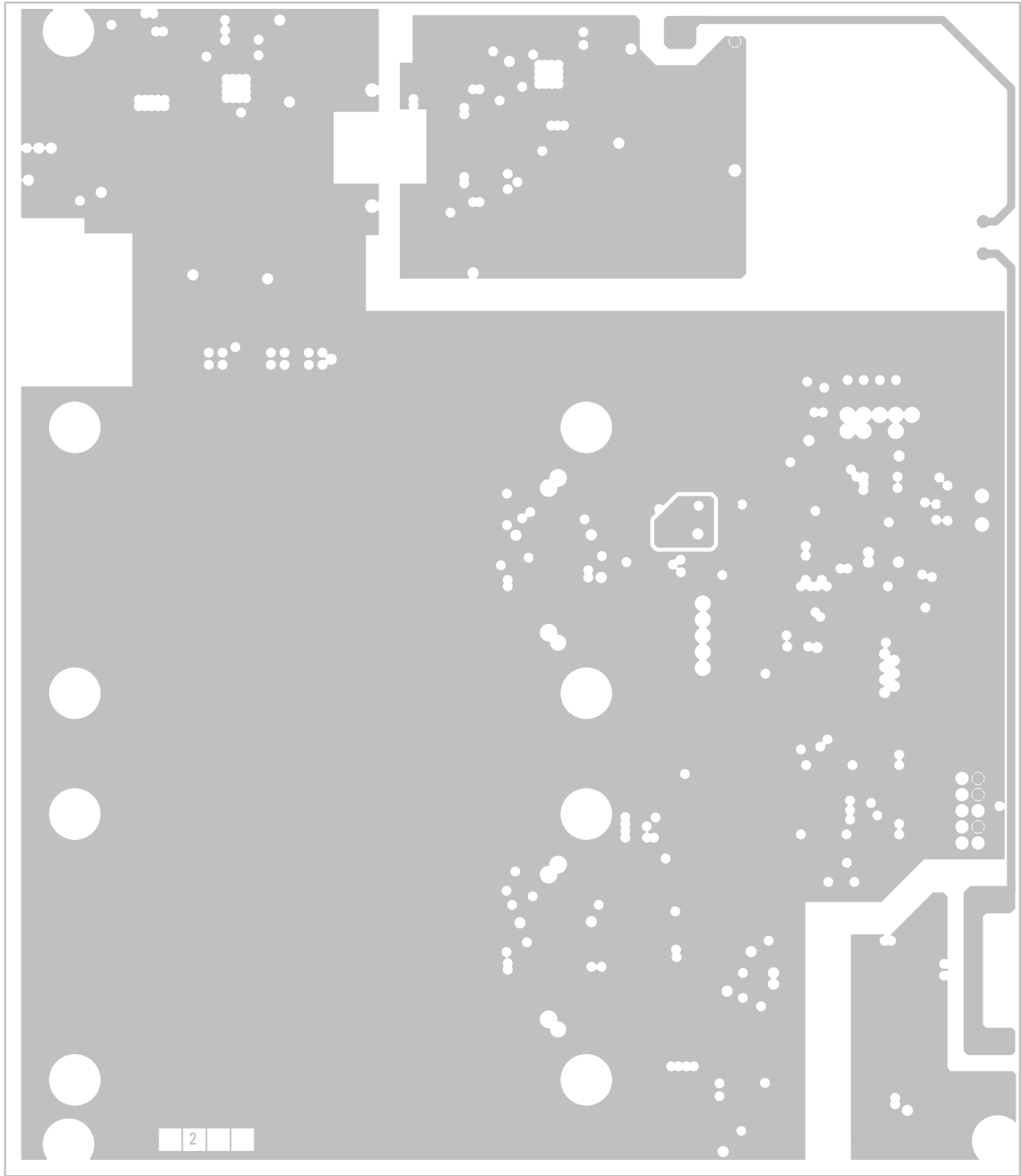
PUBLIC RELEASE		
Title	TIDA-00123 - PROGRAMMABLE LOGIC CONTROLLER (PLC) I/O MODULE FRONT-END CONTROLLER	
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The schematic diagram illustrates the circuit for the TPS2482PW (IC1). The circuit is powered by a 24V_ISO source (TP38) and a +24V_D source (TP39). The 24V_ISO source is connected to the VIN pin of the TPS2482PW through a network of capacitors (C288, C97, C98) and resistors (R134, R137). The +24V_D source is connected to the VOUT pin through a MOSFET (M3, CSD18501Q5A) and a diode (D18, BZT52C8V2-7). The TPS2482PW IC is connected to various pins including A0, A1, VINP, VINM, VS, N/C, VREF, SENSE, PROG, GATE, OUT, TIMER, and PG. The circuit includes several passive components: resistors (R127, R250, R251, R133, R138, R136, R143, R145), capacitors (C101, C102, C103, C104, C105, C106), and a diode (D18). The circuit is designed to regulate the output voltage and current, as indicated by the presence of the SENSE and PROG pins.

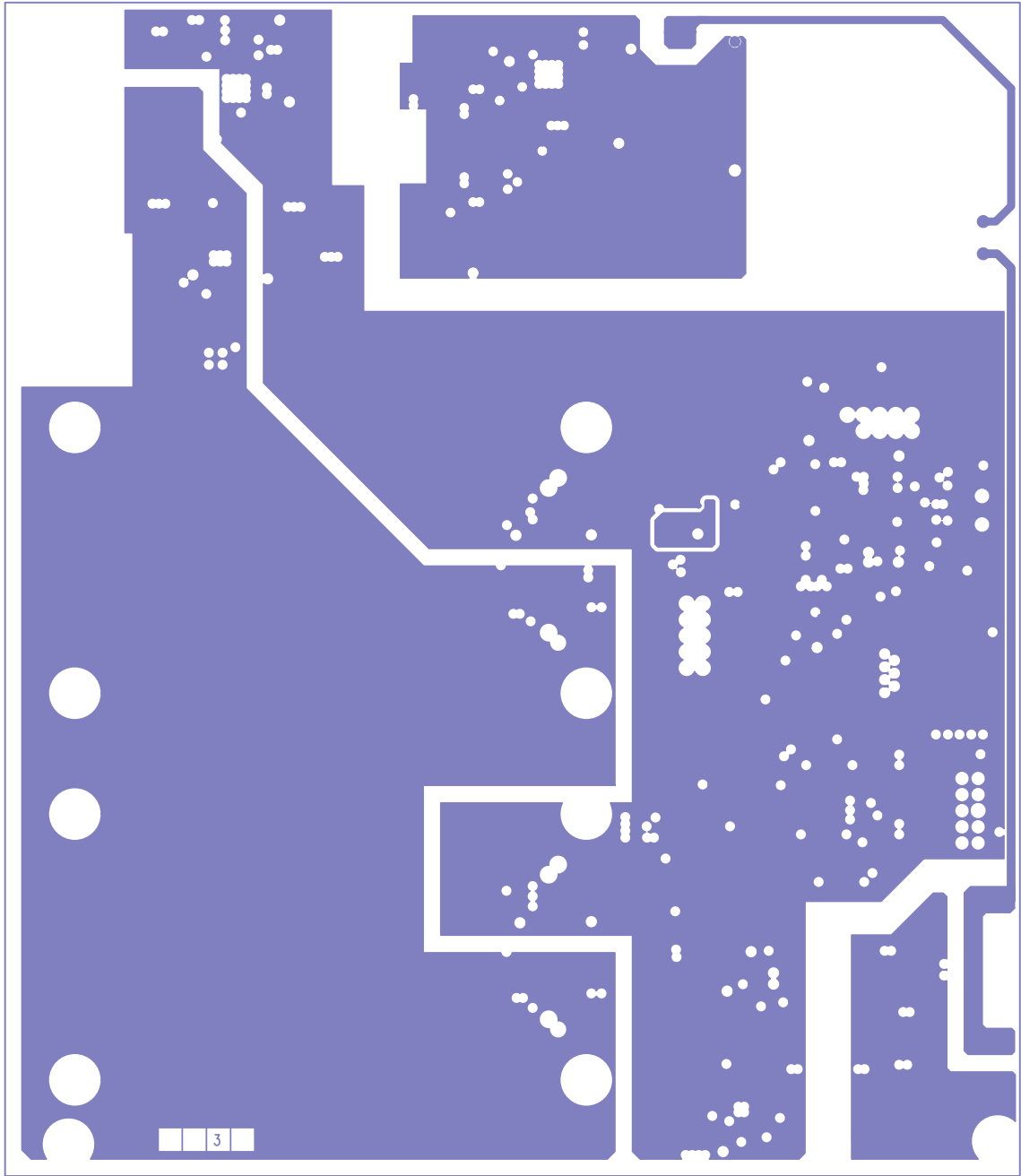
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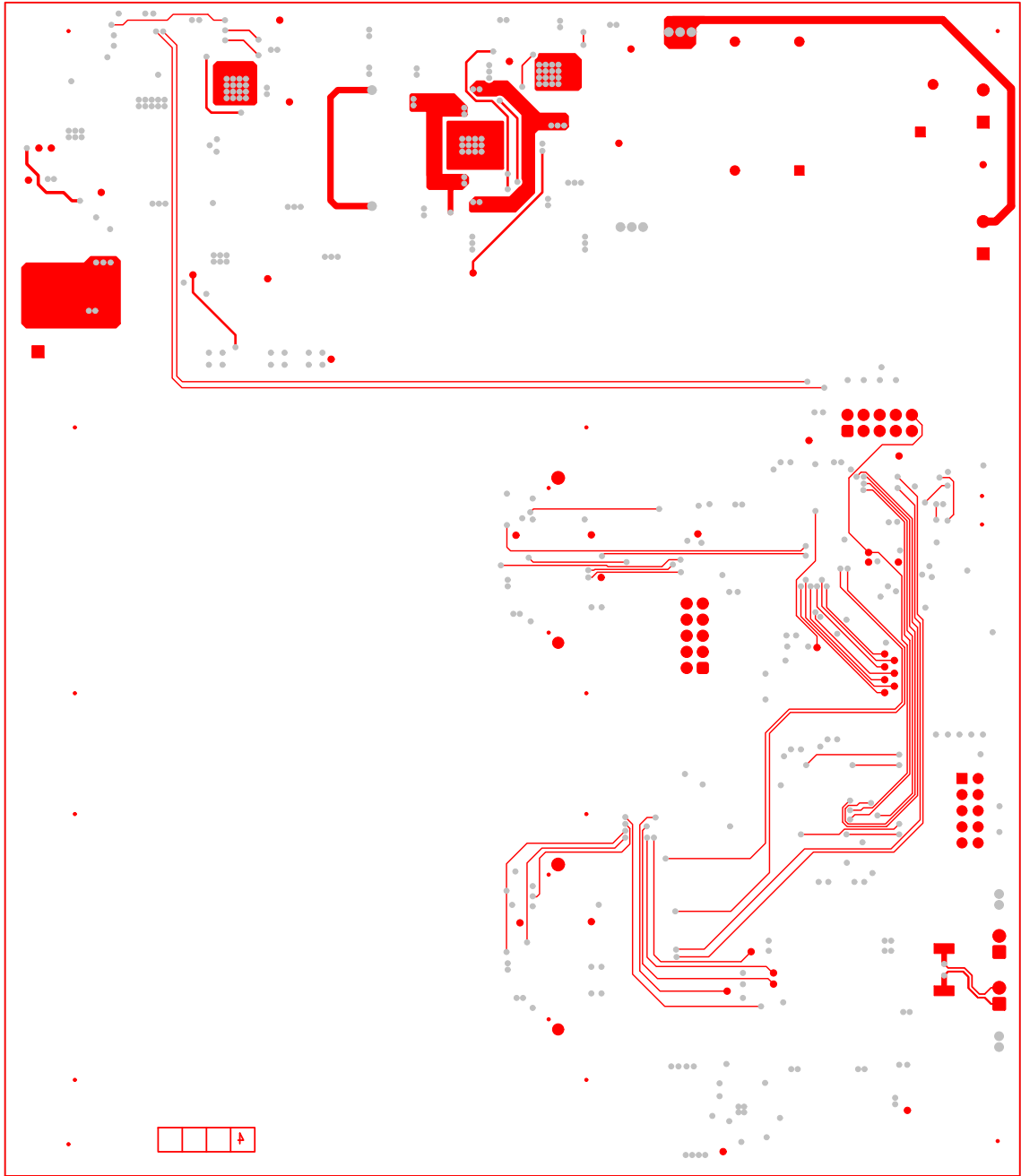
TOP LAYER



GND SPLIT PLANE



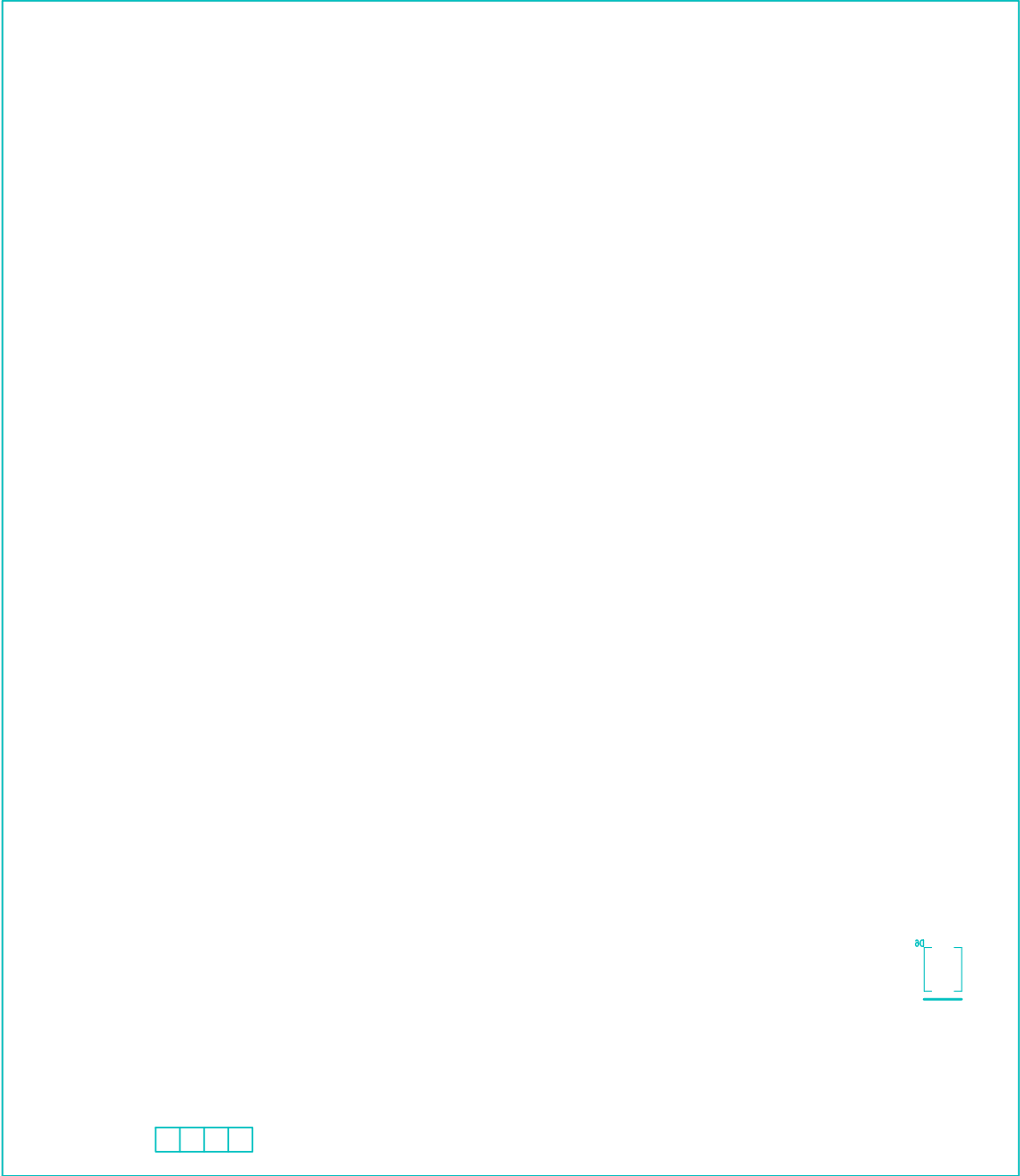
POWER SPLIT PLANE



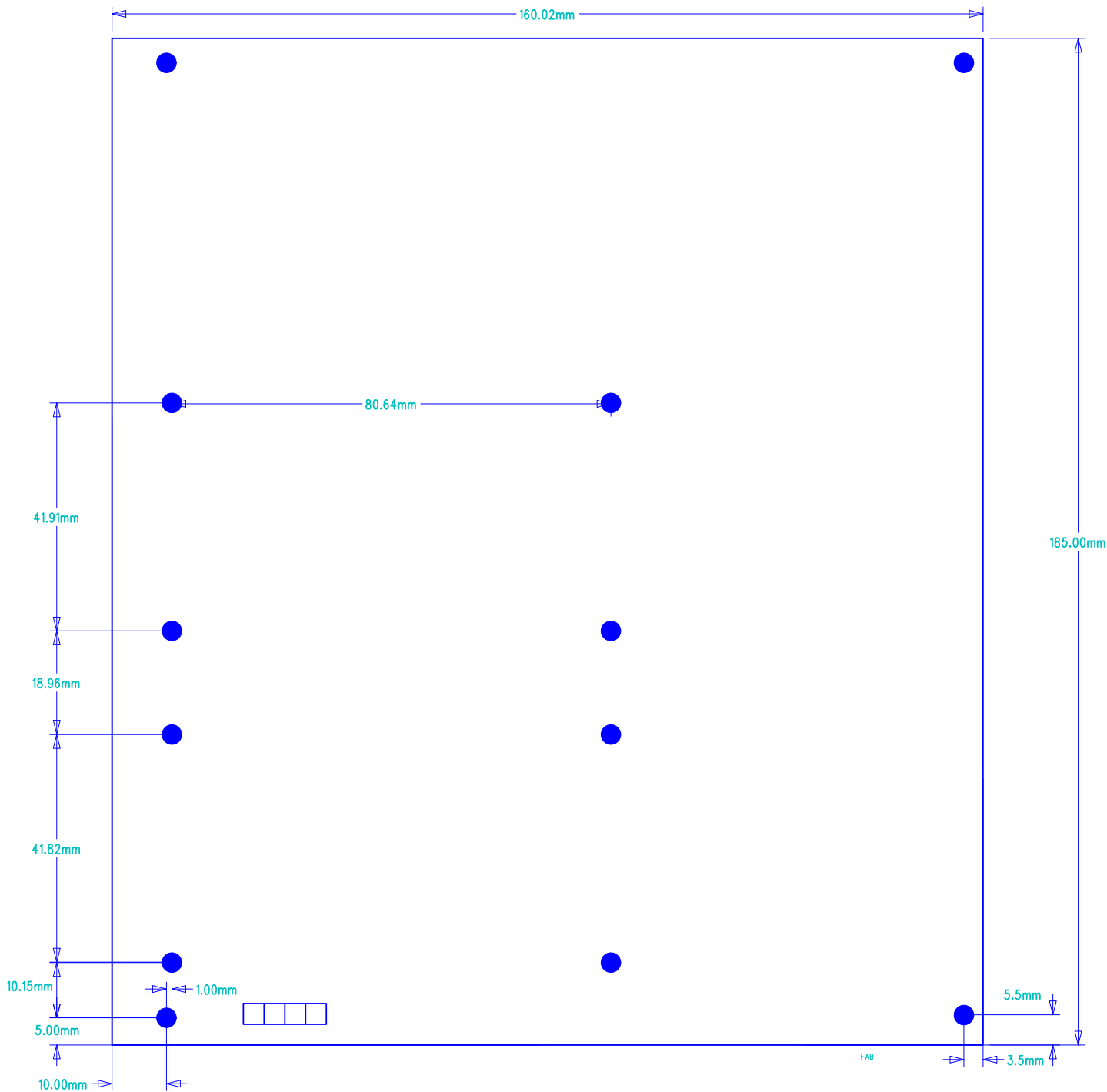
BOTTOM LAYER



SILKSCREEN TOP



SILKSCREEN BOTTOM



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