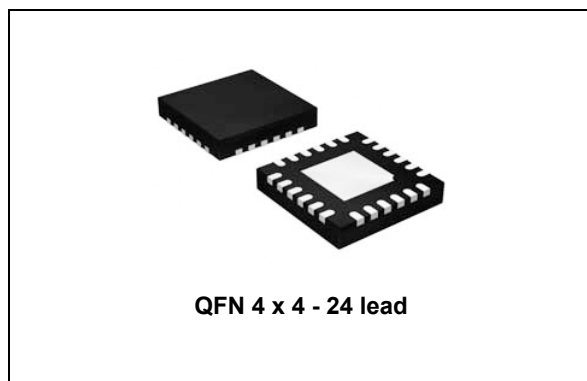


## Compact and versatile three-phase and three-sense motor driver

Datasheet - production data



### Features

- Operating voltage from 7 to 45 V
- Maximum output current 1.5 A<sub>rms</sub>
- R<sub>DSon</sub> HS + LS = 1 Ω typ.
- Supporting both single and three shunts architectures
- Current control with adjustable OFF time
- Current sensing based on external shunt resistors
- Flexible driving methodology user settable between 6 inputs (high side and low side driving) and 3 inputs (direct PWM driving)
- FOC compatible thanks to three shunts sensing topology support
- Full protections set
  - Non-dissipative overcurrent protection
  - Short-circuit protection
  - Undervoltage lockout
  - Thermal shutdown
  - Interlocking function
- Low standby current consumption

### Applications

- Industrial robotics
- Medical and health care
- Factory automation end-points
- Home appliances
- Small pumps
- Server, computing and general purpose FANs
- Office and home automation

### Description

The STSPIN830 is a compact and versatile field oriented control FOC ready three-phase motor driver. It integrates in a very small 4 x 4 mm QFN package, both the control logic and a fully protected low R<sub>DSon</sub> triple half-bridge power stage.

Thanks to a dedicated MODE input pin the device offers the freedom to decide whether to drive it through 6 inputs (one for each power switch) or a more common 3 PWM direct driving inputs.

The STSPIN830 supports both single and three shunts architectures and embeds a PWM current controller based on user settable values of reference voltage and OFF time.

The devices can be forced in a low consumption state reducing the total current consumption down to less than 45 μA.

As with all other devices from the STSPIN family, the STSPIN830 integrates a complete set of protections for the power stages (non-dissipative overcurrent, thermal shutdown, short-circuit, undervoltage lockout and interlocking) making it a bulletproof solution for the new wave of demanding industrial applications.

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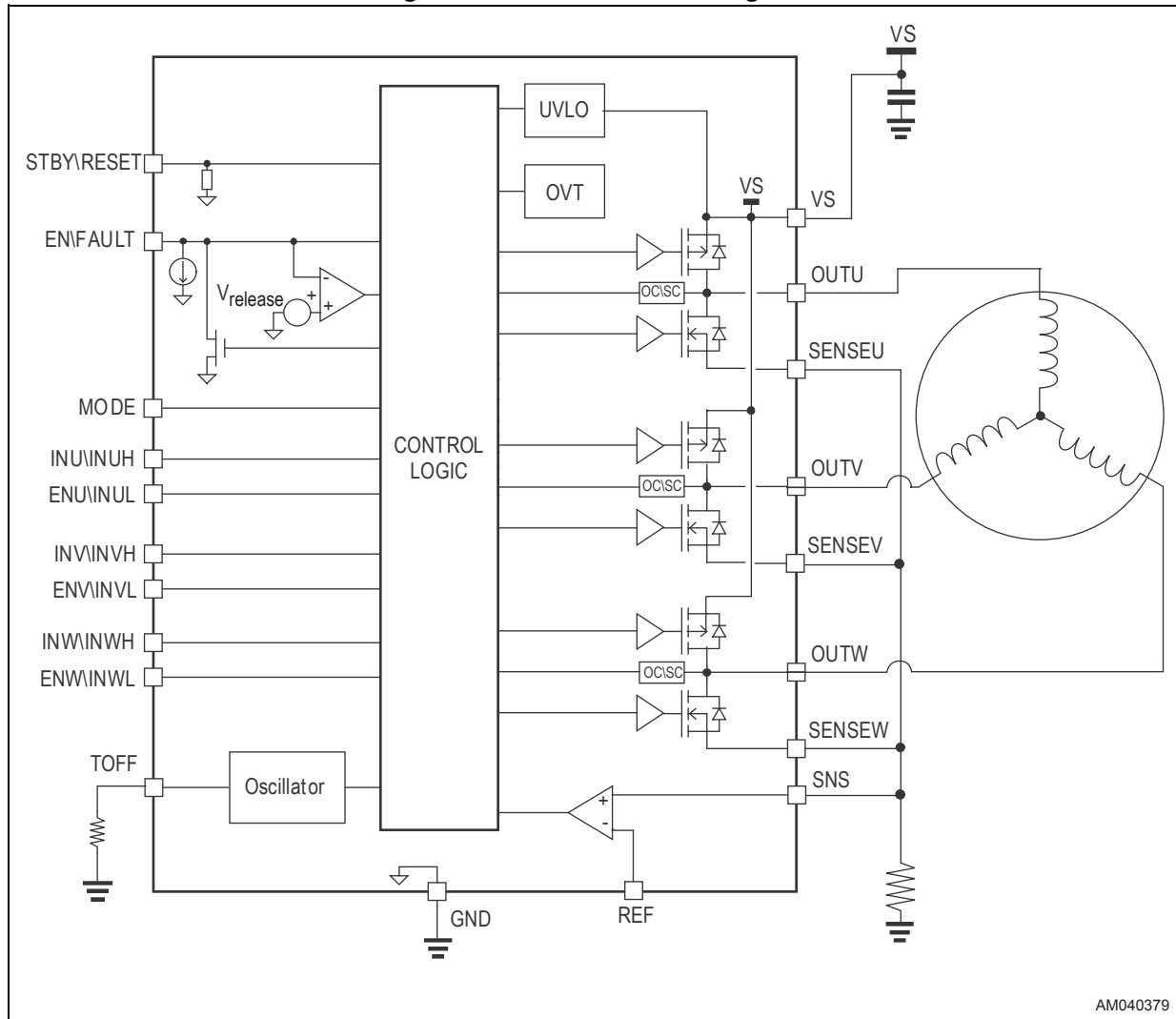
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# 1 Block diagram

Figure 1. STSPIN830 block diagram



## 2 Electrical data

### 2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
$V_S$	Supply voltage	-	-0.3 to 48	V
$V_{IN}$	Logic input voltage	-	-0.3 to 5.5	V
$V_{OUT,diff}$	Differential voltage between VSx, OUTU, OUTV, OUTW and SENSEx pins	-	up to 48	V
$V_{SENSE}$	Sense pins voltage <sup>(1)</sup>	-	-2 to 2	V
$V_{REF}$	Reference voltage input	-	-0.3 to 2	V
$I_{OUT,RMS}$	Continuous power stage output current (each bridge)	-	1.5	A <sub>rms</sub>
$T_j$	Junction temperature	-	-40 to 150	°C
$T_{STG}$	Storage temperature	-	-55 to 150	°C

1. SENSEU, SENSEV, SENSEW, SNS.

### 2.2 Recommended operating conditions

Table 2. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_S$	Supply voltage	7	-	45	V
$V_{IN}$	Logic input voltage	-	-	5	V
$V_{SENSE}$	Sense pins voltage	-1	-	+1	V
$V_{REF}$	Reference voltage input	0.1	-	1	V

## 2.3 Thermal data

**Table 3. Thermal data**

Symbol	Parameter	Conditions	Value	Unit
$R_{thJA}$	Junction to ambient thermal resistance	Natural convection, according to JESD51-2a <sup>(1)</sup>	36.5	°C/W
$R_{thJCTop}$	Junction to case thermal resistance (top side)	Cold plate on top package, according to JESD51-12 <sup>(1)</sup>	27.6	°C/W
$R_{thJCbot}$	Junction to case thermal resistance (bottom side)	Cold plate on exposed pad, according to JESD51-12 <sup>(1)</sup>	5.9	°C/W
$R_{thJB}$	Junction to board thermal resistance	according to JESD51-8 <sup>(1)</sup>	13.6	°C/W
$\Psi_{JT}$	Junction to top characterization	According to JESD51-2a <sup>(1)</sup>	1	°C/W
$\Psi_{JB}$	Junction to board characterization	According to JESD51-2a <sup>(1)</sup>	13.7	°C/W

1. Simulated on a 76.2 x 114.3 x 1.6 mm, with vias underneath the component, 2s2p board as per standard JEDEC (JESD51-7) in natural convection.

## 2.4 ESD protection ratings

**Table 4. ESD protection ratings**

Symbol	Parameter	Conditions	Class	Value	Unit
HBM	Human body model	Conforming to ANSI/ESDA/JEDEC JS001	H2	2	kV
CDM	Charge device model	Conforming to ANSI/ESDA/JEDEC JS002 All pins	C2a	500	V
		Conforming to ANSI/ESDA/JEDEC JS002 Corner pins only (1, 6, 7, 12, 13, 18, 19, 24)	-	750	V
MM	Machine model	Conforming to EIA/JESD22-A115-C	NC	200	V

### 3 Electrical characteristics

Testing conditions:  $V_S = 36\text{ V}$ ,  $T_j = 25\text{ °C}$  unless otherwise specified.

**Table 5. Electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>General</b>						
$V_{Sth(ON)}$	$V_S$ turn-on threshold	$V_S$ rising from 0 V	-	6.0	6.5	V
$V_{Sth(HYST)}$	$V_S$ turn-off threshold hysteresis	$V_S$ falling from 7 V	-	0.4		V
$I_S$	$V_S$ supply current	No commutations EN = '0' $R_{TOFF} = 10\text{ k}\Omega$	-	2.3	2.7	$\mu\text{A}$
		No commutations EN = '1' $R_{TOFF} = 10\text{ k}\Omega$	-	2.7	3	$\mu\text{A}$
$V_{STBYL}$	Standby low voltage	-	-	-	0.8	V
$V_{STBYH}$	Standby high voltage	-	2	-	-	V
$I_{S, STBY}$	$V_S$ supply standby current	STBY = 0 V	-	-	45	$\mu\text{A}$
<b>Power stage</b>						
$R_{DSon\ HS+LS}$	Total on resistance HS + LS	$V_S = 21\text{ V}$ $I_{OUT} = 1\text{ A}$	-	1	1.3	$\Omega$
		$V_S = 21\text{ V}$ $I_{OUT} = 1\text{ A}$ $T_j = 150\text{ °C}^{(1)}$	-	1.4	1.6	
$I_{DSS}$	Leakage current	OUTx = $V_S = 48\text{ V}$	-	-	20	$\mu\text{A}$
		OUTx = -0.3 V	-1	-	-	
$V_{DF}$	Freewheeling diode forward voltage	$I_D = 1.5\text{ A}$	-	1	-	V
$t_{rise}$	Rise time	$V_S = 21\text{ V}$	-	120	-	ns
$t_{fall}$	Fall time	$V_S = 21\text{ V}$	-	60	-	ns
<b>Logic IO</b>						
$V_{IH}$	High logic level input voltage	-	2	-	-	V
$V_{IL}$	Low logic level input voltage	-	-	-	0.8	V
$V_{OL}$	Low logic level output voltage	$I_{OL} = 4\text{ mA}$	-	-	0.3	V
$V_{RELEASE}$	FAULT open drain release voltage	-	-	-	0.6	V
$R_{STBY}$	STBY pull-down resistance	-	-	60	-	$\text{k}\Omega$
$I_{PDEN}$	Enable pull-down current	-	-	5	-	$\mu\text{A}$
$t_{END}$	EN input propagation delay	From EN falling edge to OUT high impedance	-	400	-	ns



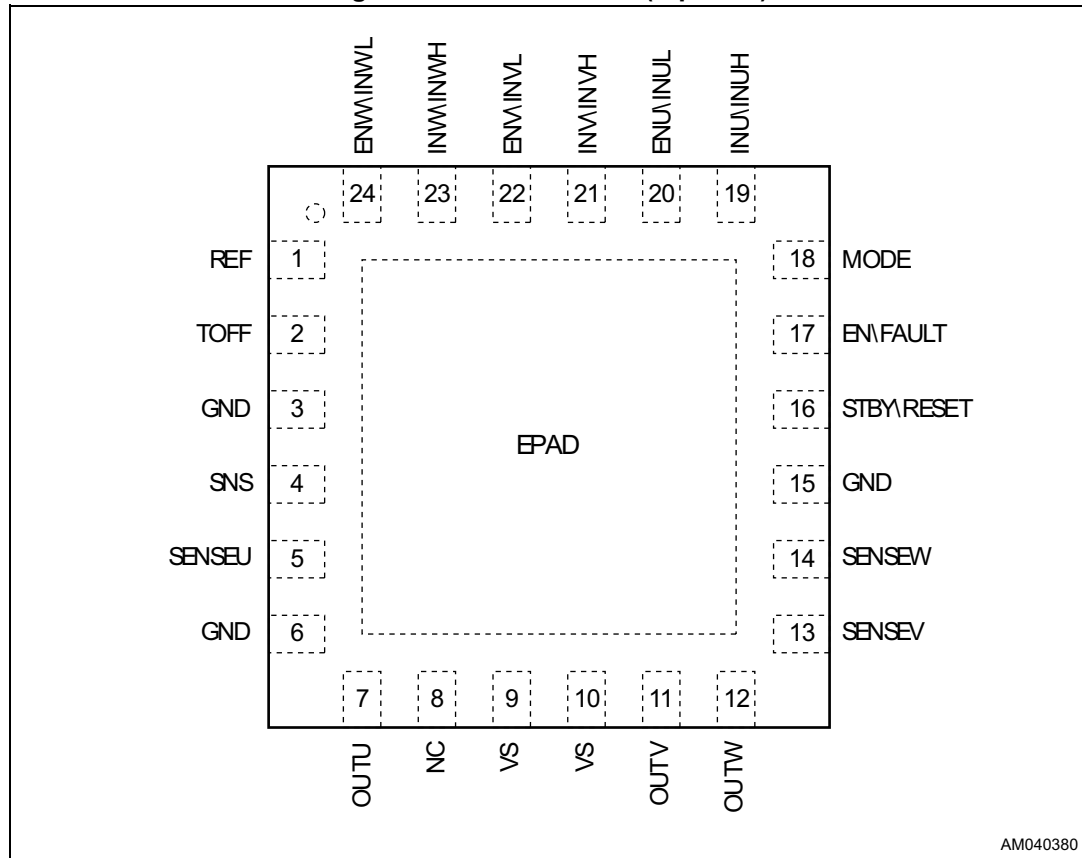
Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t <sub>IND(ON)</sub>	Turn-on propagation delay	From INxH rising edge to 10% of OUTx	-	450	-	ns
t <sub>IND(OFF)</sub>	Turn-off propagation delay	From INxL rising edge to 90% of OUTx	-	250	-	ns
PWM current control						
V <sub>SNS,OFFSET</sub>	Current control offset	-	-15	-	15	mV
t <sub>OFF</sub>	Total OFF time	R <sub>OFF</sub> = 10 kΩ	-	13	-	μs
		R <sub>OFF</sub> = 160 kΩ	-	146	-	μs
Δt <sub>OFF</sub>	OFF time precision	Full temperature range <sup>(1)</sup>	-20	-	+20	%
t <sub>OFF,jitter</sub>	Total OFF time jittering	-	-	±2	-	
Protections						
T <sub>jSD</sub>	Thermal shutdown threshold	-	-	160	-	°C
T <sub>jSD,Hyst</sub>	Thermal shutdown hysteresis	-	-	40	-	°C
I <sub>OC</sub>	Overcurrent threshold	-	-	3	3.5	A

1. Based on characterization data on a limited number of samples, not tested during production.

## 4 Pin description

Figure 2. Pin connection (top view)



Note: The exposed pad must be connected to ground.

Table 6. Pin description

No.	Name	Type	Function
1	REF	Analog input	Reference voltage for the PWM current control circuitry
2	TOFF	Analog input	Internal oscillator frequency adjustment
3, 6, 15	GND	Ground	Device ground
4	SNS	Analog input	Current regulator sense input
5	SENSEU	Power output	Sense output of the bridge U
7	OUTU	Power output	Power bridge output U
9	VS	Supply	Device supply voltage
10	VS	Supply	Device supply voltage
11	OUTV	Power output	Power bridge output V
12	OUTW	Power output	Power bridge output W
13	SENSEV	Power output	Sense output of the bridge V

Table 6. Pin description (continued)

No.	Name	Type	Function
14	SENSEW	Power output	Sense output of the bridge W
16	STBY\RESET	Logic input	Standby\reset input When forced low the device enter in low consumption mode.
17	EN\FAULT	Logic input\ open drain output	Logic input 5 V compliant with open drain output. This is the power stage input enable (when low, the power stage is turned off) and is forced low through the integrated open-drain MOSFET when a failure occurs.
18	MODE	Logic input	Inputs driving method selection. When low the ENx\INx option is selected, when high the INxH\INxL option is enabled. <sup>(1)</sup>
19	INU\INUH	Logic input	Output U high-side driving input <sup>(1)</sup>
20	ENU\INUL	Logic input	Output U low-side driving input <sup>(1)</sup>
21	INV\INVH	Logic input	Output V high-side driving input <sup>(1)</sup>
22	ENV\INVL	Logic input	Output V low-side driving input <sup>(1)</sup>
23	INW\INWH	Logic input	Output W high-side driving input <sup>(1)</sup>
24	ENW\INWL	Logic input	Output W low-side driving input <sup>(1)</sup>
8	NC	NC	Not connected.

1. Refer to [Section 5.2: Logic inputs](#) for more details.

## 5 Functional description

The STSPIN830 is a three-phase motor driver integrating a PWM current limiter and a power stage composed of three fully-protected half-bridges.

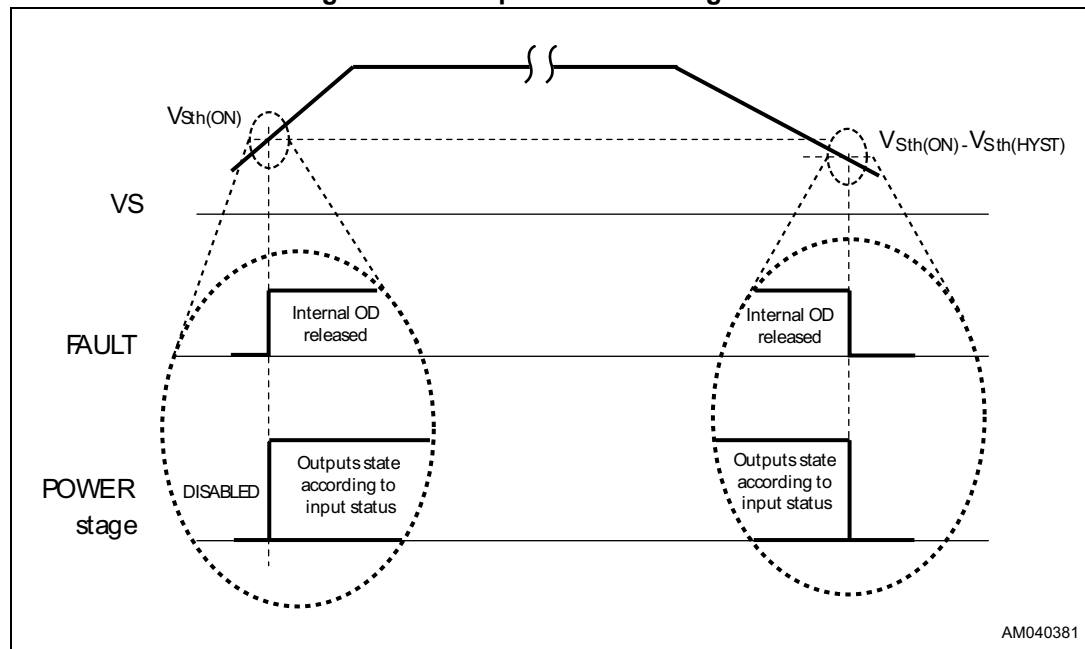
### 5.1 Power supply and standby

The device is supplied through the VS pins, the two pins **must** be at the same voltage.

At power-up the power stage is disabled and the FAULT pin is forced low until the VS voltage rise above the  $V_{Sth(ON)}$  threshold.

If the VS fall below the  $V_{Sth(ON)} - V_{Sth(HYST)}$  value the power stage is immediately disabled and the FAULT pins are forced low.

Figure 3. UVLO protection management



The device provides a low consumption mode which is set by forcing the STBY\RESET input below the  $V_{STBYL}$  threshold.

When the device is in standby status the power stage is disabled (outputs are at high impedance) and the supply to the integrated control circuitry is strongly reduced. When the device leaves the standby status, all the control circuitry is reset to power-up condition.

### 5.2 Logic inputs

The STSPIN830 offers two alternative methods to drive the power stage, which can be selected by setting the status of MODE pin.

If MODE pin is set low (connected to GND) the output of each full bridge is controlled by the respective ENx and INx inputs.

If MODE pin is set high the output of each full bridge is controlled by the respective INxH and INxL inputs.

In both cases the status of the power bridge is also determined by the PWM current limiter as indicated in [Section 5.3](#).

**Note:** *The MODE pin status must not be changed whilst the device is operational.*

When the ENFAULT input is forced low the power stage is immediately disabled (all MOSFETs are turned off). The pin is also used as FAULT indication through the integrated open-drain MOSFET as described in [Section 5.4 on page 16](#) and [Section 5.5 on page 20](#).

**Table 7. ENx and INx inputs truth table (MODE = 'L')**

MODE	ENFAULT	ENx	INx	OUTx	'x' half-bridge condition
0	0	X <sup>(1)</sup>	X <sup>(1)</sup>	High Z <sup>(2)</sup>	Disabled
0	1	0	X <sup>(1)</sup>	High Z <sup>(2)</sup>	Disabled
0	1	1	0	GND	LS on
0	1	1	1	VS	HS on

1. X: don't care.

2. High Z: high impedance.

**Table 8. INxL and INxH inputs truth table (MODE = 'H')**

MODE	ENFAULT	INxH	INxL	OUTx	'x' half-bridge condition
1	0	X <sup>(1)</sup>	X <sup>(1)</sup>	High Z <sup>(2)</sup>	Disabled
1	1	0	0	High Z <sup>(2)</sup>	Disabled
1	1	0	1	GND	LS on
1	1	1	0	VS	HS on
1	1	1	1	High Z <sup>(2)</sup>	Disabled (interlocking)

1. X: don't care.

2. High Z: high impedance.

## 5.3 PWM current limiter

The device implements a PWM current limiter.

The load current is sensed through the SNS pin monitoring the voltage drop across an external resistor connected between the source of the low side power MOSFET (SENSEx pins) and ground.

The voltage of the SNS pin ( $V_{SNS}$ ) is compared to the reference voltage pin ( $V_{REF}$ ).

When  $V_{SNS} > V_{REF}$  the current limiter is triggered, the OFF time is started and all the power outputs are disabled (high impedance) until the end of count of the timer.

During current decays the inputs values are ignored until the system returns to ON condition (decay time expired).

The reference voltage value,  $V_{REF}$ , has to be selected according the load current target value (peak value) and sense resistors value.

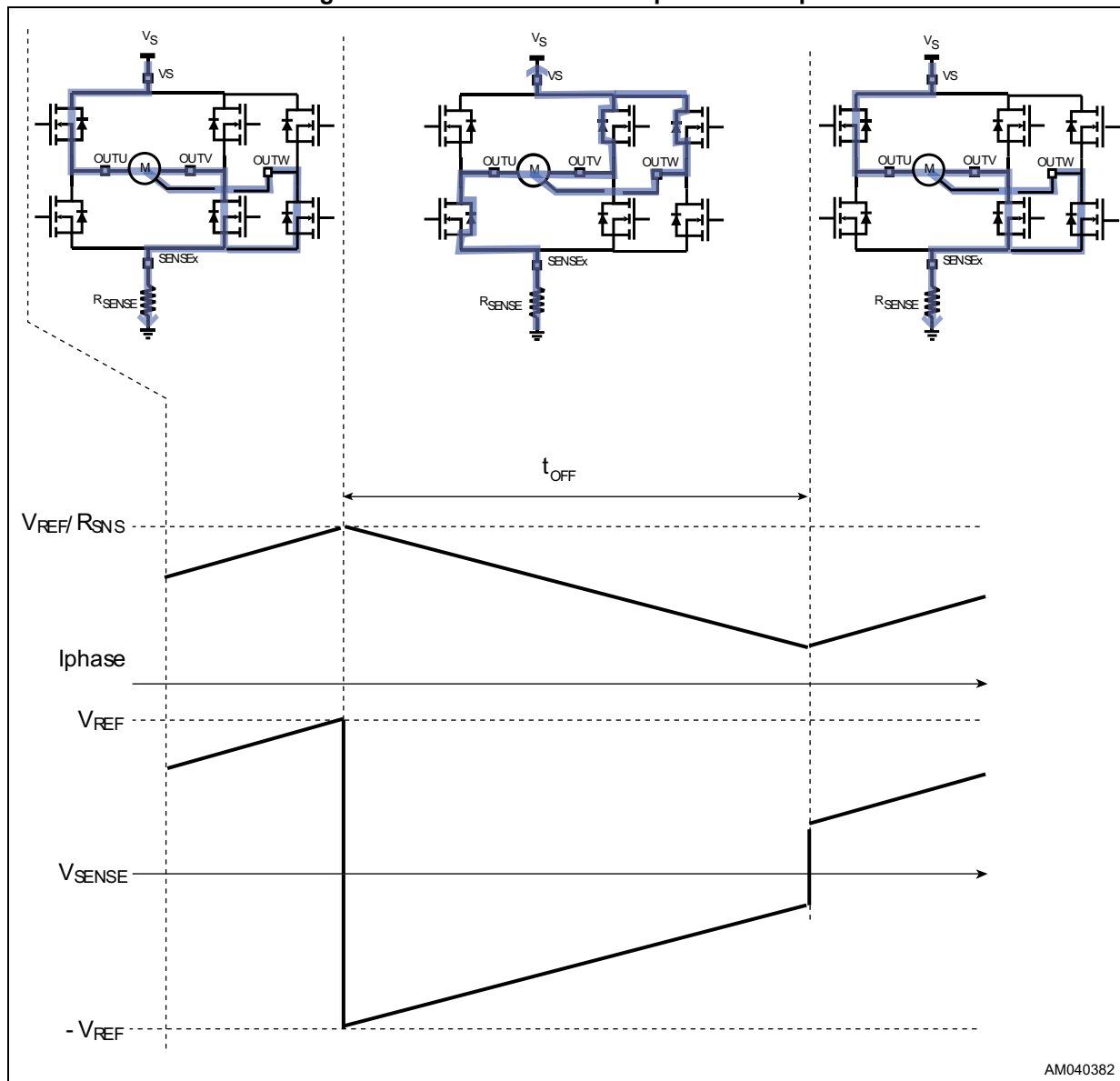
## Equation 1

$$V_{REF} = R_{SENSE} \times I_{LOAD,peak}$$

The choice of sense resistors value must be take into account two main issues:

- The sensing resistor dissipates energy and provides dangerous negative voltages on the SENSE pins during the current recirculation. For this reason the resistance of this component should be kept low (using multiple resistors in parallel will help obtaining the required power rating with standard resistors).
- The lower is the  $R_{SENSE}$  value, the higher is the peak current error due to noise on  $V_{REF}$  pin and to the input offset of the current sense comparator: too small values of  $R_{SENSE}$  must be avoided.

**Figure 4. PWM current limit sequence example**



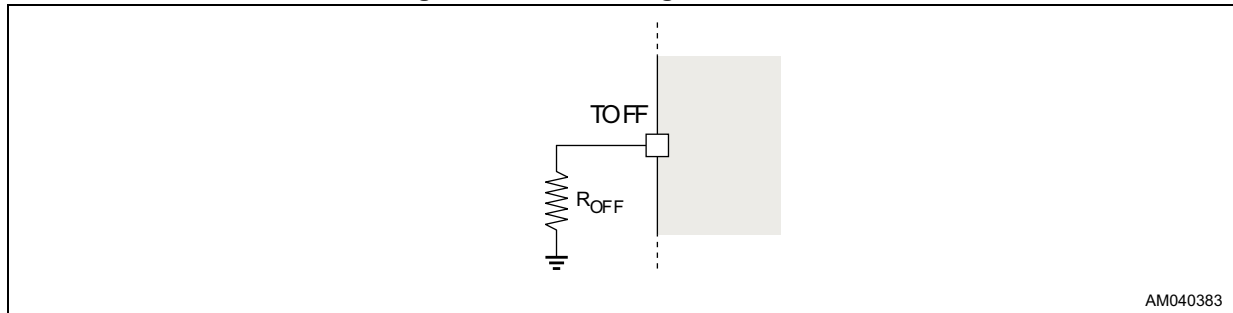
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**Note:** When the voltage on the SNS pin exceeds the absolute ratings, a fault condition is triggered and the ENFAULT output is forced low.

### TOFF adjustment

The OFF time is adjusted through an external resistor connected between the TOFF pin and ground as shown in [Figure 5](#).

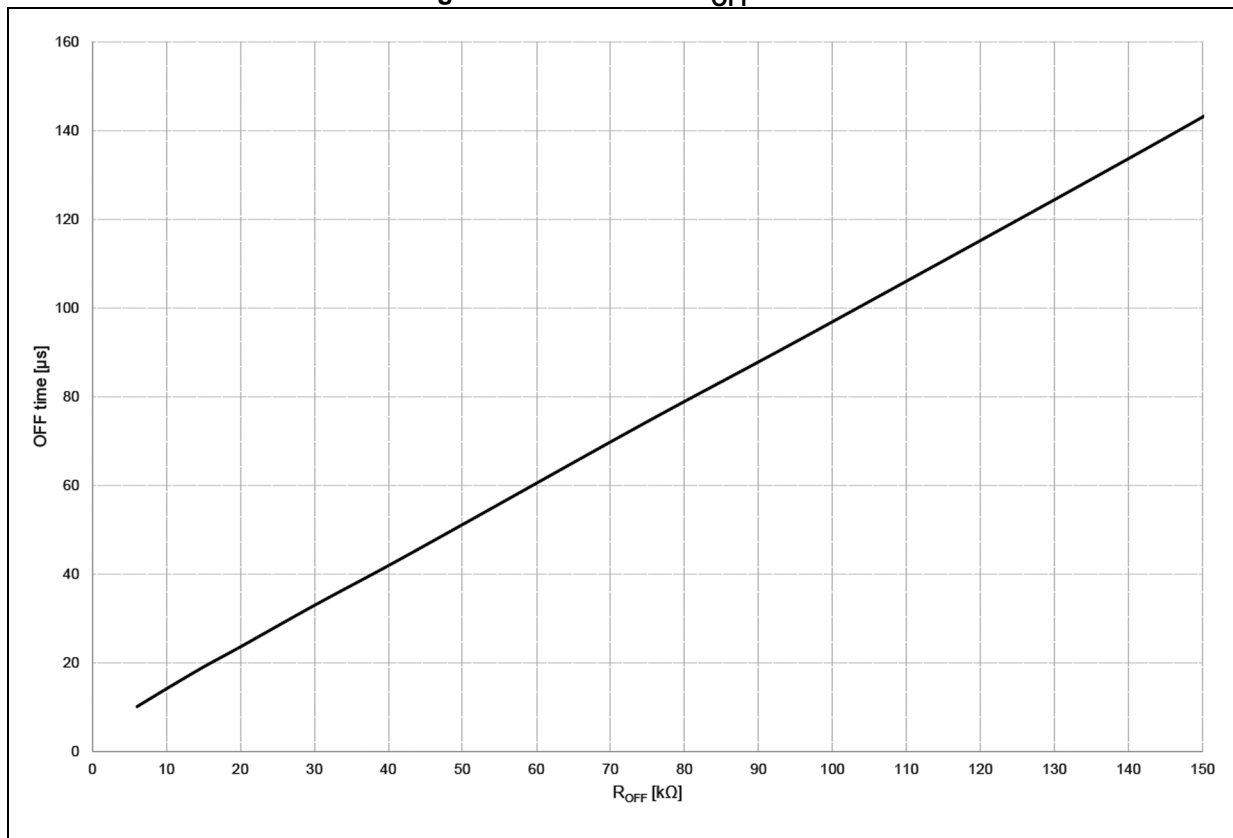
**Figure 5. OFF time regulation circuit**



The relation between the OFF time and the external resistor value is shown in the graph of [Figure 6](#). The value typically ranges from 10  $\mu$ s to 150  $\mu$ s.

The recommended value for  $R_{OFF}$  is in the range between 5 k $\Omega$  and 180 k $\Omega$ .

**Figure 6. OFF time vs  $R_{OFF}$  value**



## 5.4 Device protections

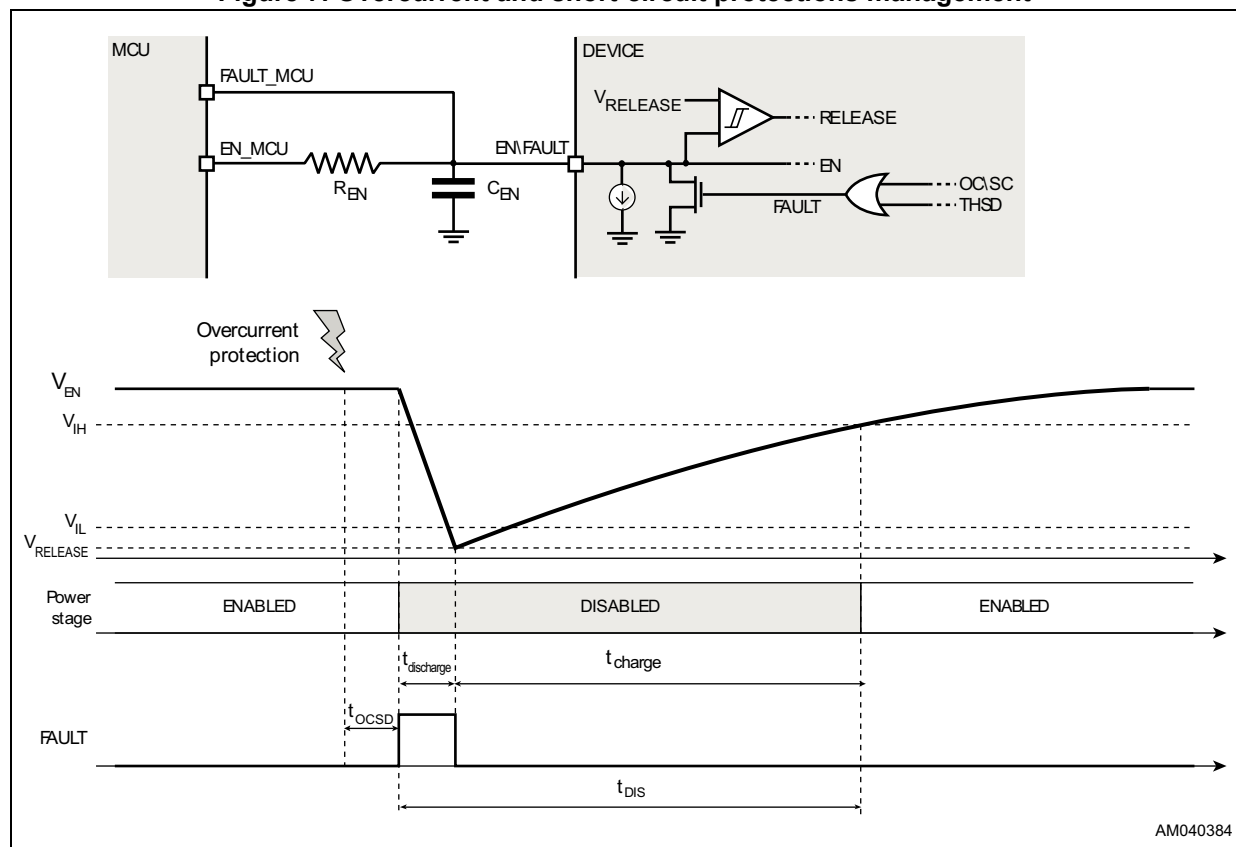
### 5.4.1 Overcurrent and short-circuit protections

The device embeds circuitry to protect each power MOSFET against the overload and short-circuit conditions (short-circuit to ground, short-circuit to VS and short-circuit between outputs).

When the overcurrent or the short-circuit protection is triggered the power stage is disabled and the EN\FAULT input is forced low through the integrated open drain MOSFET discharging the external  $C_{EN}$  capacitor.

The power stage is kept disabled and the open drain MOSFET is kept ON until the EN\FAULT input falls below the  $V_{RELEASE}$  threshold, then the  $C_{EN}$  capacitor is charged through the external  $R_{EN}$  resistor.

**Figure 7. Overcurrent and short-circuit protections management**



The total disable time after an overcurrent event is set sizing properly the external network connected to EN\FAULT pin (refer to [Figure 8](#)) and it is the sum of the discharging and charging time of the  $C_{EN}$  capacitor:

#### Equation 2

$$t_{DIS} = t_{discharge} + t_{charge}$$



Considering  $t_{\text{discharge}}$  is normally significantly lower than  $t_{\text{charge}}$ , its contribution is negligible and the disable time is almost equal to  $t_{\text{charge}}$  only:

### Equation 3

$$t_{\text{DIS}} \cong R_{\text{EN}} \times C_{\text{EN}} \times I_n \frac{(V_{\text{DD}} - R_{\text{EN}} \times I_{\text{PD}}) - V_{\text{RELEASE}}}{(V_{\text{DD}} - R_{\text{EN}} \times I_{\text{PD}}) - V_{\text{IH}}}$$

Where  $V_{\text{DD}}$  is the pull-up voltage of the  $R_{\text{EN}}$  resistor.

The recommended value for  $R_{\text{EN}}$  and  $C_{\text{EN}}$  are respectively 39 k $\Omega$  and 10 nF that allow obtaining 300  $\mu\text{s}$  disable time.

**Figure 8. Disable time versus  $R_{\text{EN}}$  and  $C_{\text{EN}}$  values ( $V_{\text{DD}} = 3.3 \text{ V}$ )**

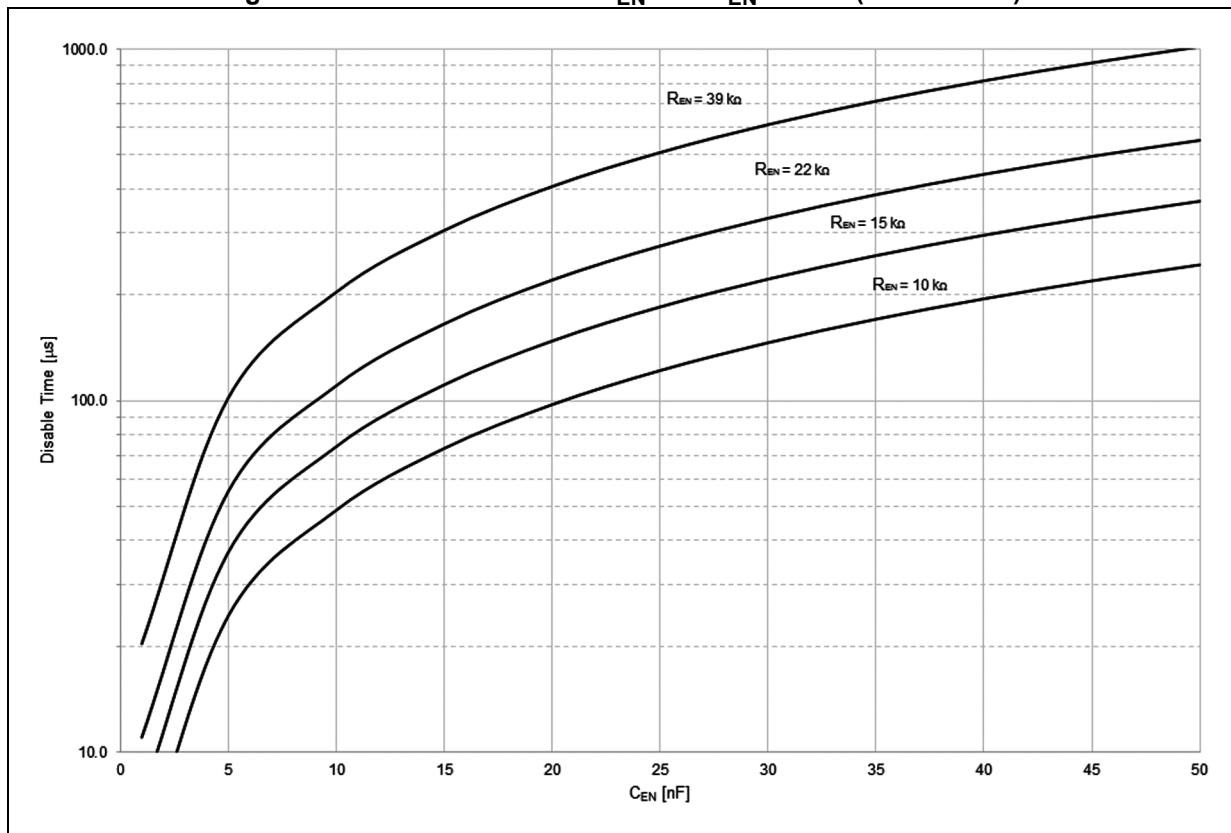
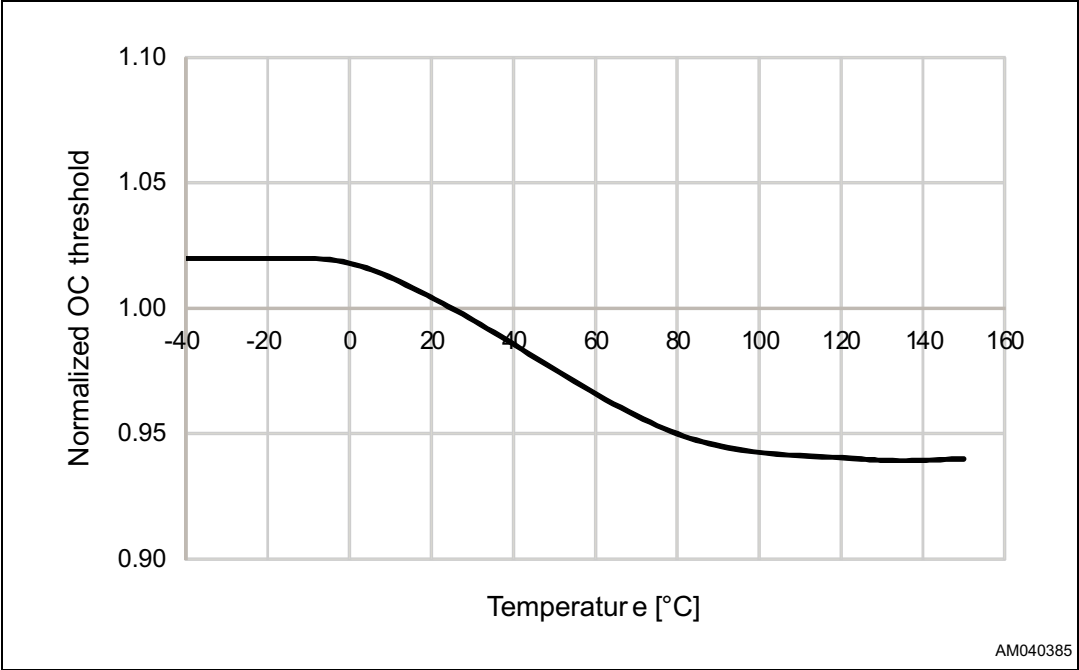


Figure 9. Overcurrent threshold versus temperature (normalized at 25 °C)



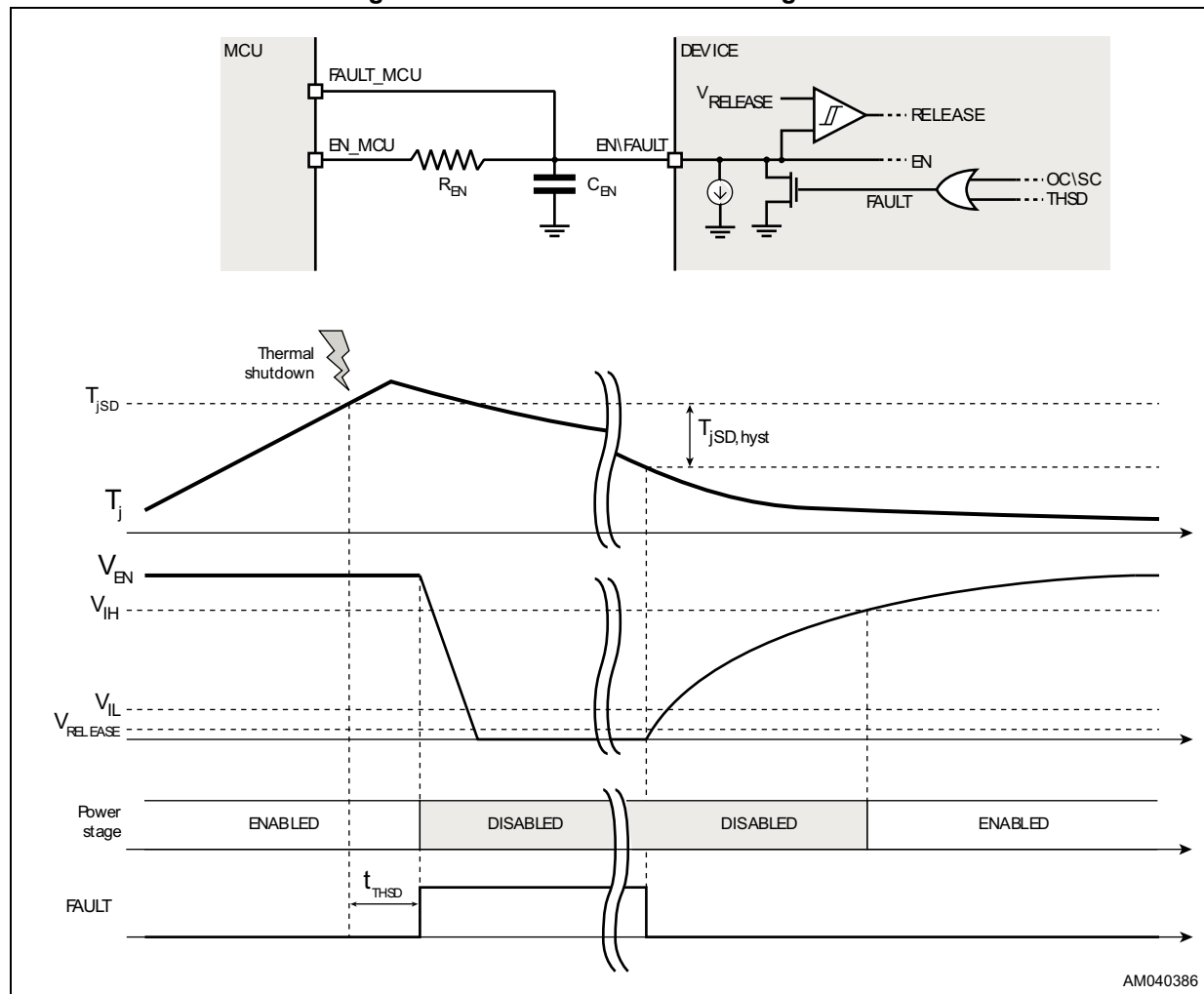
### 5.4.2 Thermal shutdown

The device embeds circuitry to protect it from overtemperature conditions.

When the thermal shutdown temperature is reached the power bridge are disabled and the EN\FAULT input is forced low through the integrated open drain MOSFET (refer to [Figure 10](#)).

The protection and the EN\FAULT output is released when the IC temperature returns below a safe operating value ( $T_{jSD} - T_{jSD,Hyst}$ ).

**Figure 10. Thermal shutdown management**



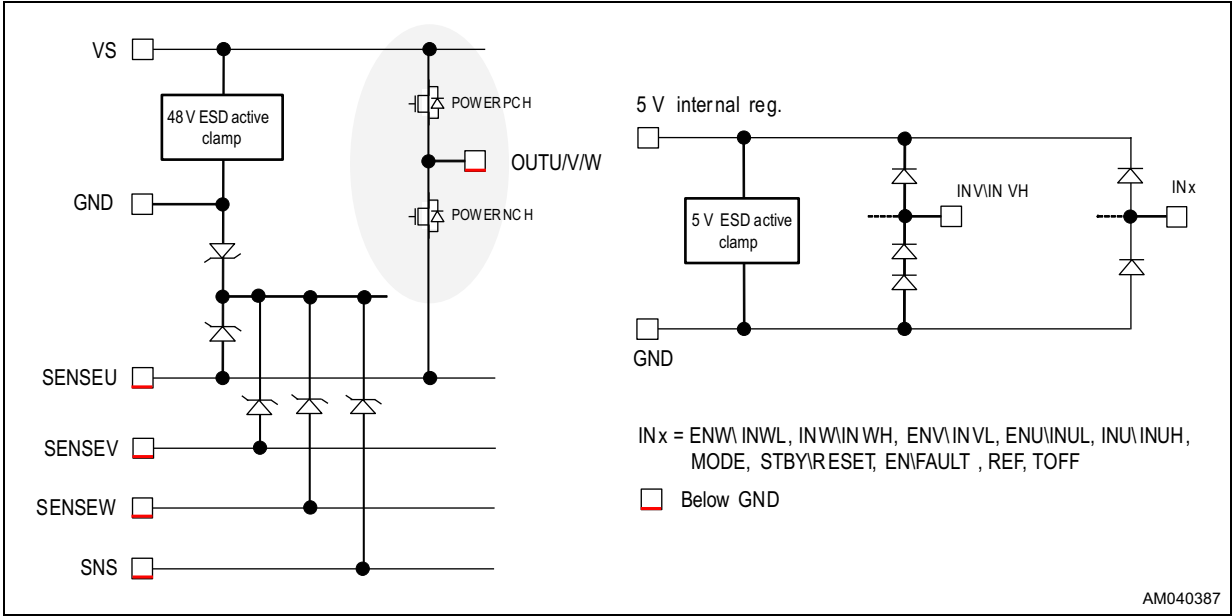
### 5.4.3 Blanking time

The device provides a blanking time  $t_{BLANK}$  after each power MOSFET commutation to prevent false triggering of protections and current limiter.

During blanking time the protections (overcurrent, short-circuit, thermal shutdown) and the comparator of the current limiter are inhibit.

5.5 ESD protection strategy

Figure 11. ESD protection strategy



## 6 Typical applications

Table 9. Typical application values

Name	Value
$C_S$	330 nF
$C_{SPOL}$	33 $\mu$ F
$R_{SNS}$	330 m $\Omega$ / 1 W
$C_{EN}$	10 nF
$R_{EN}$	39 k $\Omega$
$C_{STBY}$	1 nF
$R_{STBY}$	18 k $\Omega$
$R_{OFF}$	10 k $\Omega$ ( $T_{OFF} \cong 13 \mu$ s)

Figure 12. Typical application schematic with single shunt

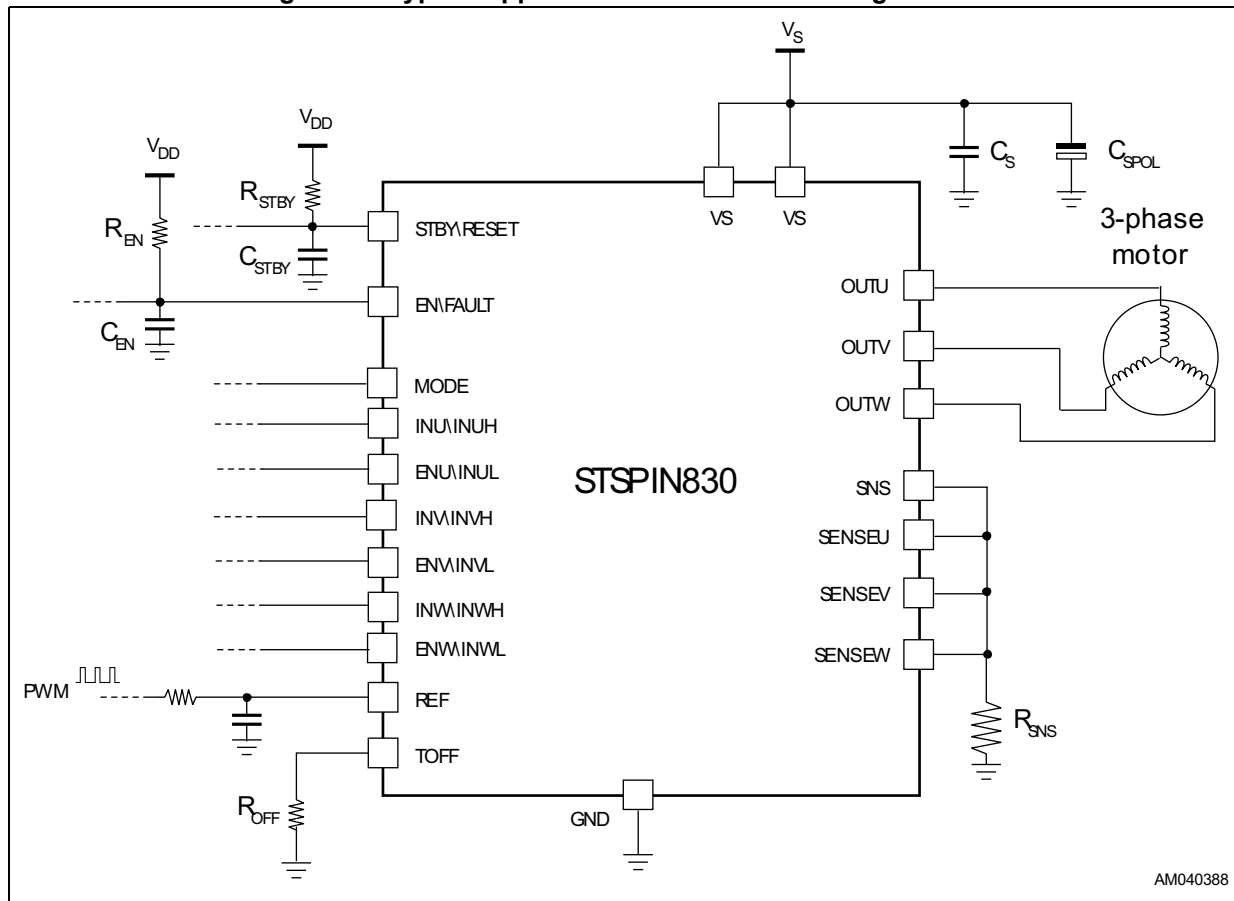
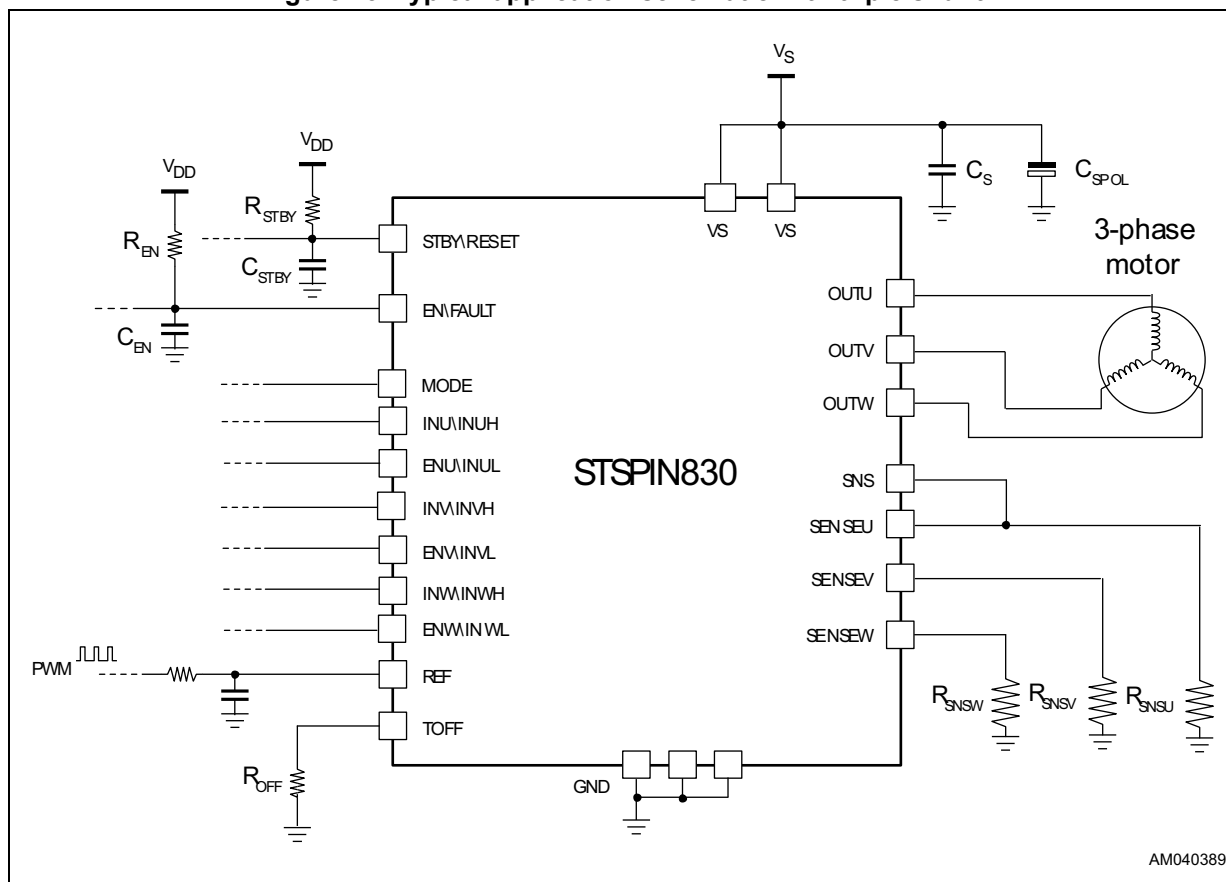


Figure 13. Typical application schematic with triple shunt



## 7 Layout recommendations

The STSPIN830 integrates the power stage; in order to improve the thermal dissipation, the exposed pad must be connected to the ground plane on the bottom layer using multiple vias equally spaced. This ground plane acts as a heatsink, for this reason it should be as wide as possible.

The voltage supply  $V_S$  must be stabilized and filtered with a ceramic bypass capacitor, typically 330 nF. It must be placed on the same side and as close as possible to  $V_S$  pin in order to reject high frequency noise components on the supply. A bulk capacitor could also be required (typically a 33  $\mu$ F). The connection between the power supply connector and the  $V_S$  pins must be as short as possible using wide traces.

In order to ensure the best ground connection between the STSPIN830 and the other components, a GND plane surrounding the device is recommended.

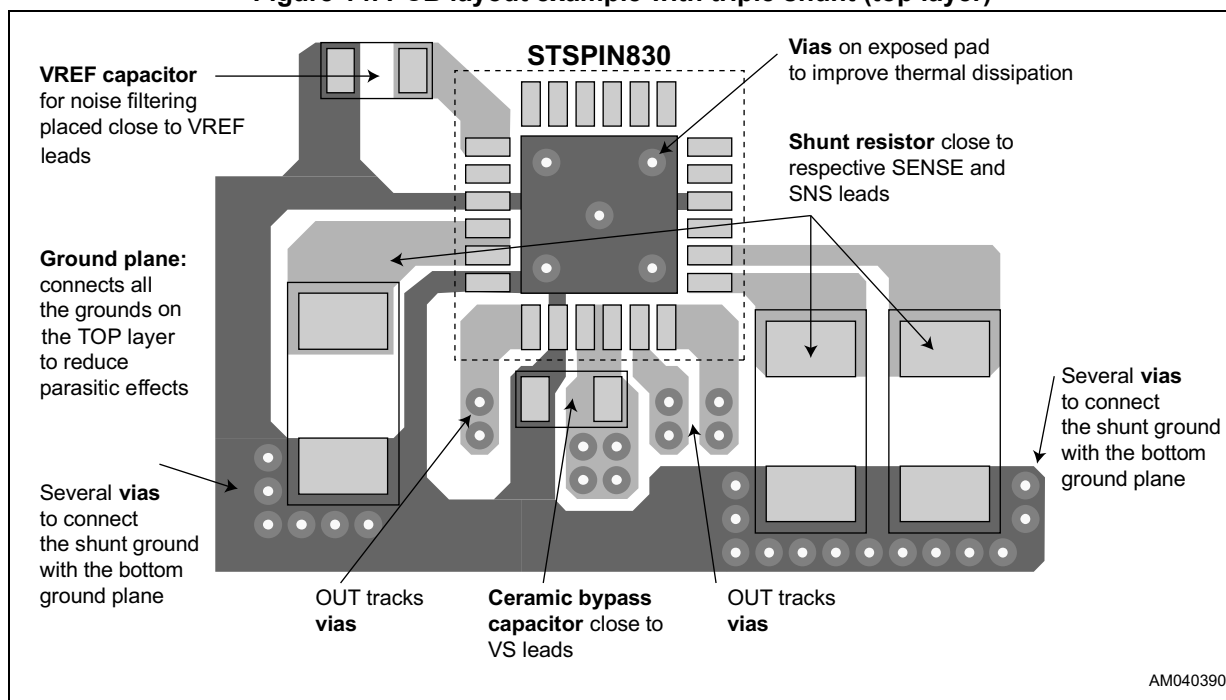
A capacitor between REF pins and ground should be positioned as near as possible to the device in order to filter the noise and stabilize the reference voltage.

Several vias should be positioned as near as possible each sense resistor connecting them to the ground plane on the bottom layer. In this way, both the GND planes provide a path for the current flowing into the power stage.

The path between the ground of the shunt resistors and the ceramic bypass capacitor of the device is critical; for this reason it must be as short as possible minimizing parasitic inductances that can cause voltage spikes on SENSE and OUT pins.

The OUT pins and the VS nets can be routed using the bottom layer, it is recommended to use two vias for output connections.

**Figure 14. PCB layout example with triple shunt (top layer)**



In case of single shunt configuration take special care for the SENSE and SNS pins connection.

As suggested in [Figure 15](#) and [Figure 16](#), the shunt resistor can be placed in the top layer close to SENSEU and SNS pins with a wide copper area and vias. The connection with other sense pins (SENSEV and SENSEW) can be routed in the bottom layer taking care to maximize the track area and add more vias near to the pins.

**Figure 15. PCB layout example with single shunt (top layer)**

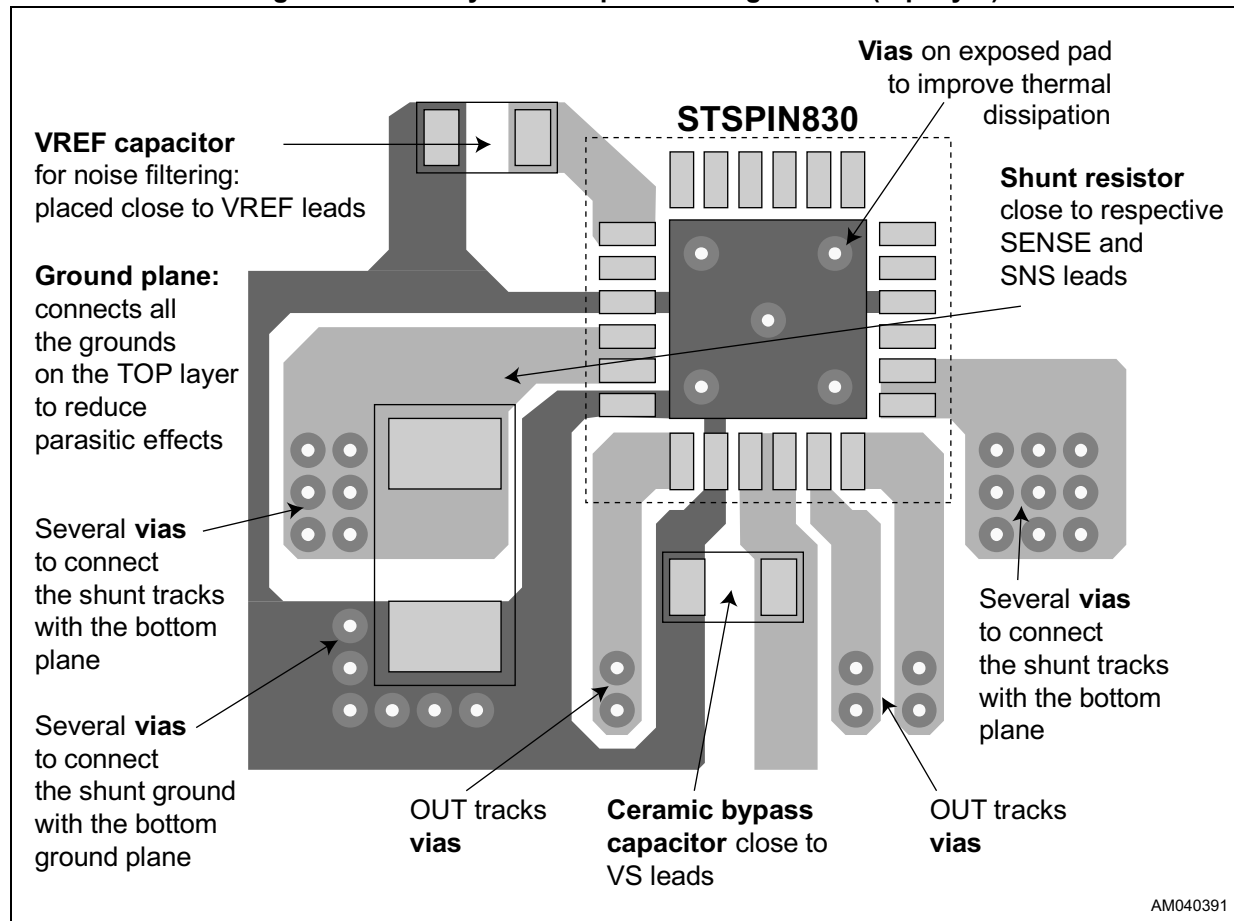
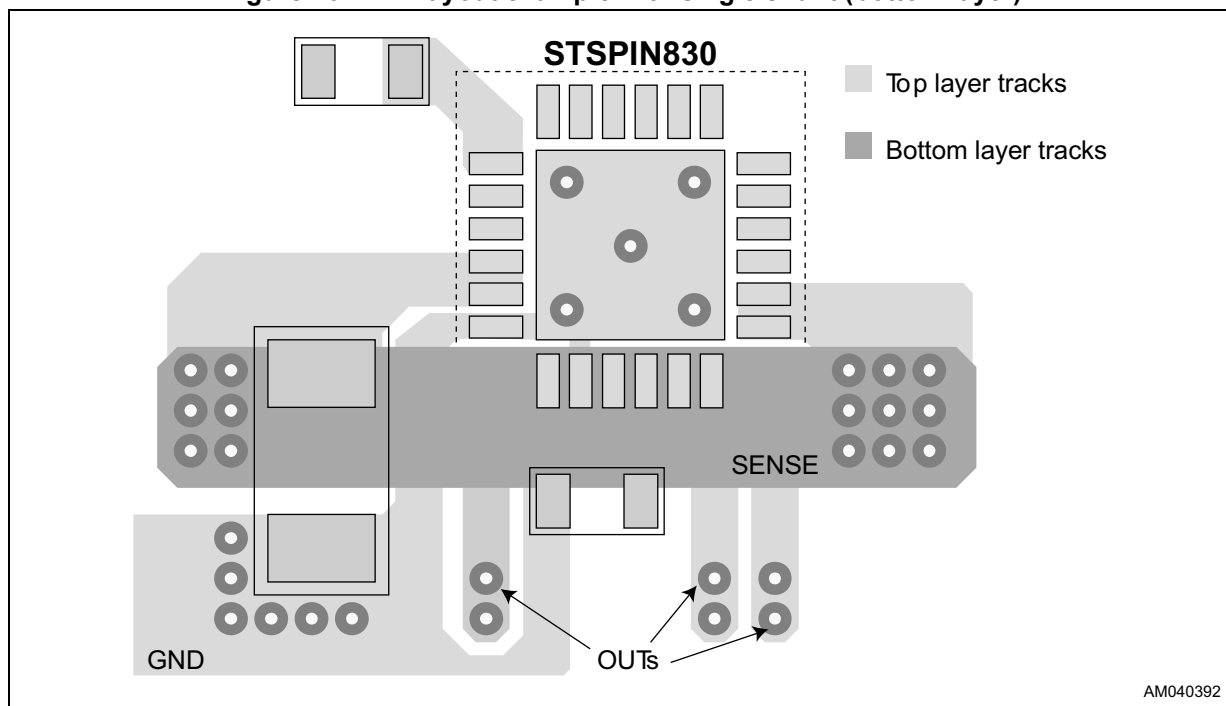




Figure 16. PCB layout example with single shunt (bottom layer)



## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 8.1 TFQFPN 4 x 4 x 1.05 - 24L package information

Figure 17. TFQFPN 4 x 4 x 1.05 - 24L package outline

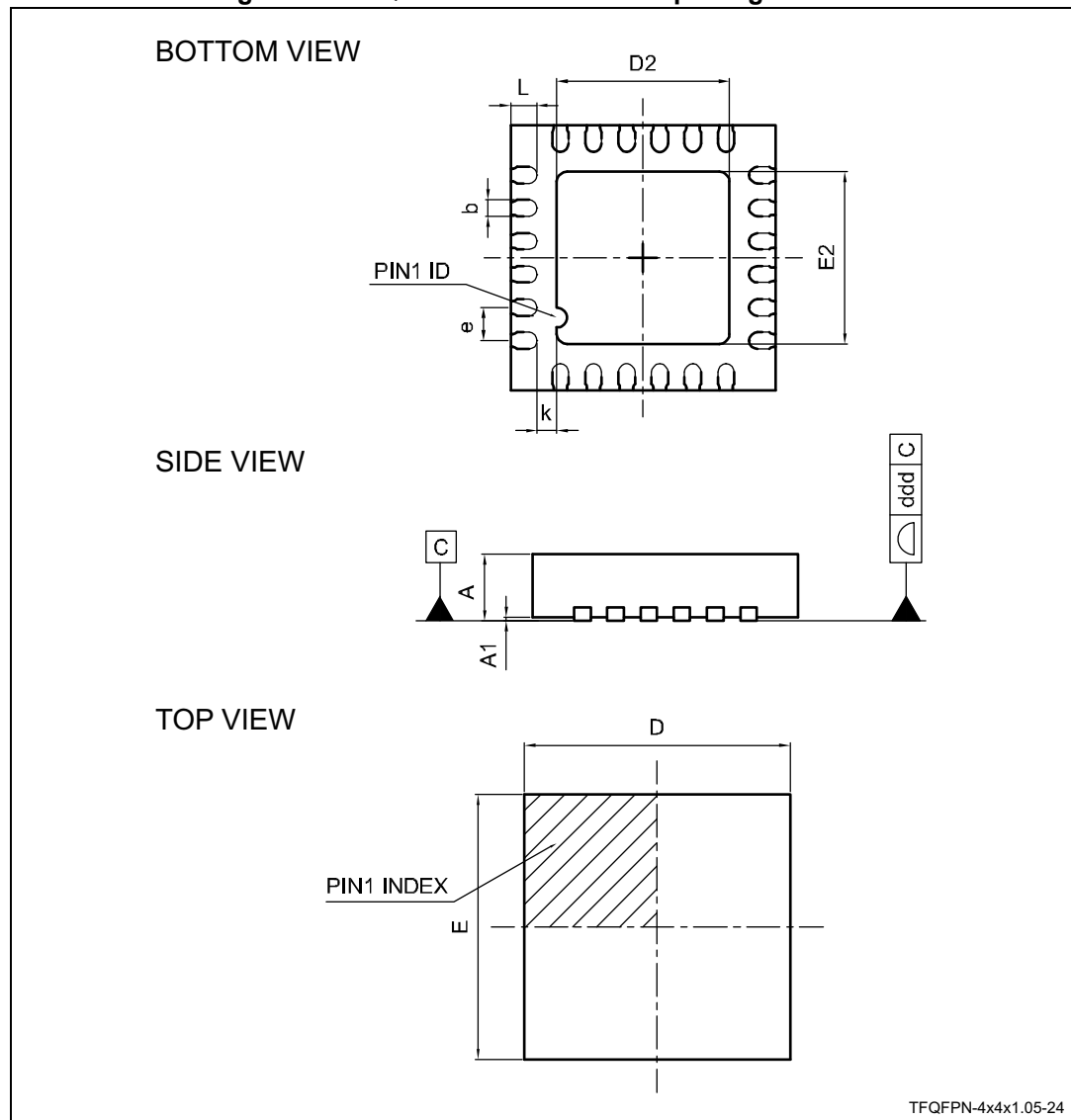
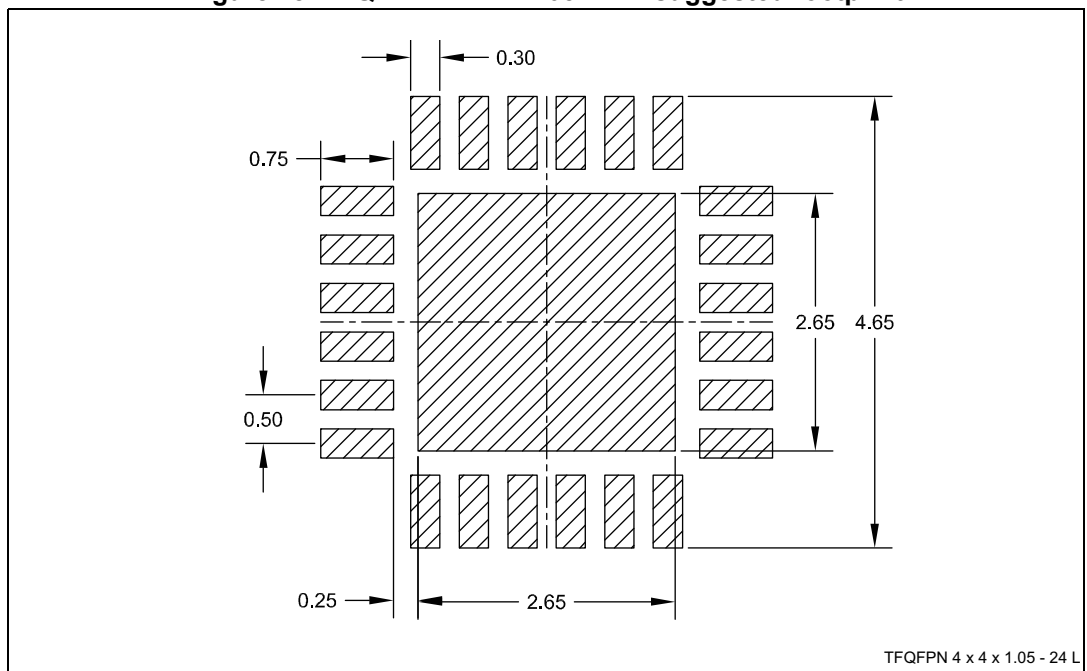


Table 10. TFQFPN 4 x 4 x 1.05 - 24L package mechanical data

Symbol	Dimensions (mm)			Note
	Min.	Typ.	Max.	
A	0.90	1.00	1.10	-
A1	0.00	0.02	0.05	-
b	0.20	0.25	0.30	(1)
D	3.90	4.00	4.10	-
D2	2.55	2.60	2.65	-
E	3.90	4.00	4.10	-
E2	2.55	2.60	2.65	-
e	-	0.50	-	-
L	0.35	0.40	0.45	-
k	-	0.30	-	-
ddd	-	0.05	-	-

1. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm

Figure 18. TFQFPN 4 x 4 x 1.05 - 24L suggested footprint



## 9 Ordering information

**Table 11. Device summary**

Order code	Package	Packaging
STSPIN830	TFQFPN 4 x 4 x 1.05 - 24L	Tape and reel

## 10 Revision history

**Table 12. Document revision history**

Date	Revision	Changes
18-May-2018	1	Initial release.

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