STEVAL-POE001V1

Data brief

Smart evaluation board for high power 4-pair PoE/PoE + PD systems

Features

- System in package including a dual active bridge, a hot swap MOSFET and a PoE-PD interface
- Robust 100V N-ch MOSFETs with 0.2 Ω total path resistance for each active bridge
- Robust 100 V, 0.1 Ω high side N-ch hot swap MOSFET
- PoE-PD single-signature interface compliant with IEEE 802.3bt Draft 3.7
- Detection and support of high power, 4-pair applications
- Identifies which kind of PSE (standard or legacy) it is connected with, and provides successful IEEE802.3 af / at / bt classification indication through combination of the T0, T1 and T2 signals (open drain)
- Programmable classification current with 3.3 ms delay
- Advanced energy-saving MPS timings
- Two step hot swap current protection: DC with 1 ms delay and overload with 10 µs delay
- Startup phase (pre-charge of the output capacitor), performed using an internally limited current source
- PGD signal (open drain) to enable an external PWM controller
- Thermal shutdown protection
- RoHS compliant
- WEEE compliant

Product summary	
Smart evaluation board for high power 4-pair PoE/PoE + PD systems	STEVAL-POE001V1
IEEE802.3bt PoE-PD interface with integrated dual-active bridge	PM8805

Description

This evaluation board, which integrates a high power standard PD PoE interface, lets you try the features of the PM8805 IEEE802.3bt PoE-PD interface with integrated dual-active-bridge.

The PM8805 is a system in package for the smart power supply of Power over Ethernet (PoE) Powered Devices (PD), and is applicable for power levels up to 99.9 W.

It embeds two active bridges with driving circuitry, a charge pump to drive the high side MOSFETs, a hot swap MOSFET and a standard single-signature interface compliant with IEEE 802.3bt Draft 3.7, including detection, classification, UVLO and inrush current limitation.

The active bridges sustain up to 1 A current and the hot swap MOSFET is designed to work with up to 2 A.

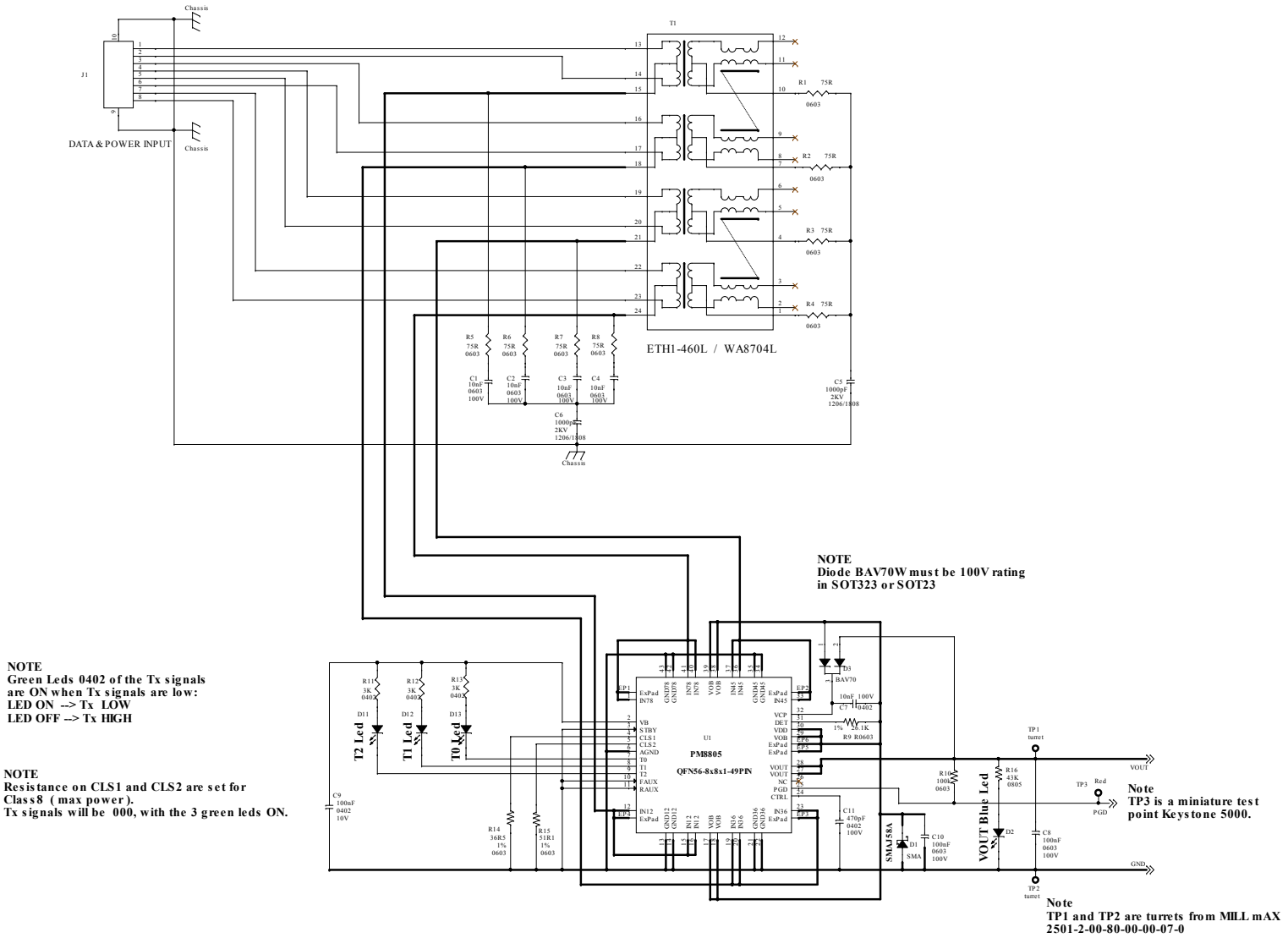
The device performs IEEE 802.3bt Draft 3.7 physical layer classification schemes, providing an indication of successful PSE type identification to the system.

The device identifies a 4-pair PSE, monitoring the pairs of the Ethernet cable and providing the system with a dedicated matrix of Tx signals.

The device is suitable for building the interface of PoE switch mode power supplies for maximum conversion efficiency. It provides a PGD signal that can be used to enable a PWM controller, a DC-DC converter or a LED driver.

1 Schematic diagram

Figure 1. STEVAL-POE001V1 board schematic



2 Bill of material

Table 1. **Bill of material**

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
1	4	C1, C2, C3, C4	10 nF	Capacitor X5R 100V 20% 0603	Several	
2	2	C5, C6	1000 pF	Capacitor X7R 2KV 10% 1808	TDK	C4520X7R3D102K130KA
3	1	C7	10 nF	Capacitor X7R 100V 10% 0402	Several	
4	2	C8, C10	100 nF	Capacitor X7R 100V 10% 0603	Several	
5	1	C9	100 nF	Capacitor X7R 100V 10% 0402	Several	
6	1	C11	NM	Capacitor X7R 100V 10% 0402	Several	
7	1	D1	SMAJ58A	TVS diode in SMA 400 W	ST	SMAJ58A
8	1	D2	Led	Blue LED 0402	Kingbright	KPHHS-1005MGCK
9	1	D3	BAV70W	Diode SOT323	NXP, ONsemi	
10	1	D11, D12, D13	Led	Green LED 0402	Kingbright	KPHHS-1005QBC-D-V
11	1	J1	RJ45	Shielded RJ45-8pin	Several	
12	8	R1, R2, R3, R4, R5, R6, R7, R8	75R	Resistor 5% 0603	Several	
13	1	R9	26.1 K	Resistor 1% 0603	Several	
14	1	R10	100 K	Resistor 5% 0603	Several	
15	3	R11, R12, R13	3 K	Resistor 5% 0402	Several	
16	1	R14	35R6	Resistor 1% 0603	Several	
17	1	R15	51R1	Resistor 1% 0603	Several	
18	1	R16	43 K	Resistor 5% 0805	Several	
19	2	TP1, TP2		Turret	Mill – Max	2501-2-00-80-00-00-07-0
20	1	TP3		Test Point	Keystone	5000
21	1	T1		Data transformer Alternative	Coilcraft Coilcraft	ETH1-460L WA8704-AL
22	1	U1	PM8805	Dual act bridge +.bt interface	ST	PM8805
23	1		Pcb	6 layers, each 35um	Several	

2.1 Output pins description

Table 2. Pin description

Pin#	Name	Function
TPI	VOUT	Source of the high side, hot swap mosfet. This voltage can be used as input voltage for a DC/DC converter.
TP2	GND	Negative output of the active bridge
TP3	PGD	High voltage rating, open drain output signal to be used as Enable for a DC/DC converter feed with VOUT voltage. It is pulled down until the PoE voltage is below UVLO and the hot Swap MOSFET is completely closed. A 85 ms delay typ. is required when receiving power from a PSE before this signal is asserted. A pullup resistor of 100k to VOUT is mounted on-board.

2.2 LED description

Table 3. LED description

Ref.	Type	Function	Logic
D11	Green LED	Monitor of T2 signal	LED on when T2 low
D12	Green LED	Monitor of T1 signal	LED on when T1 low
D13	Green LED	Monitor of T0 signal	LED on when T0 low
D2	Blue LED	Monitor of PGD signal	LED on when PGD high

3 Recommended operating conditions

Table 4. Recommended operating conditions

Parameter	Min.	Max.	Unit
PoE input voltage range VOB to AGND	40	57	V
Output current from VOUT signal pins	-	2	A
Input current for each INxx pair signals	-	1	A
Ambient temperature	0	50	°C

Note: A load on output connector can only be applied after the PGD jumps to the high level.

During the startup sequence, a load connected directly on the output connector will draw a portion of the charging current. If the load applied is higher than the first current limitation step (about 20 mA, also depending on Vin), the application cannot start.

The board has embedded overload protection, but it is not protected against strong short-circuits on the output terminals.

Overall peak efficiency>97% at 2 A.

Revision history

Table 5. **Document revision history**

Date	Version	Changes
25-Sep-2018	1	Initial release.
26-Oct-2018	2	Modified Section 1 Schematic diagram