AND9071/D

Noise Management in Motor Drives with IGBTs

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APPLICATION NOTE

INTRODUCTION

The introduction of IGBTs has enabled motor drives to move to higher switching frequencies and hence, more compact implementations. However, a side product of these advances is the increased vulnerability to the EMI/noise issues. The EMI/EMC management has always been a challenging aspect of any motor drive design and development, with a significant amount of time spent in finding empirical solutions to problems that manifest themselves during the development. The introduction of IGBTs switching at higher frequencies may complicate this task due to (a) higher switching frequencies and (b) increased proximity between components/subsystems offered by the higher level of compactness.

However, as many practicing engineers recognize, techniques exist to address EMI issues effectively. A number of these techniques are discussed in this section. The focus is on building preventive solutions into the design and layout rather than dealing with them through debugging and redesign.

A typical block diagram of the motor drive circuit is shown in Figure 1 and will be used to illustrate various techniques for EMI management.

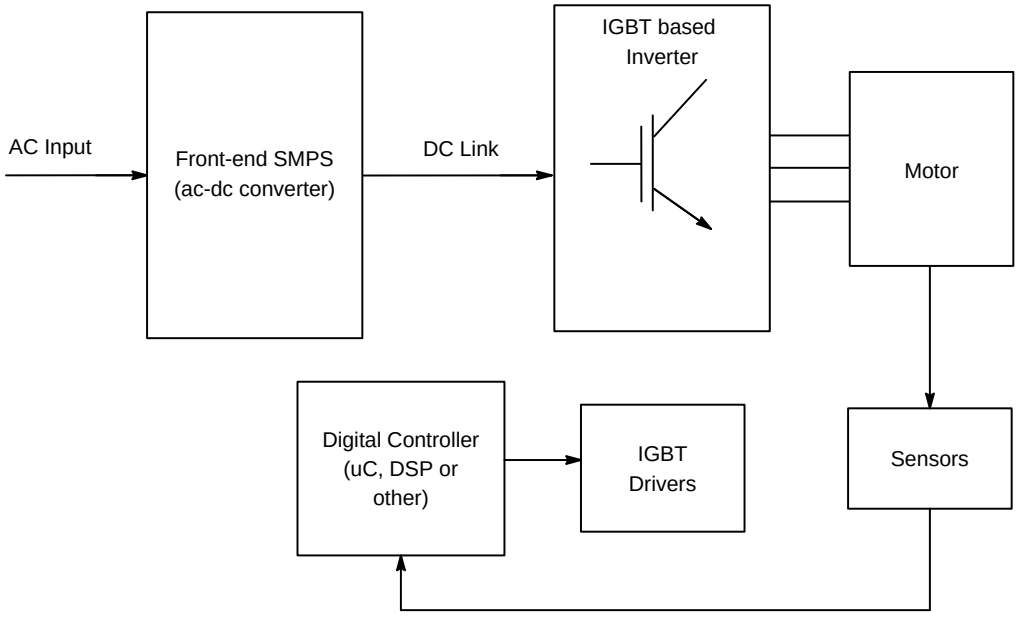

Figure 1. Typical Motor Drive System Block Diagram

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As shown in this block diagram, the motor drive system contains blocks that process high power as well as those that process low level signals. Sensitivity of these blocks to EMI does differ and when they are colocated, it is important to minimize the interactions between the two types. In general, the following areas of EMI management can be identified:

1. Ensuring that digital controller circuits do not get perturbed by the high power switching noise in the inverter or the ac-dc converter.
2. Ensuring that the integrity of the sensed signals from the motor is not compromised due to the EMI generated in other blocks.
3. Ensuring that the power blocks do not get into false switching states due to presence of parasitic switching noise.
4. Ensuring that the driver (which is an interface block) acts as a proper buffer between low power circuits and high power circuits.
5. Ensuring that the motor drive circuit as a whole does not emit or conduct interference signals beyond the limits specified in the EMI/EMC compliance requirements.

The first four items above are necessary for acceptable and robust functioning of the motor drive systems, while the last one is clearly for meeting the external agency compliance requirements.

The techniques for noise management include better circuit design, relevant component choices and proper layout. Each of these will be addressed in the following sections.

CIRCUIT TECHNIQUES

Circuit design can have a profound influence on both the amount of noise produced and the susceptibility of motor drive circuits to the noisy environments in which they operate.

Front-end SMPS

When looking at the front-end ac-dc SMPS, it is important to minimize its contribution to the ambient noise. This can be done by using soft-switching techniques or at the very least, using effective snubbers to minimize the radiated EMI. Any high di/dt or dv/dt in the SMPS can lead to malfunction of more sensitive adjacent blocks such as controller, driver or sensor.

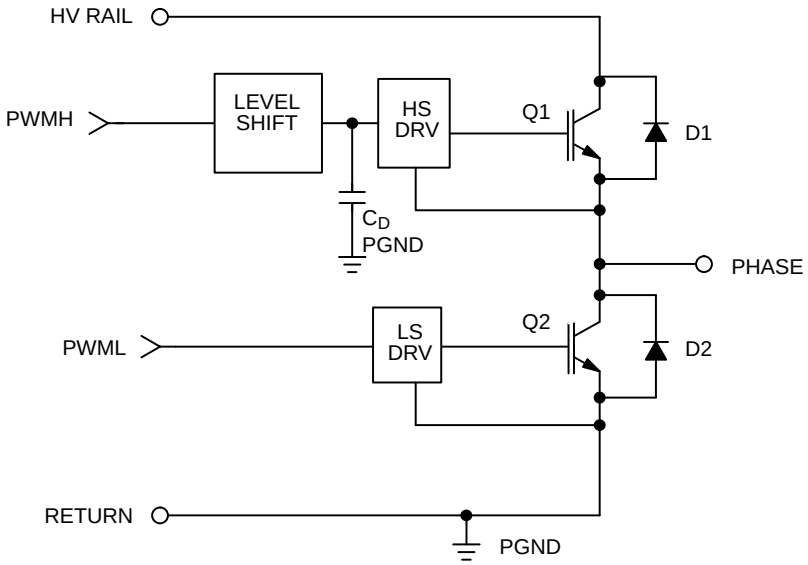

Figure 2. Typical IGBT-based Inverter Stage (one phase)

Inverter and Driver

When considering the inverter and driver blocks, IGBTs are typically used in the high voltage applications only. In these applications, the inverter consists of three identical dual n-channel stages (each phase consisting of one high-side IGBT and one low-side IGBT, anti-parallel diodes for each and associated drive circuitry as shown in Figure 2). Here, the challenge is to provide the level shifting for the high-side IGBT drive. The options for the drive circuit include:

- Low side discrete/integrated drivers followed by gate drive transformers – this option allows the gate drive transformer to provide the required level shifting for high-side IGBT, while the low side is coupled directly

to the driver. Needs adequate delay matching and timing management to control the turn-on and turn-off of the two IGBTs. Noise susceptibility is limited with correct gate drive transformer design which would minimize the capacitance between the windings and may also require a shield.

- Use of integrated high-side, low-side driver with internal timing management – this option integrates the drive circuit into a single IC. Although the early versions of such drivers gained some notoriety due to their noise susceptibility and also noise radiation, subsequent versions have incorporated better layout and control to overcome the noise issues.
- Use of optocouplers to transmit the gate drive signal from controller and use of local drivers for each IGBT – this option provides the best decoupling between the power and control stages. However, it comes with the price of requiring special bias and drive circuits and the need for high speed optocouplers.

While the choice amongst these options depends on the designer familiarity, BOM budget constraints and power levels, it is safe to say that good design and layout practices will allow successful implementation of any of these options in the motor drive applications.

Sensor

The sensor block can also benefit from common design practices such as filtering and buffering to improve noise immunity. In general, the sensor signals have time constants an order of magnitude below the one seen in the PWM inverter, so it is easy to eliminate the noise coupling through good low pass filtering techniques followed by use of Schmitt trigger gates to provide additional noise immunity. This is illustrated in Figure 3. The Hall sensors are in a typically noisy environment since they are close to motor windings with their PWM noise. In order to isolate the sensed position signal from the noise picked up by the Hall sensors before it reaches the controller, filtering and buffering are used. The filter consisting of R2, R3 and C2, has a time constant of 100 ns – much lower than the Hall sensor response times which are typically in micro-seconds. This is good enough to filter out the high-frequency noise spikes, while not disturbing the sensed signal. The filtered signal is next fed to a gate with a Schmitt trigger that has a relatively slow response time and built-in hysteresis. The digitization effect offered by the Schmitt trigger allows the sensed signal to be fed into the controller in a relatively noise-free manner.

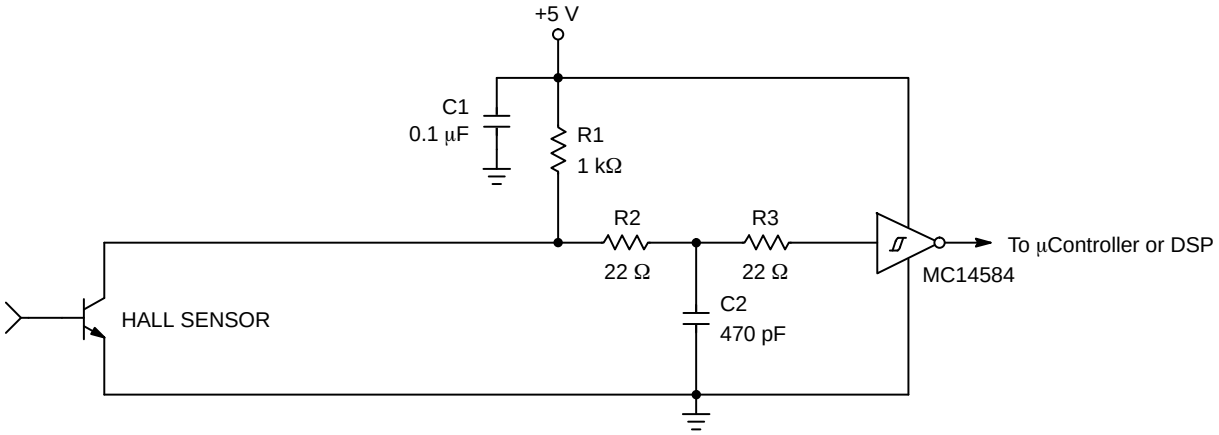

Figure 3. Processing of Hall Sensor Input for Low Noise Immunity

Controller

Finally, the controller, which may be the most noise sensitive block, also requires special attention. It needs good bypassing of critical inputs and buffering of the outputs. The immunity of the controller to noise can be further improved by firmware control where the code provides additional protection against random sequencing of drive signals caused by noise.

COMPONENT CHOICES

In addition to good circuit design techniques, appropriate component choices play an important role in EMI mitigation. Major component groups in a motor drive system are addressed in this section.

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Switching elements such as IGBTs and MOSFETs act as source of EMI and also exhibit susceptibility to it under certain conditions. To address susceptibility, it is important to choose devices which have reasonably high threshold voltages to prevent noise spikes from turning them on spuriously. Good, low impedance drive circuits are also important to prevent faulty turn-on of the switching devices.

While the noise emissions from switching devices are strictly a function of the switching speeds and can be controlled by shaping the switching intervals through the drive circuit, the built-in body diode of the MOSFET is often a major contributor to EMI. In motor drive applications, since the bidirectional switch currents are a norm, this phenomenon is more of a factor. Here, IGBTs provide a better alternative, since they do not have a body diode and an external anti-parallel diode can be independently chosen to meet the system requirements. Typically, a soft recovery diode (with low Qrr) is chosen. The reverse recovery of the high voltage diodes is also a concern in the high side drive circuits, where a high voltage diode is used to bootstrap the bias voltage for the floating high-side bias voltage. In many integrated drivers, this diode is built-in with very snappy turn-off behavior and this leads to radiated EMI issues.

Controllers and Drivers (ICs)

Since the controllers provide the required drive signals for the switching devices, it is important to build noise immunity in these devices. Some controllers (both digital and analog) are inherently more noise immune than others. However, this fact is rarely acknowledged in public domain and it requires careful perusal of datasheets and/or application notes of a particular controller and/or prior experience designing with it to understand its vulnerability to EMI. In controllers and drivers designed for better noise immunity, following features are generally observed:

- Physical separation of power related pins and low level signals which may be noise sensitive
- Sufficient hysteresis on any comparator inputs
- Separate analog and power ground pins
- Signal thresholds which are not too low so that noise can trigger them
- Specified noise immunity on critical pins (50 V/ns or better)
- Ability to withstand negative transient for short duration without latching up

The vulnerability can be minimized by good layout and bypassing practices and the product documentation usually provide guidance to the user regarding these practices. Drivers are meant to be buffers between the vulnerable control circuits and high-noise switching devices. However, in the absence of good design and layout practices, they can inadvertently become the conduits for the noise coupling. Similar to the controllers, the IC drivers vary widely with regards to their EMI generation and susceptibility behavior.

Magnetics

The choices for power magnetics, EMI filter and noise filtering can have a significant impact on the system EMI performance. Often, the characterization of the magnetic components is not as extensive as other components, leading to uninformed and faulty choices of magnetics in circuits. With respect to EMI, it is important to recognize that all inductors have a self-resonant frequency (SRF) beyond which they cease to be inductors. Since the function of the inductor is to typically provide a high impedance at a specified frequency, the SRF is a very critical parameter. The DC resistance of inductors provides damping which is good from an EMI point of view, but adds to the power losses. Also, depending on which section of the circuit the inductor is used in, the type of inductor may differ in terms of core material (Ferrite, powder-iron etc.) and geometries (rod, toroid, EE cores etc.). The transformers used in the front-end SMPS also play a big role in EMI generation if not properly designed. EMI shields are often used to reduce the radiated EMI and y-caps from primary to secondary are employed to provide low impedance path for common mode noise. Ferrite beads provide the quickest “band-aid” solution to the EMI problems during debugging stages, as they can be inserted easily (generally without altering the layout) and are effective in slowing down the fast edges that cause EMI. However, overreliance on these beads is not a good practice because (a) they invariably add to the losses and (b) they are not mechanically robust.

Other Passives

Capacitors are extensively used for bypassing, while a judicious combination of resistors and capacitors is used for passive snubber implementations. The choice of capacitors is important because the ESR values can impact the high frequency performance of capacitors adversely. In general, an SMT ceramic cap is the best choice for bypass filtering. Ceramic capacitors have very low ESR and an SMT package eliminates the lead inductance. The capacitor should be connected as closely as possible to the leads of the chip that it is bypassing. Typically a bypass capacitor is in the capacitance range of 0.01 μF to 1 μF.

LAYOUT

In a motor drive, layout is a critical part of the total design. Often, getting a system to work properly is actually more a matter of layout than circuit design. The following discussion covers some general layout principals, power stage layouts, and controller layouts. It is realized by practicing engineers that there is no single “correct” layout for an application. A good layout generally involves making a number of on the spot technical trade-offs that cumulatively lead to better system performance.

General Principles:

There are several general layout principles that are important to motor drive design. They can be described as five rules:

Rule 1: Minimize Loop Areas. A loop is the circuit trace path from the source of a signal (e.g. driver, FB node) to its destination (e.g. IGBT, error amp) and back to its source through the return path. This is a general principle that applies to both power stages and noise sensitive inputs. Loops are antennas. At noise sensitive inputs, the area enclosed by an incoming signal path and its return is proportional to the amount of noise picked up by the input. At power stage outputs, the amount of noise that is radiated is also proportional to loop area. A corollary of this rule is that the placement of key components that are connected is very critical and they should be placed as close to each other as possible.

Rule 2: Cancel fields by running equal currents that flow in opposite directions as close as possible to each other. If two equal currents flow in opposite directions, the resulting electromagnetic fields will cancel as the two currents are brought infinitely close together. In printed circuit board layout, this situation can be approximated by running signals and their returns along the same path but on different layers. Field cancellation is not perfect due to the finite physical separation, but is sufficient to warrant serious attention in motor drive layouts. Looked at from a different perspective, this is another way of looking at Rule 1, i.e. minimize loop areas.

Rule 3: On traces that carry high speed signals avoid 90 degree angles, including “T” connections. If you think of high speed signals in terms of wavefronts moving down a trace, the reason for avoiding 90 degree angles is straightforward. To a high speed wavefront, a 90 degree angle is a discontinuity that produces unwanted reflections. From a practical point of view, 90 degree turns on a single trace are easy to avoid by using two 45 degree angles or a curve. Where two traces come together to form a “T” connection, adding some copper pour to cut across the right angles accomplishes the same thing.

Rule 4: Connect signal circuit grounds to power grounds at only one point. The reason for this constraint is that transient voltage drops along power grounds can be substantial, due to high values of di/dt flowing through finite inductance. If signal processing circuit returns are connected to power ground a multiple points, then these transients will show up as return voltage differences at different points in the signal processing circuitry. Since signal processing circuitry seldom has the noise immunity to handle power ground transients, it is generally necessary to tie the signal ground to the power ground at only one point. This rule can also be extended to use of ground planes. For power circuits, it is important to have either separate ground planes or ensure that the high current path on the ground plane does not traverse through sensitive signal ground areas on the same plane.

Rule 5: Use Vias very sparingly and selectively. Although vias offer an easy routing solution for complex/dense pcbs, injudicious use of them could lead to EMI and other problems. Vias are used primarily for 3 purposes:

1. To provide signal connection to/from an inner layer plane such as ground plane as well as to provide signal connection between components places on separate layers.
2. To provide alternative routing path for a trace when routing is not possible on the same layer due to presence of other higher priority traces.
3. To provide thermal relief for high current carrying paths/planes on the inner layers.

However, insertion of vias reduces the area of a plane or copper pour, adds capacitance between the vias and the adjoining signals on all layers and causes diversion in traces which could have been more directly routed. Thus, addition of vias involves trade-offs that can be made by experienced layout designers and circuit designers together during the layout.

Layout Consideration for Power Stage:

There are two overriding objectives with regard to power stage layout. First, it is necessary to control noise at the gate drives so power devices are not turned on when they are supposed to be off or vice versa. Second, it is highly desirable to minimize radiated noise with layout, where tight loops and field cancellation can reduce the cost of filters and enclosures. Looking first at the gate drive, noise management is greatly facilitated by using the source or emitter connection for each power device as a miniature ground plane for that device’s gate drive. This is particularly important for high side N-Channel gate drives, where the gate drivers have high dv/dt displacements with respect to power ground. If the power device’s source or emitter connection is used like a ground plane, parasitic capacitive coupling back to power ground is minimized, thereby increasing the dv/dt immunity of the gate drive.

To illustrate this point, let’s refer to and assume that the high-side phase output swings 300 V in 100 nsec as a result of a switching transition, and that the parasitic capacitance to power ground, Cp, is only 1 pF. Then a simple $i = C(dv/dt)$ calculation suggests that 3 mA of charging current will flow through Cp. This 3 mA into 5.6 kΩ of node impedance is much more than enough to cause false transitions. These numbers illustrate a very high sensitivity to parasitic

coupling, which makes layout of this part of the circuit very important.

In addition to viewing source or emitter connections as miniature ground planes, it is also important to keep any signals referenced to ground away from high side gate driver inputs.

Gate drive noise immunity is also facilitated by minimizing the loop area that contains the gate drive decoupling capacitor, gate driver, gate, and source or emitter of the power device. One way to do this is to route the gate drive signal either directly above or beneath its return. If the return is relatively wide (2.5 mm or greater) it forms the miniature ground plane that was previously discussed. The resulting minimum loop area minimizes capacitive coupling as well as antenna effects that inject noise at the input of the gate driver. In addition, relatively high peak gate drive currents get some field cancellation, which reduces radiated noise. The other major source of gate drive noise that causes false transitions is non-zero voltage drops in power grounds. Using opto couplers and routing each gate drive return directly to the emitter of its corresponding power device is one of the ways to provide noise immunity. For motor drives where opto couplers are not practical, taking care to minimize the inductance between power device emitters or sources is a viable alternative.

In terms of reducing the amount of noise that is produced by power stages, minimizing loop areas is a key consideration. The most important is the loop that includes the upper half-bridge IGBT drain, lower half-bridge IGBT source, and high frequency bus decoupling cap. The idea here is to try to keep the high di/dt that is produced during diode reverse recovery in as small an area as possible. This is a part of the circuit where running traces that have equal but opposite currents directly over each other is a priority. Since the currents into and out of the decoupling cap are equal and opposite, running these two traces directly over each other provides field cancellation and minimum loop areas where they are needed most.

Figure 4 illustrates the difference between a loop that has been routed correctly and one that has not. In this figure, the solid circles represent pads, the schematic symbols show the components that are connected to the pads, and two routing layers are shown with cross-hatching that goes in opposite directions. Note that by routing the two traces one over the other that the critical loop area is minimized.

For similar reasons it is desirable to run power and return traces one directly on top of the other. In addition, if a current sensing resistor is used in the return, using a surface mount resistor is preferable due to its lower inductance. It also can be placed directly over the power trace, providing uninterrupted field cancellation from placing power and return traces over each other. Again for field cancellation, it is also desirable to run phase outputs parallel and as close as possible to each other.

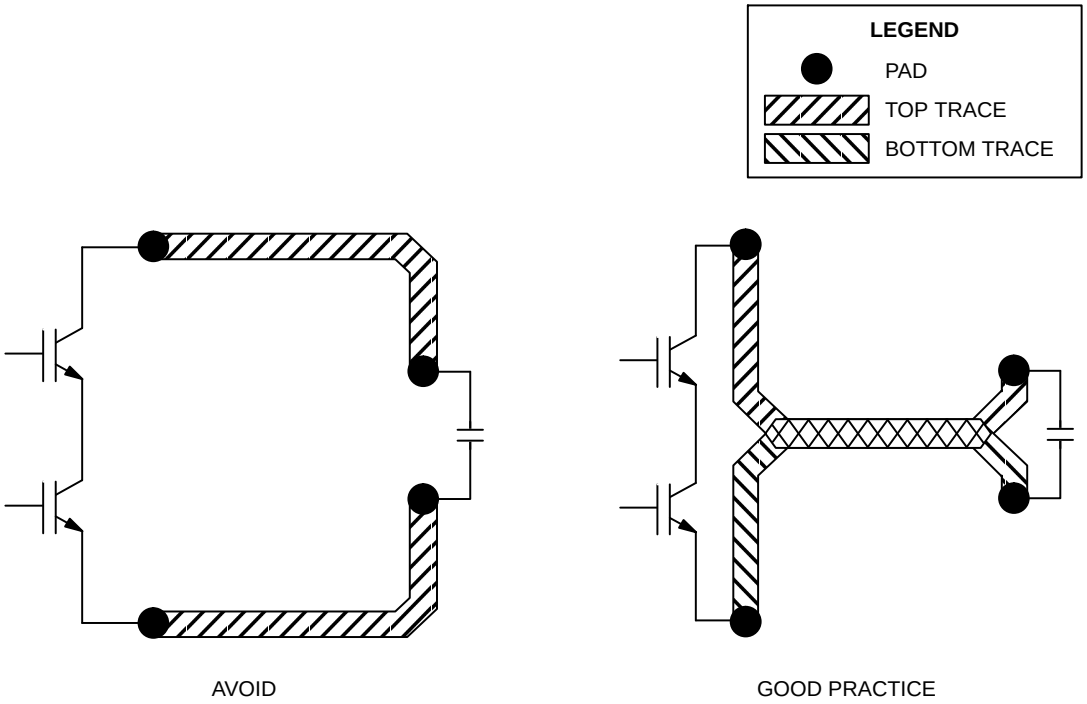

Figure 4. Minimizing Loop Areas

The power stage is the place where avoiding right angles is most important. Single traces are easy, two forty five degree angles or a curve easily accomplish a 90 degree turn. It is just as important to avoid 90 degree angles in T connections. illustrates correct versus incorrect routing for both cases.

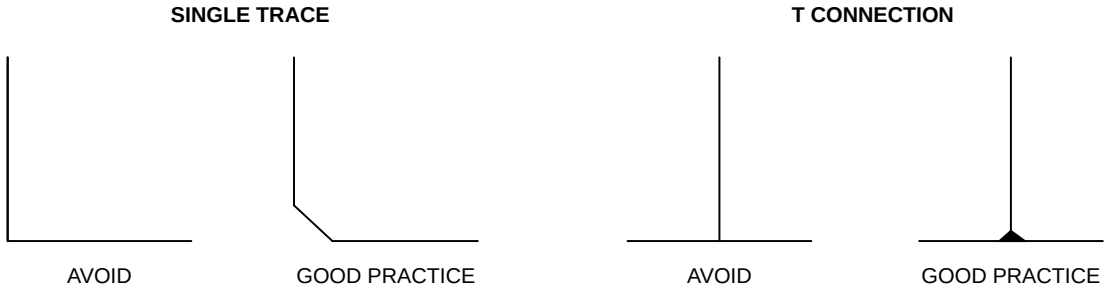

Figure 5. Routing to Avoid 90 Degree Angles

Layout considerations for Controllers:

The primary layout issue with controllers is ground partitioning. A good place to start is with the architecture that is shown in Figure 6. This architecture has several key attributes. Analog ground and power ground are both separate and distinct from digital ground, and both contact digital ground at only one point. For the analog ground, it is preferable to make the one point as close as possible to the digital converter's ground reference (VREFL). The power ground the connection should be as close as possible to the microcomputer's power supply return (VSS). Note also that the path from VREFL to VSS is isolated from the rest of digital ground until it approaches VSS.

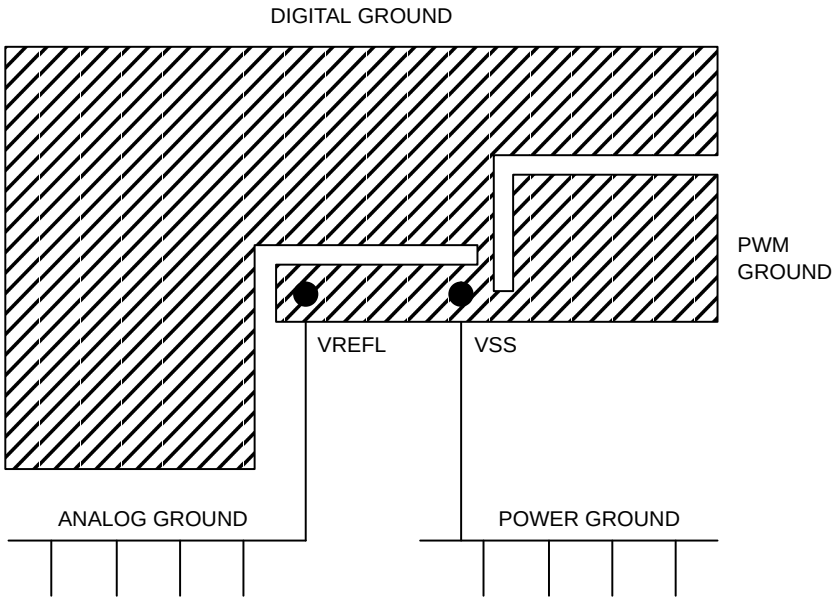

Figure 6. Ground Architecture for Controller Layout

The PWM ground is also isolated as a separate ground plane section until it approaches VSS. This is most important in systems that use optocouplers, since the current that flows through the PWM ground return will be higher than other digital return currents. If a two layer board is used, traces replace the ground planes that are shown in Figure 6. The partitioning, however, remains the same. In addition to grounding, controllers benefit from attention to avoiding 90 degree angles, since there are generally a lot of high speed signals on the digital portion of the board. Routing with 45 degree angles or curves minimizes unwanted reflections, which increases noise immunity.

CONCLUSION

For the most part, the functional architecture of motor drives is much more straightforward than some of the techniques that are required to get them to work. These challenging aspects arise from high levels of both di/dt and dv/dt that produce many noise management issues. These are systems in which a fraction of a picofarad of stray capacitance in the wrong place, a ground connection that is not carefully routed, or the absence of a functionally not so obvious component will all cause improper operation.

The most important design issues are careful attention to grounding, minimizing critical loop areas, use of series bootstrap capacitors, careful attention to power transistor transition times, and filtering sensor inputs. Additional benefits are gained by avoiding 90 degree angles in board layout and cancelling fields by routing equal and opposite current flows as close as possible to each other. As expected, consideration given to these issues up front pays off when it comes to getting a design to work right the first time.

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