

## Product Family Specification

**SCA3060 Series**  
3-axis accelerometer

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## 1 General Description

### 1.1 Introduction

SCA3060 is a three axis accelerometer targeted for automotive applications requiring high performance with low power consumption. It consists of a 3D-MEMS sensing element and a signal conditioning ASIC packaged into Dual Flat Lead (DFL) housing.

The sensing element is manufactured using proprietary bulk 3D-MEMS process, which enables robust, stable and low noise & power capacitive sensors.

Sensors are factory calibrated and the trimmed parameters are gain, offset and frequency of the internal oscillator. Calibration parameters will be read automatically from the internal non-volatile memory during sensor startup.

#### 1.1.1 Operation modes

##### 1.1.1.1 Measurement

The SCA3060 is in normal measurement mode by default after start up. The sensor offers acceleration information via SPI or I<sup>2</sup>C bus when the master requires it. The master can acquire one axis acceleration or all three axis acceleration depending on the application.

##### 1.1.1.2 Motion Detection

Motion Detection (MD) mode is intended to be used to save system level power consumption. In this mode, the SCA3060 activates an interrupt via the INT-pin when motion is detected. Sensitivity levels can be configured via the SPI or I<sup>2</sup>C bus for each axis. Moreover, the detection condition can be defined using sensitivity directions with AND / OR / mux logic. Once the interrupt has happened, the detected direction can be read out from the corresponding status register.

Normal acceleration information is not available in MD mode.

### 1.1.2 Interrupt

The SCA3060 has a dedicated output pin (INT) to be used as the interrupt for the master controller. Interrupt conditions can be activated and deactivated via the SPI or I<sup>2</sup>C bus. Once the interrupt has happened, the interrupt source can be read out from the corresponding status register.

### 1.1.3 Output ring buffer

In those applications where real time acceleration information is not needed, the ring buffer memory can be used to buffer acceleration data. This will release  $\mu$ C resources for other tasks or for example, to offer a power saving mode while SCA3060 samples acceleration data into its buffer memory.

Acceleration data is sampled at a constant sample rate by the sensor. The buffer is a FIFO type (First In First Out) where the oldest data is shifted out first. It has separate read and write address pointers, so it can be read and written simultaneously. If the buffer overflows, the oldest data is lost and the new data replaces the oldest samples.

Ring buffer logic can be configured to give an interrupt when the buffer is  $\frac{1}{2}$  or  $\frac{3}{4}$  full. The entire ring buffer content can be read by one read sequence.

## 2 Reset and power up, Operation Modes, HW functions and Clock

### 2.1 Reset and power up

The SCA3060 has an external active low reset pin. Power supplies must be within the specified range before the reset can be released.

After releasing the reset, the SCA3060 will read configuration and calibration data from non-volatile memory to volatile registers. Then the SCA3060 will make a check sum calculation to the read memory content. The STATUS register's CSME-bit="0" shows successful memory read operation.

### 2.2 Operation modes

#### 2.2.1 Normal measurement mode

The SCA3060 enters the measurement mode by default after power-on and the CV-converter will start to feed data to the signal channel. Data will be reliable in the output registers after the product specific turn-on time.

#### 2.2.2 Wide band measurement mode

In wide band measurement mode, the signal bandwidth of the SCA3060 is increased by removing low-pass filtering in signal channel. In addition, the output data rate is doubled.

#### 2.2.3 Usage

Measurement modes can be selected by setting the bits called MODE\_BITS in MODE register. See section 3.4 for MODE register details.

Acceleration data can be read from data output registers X\_LSB, X\_MSB, Y\_LSB, Y\_MSB, Z\_LSB and Z\_MSB in all measurement modes. Each of these registers can be read one by one or using the decremented register read, which is described in section 4.1.3.2 for SPI and 4.2.1.3 for I<sup>2</sup>C interface. See section 3.3 for output register details.

### 2.2.3.1 Overflow condition

Since acceleration data registers have no limiter, the possible overflow needs to be detected using bits [B7, B6, B5]. If bits [B7, B6, B5] are '010' (also '011') or '101' (also '100'), data overflow has occurred (see Table 1). This applies for all acceleration output registers (X\_LSB ... Z\_MSB and BUF\_DATA).

Table 1. Overflow bit patterns in acceleration data registers (X\_LSB ... Z\_MSB and BUF\_DATA).

Byte	MSB byte								LSB byte					
Bit number	B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2:B0
Acceleration data bit	Sign	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	
Data overflow on positive acceleration	0	1	0	x	x	x	x	x	x	x	x	x	x	xxx
Data overflow on negative acceleration	1	0	1	x	x	x	x	x	x	x	x	x	x	xxx

x = ignore

In case of overflow, the output register value must be discarded. When an overflow is detected, the bit pattern '0011 1111 1111 1xxx' is used for positive accelerations and '1100 0000 0000 0xxx' for negative accelerations until a valid acceleration value is read. In Table 2 the maximum and minimum acceleration register values that are in measuring range (for registers X\_LSB ... Z\_MSB) for SCA3060 are presented.

Table 2. Maximum and minimum values in the SCA3060 measuring range.

		SCA3060
First positive acceleration value	[mg]	-
out of range	dec	2048
	bin	0100 0000 0000 0xxx
Maximum positive acceleration value	[mg]	2047 mg
in range	dec	2047
	bin	0011 1111 1111 1xxx
Minimum negative acceleration value	[mg]	-2047 mg
in range	dec	-204
	bin	1100 0000 0000 0xxx
First negative acceleration value	[mg]	-
out of range	dec	-2048
	bin	1011 1111 1111 1xxx

## 2.3 Motion Detection Mode

### 2.3.1 Description

In MD mode, the ADC's data is not fed to the signal processing channel but to the MD block. It consists of a digital band-pass filter (BPF), threshold level programmable digital comparator and a configurable trigger function.

BPF's -3 dB low-pass frequency is 25 Hz ...60 Hz and -3 dB high-pass frequency is 0.05 Hz ...1 Hz. See Figure 1 below.

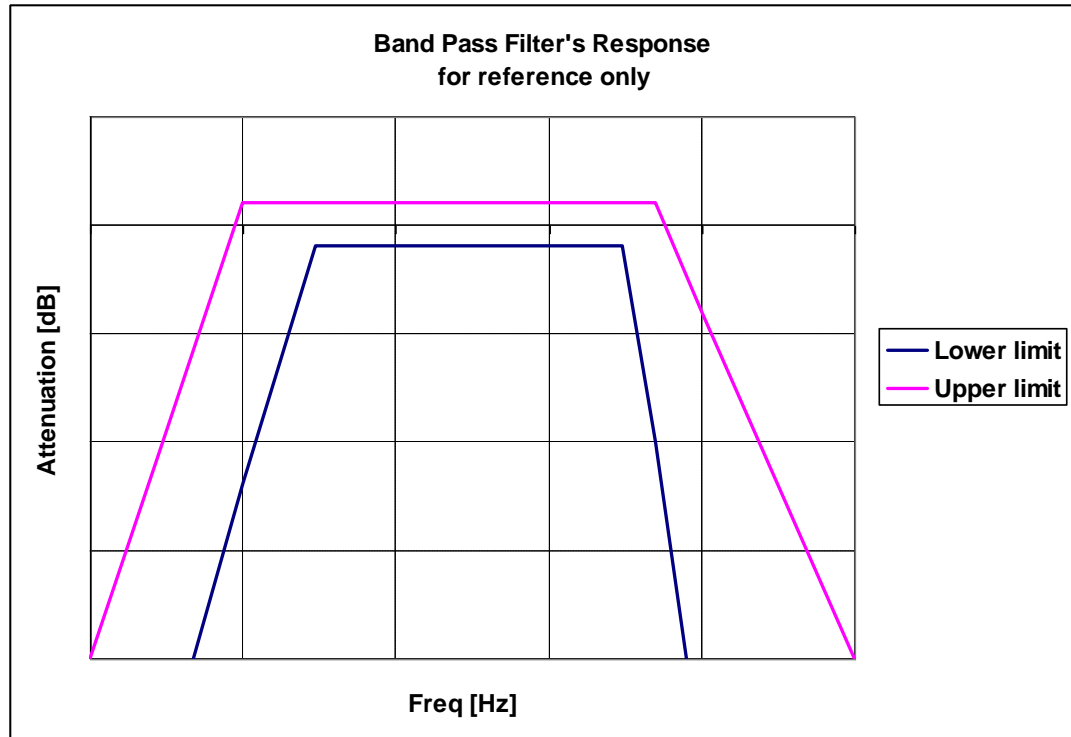


Figure 1. The MD band-pass filter's frequency response.

The absolute value of programmable Threshold Level (TL) is  $0 < |TL| < FS$  (FS is sensor full scale measuring range). NOTE: Due to power consumption optimization, the step size between each step and axis is not the same, see section 3.4 for threshold level details.

Motion detection is sensitive to directions according to Figure 2,

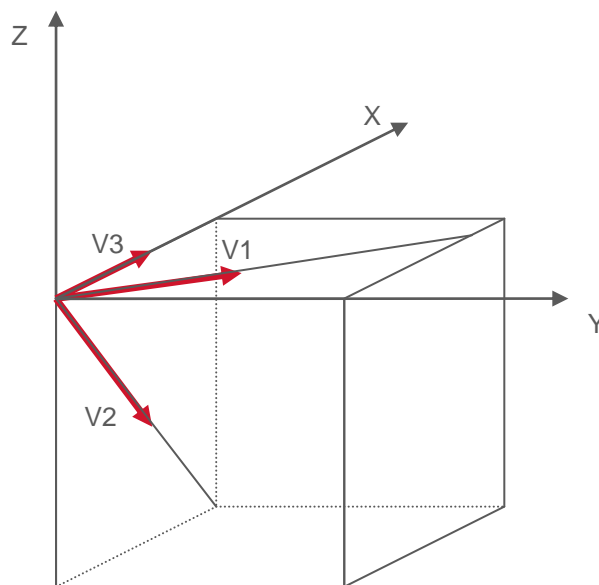


Figure 2. MD Sensitive axis

where X, Y and Z represent Component axis and V1, V2, and V3 MD sensitive axis. Correlation between axis is  $V1 = X + \sqrt{2} \cdot Y$ ,  $V2 = X - Z$  and  $V3 = X$ .

The triggering condition can be defined using OR/AND logic:

1. Any sensing direction can be configured to trigger the interrupt (OR condition).
2. Any sensing direction can be configured to be required to trigger the interrupt (AND condition).

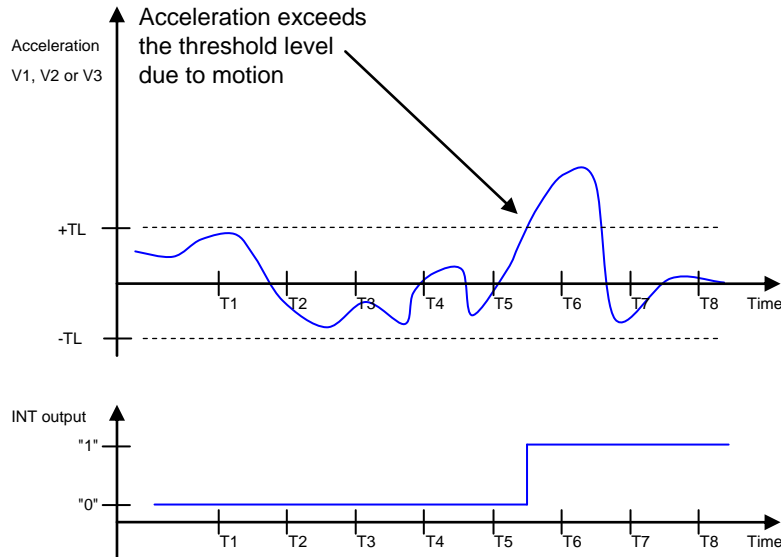


Figure 3. Motion detector operation.

### 2.3.2 Usage

The MD mode can be enabled by setting the MODE bits in the MODE register to "011". The trigger condition can be defined by setting REQ\_V3, REQ\_V2, REQ\_V1, EN\_V3, EN\_V2 and EN\_V1 bits in MD\_CTRL register and V3\_TH, V2\_TH and V1\_TH bits in MD\_V3\_TH, MD\_V2\_TH and MD\_V1\_TH registers, respectively. See section 3.4 for the configuration register and section 2.5 for the interrupt functionality details.

In MD mode, acceleration data is not available in registers X\_LSB, X\_MSB, Y\_LSB, Y\_MSB, Z\_LSB, Z\_MSB and BUF\_DATA.

### 2.3.3 Examples

A simple example of motion detection usage:

1. Write "00000011" (03h) into the MODE register (enable motion detection mode, MODE\_BITS = '011').
2. Acceleration data is not available when the SCA3060 is in motion detection mode.
3. The INT-pin is activated when motion is detected, see section 2.5 for detailed INT-pin information.

In the next example, the motion detector is configured to give an interrupt on motion only in the V1-OR V2-axis direction:

1. Write "00000011" (03h) into MODE register (enable motion detection mode, MODE\_BITS = '011')
  2. Write "00000000" (00h) into UNLOCK register
  3. Write "01010000" (50h) into UNLOCK register
  4. Write "10100000" (A0h) into UNLOCK register
  5. Write "00000010" (02h) into CTRL\_SEL register (to select indirect MD\_CTRL register)
  6. Write "00000011" (03h) into CTRL\_DATA register (this data is written into MD\_CTRL register, enable trigger on V2-channel, EN\_V2 = '1', enable trigger on V1-channel, EN\_V1 = '1')
- } Unlock sequence for register lock



7. Acceleration data is not available when the SCA3060 is in motion detection mode. The INT-pin is activated when motion is detected in the V1- or V2-axis direction (V3-axis direction is ignored), see section 2.5 for detailed INT-pin information

## 2.4 Ring Buffer

### 2.4.1 Description

The SCA3060's Ring Buffer is a 192 acceleration data samples long (for example 64 samples of 11 bit three axis data) internal memory to relax real-time operation requirements of the host processor. The following parameters are configurable:

1. Each measurement axis can be individually disabled. If measurement data from e.g. Y-axis is not needed, available memory can be used for X- and Z-axis data.
2. Buffer data length can be changed from 11 to 8 bits. In 8-bit mode, data can be read out using shorter read sequence.
3. Ring buffer's input sample rate can be the same as the sensor's data rate or divided by either 2 or 4. When the divider is e.g. 2, only every 2<sup>nd</sup> acceleration data will be stored.
4. The Interrupt condition, when enabled, can be selected from two options: interrupt in INT-pin occurs when the buffer is 50% or 75% full.

### 2.4.2 Usage

The ring buffer can be enabled by setting BUF\_EN bit in MODE register to "1". After enabling the buffer, acceleration data can be read from BUF\_DATA register using decremented register read, which is described in section 4.1.3.2 for SPI and 4.2.1.3 for I<sup>2</sup>C interface.

Each measurement axis can be individually disabled by setting corresponding bits in BUF\_X\_EN, BUF\_Y\_EN and BUF\_Z\_EN in OUT\_CTRL register to "0".

Output data length can be changed from 11 bits to 8 bits by setting bit BUF\_8BIT in MODE register to "1". See section 3.3 for bit level descriptions.

The count of available data samples in output ring buffer can be read from BUF\_COUNT register. Register value is updated only when it is accessed over the SPI or I<sup>2</sup>C.

Data shift out order is X,Y,Z. In 11 bit mode two bytes must be read to get all 11 bits out. In that case, the MSB byte is 1<sup>st</sup>. Examples:

1. 11 bits data length, X&Y&Z axis enabled:  
X1\_MSB, X1\_LSB, Y1\_MSB, Y1\_LSB, Z1\_MSB, Z1\_LSB, X2\_MSB, X2\_LSB, ... latest Z\_LSB
2. 11 bits data length, Y&Z axis enabled:  
Y1\_MSB, Y1\_LSB, Z1\_MSB, Z1\_LSB, Y2\_MSB, Y2\_LSB, Z2\_MSB, Z2\_LSB, Y3\_MSB, Y3\_LSB, ..., latest Z\_LSB
3. 8 bits data length, all axis enabled:  
X1, Y1, Z1, X2, Y2, Z2,..., latest Z
4. 8 bits data length, X&Z axis enabled:  
X1, Z1, X2, Z2, X3, Z3, ..., latest Z
5. 8 bits data length, Z axis enabled:  
Z1, Z2, Z3, ... , latest Z

See section 2.5 for interrupt functionality details.

Acceleration data is available in X\_LSB, X\_MSB, Y\_LSB, Y\_MSB, Z\_LSB and Z\_MSB when the ring buffer is enabled.

### 2.4.2.1 Overflow condition

Overflow is detected from data ring buffer in the same way as from the output registers. See section 2.2.3.1 for details.

### 2.4.3 Examples

A simple example of output ring buffer usage:

1. Write "10000000" (C0h) into MODE register (enable output ring buffer, BUF\_EN = '1')
2. Acceleration data can be read normally
3. INT-pin is activated when buffer is ½ full, see section 2.5 for detailed INT-pin information.

In the next example, the output Ring Buffer is configured to sample only the Z-axis acceleration data with 8 bit resolution and reduced data rate (only every second sample is stored into output ring buffer). In addition, the SCA3060 is configured to give an interrupt when the output ring buffer is ¾ full:

1. Write "00000000" (00h) into UNLOCK register
2. Write "01010000" (50h) into UNLOCK register
3. Write "10100000" (A0h) into UNLOCK register
4. Write "00001011" (0Bh) into CTRL\_SEL register (to select indirect OUT\_CTRL register)
5. Write "00000101" (03h) into CTRL\_DATA register (this data is written into OUT\_CTRL register, store Z-axis data, BUF\_Z\_EN = '1', divide data rate by 2, BUF\_RATE = '01')
6. Write "10000001" (81h) into INT\_MASK register (set buffer interrupt level to ¾ full, BUF\_F\_EN = '1', set INT-pin to active high, INT\_ACT = '1')
7. Write "11000000" (C0h) into the MODE register (enable output ring buffer, BUF\_EN = '1', set data length to 8 bits, BUF\_8BIT = '1')
8. Acceleration data can be read normally for all axis and with full resolution. The buffer data can be read from BUF\_DATA register
9. INT-pin is activated when the output ring buffer is ¾ full of Z-axis acceleration data, see section 2.5 for detailed INT-pin information.

## 2.5 Interrupt function (INT-pin)

### 2.5.1 Usage

The Motion Detector will generate an interrupt to INT-pin when the corresponding function is enabled and the interrupt condition is met. The SCA3060's ring buffer will generate an interrupt when interrupt functionality has been enabled. Setting BUF\_F\_EN bit in INT\_MASK register "1" results in interrupt when the register is 75% full. Setting BUF\_H\_EN bit in INT\_MASK register "1" results in interrupt when the register is 50% full.

Setting INT\_ALL bit in INT\_MASK register will mask all interrupts.

The interrupt polarity (active high/low) can be configured with INT\_MASK register's INT\_ACT bit.

Once the interrupt has happened, the INT\_STATUS register must be read to acknowledge the interrupt.

1. If at least one of MD bits in INT\_STATUS register is "1", motion has been detected.
2. If BUF\_FULL bit is "1", Ring Buffer is 75% full. Correspondingly, if BUF\_HALF is "1", the Ring Buffer is 50% full.

See section 3.3 for INT\_STATUS register details.

## 2.6 Clock

The SCA3060 has an internal factory trimmed oscillator and clock generator.

### 3 Addressing Space

The SCA3060 register contents and bit definitions are described in more detail in the following sections.

#### 3.1 Register Description

The SCA3060 addressing space is presented in Table 3 below.

Table 3. List of registers.

Addr.	Name	Description	Mode (R, W, RW, IA)	Reg. type	Locked
00h	REVID	ASIC revision ID number	R	Conf	
01h		Reserved			-
02h	STATUS	Status register	R	Conf	
03h		Reserved			-
04h	X_LSB	X-axis LSB frame	R	Output	
05h	X_MSB	X-axis MSB frame	R	Output	
06h	Y_LSB	Y-axis LSB frame	R	Output	
07h	Y_MSB	Y-axis MSB frame	R	Output	
08h	Z_LSB	Z-axis LSB frame	R	Output	
09h	Z_MSB	Z-axis MSB frame	R	Output	
0Ah ... 0Eh		Reserved			-
0Fh	BUF_DATA	Ring buffer output register	R	Output	
10h ... 11h		Reserved			-
12h		Reserved			
13h		Reserved			
14h	MODE	Operating mode selection, control and configuration for: - mode selection - output buffer	RW	Conf	
15h	BUF_COUNT	Count of unread data samples in output buffer	R	Output	
16h	INT_STATUS	Interrupt status register: - output buffer is not full, ½ full or ¾ full - information of which axis triggered motion	R	Output	
17h		Reserved			
18h	CTRL_SEL	Register address pointer for indirect control registers	RW	Conf	x
19h		Reserved			-
... 1Dh		Reserved			
1Eh	UNLOCK	Unlock register	RW	Conf	
1Fh ... 20h		Reserved			-

Addr.	Name	Description	Mode (R, W, RW, IA)	Reg. type	Locked
21h	INT_MASK	HW interrupt mask register (configures the operation of INT-pin): - interrupt when output buffer is $\frac{3}{4}$ full (enable / disable) - interrupt when output buffer is $\frac{1}{2}$ full (enable / disable) - mask all interrupts on INT-pin (enable / disable) - INT-pin activity (INT active low / INT active high)	RW, NV	Conf	
22h	CTRL_DATA	Data to/from register which address is in CTRL_SEL (18h) register	RW, NV, IA	Conf	x
23h ... 3Fh		Reserved			-

Add. is the register address in hex format.

RW – Read / Write register, R – Read-only register, NV – Register mirrors NV-memory data (NV = non-volatile).

IA – indirect addressing used.

Registers whose read and write access is blocked by register lock is marked in "Locked" column.

## 3.2 Non-volatile memory

The SCA3060 has an internal non-volatile memory for calibration and configuration data. Memory content will be programmed during production and is not user configurable. Initial configuration values can be found in the following section 3.4.

## 3.3 Output Registers

The SCA3060 output registers (marked with 'Output' in Table 3) contents and bit definitions are described in this section. Output registers contain information of measured acceleration and temperature as well as information of the operating state and interrupts of SCA3060.

When reading the output values an MSB register must be read first because MSB register reading latches the data in to all other acceleration output registers

Address: **04h**

Register name: **X\_LSB**, X-axis LSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	X-axis LSB frame

Address: **05h**

Register name: **X\_MSB**, X-axis MSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	X-axis MSB frame

Address: **06h**

Register name: **Y\_LSB**, Y-axis LSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Y-axis LSB frame

Address: **07h**

Register name: **Y\_MSB**, Y-axis MSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Y-axis MSB frame

Address: **08h**

Register name: **Z\_LSB**, Z-axis LSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Z-axis LSB frame

Address: **09h**

Register name: **Z\_MSB**, Z-axis MSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Z-axis MSB frame

Address: **0Fh**

Register name: **BUF\_DATA**, ring buffer output register

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Ring buffer output register

Bit level description for acceleration data from X\_LSB ... Z\_MSB and BUF\_DATA registers is presented in Table 4. Acceleration data is presented in 2's complement format. At 0 g acceleration the output is ideally 00h.

Table 4. Bit level description for acceleration registers of SCA3060-D01

Byte	MSB byte								LSB byte					
Bit number	B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2:B0
Acceleration [mg]	Sign	2048	1024	512	256	128	64	32	16	8	4	2	1	xxx
SCA3060-D01 [X_LSB...Z_MSB]	s	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	xxx
SCA3060-D01														
Ring buffer in 11-bit mode [BUF_DATA]	s	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	x	x	xxx
SCA3060-D01														
Ring buffer in 8-bit mode [BUF_DATA]	s	d6	d5	d4	d3	d2	d1	d0	x	x	x	x	x	xxx

s = sign bit

x = not used bit

Address: **15h**

 Register name: **BUF\_COUNT**, output ring buffer status

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	COUNT	Count of available data samples in output ring buffer, for more information see section 2.4.2.

 Address: **16h**

 Register name: **INT\_STATUS**, interrupt status register (all interrupts that are available in current operation mode)

Bits	Mode	Initial Value	Name	Description
7	R	0	BUF_FULL	Output ring buffer is $\frac{3}{4}$ full 1 – Ring buffer is $\frac{3}{4}$ full 0 – Ring buffer is not full
6	R	0	BUF_HALF	Output ring buffer is $\frac{1}{2}$ full 1 – Ring buffer is $\frac{1}{2}$ full 0 – Ring buffer is not full
5:3				Reserved
2:0	R	000	MD	Motion detector triggered channel indication 1xx – Trigger on V1-axis x1x – Trigger on V2-axis xx1 – Trigger on V3-axis

### 3.4 Configuration Registers

SCA3060 configuration register (marked with 'Conf' in Table 3) contents and bit definitions are described in this section. Configuration registers are used to configure SCA3060 operation and the operation parameters.

 Address: **00h**

 Register name: **REVID**, ASIC revision ID number tied in metal

Bits	Mode	Initial Value	Name	Description
7:4	R	2h	REVMaj	Major revision number
3:0	R	1h	REVMIN	Minor revision number

 Address: **02h**

 Register name: **STATUS**, status register

Bits	Mode	Initial Value	Name	Description
7:6				Reserved
5	R	0	LOCK	Status of lock register 0 – Lock is closed 1 – Lock is open
4:2				Reserved
1	R	0	CSME	EEPROM checksum error 1 – EEPROM checksum error 0 – No error
0	R	0	SPI_FRAME	SPI frame error. Bit is reset, when next correct SPI frame is received (only for products with SPI bus). 1 – SPI frame error 0 – No error

Address: **14h**

Register name: **MODE**, operation mode selection

Bits	Mode	Initial Value	Name	Description
7	RW	0	BUF_EN	Output ring buffer 1 – Enabled 0 – Disabled (Buffer in power down)
6	RW	0	BUF_8BIT	Output ring buffer data length 1 – Ring buffer is read in single 8 bit frame per stored axis (8 bit mode) 0 – Ring buffer is read in two 8 bit frames per stored axis (11 bit mode). Unused bits are set to 0.
5:3				Reserved
2:0	RW	000	MODE_BITS	Selects SCA3060-D01 operation mode 000 – Normal measurement mode 001 – Wide band measurement mode 011 – MD, Motion Detector Other combinations are reserved

Address: **17h**

Register name: **I2C\_RD\_SEL**, register address for I<sup>2</sup>C read operation

Bits	Mode	Initial Value	Name	Description
7:0	W	00h	ADDR	Address of register to be read via I <sup>2</sup> C. Register is used only for I <sup>2</sup> C read access.

Address: **18h**

Register name: **CTRL\_SEL**, Control register selector, **UNLOCK REQUIRED**

Bits	Mode	Initial Value	Name	Description
7:5	RW	000		Reserved
4:0	RW	00000	SELECT	Indirect control registers, select register address for read / write access: 00010 – MD_CTRL (Motion Detector control) 00011 – MD_V1_TH (Motion Detector V1-threshold) 00100 – MD_V2_TH (Motion Detector V2-threshold) 00101 – MD_V3_TH (Motion Detector V3-threshold) 01011 – OUT_CTRL (Output control) Other combinations are reserved

CTRL\_SEL register works as an address pointer for registers listed below. When this register is written the content of selected register is available for reading/writing from/to register CTRL\_DATA.

Address value: **00010**

Register name: **MD\_CTRL**, Motion Detector control (Indirect access via CTRL\_SEL)

Bits	Initial Value	Name	Description	Note
7:6			Reserved	
5	0	REQ_V3	1 – Require trigger on V3-channel 0 – Not required	Bits 5:3 can be used to build logical AND operation between channels. Example: V1 and V2 = Require V1 and V2, ignore V3 → 00 011 011
4	0	REQ_V2	1 – Require trigger on V2-channel 0 – Not required	
3	0	REQ_V1	1 – Require trigger on V1-channel 0 – Not required	
2	1	EN_V3	1 – Enable trigger on V3-channel 0 – Not required	Bits 2:0 can be used to build logical OR operation between channels. Example: V1 or V2 = Disable V3 → 00 000 011
1	1	EN_V2	1 – Enable trigger on V1-channel 0 – Not required	
0	1	EN_V1	1 – Enable trigger on V2-channel 0 – Not required	

Address value: **00011**

Register name: **MD\_V1\_TH**, Motion Detector V1-threshold (Indirect access via CTRL\_SEL)

Bits	Initial Value	Name	Description
7:0	08h	V1_TH	Threshold for V1 direction acceleration change when MD is used.

Address value: **00100**

Register name: **MD\_V2\_TH**, Motion Detector V2-threshold (Indirect access via CTRL\_SEL)

Bits	Initial Value	Name	Description
7:0	08h	V2_TH	Threshold for V2 direction acceleration change when MD is used.

Address value: **00101**

Register name: **MD\_V3\_TH**, Motion Detector V3-threshold (Indirect access via CTRL\_SEL)

Bits	Initial Value	Name	Description
7:0	08h	V3_TH	Threshold for V3 direction acceleration change when MD is used.

- Initial values for registers MD\_V1\_TH, MD\_V2\_TH and MD\_V3\_TH are 08h.

The bit level descriptions for registers MD\_V1\_TH, MD\_V2\_TH and MD\_V3\_TH are presented in Table 5 below. The threshold levels are in unsigned format and they are absolute values for the acceleration that triggers the motion detector interrupt. Values presented below are typical threshold values and they are not factory calibrated.



Table 5. Bit level description for motion detector typical threshold levels **(preliminary values)**

Bit number	Typical bit weights							
	B7	B6	B5	B4	B3	B2	B1	B0
SCA3060								
Acceleration [mg]	x	1728	864	432	216	108	54	27
<b>MD_V1_TH</b>								
SCA3060								
Acceleration [mg]	x	2000	1000	500	250	125	63	31
<b>MD_V2_TH, MD_V3_TH</b>								

x = not used bit

Address value: **01011**

Register name: **OUT\_CTRL**, Output configuration (Indirect access via CTRL\_SEL)

Bits	Initial Value	Name	Description
7:5			Reserved
4	1	BUF_X_EN	Store X-axis acceleration data to ring buffer 1 – enabled 0 – disabled
3	1	BUF_Y_EN	Store Y-axis acceleration data to ring buffer 1 – enabled 0 – disabled
2	1	BUF_Z_EN	Store Z-axis acceleration data to ring buffer 1 – enabled 0 – disabled
1:0	00	BUF_RATE	Additional data rate reduction after calibration before data is loaded to ring buffer (no effect on output registers data rate, see section 2.4.1) 11 – No rate reduction 10 – divide rate by 4 01 – divide rate by 2 00 – No rate reduction

Address: **1Eh**

Register name: **UNLOCK**, Unlock register lock

Bits	Mode	Initial Value	Name	Description
7:0	RW	00h	KEY	Lock can be opened by writing the following sequence into this register: 00h, 50h, A0h Writing any other sequence closes the lock. Lock state can be read from STATUS register.

Address: **21h**

Register name: **INT\_MASK**, HW interrupt mask register configures the operation of the INT pin.

Bits	Mode	Initial Value	Name	Description
7	RW	0	BUF_F_EN	Interrupt when output ring buffer is $\frac{3}{4}$ full 1 – Enabled 0 – Disabled
6	RW	1	BUF_H_EN	Interrupt when output ring buffer is $\frac{1}{2}$ full 1 – Enabled 0 – Disabled
5:2				Reserved
1	RW	0	INT_ALL	Mask all interrupts (only effects on the INT-pin) 1 – Mask all interrupts 0 – Mask interrupts according to configured mode
0	RW	1	INT_ACT	INT-pin signal activity 1 – INT active high (INT-pin high) 0 – INT active low (INT-pin low)

Address: **22h**

Register name: **CTRL\_DATA**, Control register data, **UNLOCK REQUIRED**

Bits	Mode	Initial Value	Name	Description
7:0	RW	00h	DATA	Data bits [7:0] of selected 8-bit control register. Write this register to actually perform the write operation to selected location. See register CTRL_SEL for information on register contents.

## 4 Serial Interfaces

Communication between the SCA3060 sensor and master controller is based on serial data transfer and a dedicated interrupt line (INT-pin). Two different serial interfaces are available for the SCA3060 sensor: SPI and I<sup>2</sup>C (Phillips specification V2.1). However, only one per product is enabled by pre-programming at the factory. The SCA3060 acts as a slave on both the SPI and I<sup>2</sup>C bus.

### 4.1 SPI Interface

SPI bus is a full duplex synchronous 4-wire serial interface. It consists of one master device and one or more slave devices. The master is defined as a micro controller providing the SPI clock, and the slave as any integrated circuit receiving the SPI clock from the master. The SCA3060 sensor always operates as a slave device in master-slave operation mode. A typical SPI connection is presented in Figure 4.

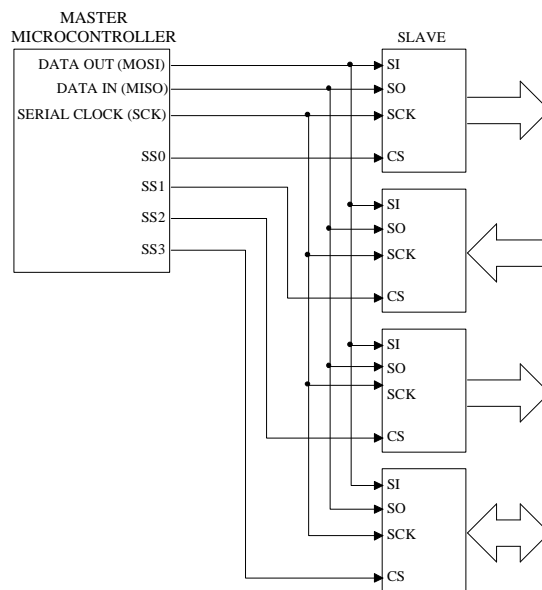


Figure 4. Typical SPI connection.

The data transfer uses the following 4-wire interface:

MOSI	master out slave in	$\mu\text{C} \rightarrow \text{SCA3060}$
MISO	master in slave out	$\text{SCA3060} \rightarrow \mu\text{C}$
SCK	serial clock	$\mu\text{C} \rightarrow \text{SCA3060}$
CSB	chip select (low active)	$\mu\text{C} \rightarrow \text{SCA3060}$

#### 4.1.1 SPI frame format

SCA3060 SPI frame format and transfer protocol is presented in Figure 5.

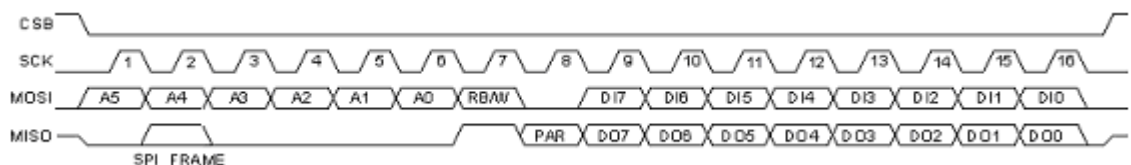


Figure 5. SPI frame format.

Each communication frame contains 16 bits. The first 8 bits in MOSI line contains info about the operation (read/write) and the register address being accessed. The first 6 bits define the 6 bit

address for the selected operation, which is defined by bit 7 ('0' = read '1' = write), which is followed by one zero bit. The later 8 bits in the MOSI line contain data for a write operation and are 'don't-care' for a read operation. Bits from MOSI line are sampled in on the rising edge of SCK and bits to MISO line are latched out on falling edge of SCK.

The first bits in the MISO line are the frame error bit (SPI\_FRAME, bit 2) of the previous SPI frame and odd parity bit (PAR, bit 8). Parity is calculated from data which is currently sent. Bit 7 is always '1'. The later 8 bits contain data for a read operation. During the write operation, these data bits are previous data bits of the addressed register.

For write commands, data is written into the addressed register on the rising edge of CSB. If the command frame is invalid data will not be written into the register (please see "error conditioning" in section 4.1.2).

For read commands, data is latched into the internal SPI output register (shift register) on the 8th rising edge of SCK. The output register is shifted out MSB first over MISO output.

When the CSB is high state between data transfers, the MISO line is in the high-impedance state.

### 4.1.2 SPI bus error conditioning

While sending an SPI frame, if the CSB is raised to 1

- before sending 16 SCKs or
- the number of SCK pulses is not divisible by 8,

the frame error is activated and the frame is considered invalid. The status bit STATUS.SPI\_FRAME is set to indicate the frame error condition. During the next SPI, the frame error bit is sent out as SPI\_FRAME bit (see SPI\_FRAME in MISO line in Figure 5). STATUS.SPI\_FRAME bit is reset, if correct frame is received.

When an invalid frame is received, the last command is simply ignored and the register contents are left unchanged. If frame error happens while sending multiple samples in ring buffer mode, only the last output value is considered invalid.

### 4.1.3 Examples of SPI communication

#### 4.1.3.1 Example of register read

An example of 11 bit X-axis acceleration read command is presented in Figure 6. The master gives the register address to be read via the MOSI line: '05' in hex format and '000101' in binary format, register name is X\_MSB (X-axis MSB frame). 7<sup>th</sup> bit is set to '0' to indicate the read operation.

The sensor replies to a requested operation by transferring the register content via MISO line. After transferring the asked X\_MSB register content, the master gives next register address to be read: '04' in hex format and '000100' in binary format, register name is X\_LSB (X-axis LSB frame). The sensor replies to the requested operation by transferring the register content MSB first.

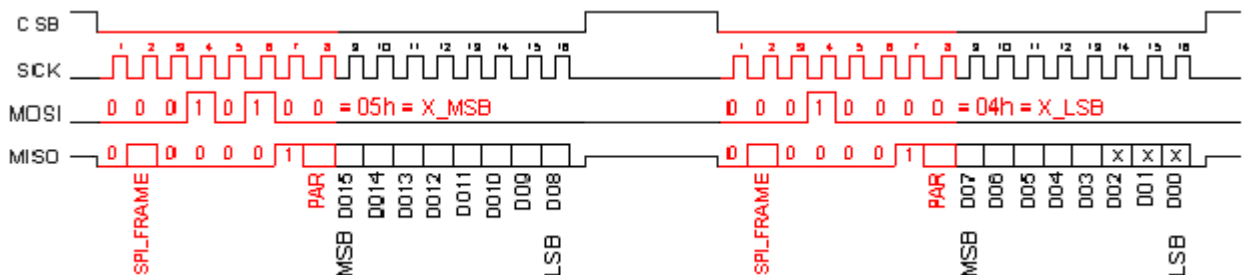


Figure 6. An example of SPI read communication.

#### 4.1.3.2 Example of decremented register read

Figure 7 presents a decremented read operation where the content of four output registers is read by one SPI frame. After normal register addressing and one register content reading, the  $\mu\text{C}$  keeps the CSB line low and continues supplying the SCK pulses. After every 8 SCK pulses, the output data address is decremented by one and the previous acceleration output register's content is shifted out without parity bits. The parity bit in Figure 4 is calculated and transferred only for the first data frame. From the X\_LSB register address, the SCA3060 jumps to Z\_MSB. Decremental reading is possible only for registers X\_LSB ... Z\_MSB.

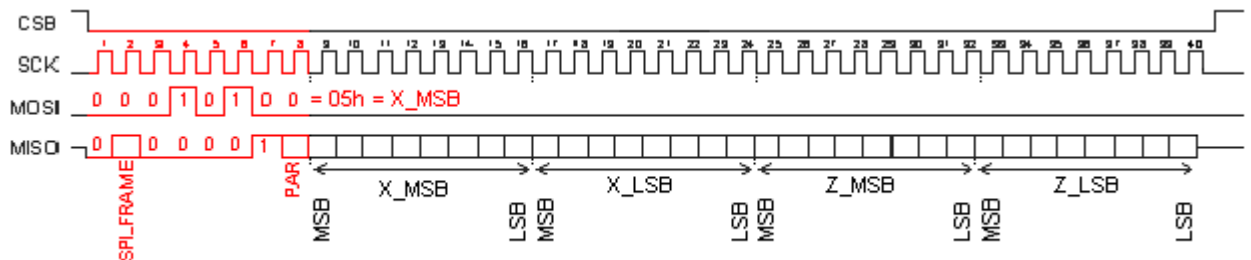


Figure 7. An example of decremented read operation.

#### 4.1.3.3 Example of ring buffer read

An example of output ring buffer read by one SPI frame (ring buffer data length 8 bits) is presented in Figure 8. The whole ring buffer read procedure is very similar to decremented read described above. The output ring buffer is addressed (register name BUF\_DATA). The SCA3060 sensor continues shifting out the ring buffer content as long as  $\mu\text{C}$  continues supplying the SCK pulses.

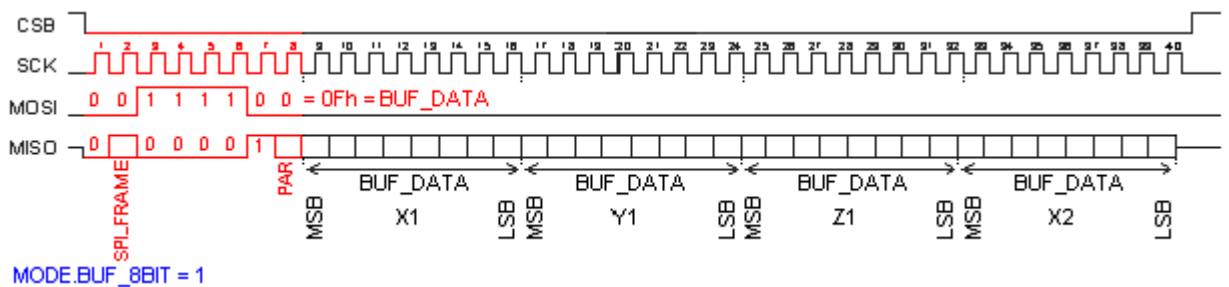


Figure 8. An example of output ring buffer read operation.

## 4.2 I<sup>2</sup>C Interface

I<sup>2</sup>C is a 2-wire serial interface. It consists of one master device and one or more slave devices. The master is defined as a micro controller providing the serial clock (SCL), and the slave as any integrated circuit receiving the SCL clock from the master. The SCA3060 sensor always operates as a slave device in master-slave operation mode. When using an SPI interface, a hardware addressing is used (slaves have dedicated CSB signals), the I<sup>2</sup>C interface uses a software based addressing (slave devices have dedicated bit patterns as addresses).

The SCA3060 is compatible to the Philips I<sup>2</sup>C specification V2.1. Main used features of the I<sup>2</sup>C interface are:

- 10-bit addressing, SCA3060 I<sup>2</sup>C device address is 0x1F1
- Supports standard mode and fast mode
- Start / Restart / Stop
- Slave transceiver mode
- Designed for low power consumption

In addition to the Philips specification, the SCA3060 I<sup>2</sup>C interface supports multiple write and read mode.

### 4.2.1 I<sup>2</sup>C frame format

#### 4.2.1.1 I<sup>2</sup>C write mode

In I<sup>2</sup>C write mode, the first 8 bits after device address define the SCA3060 internal register address to be written. If multiple data words are transferred by the master, the register address is decreased automatically by one (see cases 1 and 2 in Figure 9).

#### 4.2.1.2 I<sup>2</sup>C read mode

The read mode operates as described in Philips I<sup>2</sup>C specification. I<sup>2</sup>C read operation returns the content of the register which address is defined in I2C\_RD\_SEL register. So when performing the I<sup>2</sup>C read operation, the register address to be read has to be written into I2C\_RD\_SEL register before actual read operation. Read operation starts from register address that has been written earlier in I2C\_RD\_SEL register. Read data is acknowledged by I<sup>2</sup>C master. Automatic read address change depends on the selected start address (see cases 3 and 4 in Figure 9).

- If address is some of registers between X\_LSB → Z\_MSB the register address is automatically cycled as follows:  
... → Y\_MSB → Y\_LSB → X\_MSB → X\_LSB → Z\_MSB → Z\_LSB → Y\_MSB → Y\_LSB → ...
- If the start address is any other register, the read address is NOT automatically incremented or decremented (the data transfer continues from the same address.) This enables the burst read from output ring buffer (register BUF\_DATA).

#### 4.2.1.3 Decremental register read

Decremental reading is possible only for registers X\_LSB ... Z\_MSB. Refer to decremental read with SPI interface section 4.1.3.2.

## 4.2.2 Examples of I<sup>2</sup>C communication

Examples of I<sup>2</sup>C communication are presented below in Figure 9.

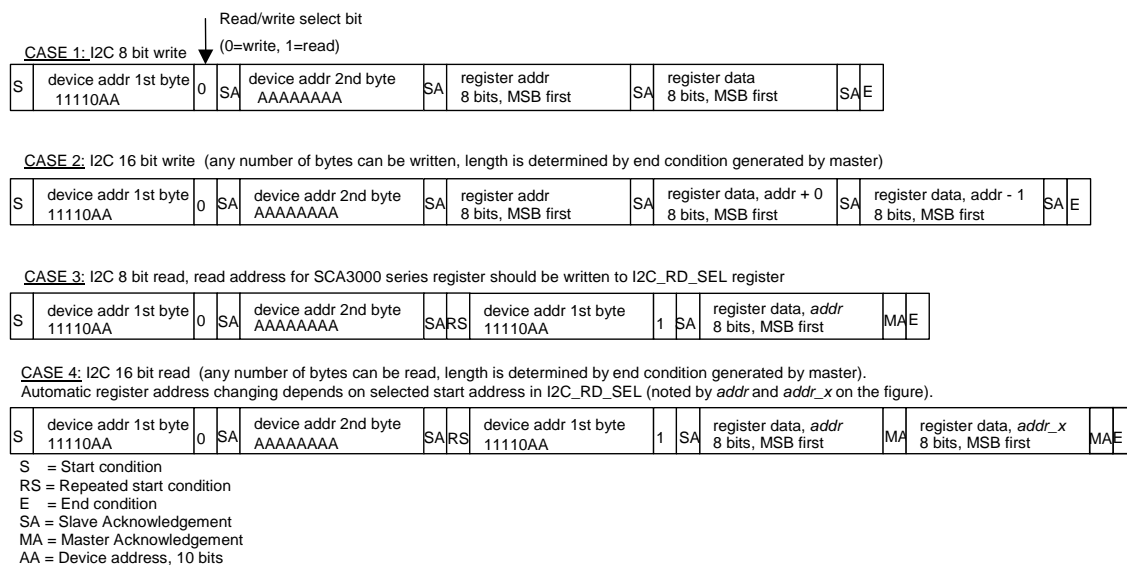


Figure 9. I<sup>2</sup>C frame format.

## 5 Electrical Characteristics

All voltages are reference to ground. Currents flowing into the circuit have positive values.

### 5.1 Absolute maximum ratings

The absolute maximum ratings of the SCA3060 are presented in Table 6 below.

Table 6. Absolute maximum ratings of the SCA3060

Parameter	Value	Unit
Supply voltage ( $V_{dd}$ )	-0.3 to +3.6	V
Voltage at input / output pins	-0.3 to ( $V_{dd} + 0.3$ )	V
ESD (Human body model)	$\pm 2$	kV
Storage temperature	-40 ... +125	°C
Operating temperature	-40 ... +105	°C
Mechanical shock *	> 10 000	g
Ultrasonic cleaning	Not allowed	

\* 1 m drop on concrete may cause >>10000 g shock.

ULTRASONIC AGITATION NOT ALLOWED.

### 5.2 Power Supply

Please refer to the corresponding product datasheet.

### 5.3 Digital I/O Specification

#### 5.3.1 Digital I/O DC characteristics

Table 7. DC characteristics of digital I/O pins.

No.	Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Input: CSB, MOSI, Xreset, SCK has no pull up / pull down							
1	Pull up current: CSB	$V_{IN} = 0 \text{ V}$	$I_{PU}$	10		50	$\mu\text{A}$
2	Pull down current: MOSI	$V_{IN} = V_{dd}$	$I_{PD}$	10		50	$\mu\text{A}$
3	Pull up current Xreset	$V_{IN} = 0 \text{ V}$	$I_{PU}$	3		10	$\mu\text{A}$
4	Input high voltage		$V_{IH}$	0.7* $V_{dd}$			V
5	Input low voltage		$V_{IL}$			0.3* $V_{dd}$	V
6	Hysteresis		$V_{HYST}$	0.1* $V_{dd}$			V
Output terminal: MISO, INT							
7	Output high voltage	$I > -4 \text{ mA}$	$V_{OH}$	0.8* $V_{dd}$		$V_{dd}$	V
8	Output low voltage	$I < 4 \text{ mA}$	$V_{OL}$	0		0.2* $V_{dd}$	V
9	Tristate leakage	$0 < V_{MISO} < 2.7 \text{ V}$	$I_{LEAK}$	-2		2	$\mu\text{A}$



### 5.3.2 SPI AC characteristics

The AC characteristics of the SCA3060 SPI interface are defined in Figure 10 and in Table 8.

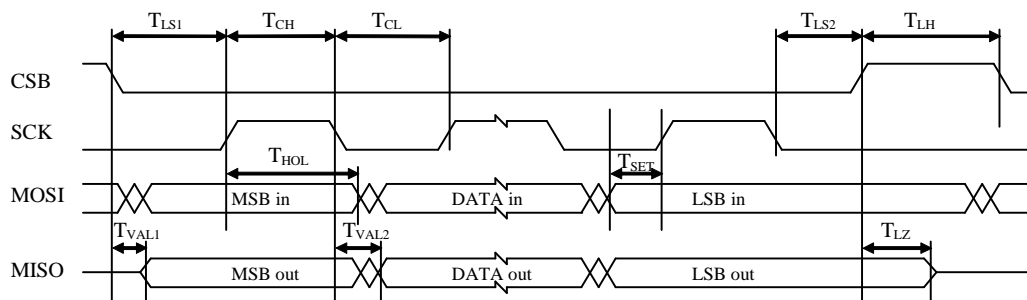


Figure 10. Timing diagram for SPI communication.

Table 8. AC characteristics of SPI communication.

	Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Terminal CSB, SCK							
1	Time from CSB (10%) to SCK (90%) <sup>1</sup>		$T_{LS1}$	$T_{per}/2$			ns
2	Time from SCK (10%) to CSB (90%) <sup>1</sup>		$T_{LS2}$	$T_{per}/2$			ns
Terminal SCK							
3	SCK low time	Load capacitance at MISO < 35 pF	$T_{CL}$	0.80* $T_{per}/2$	$T_{per}/2$		ns
4	SCK high time	Load capacitance at MISO < 35 pF	$T_{CH}$	0.80* $T_{per}/2$	$T_{per}/2$		ns
5	SCK Frequency		$f_{sck} = 1/T_{per}$			Product specific	MHz
Terminal MOSI, SCK							
6	Time from changing MOSI (10%, 90%) to SCK (90%) <sup>1</sup> . Data setup time		$T_{SET}$	$T_{per}/4$			ns
7	Time from SCK (90%) to changing MOSI (10%, 90%) <sup>1</sup> . Data hold time		$T_{HOL}$	$T_{per}/4$			ns
Terminal MISO, CSB							
8	Time from CSB (10%) to stable MISO (10%, 90%)	Load capacitance at MISO < 35 pF	$T_{VAL1}$			$T_{per}/4$	ns
9	Time from CSB (90%) to high impedance state of MISO <sup>1</sup> .	Load capacitance at MISO < 35 pF	$T_{LZ}$			$T_{per}/4$	ns
Terminal MISO, SCK							
10	Time from SCK (10%) to stable MISO (10%, 90%) <sup>1</sup> .	Load capacitance at MISO < 35 pF	$T_{VAL2}$			$1.3 \cdot T_{per}/4$	ns

Terminal MOSI, CSB				
11	Time between SPI cycles, CSB at high level (90%)	$T_{LH}$	$4 \cdot T_{per}$	ns

$T_{per}$  is SCK period

### 5.3.3 I<sup>2</sup>C AC characteristics

Please see Phillips Semiconductors, The I<sup>2</sup>C bus specification, Version 2.1, January 2000, pp. 31-33.

## 5.4 Recommended circuit diagram

Recommended circuit diagram for the SCA3060 with SPI interface is presented in Figure 11 below.

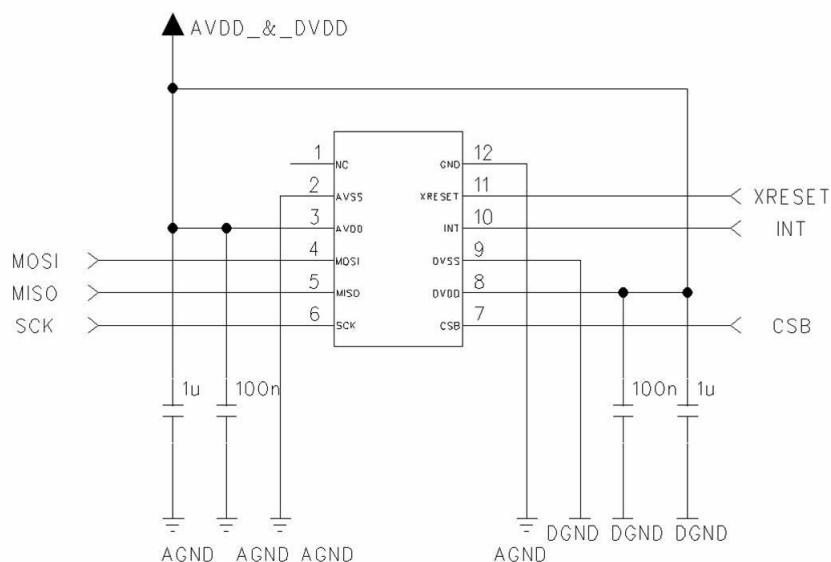


Figure 11. Recommended circuit diagram for the SCA3060 with SPI interface.

Recommended circuit diagram for the SCA3060 with I<sup>2</sup>C interface is presented in Figure 12 below.

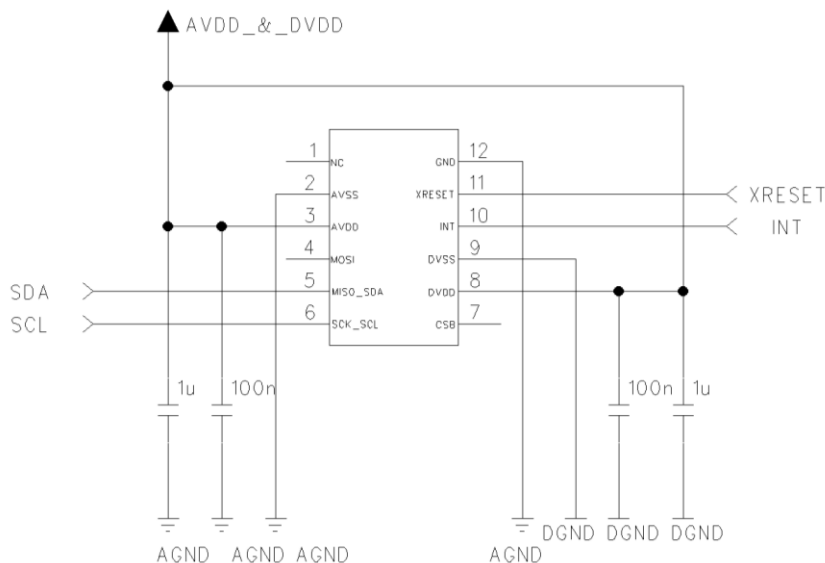


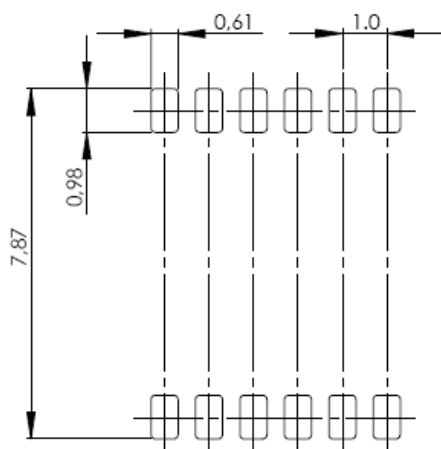
Figure 12. Recommended circuit diagram for the SCA3060 with I<sup>2</sup>C interface.

## 5.5 Recommended PWB layout

General PWB layout recommendations for SCA3060 products:

1. Locate 100 nF SMD capacitors right next to the SCA3060 package.
2. 1  $\mu$ F capacitors can be located near the node where AVDD and DVDD are routed on separate ways.
3. Use separate ground planes for AGND and DGND. Connect separate ground planes together on PWB.
4. Use double sided PWB, connect the bottom side plane to DGND.

Recommended PWB pad layout for SCA3060 is presented in figure below (dimensions in millimeters, [mm]).



Recommended PWB layout for the SCA3060 with SPI interface is presented in Figure 13 below (circuit diagram presented in Figure 11 above).

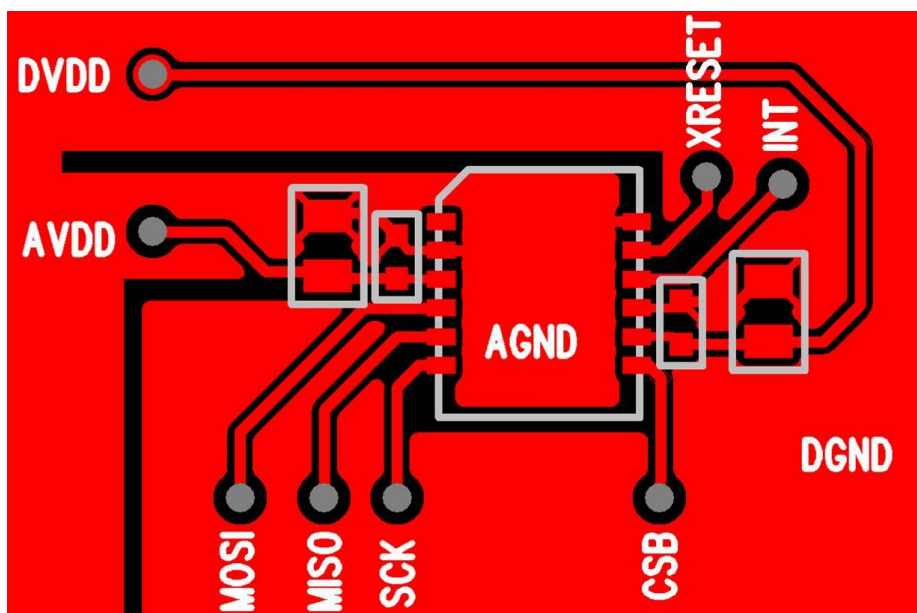


Figure 13. Recommended PWB layout for SCA3060 with SPI interface (not actual size, for reference only).

Recommended PWB layout for SCA3060 with I<sup>2</sup>C interface is presented in Figure 14 below (circuit diagram presented in Figure 12 above).

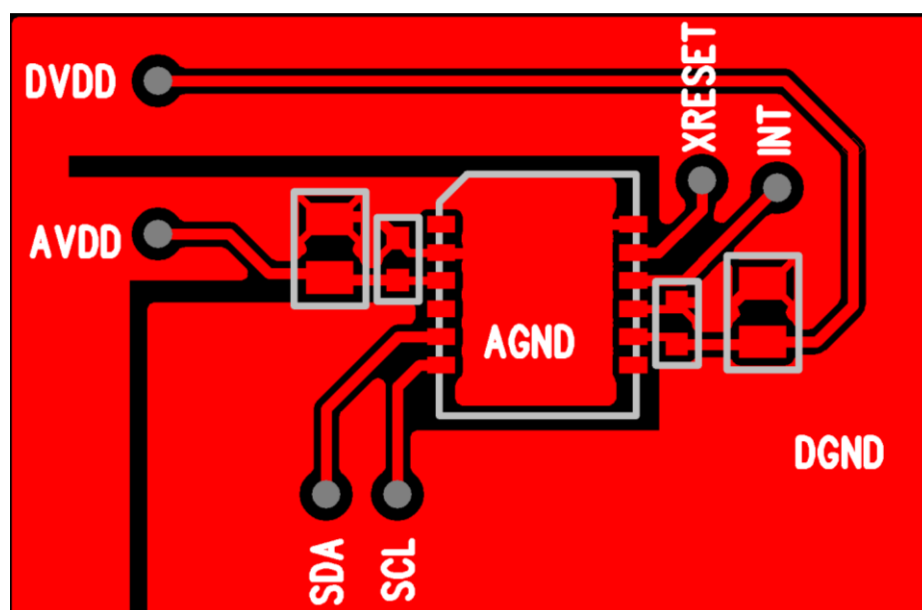


Figure 14. Recommended PWB layout for SCA3060 with I<sup>2</sup>C interface (not actual size, for reference only).

## 5.6 Assembly instructions

The Moisture Sensitivity Level (MSL) of the SCA3060 component is 3 according to the IPC/JEDEC J-STD-020C. Please refer to the document "TN53 Assembly Instructions for DFL Package" for more detailed information of SCA3060 assembly.

## 5.7 Tape and reel specifications

Please refer to the document "TN53 Assembly Instructions for DFL Package" for tape and reel specifications.

[illegible]

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