100 mA Ultra-low Supply Current (0.3 μA) LDO Regulator with Battery Monitor

No. EA-503-180806

OVERVIEW

The RP124x is an LDO regulator with a battery monitor (BM) featuring ultra-low supply current. The battery monitor has a function which divides the input voltage (V_{IN}) into 1/3 or 1/4. The battery charge remaining can be monitored by MCU. The buffering output enables directly inputting a signal into the low voltage A/D converter (ADC) with built-in MCU.

KEY BENEFITS

- Achieving Low Supply Current of 0.3 μA, Longer Battery Life and Downsizing
- Requiring Only Three External Capacitors and Suitable for Space-saving Mounting for the Smaller Packages

KEY SPECIFICATIONS

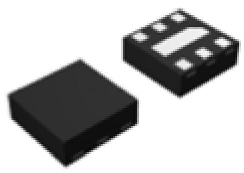
LDO Section

- Input Voltage Range: 1.7 V to 5.5 V
- Supply Current: Typ. 0.2 μA
- Output Voltage Accuracy: ±0.8%
- Output Current: 100 mA
- Ceramic Capacitor Compatible: 1.0 μF or more

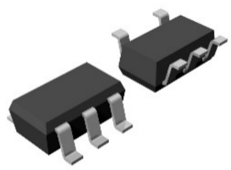
BM Section

- Output Voltage: V_{IN}/3 (RP124xxx3x)
  V_{IN}/4 (RP124xxx4x)
- Supply Current: Typ. 0.1 μA
- Ceramic Capacitor Compatible: 0.1 μF to 0.22 μF

PACKAGES

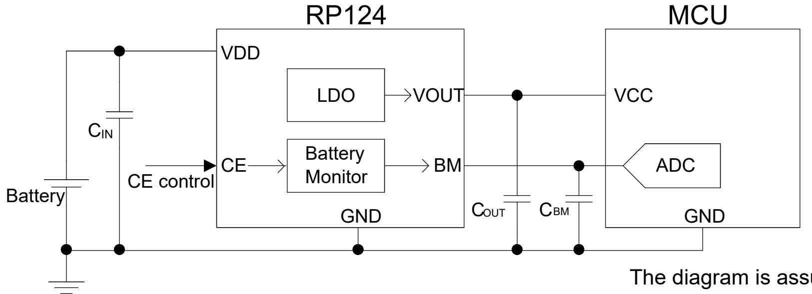


DFN1212-6
1.20 mm x 1.20 mm, t = 0.4 mm (1)



SOT-23-5
2.9 mm x 2.8 mm, t = 1.1 mm

TYPICAL APPLICATIONS



The diagram is assumed to be used for RP124xxxxE.

APPLICATIONS

- Battery powered IoT devices
- Energy harvesting devices
- Low power wireless communication modules including: *Bluetooth*® LE, Zigbee, and LPWA
- Low power consumption CPUs, memories, and sensors

(1) maximum dimension

SELECTION GUIDE

The LDO set output voltage, the divided ratio of BM output voltage, the CE pin function and the auto-discharge function are user-selectable options.

Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
RP124Lxx#∗-TR	DFN1212-6	5,000 pcs	Yes	Yes
RP124Nxx#∗-TR-FE	SOT-23-5	3,000 pcs	Yes	Yes

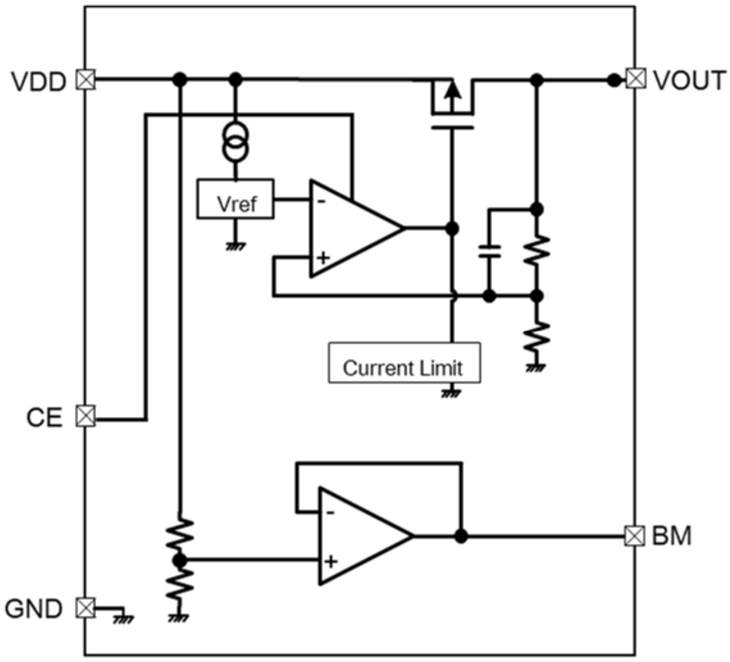
xx: Specify the LDO set output voltage (V_{SET}).
1.2 V (12) / 1.5 V (15) / 1.8 V (18) / 2.1 V (21)† / 2.4 V (24) / 2.5 V (25) / 2.7 V (27) / 2.8 V (28) / 3.0 V (30) /3.1 V (31) / 3.3 V (33) / 3.6 V (36)
† Note: 2.1V (21) is selectable for only RP124x21xE.

#: Specify the divided ratio of BM output voltage.
3: V_{IN}/3
4: V_{IN}/4

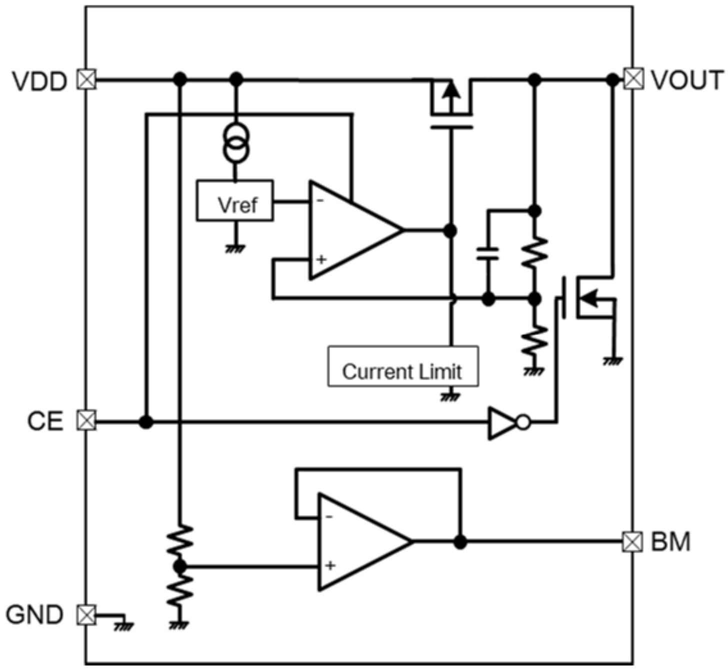
∗: Specify the CE pin and the auto-discharge option.

∗	CE pin	Auto-discharge	
B	Controlling LDO with the CE pin (Active-high)	LDO	No
		BM	No
D	Controlling LDO with the CE pin (Active-high)	LDO	Yes
		BM	No
E	Controlling BM with the CE pin (Active-high)	LDO	No
		BM	Yes

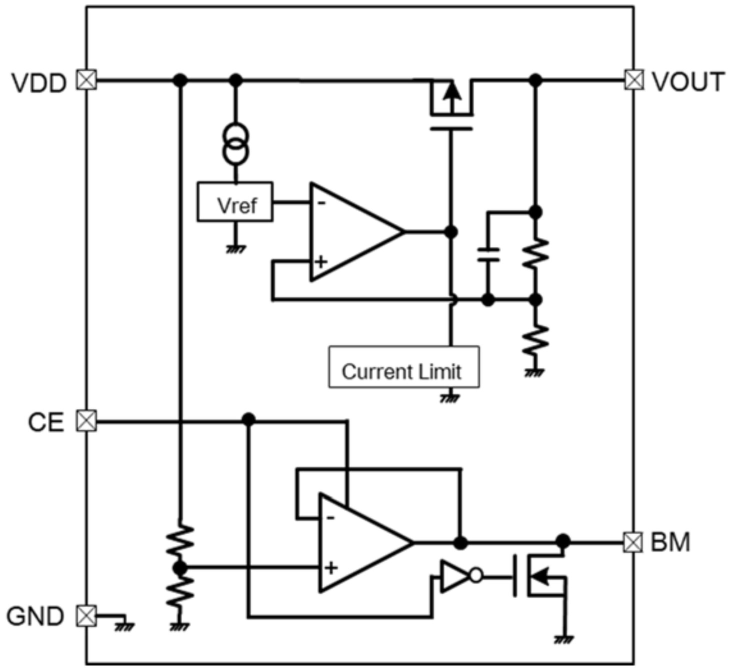
BLOCK DIAGRAMS



RP124xxxxB Block Diagram

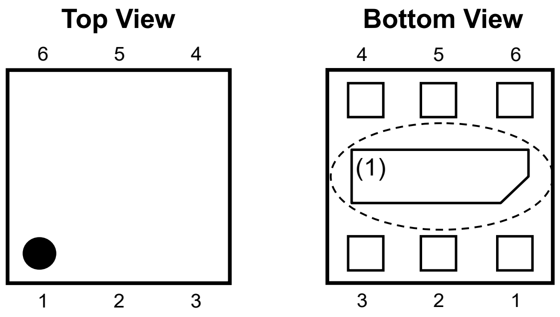


RP124xxxxD Block Diagram

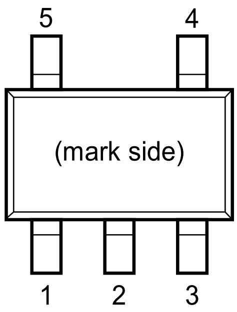


RP124xxxxE Block Diagram

PIN DESCRIPTIONS



DFN1212-6 Pin Configuration



SOT-23-5 Pin Configuration

DFN1212-6 Pin Description

Pin No.	Symbol	Description
1	VOUT	Output Pin
2	GND	Ground Pin
3	BM	Battery Monitoring Output Pin
4	CE	Chip Enable Pin, Active-high
5	NC	No Connection
6	VDD	Input Pin

SOT-23-5 Pin Description

Pin No.	Symbol	Description
1	VDD	Input Pin
2	GND	Ground Pin
3	CE	Chip Enable Pin, Active-high
4	BM	Battery Monitoring Output Pin
5	VOUT	Output Pin

(1) The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

Symbol	Item		Rating	Unit
V_{IN}	Input Voltage		−0.3 to 6.5	V
V_{CE}	CE Pin Voltage		−0.3 to 6.5	V
V_{OUT}	VOUT Pin Voltage		−0.3 to V_{IN} + 0.3	V
V_{BM}	BM Pin Voltage		−0.3 to V_{IN} + 0.3	V
I_{OUT}	Output Current		130	mA
P_D	Power Dissipation[(1)]	DFN1212-6 (JEDEC STD. 51-7 Test Land Pattern)	850	mW
		SOT-23-5 (JEDEC STD. 51-7 Test Land Pattern)	660	mW
Tj	Junction Temperature Range		−40 to 125	°C
Tstg	Storage Temperature Range		−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS
Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Item		Rating	Unit
V_{IN}	Input Voltage	RP124xxx3x	1.7 to 5.5	V
		RP124xxx4x	2.4 to 5.5	
Ta	Operating Temperature		−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS
All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

(1) Refer to *POWEWR DISSIPATION* for detailed information.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{SET} + 1.0 V, I_{OUT} = 1.5 mA, C_{IN} = C_{OUT} = 1.0 µF, unless otherwise noted.

The specifications surrounded by [ ] are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

RP124x Electrical Characteristics: LDO Section (Ta = 25°C)

Symbol	Parameters	Test Conditions/Comments	Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	V_{SET} > 2.0 V	x0.992		x1.008	V
			[x0.987]		[x1.013]	
		V_{SET} ≤ 2.0 V	−16		16	mV
			[−26]		[26]	
I_{OUT}	Output Current		[100]			mA
ΔV_{OUT}	Output Voltage Deviation When Switching Mode	1 µA ≤ I_{OUT} ≤ I_{OUTH}, V_{SET} > 2.0 V	[−1]		[1]	%
		1 µA ≤ I_{OUT} ≤ I_{OUTH}, V_{SET} ≤ 2.0 V	[−20]		[20]	mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	1.5 mA ≤ I_{OUT} ≤ 100 mA	[−40]	2	[40]	mV
V_{DIF}	Dropout Voltage	I_{OUT} = 100 mA	Refer to *Product-specific Electrical Characteristics*			
I_{SS}	Supply Current	V_{CE} = V_{IN}, I_{OUT} = 0 mA		0.2	0.42	µA
					[0.5]	µA
I_{OUTH}	Fast Mode Switching Current	I_{OUT} = From Light Load to Heavy Load, V_{IN} = 5.0 V		0.5		mA
I_{OUTL}	Low Power Mode Switching Current	I_{OUT} = From Heavy Load to Light Load, V_{IN} = 5.0 V	[0.08]			mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{SET} + 0.5 V ≤ V_{IN} ≤ 5.5 V		0.02	[0.2]	%/V
I_{SC}	Short Current Limit	V_{OUT} = 0 V		65		mA
V_{CEH}	CE Pin Input Voltage, high	RP124xxxxB/D	[1.0]			V
V_{CEL}	CE Pin Input Voltage, low	RP124xxxxB/D			[0.4]	V
R_{DISN}	Auto-discharge NMOS On-resistance	V_{IN} = 4.0 V, V_{CE} = 0 V, RP124xxxxD		50		Ω

All test items listed under Electrical Characteristics are done under the pulse load condition Tj ≈ Ta = 25°C.

ELECTRICAL CHARACTERISTICS (continued)

The specifications surrounded by [ ] are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

RP124x Product-specific Electrical Characteristics: LDO Section

Product Name	V_{OUT} [V]						V_{DIF} [V]	
	Ta = 25°C			−40°C ≤ Ta ≤ 85°C				
	Min.	Typ.	Max.	Min.	Typ.	Max.	Typ.	Max.
RP124x12xx	1.184	1.200	1.216	1.174	1.200	1.226	0.640	0.975
RP124x15xx	1.484	1.500	1.516	1.474	1.500	1.526	0.410	0.660
RP124x18xx	1.784	1.800	1.816	1.774	1.800	1.826	0.230	0.380
RP124x21xE	2.084	2.100	2.116	2.073	2.100	2.127	0.150	0.285
RP124x24xx	2.381	2.400	2.419	2.369	2.400	2.431	0.130	0.230
RP124x25xx	2.480	2.500	2.520	2.468	2.500	2.532	0.110	0.180
RP124x27xx	2.679	2.700	2.721	2.665	2.700	2.735		
RP124x28xx	2.778	2.800	2.822	2.764	2.800	2.836	0.100	0.160
RP124x30xx	2.976	3.000	3.024	2.961	3.000	3.039		
RP124x31xx	3.076	3.100	3.124	3.060	3.100	3.140		
RP124x33xx	3.274	3.300	3.326	3.258	3.300	3.342	0.090	0.145
RP124x36xx	3.572	3.600	3.628	3.554	3.600	3.646		

ELECTRICAL CHARACTERISTICS (continued)

C_{IN} = 1.0 μF, C_{BM} = 0.22 μF, unless otherwise noted.

The specifications surrounded by [ ] are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

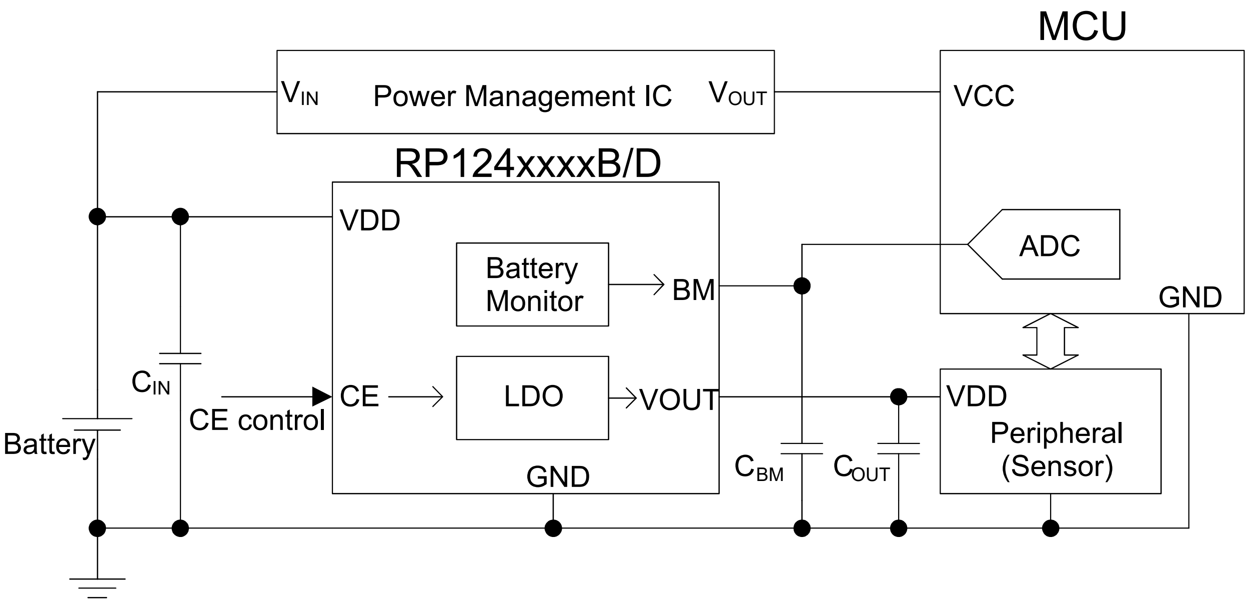
RP124x Electrical Characteristics: Battery Monitor Section (Ta = 25°C)

Symbol	Parameters	Test Conditions/Comments		Min.	Typ.	Max.	Unit
V_{BM}	Output Voltage	−10 μA ≤ I_{BM} ≤ 10 μA	1.7 V ≤ V_{IN} ≤ 5.5 V, RP124xxx3x	V_{IN}/3−20	V_{IN}/3	V_{IN}/3+20	mV
				[V_{IN}/3−25]	V_{IN}/3	[V_{IN}/3+25]	
			2.4 V ≤ V_{IN} ≤ 5.5 V, RP124xxx4x	V_{IN}/4−20	V_{IN}/4	V_{IN}/4+20	
				[V_{IN}/4−25]	V_{IN}/4	[V_{IN}/4+25]	
I_{BM}	Output Current	1.7 V ≤ V_{IN} ≤ 5.5 V, RP124xxx3x		[−10]		[10]	μA
		2.4 V ≤ V_{IN} ≤ 5.5 V, RP124xxx4x					
I_{SSBM}	Supply Current	V_{IN} = V_{CE} = 3.6 V , I_{BM} = 0 μA			0.1	0.2	μA
V_{CEHBM}	CE Pin Input Voltage, high	1.7 V ≤ V_{IN} ≤ 5.5 V, RP124xxx3E		[1.0]			V
		2.4 V ≤ V_{IN} ≤ 5.5 V, RP124xxx4E					
V_{CELBM}	CE Pin Input Voltage, low	1.7 V ≤ V_{IN} ≤ 5.5 V, RP124xxx3E				[0.4]	V
		2.4 V ≤ V_{IN} ≤ 5.5 V, RP124xxx4E					
R_{DISNBM}	Auto-discharge NMOS On-resistance	V_{IN} = 4.0 V, V_{CE} = 0 V, RP124xxxxE			50		Ω

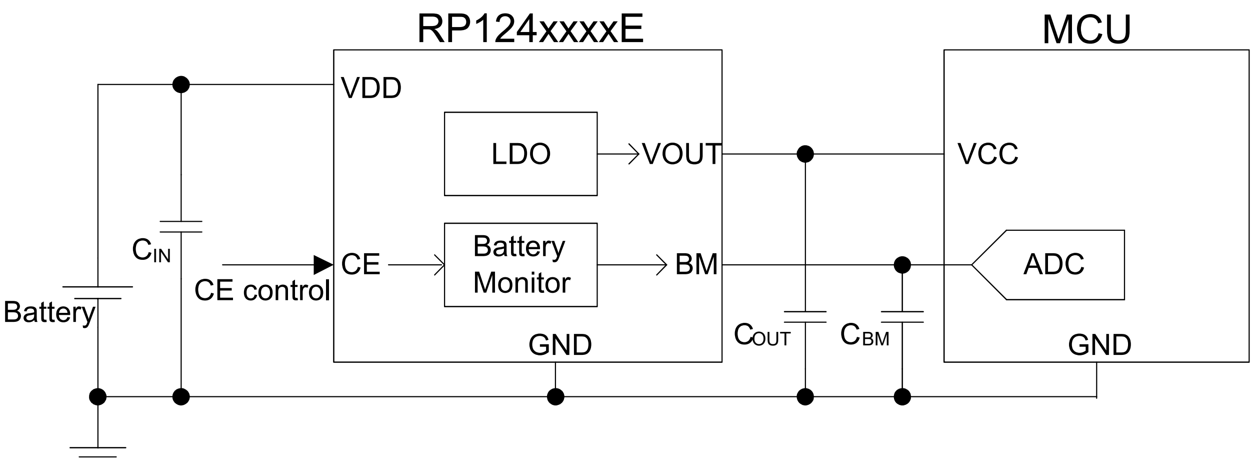
All test items listed under Electrical Characteristics are done under the pulse load condition Tj ≈ Ta = 25°C.

APPLICATION INFORMATION

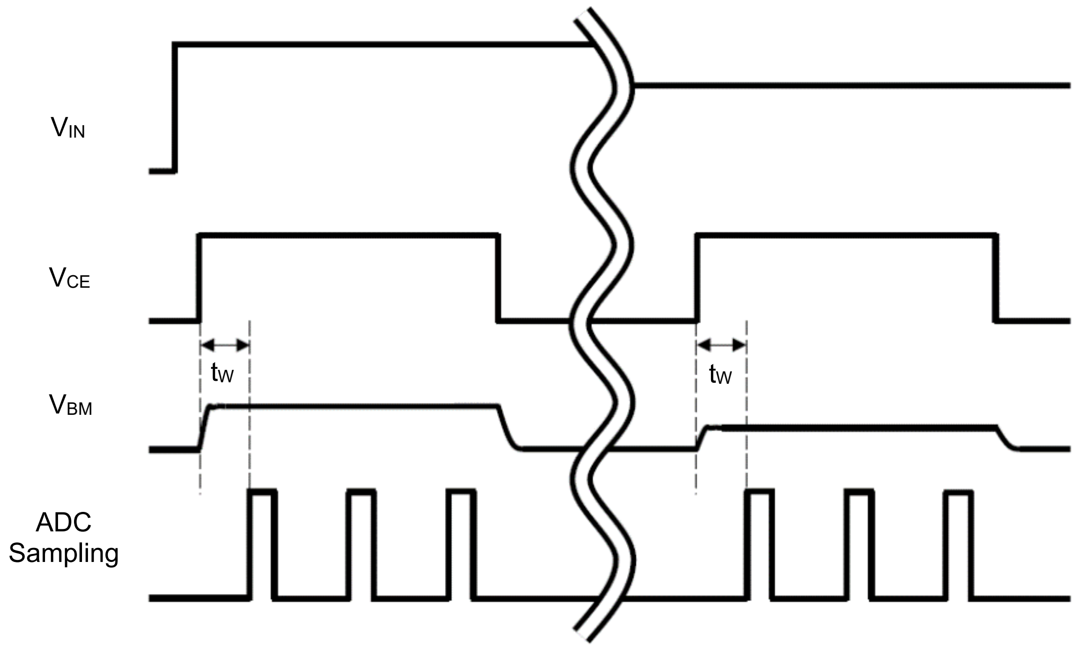
TYPICAL APPLICATION



RP124xxxxB/D Typical Application Circuit



RP124xxxxE Typical Application Circuit



Timing Chart Example of RP124xxxxE Circuit

The above diagram shows the example of using the RP124xxxxE typical application circuit and its timing chart. Connecting BM pin and ADC input pin of MCU enables monitoring the battery voltage. Controlling the start-up and stop of Battery Monitor with CE pin by the timing based on the ADC sampling reduces power consumption of the entire system. When monitoring the battery voltage, set the waiting time (t_W) in order to stabilize waveform after the CE input voltage is set to “H”. It is recommended to set $t_W \geq 10$ ms for this product.

Notes on External Components

- Phase compensation is provided to secure stable operation even when the load current is varied. For this purpose, use a 1.0-μF or more output capacitor (C_{OUT}) between the VOUT and GND pins, and a 0.1-μF to 0.22-μF capacitor (C_{BM}) between the BM and GND pins with shortest-distance wiring. In case of using a tantalum type capacitor with a large ESR (Equivalent Series Resistance), the output might become unstable. Evaluate your circuit including consideration of frequency characteristics.
- Connect a 1.0-μF or more input capacitor (C_{IN}) between the VDD and GND pins with shortest-distance wiring.

TECHNICAL NOTES

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. A peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, please be fully aware of the following points.

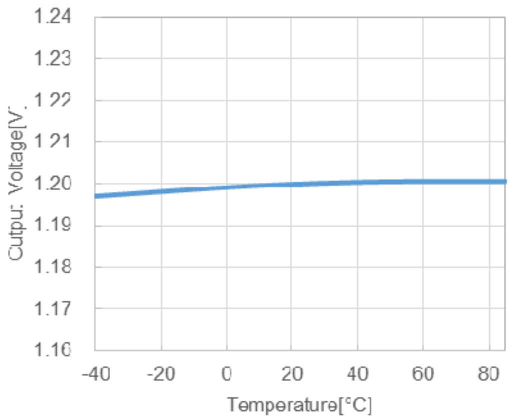
- The high impedance of the wirings may result in noise pickup and unstable operation of the device. Reduce the impedance of the VDD and GND wirings.
- When an intermediate voltage other than V_{IN} or GND is input to the CE pin, a supply current may be increased with a through current of a logic circuit in the IC. The CE pin is neither pulled up nor pulled down, therefore an operation is not stable at open.

TYPICAL CHARACTERISTICS

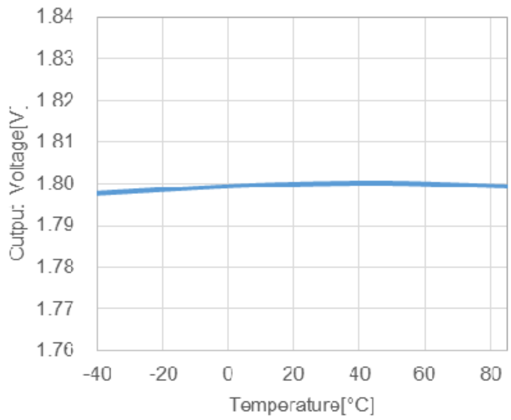
Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) LDO Output Voltage vs. Temperature (C_{IN} = Ceramic 1.0 μF, C_{OUT} = Ceramic 1.0 μF)

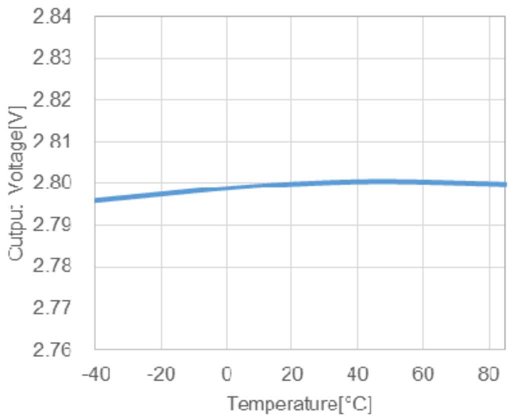
RP124x12xx, V_{IN} = 2.2 V, I_{OUT} = 1.5 mA



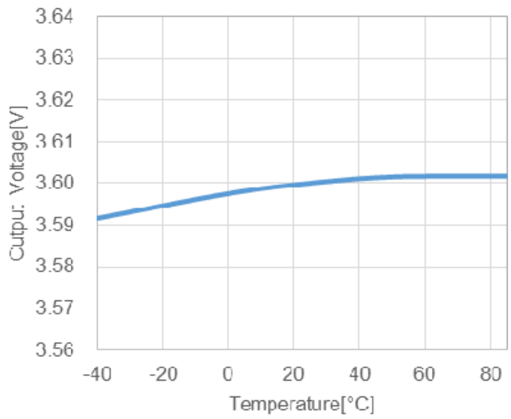
RP124x18xx, V_{IN} = 2.8 V, I_{OUT} = 1.5 mA



RP124x28xx, V_{IN} = 3.8 V, I_{OUT} = 1.5 mA

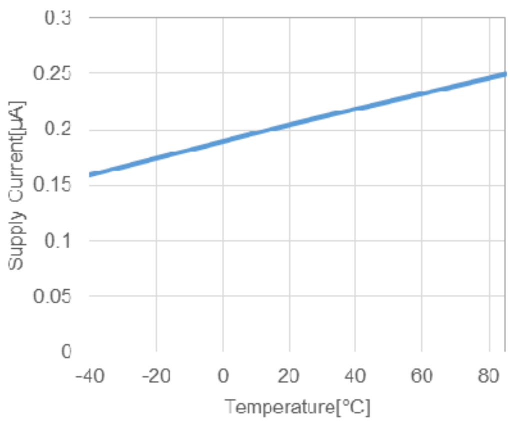


RP124x36xx, V_{IN} = 4.6 V, I_{OUT} = 1.5 mA

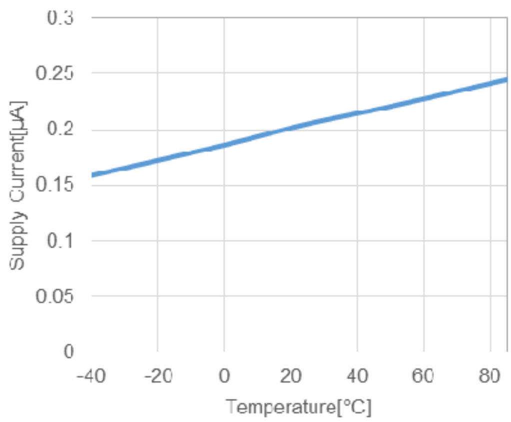


2) LDO Supply Current vs. Temperature (C_{IN} = Ceramic 1.0 μF, C_{OUT} = Ceramic 1.0 μF)

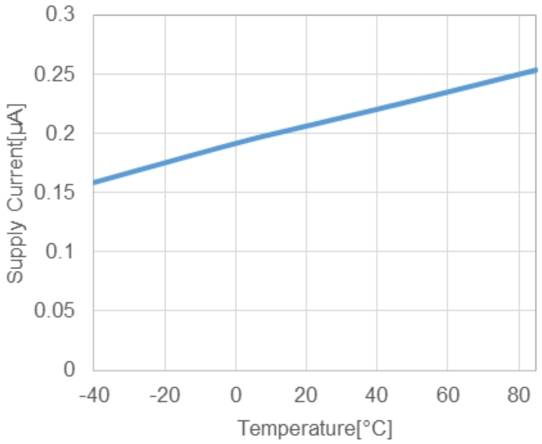
RP124x12xx, V_{IN} = 2.2 V



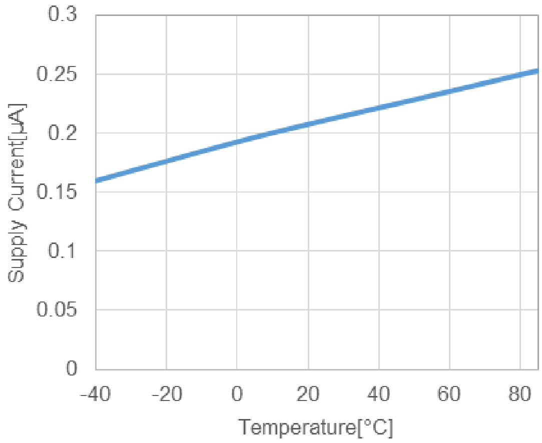
RP124x18xx, V_{IN} = 2.8 V



RP124x28xx, V_{IN} = 3.8 V

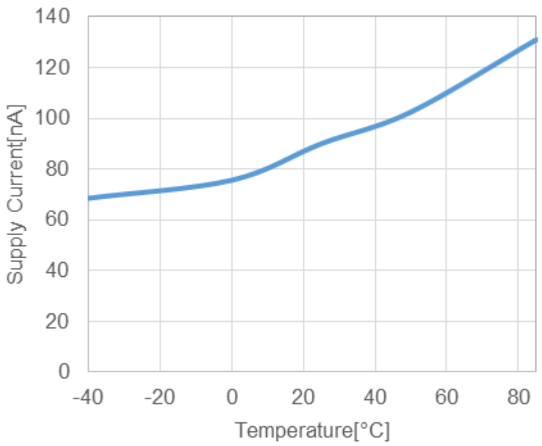


RP124x36xx, V_{IN} = 4.6 V

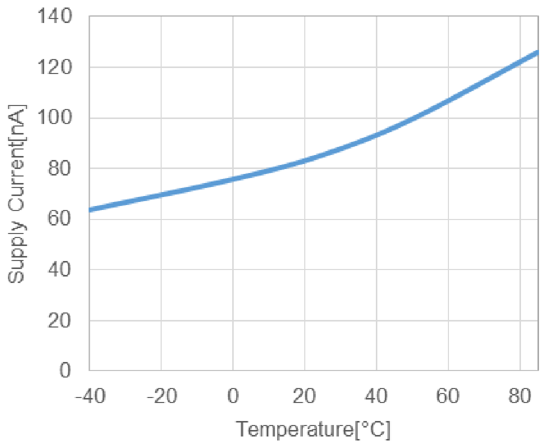


3) BM Supply Current vs. Temperature (C_{IN} = Ceramic 1.0 µF, C_{BM} = Ceramic 0.1 µF)

RP124xxx3x, V_{IN} = 3.6 V

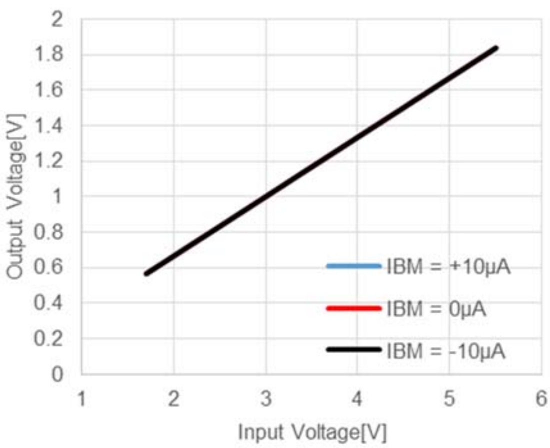


RP124xxx4x, V_{IN} = 3.6 V

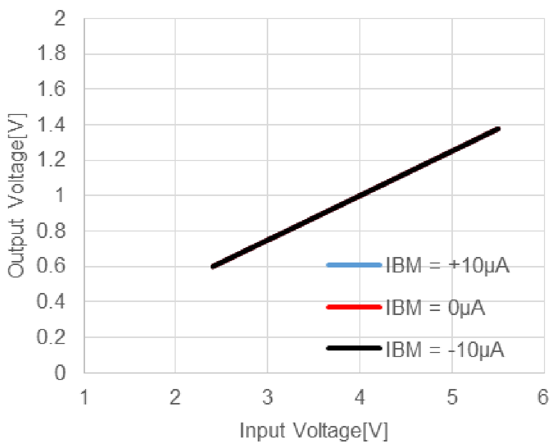


4) BM Output Voltage vs. Input Voltage (C_{IN} = Ceramic 1.0 µF, C_{BM} = Ceramic 0.1 µF, Ta = 25°C)

RP124xxx3x

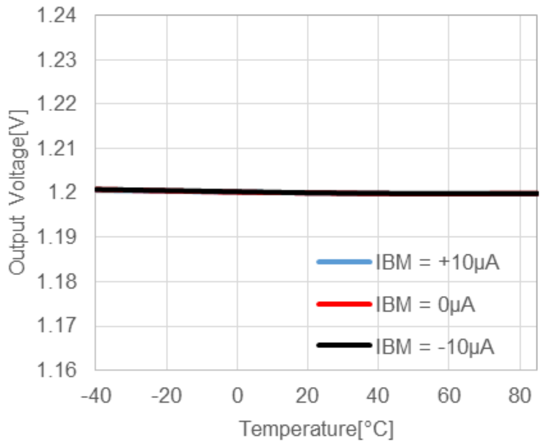


RP124xxx4x

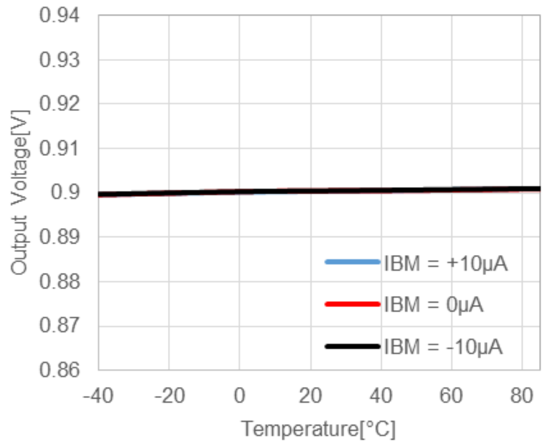


5) BM Output Voltage vs. Temperature (C_{IN} = Ceramic 1.0 µF, C_{BM} = Ceramic 0.1 µF)

RP124xxx3x, V_{IN} = 3.6 V

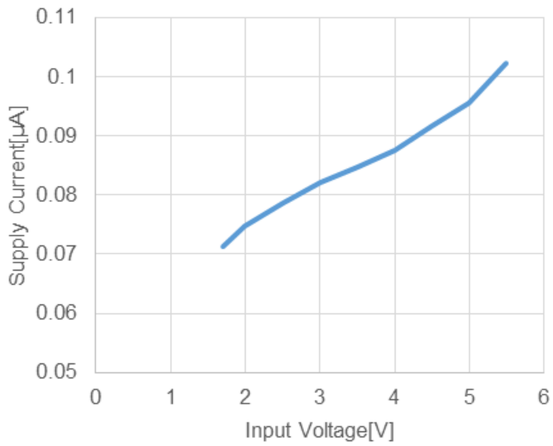


RP124xxx4x, V_{IN} = 3.6 V

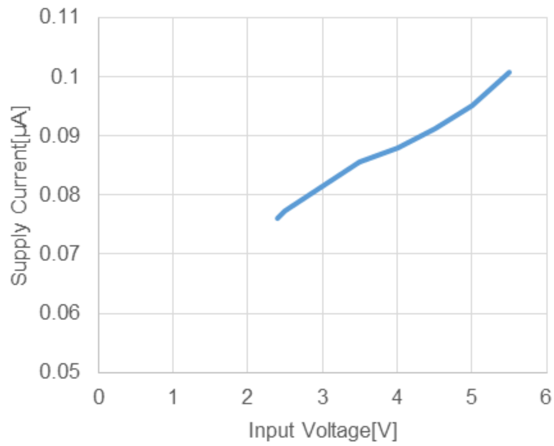


6) BM Supply Current vs. Input Voltage (C_{IN} = Ceramic 1.0 µF, C_{BM} = Ceramic 0.1 µF, Ta = 25°C)

RP124xxx3x

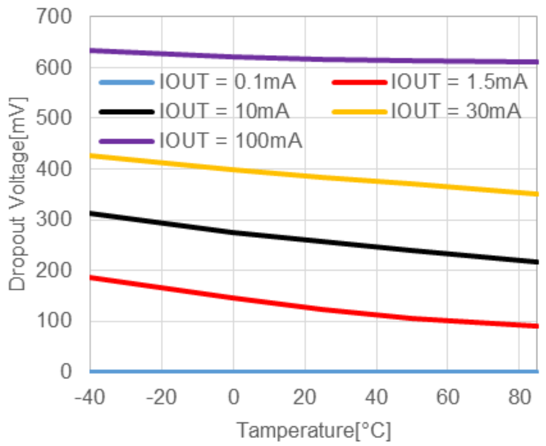


RP124xxx4x

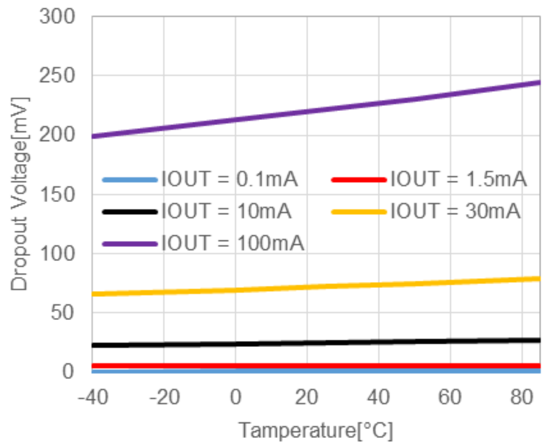


7) LDO Dropout Voltage vs. Temperature (C_{IN} = Ceramic 1.0 µF, C_{OUT} = Ceramic 1.0 µF)

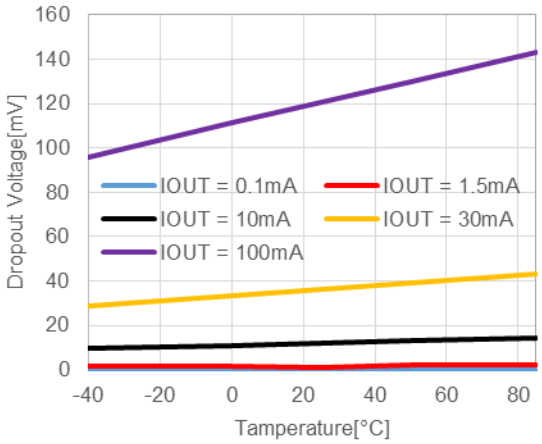
RP124x12xx



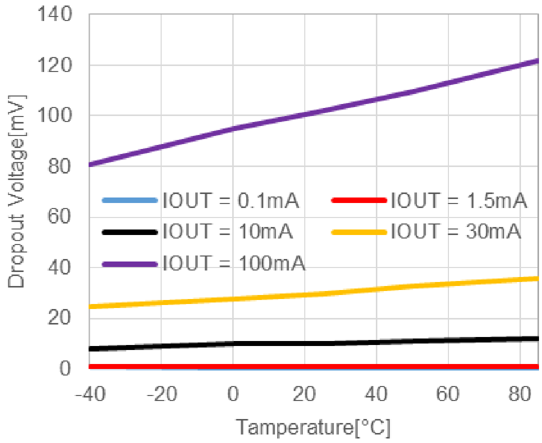
RP124x18xx



RP124x28xx

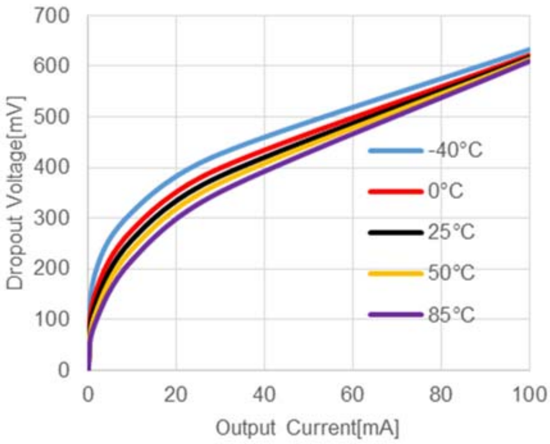


RP124x36xx

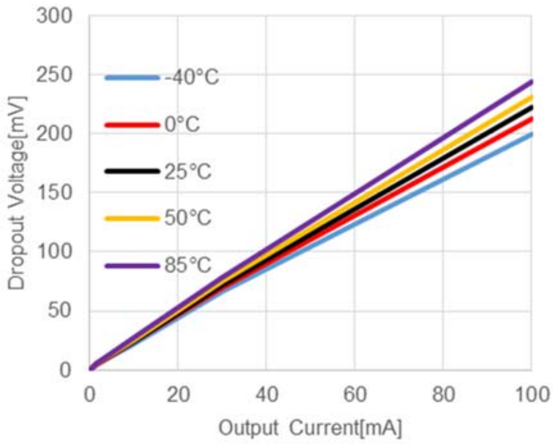


8) LDO Dropout Voltage vs. Output Current (C_{IN} = Ceramic 1.0 µF, C_{OUT} = Ceramic 1.0 µF)

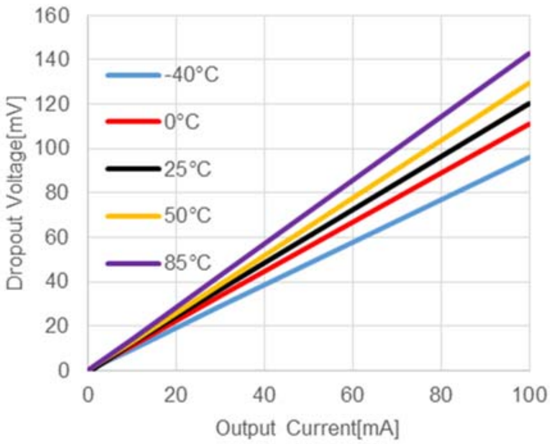
RP124x12xx



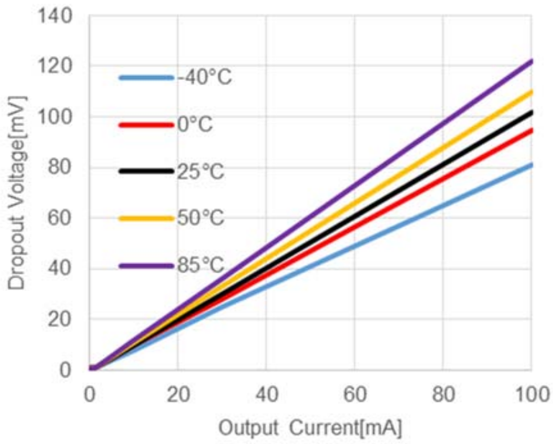
RP124x18xx



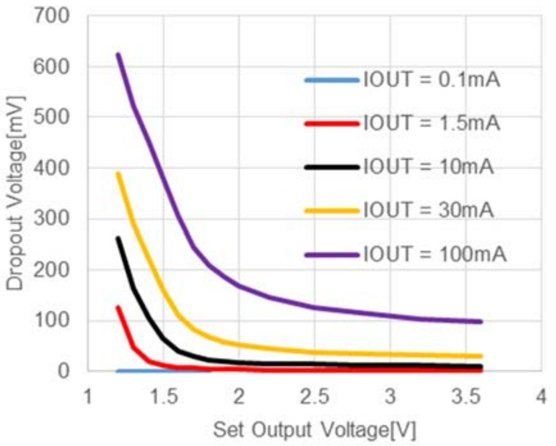
RP124x28xx



RP124x36xx

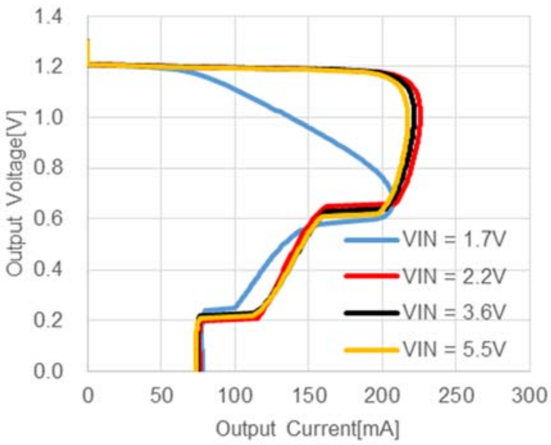


9) LDO Dropout Voltage vs. Set Output Voltage (C_{IN} = Ceramic 1.0 µF, C_{OUT} = Ceramic 1.0 µF, Ta = 25°C)

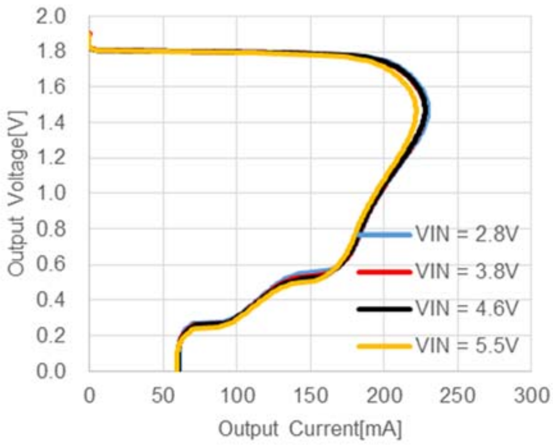


10) LDO Output Voltage vs. Output Current (C_{IN} = Ceramic 1.0 µF, C_{OUT} = Ceramic 1.0 µF, Ta = 25°C)

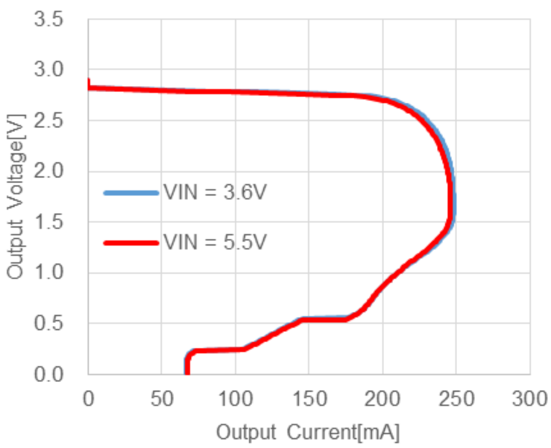
RP124x12xx



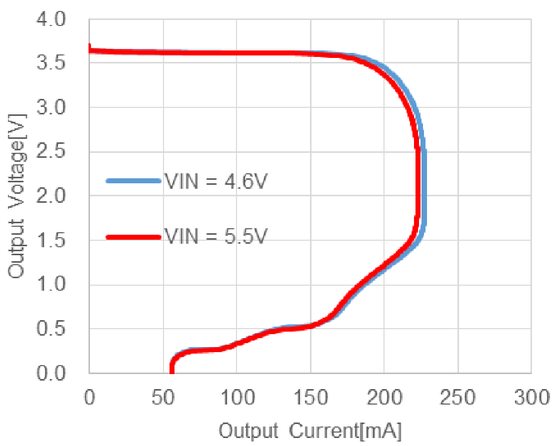
RP124x18xx



RP124x28xx

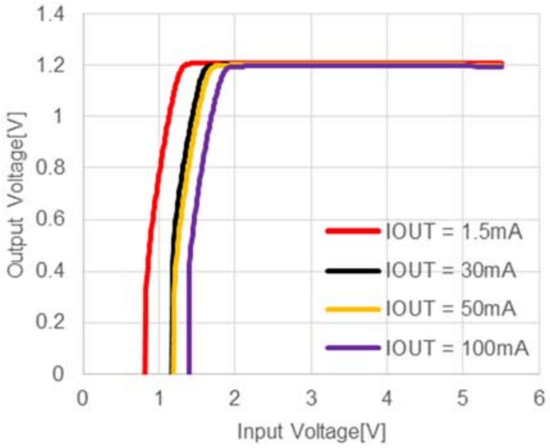


RP124x36xx

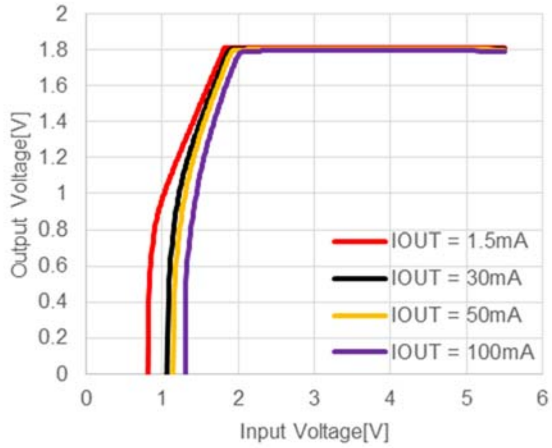


11) LDO Output Voltage vs. Input Voltage (C_{IN} = Ceramic 1.0 μF, C_{OUT} = Ceramic 1.0 μF, Ta = 25°C)

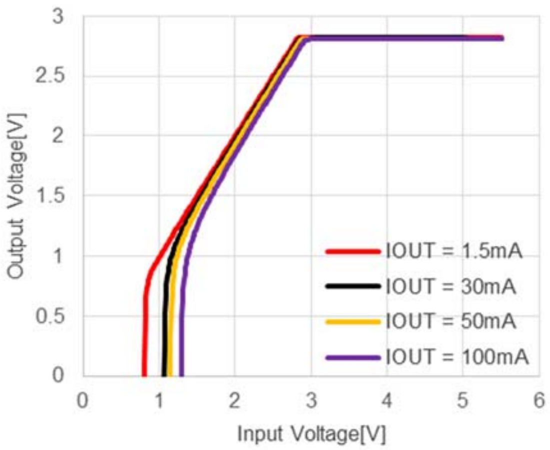
RP124x12xx



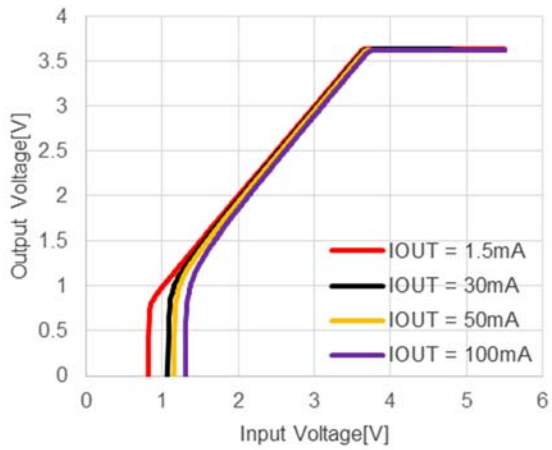
RP124x18xx



RP124x28xx

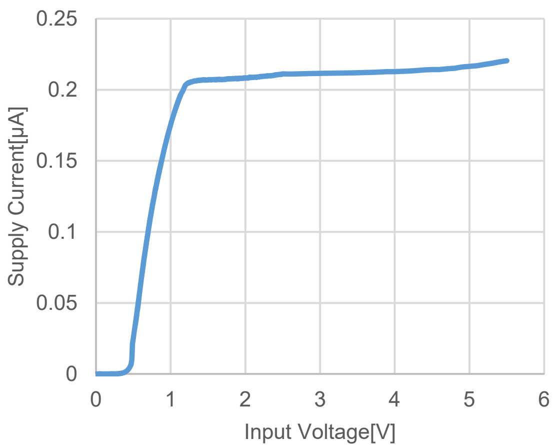


RP124x36xx

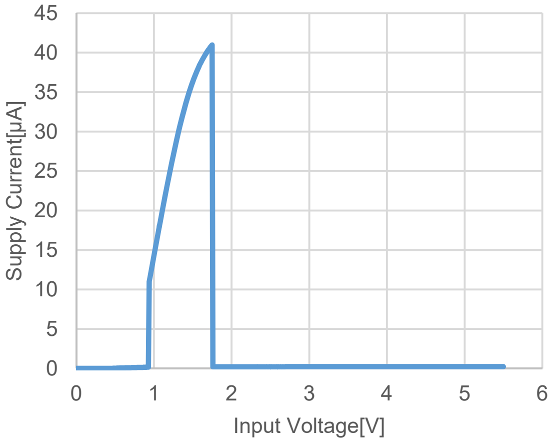


12) LDO Supply Current vs. Input Voltage (C_{IN} = Ceramic 1.0 μF, C_{OUT} = Ceramic 1.0 μF, Ta = 25°C)

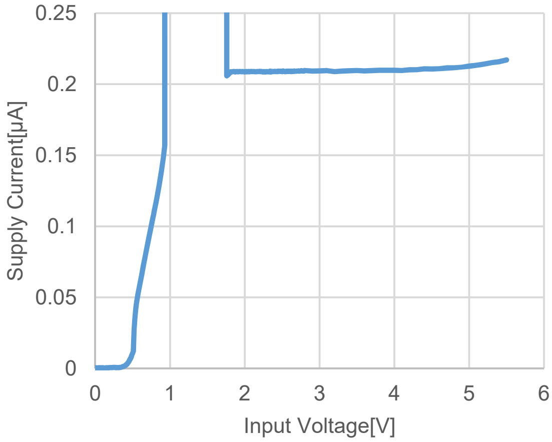
RP124x12xx



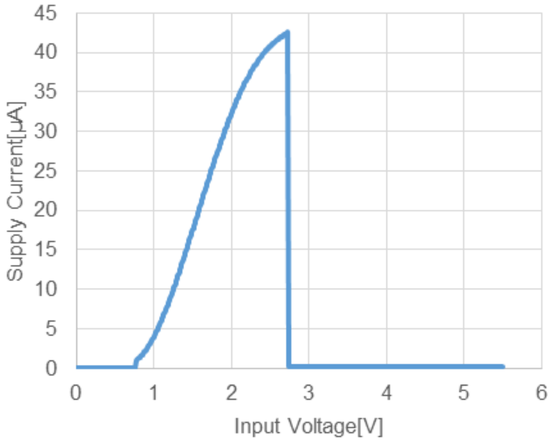
RP124x18xx (10μA/div)



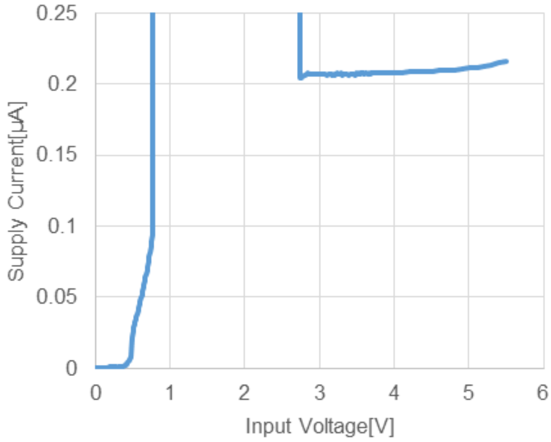
RP124x18xx (0.05μA/div)



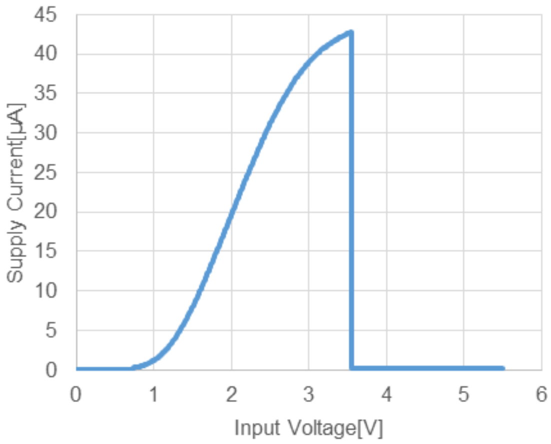
RP124x28xx (10μA/div)



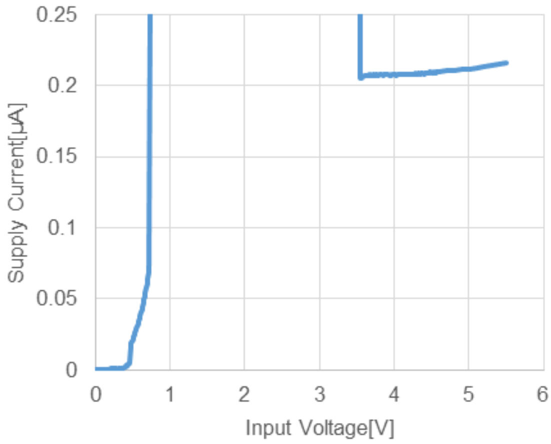
RP124x28xx (0.05μA/div)



RP124x36xx (10μA/div)

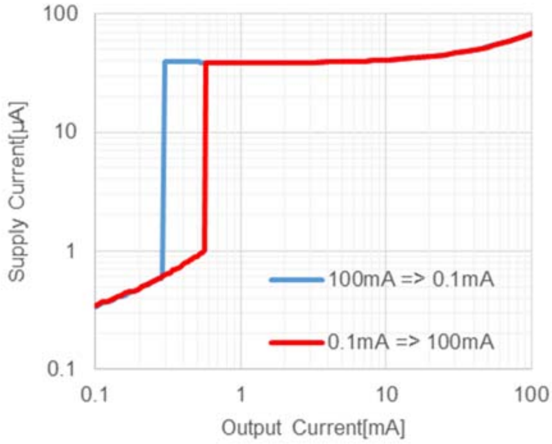


RP124x36xx (0.05μA/div)

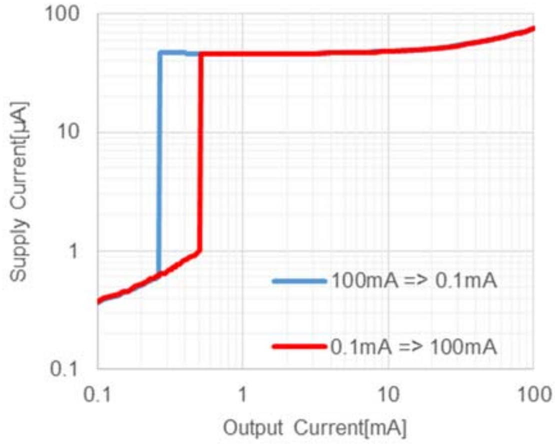


13) LDO Supply Current vs. Output Current (C_{IN} = Ceramic 1.0 µF, C_{OUT} = Ceramic 1.0 µF, Ta = 25°C)

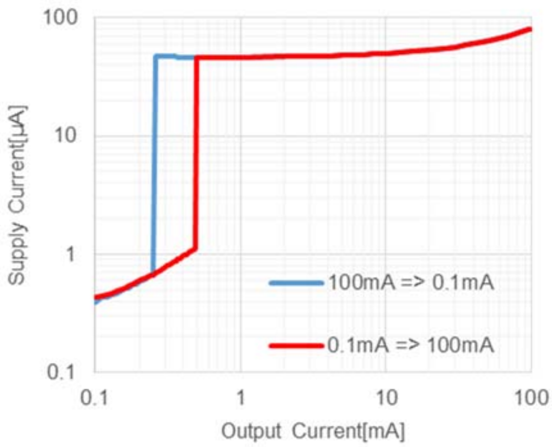
RP124x12xx



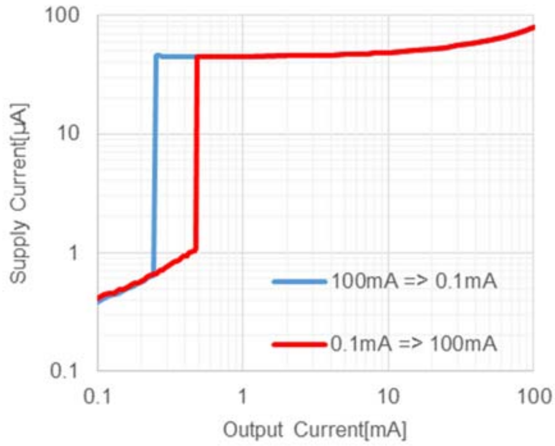
RP124x18xx



RP124x28xx

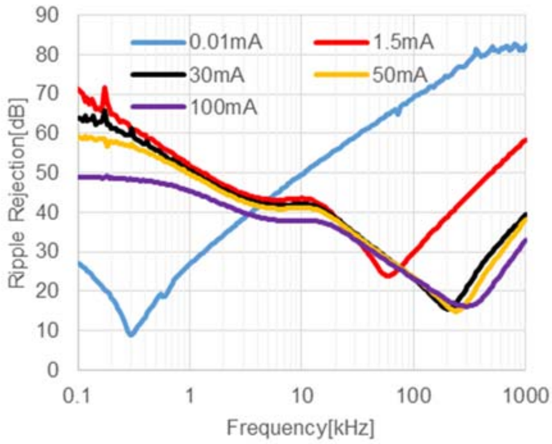


RP124x36xx

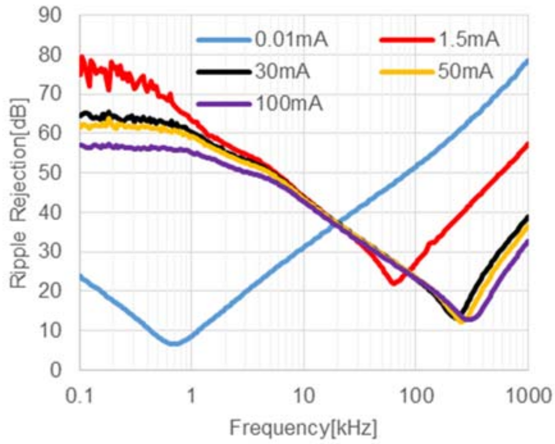


14) Ripple Rejection vs. Frequency (C_{IN} = none, C_{OUT} = Ceramic 1.0 µF, Ta = 25°C)

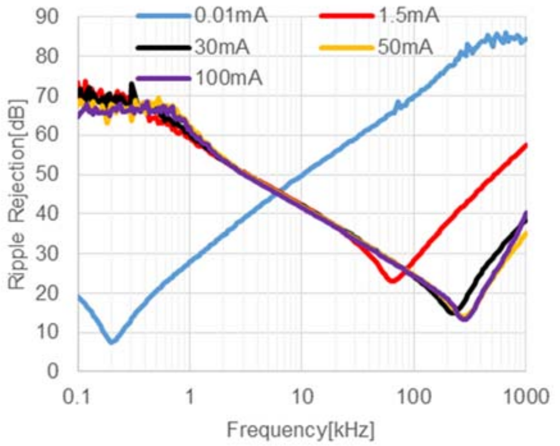
RP124x12xx, V_{IN} = 2.2 V



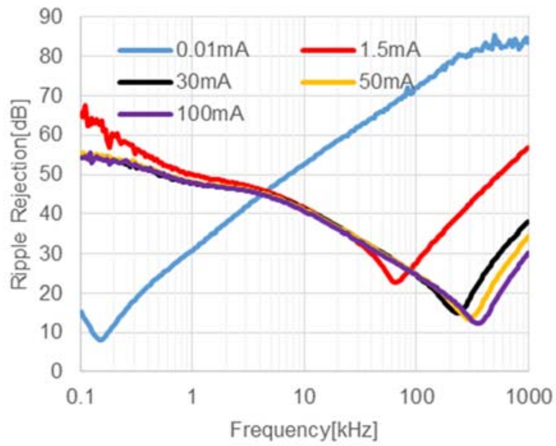
RP124x18xx, V_{IN} = 2.8 V



RP124x28xx, V_{IN} = 3.8V

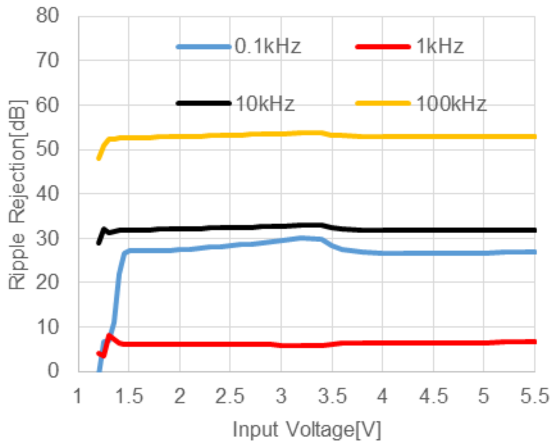


RP124x36xx, V_{IN} = 4.6V

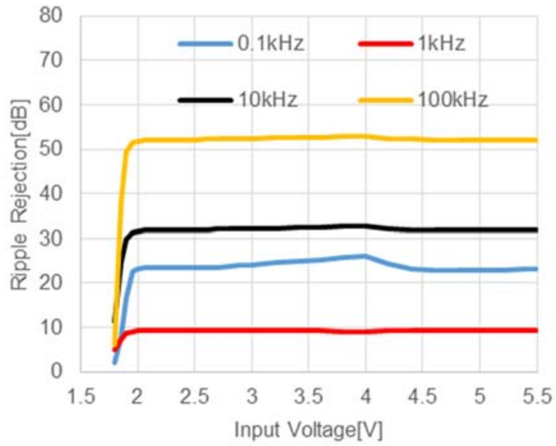


15) Ripple Rejection vs. Input Voltage (C_{IN} = none, C_{OUT} = Ceramic 1.0 μF, Ta = 25°C)

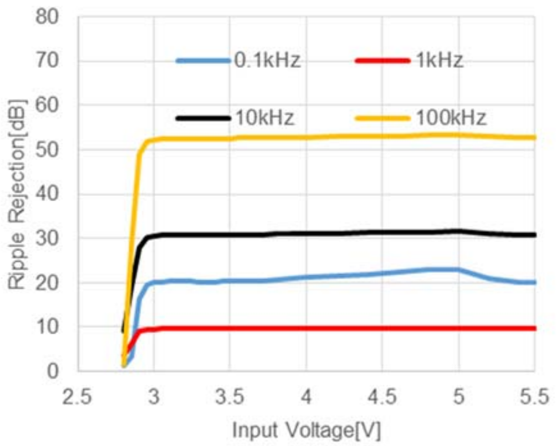
RP124x12xx, I_{OUT} = 100 μA



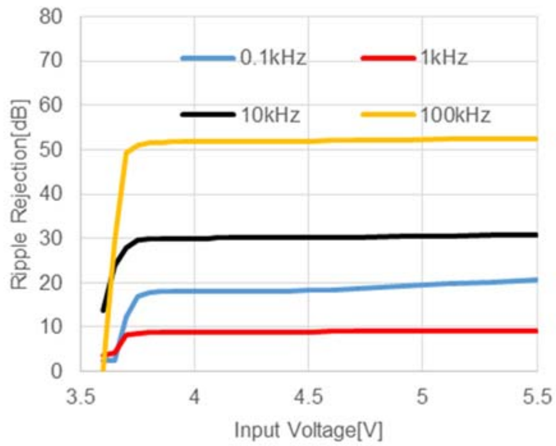
RP124x18xx, I_{OUT} = 100 μA



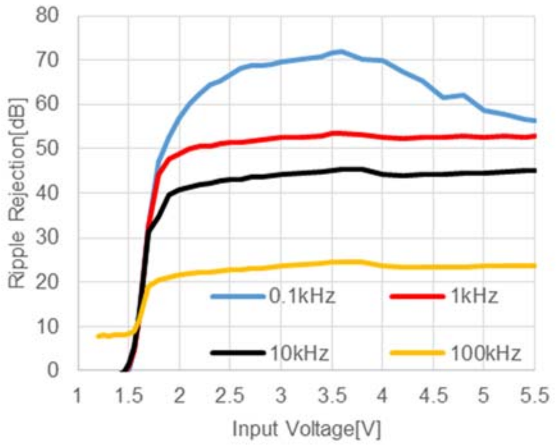
RP124x28xx, I_{OUT} = 100μA



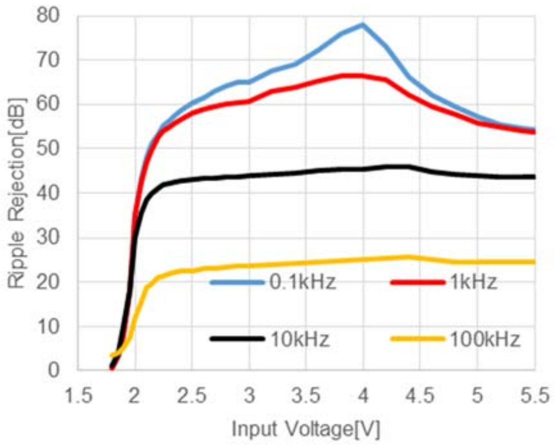
RP124x36xx, I_{OUT} = 100μA



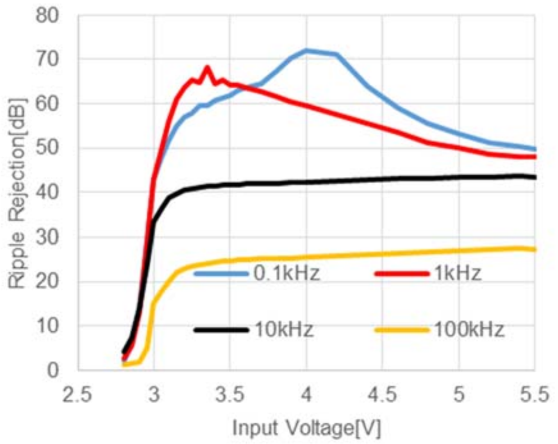
RP124x12xx, I_{OUT} = 30mA



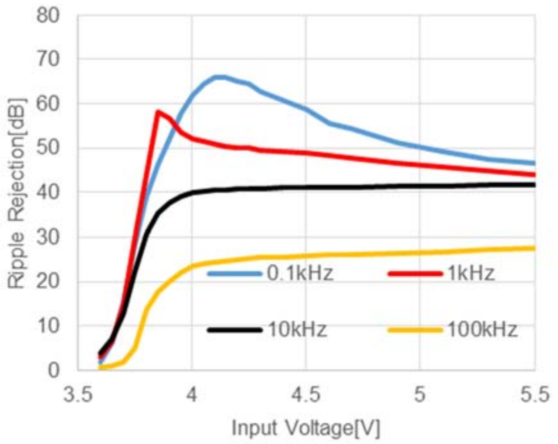
RP124x18xx, I_{OUT} = 30mA



RP124x28xx, I_{OUT} = 30mA

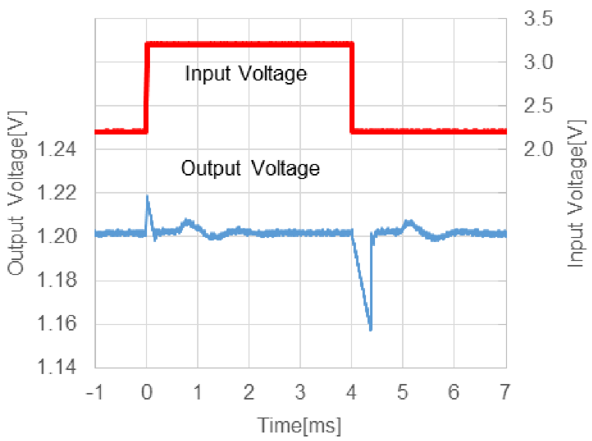


RP124x36xx, I_{OUT} = 30mA

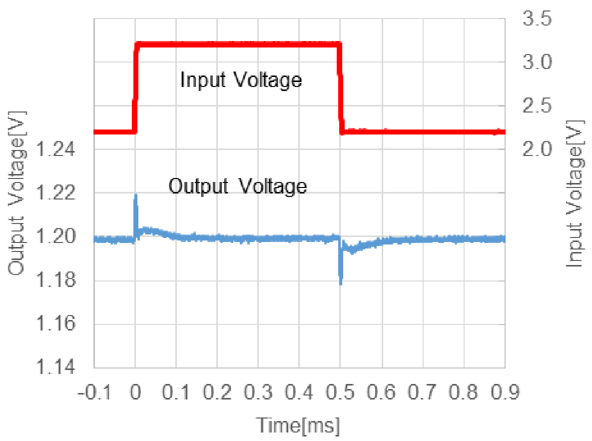


16) LDO Input Transient Response (C_{IN} = Ceramic 0.1 μF, C_{OUT} = Ceramic 1.0 μF, Ta = 25°C)

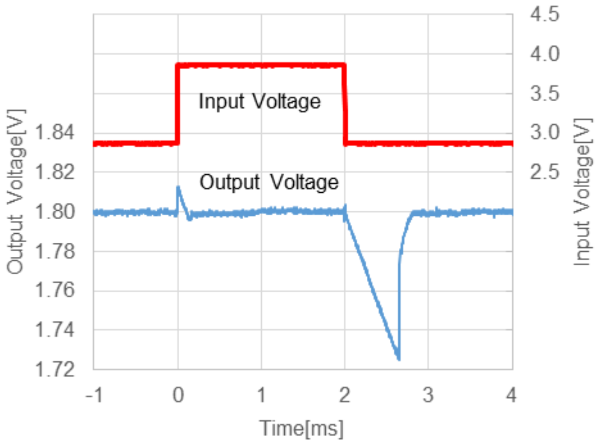
RP124x12xx, I_{OUT} = 100 μA, t_R = t_F = 5 μs



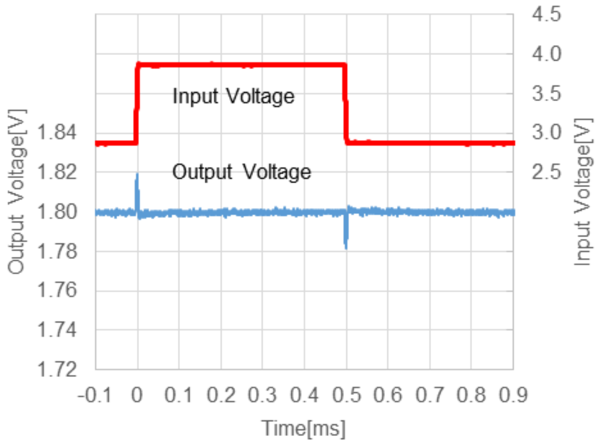
RP124x12xx, I_{OUT} = 30 mA, t_R = t_F = 5 μs



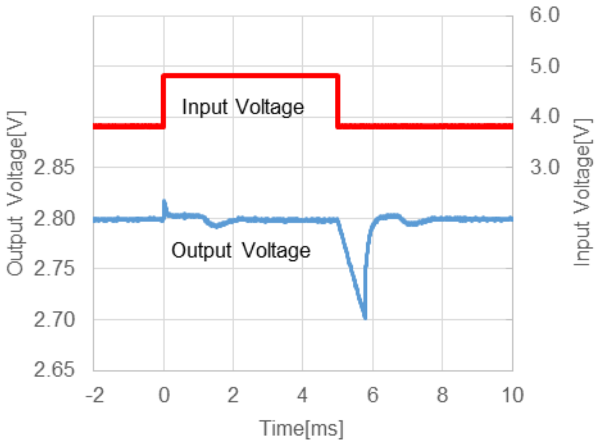
RP124x18xx, I_{OUT} = 100 µA, t_R = t_F = 5 µs



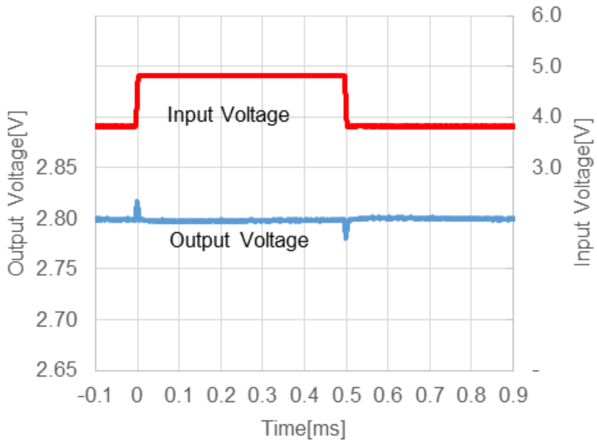
RP124x18xx, I_{OUT} = 30 mA, t_R = t_F = 5 µs



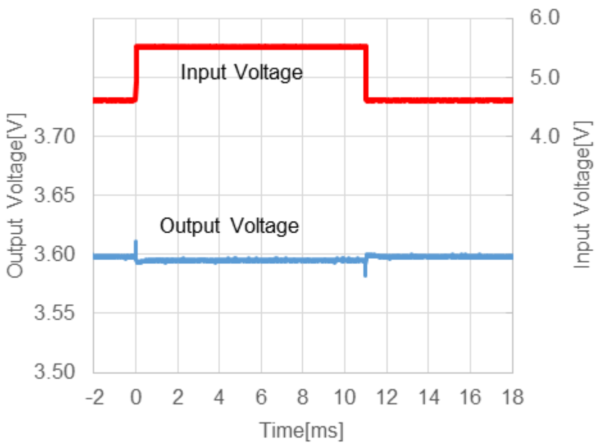
RP124x28xx, I_{OUT} = 100 µA, t_R = t_F = 5 µs



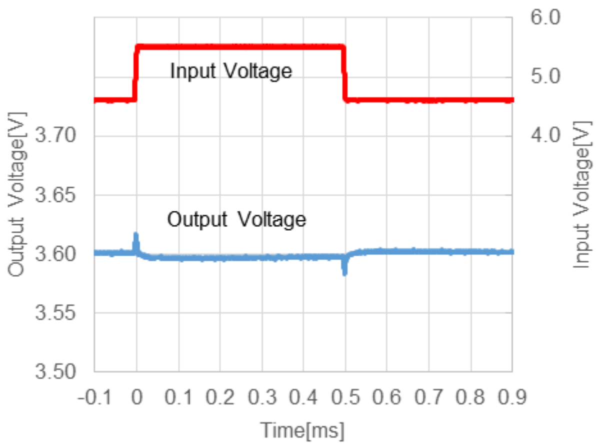
RP124x28xx, I_{OUT} = 30 mA, t_R = t_F = 5 µs



RP124x36xx, I_{OUT}= 100 µA, t_R = t_F = 5 µs



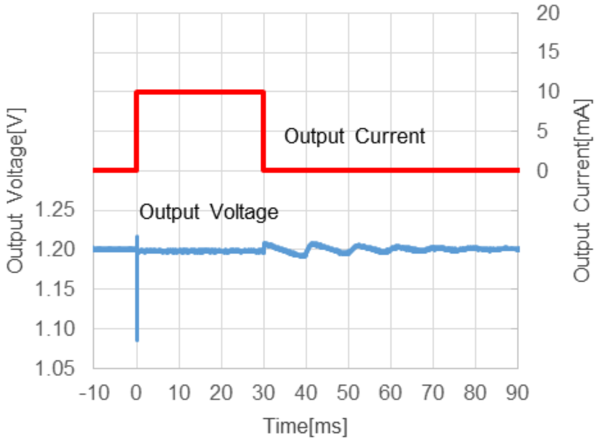
RP124x36xx, I_{OUT} = 30 mA, t_R = t_F = 5 µs



17) LDO Load Transient Response (C_{IN} = Ceramic 1.0 μF, C_{OUT} = Ceramic 1.0 μF, Ta = 25°C)

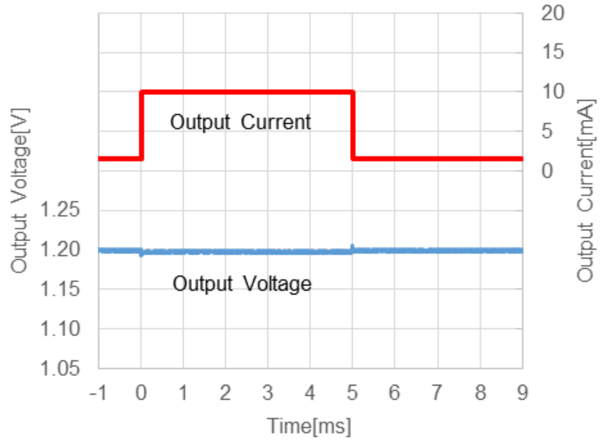
RP124x12xx

V_{IN} = 2.2 V, I_{OUT} = 1 μA <=> 10 mA, t_R = t_F = 5 μs



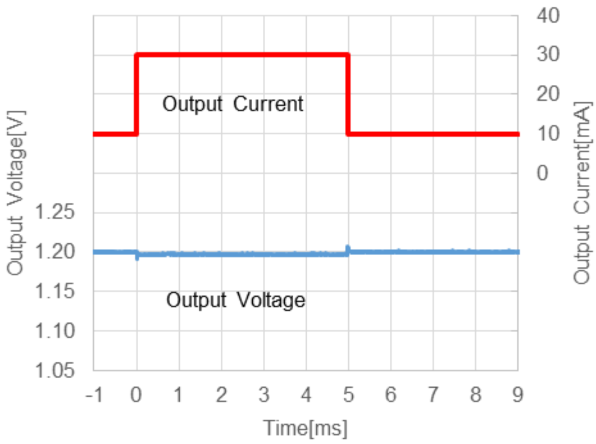
RP124x12xx

V_{IN} = 2.2 V, I_{OUT} = 1.5 mA <=> 10 mA, t_R = t_F = 5 μs



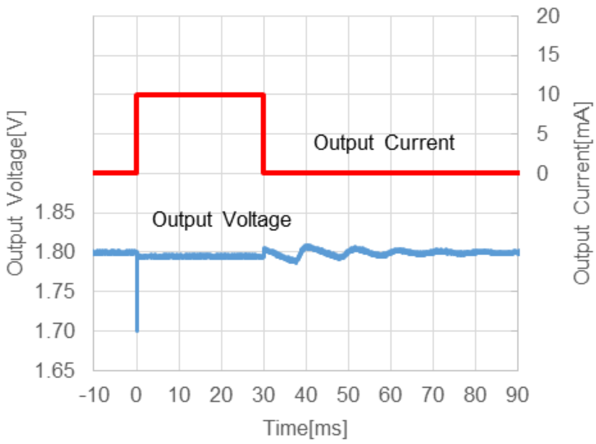
RP124x12xx

V_{IN} = 2.2 V, I_{OUT} = 10 mA <=> 30 mA, t_R = t_F = 5 μs



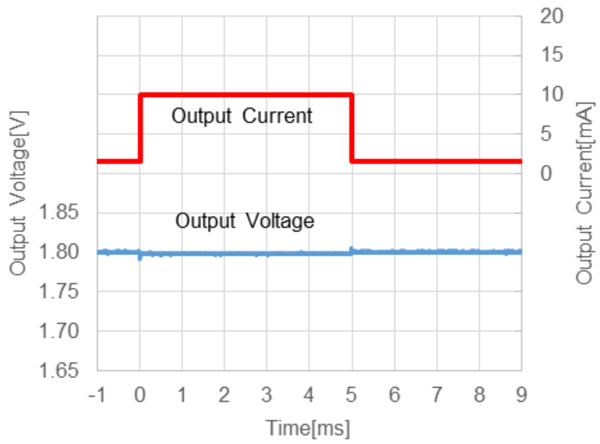
RP124x18xx

V_{IN} = 2.8 V, I_{OUT} = 1 μA <=> 10 mA, t_R = t_F = 5 μs

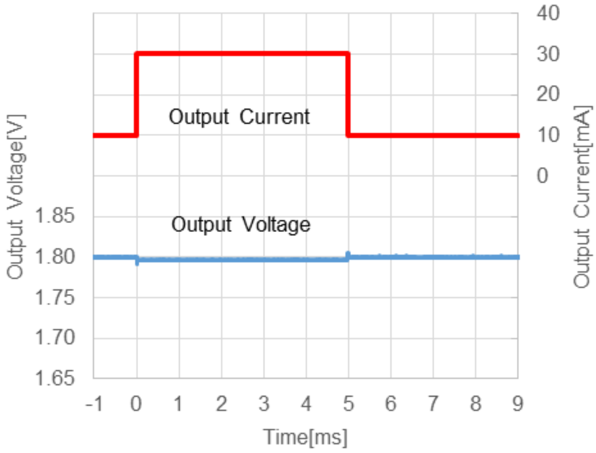


RP124x18xx

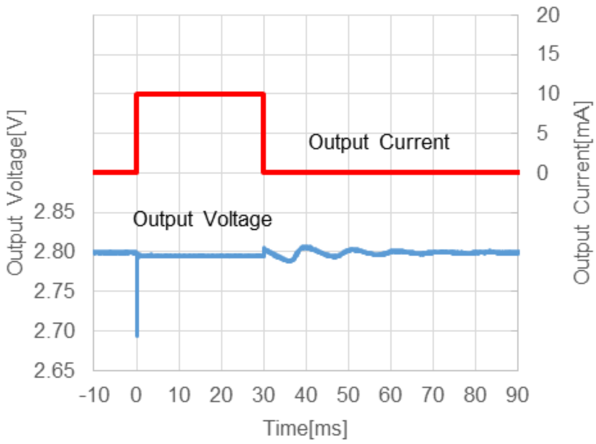
V_{IN} = 2.8 V, I_{OUT} = 1.5 mA <=> 10 mA, t_R = t_F = 5 μs



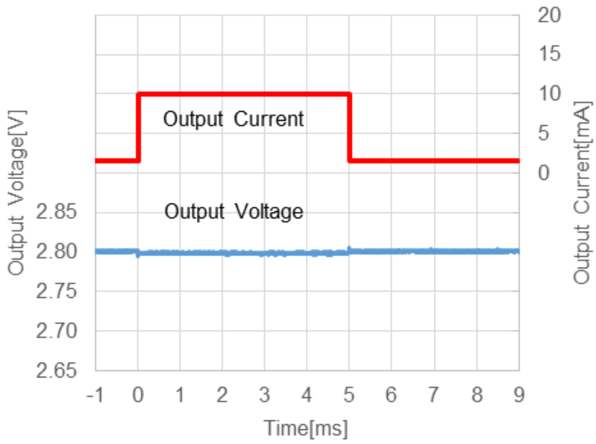
RP124x18xx
V_{IN} = 2.8 V, I_{OUT} = 10 mA <=> 30 mA, t_R = t_F = 5 μs



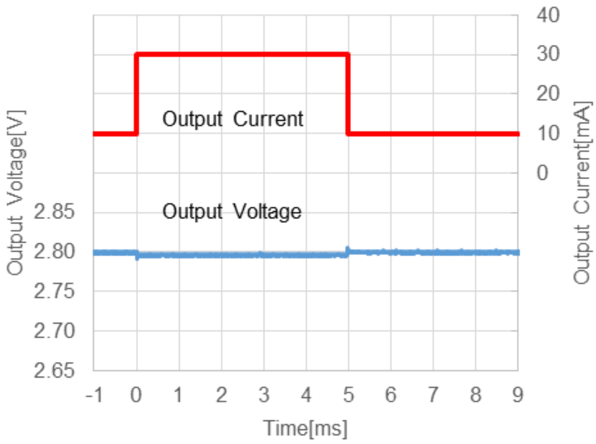
RP124x28xx
V_{IN} = 3.8 V, I_{OUT} = 1 μA <=> 10 mA, t_R = t_F = 5 μs



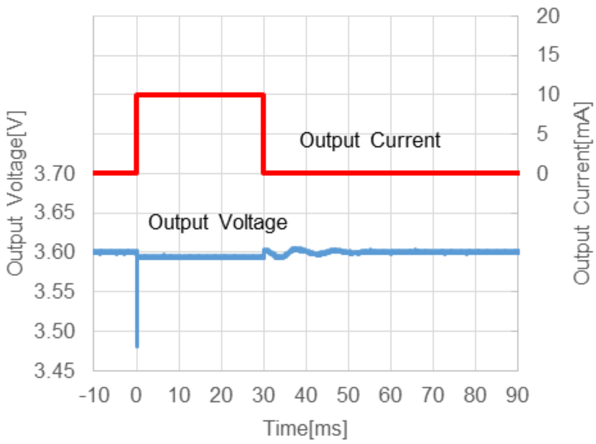
RP124x28xx
V_{IN} = 3.8 V, I_{OUT} = 1.5 mA <=> 10 mA, t_R = t_F = 5 μs



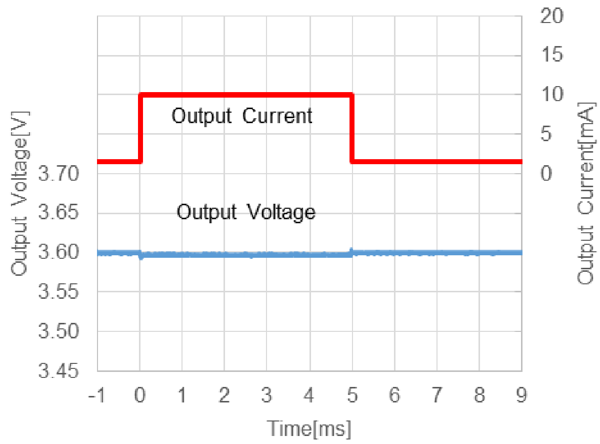
RP124x28xx
V_{IN} = 3.8 V, I_{OUT} = 10 mA <=> 30 mA, t_R = t_F = 5 μs



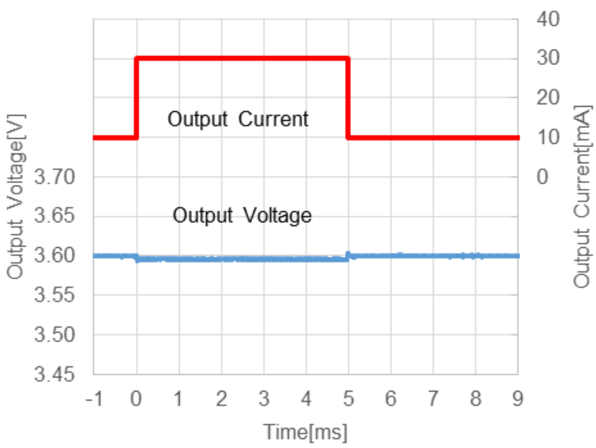
RP124x36xx
V_{IN} = 4.6 V, I_{OUT} = 1 µA <=> 10 mA, t_R = t_F = 5 µs



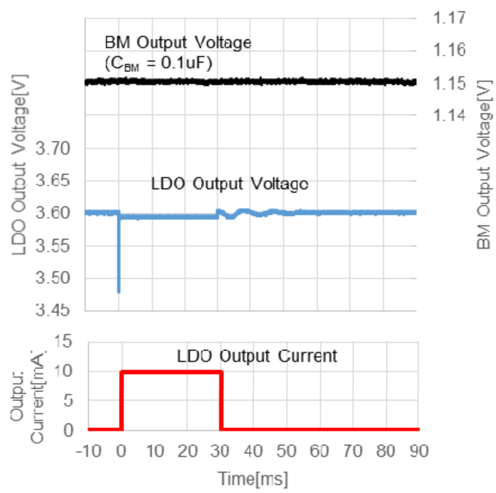
RP124x36xx
V_{IN} = 4.6 V, I_{OUT} = 1.5 mA <=> 10 mA, t_R = t_F = 5 µs



RP124x36xx
V_{IN} = 4.6 V, I_{OUT} = 10 mA <=> 30 mA, t_R = t_F = 5 µs

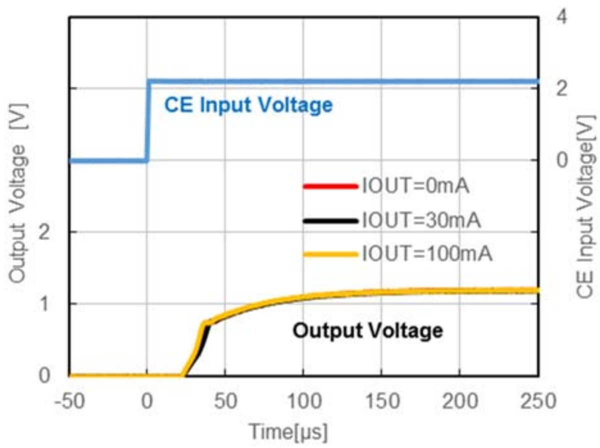


RP124x364x
V_{IN} = 4.6 V, I_{OUT} = 1 µA <=> 10 mA, t_R = t_F = 5 µs

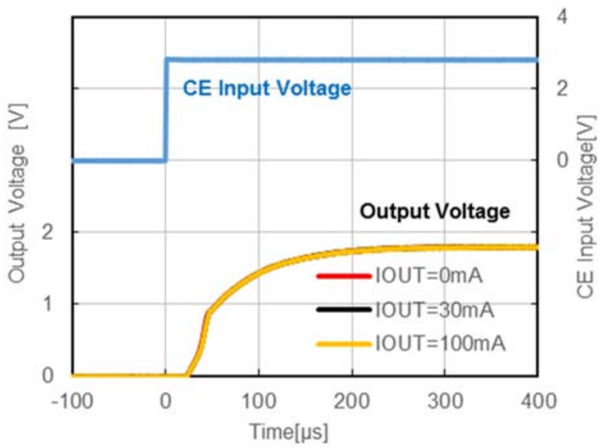


18) LDO Turning-on with CE Pin (C_{IN} = Ceramic 1.0 µF, C_{OUT} = Ceramic 1.0 µF, Ta = 25°C)

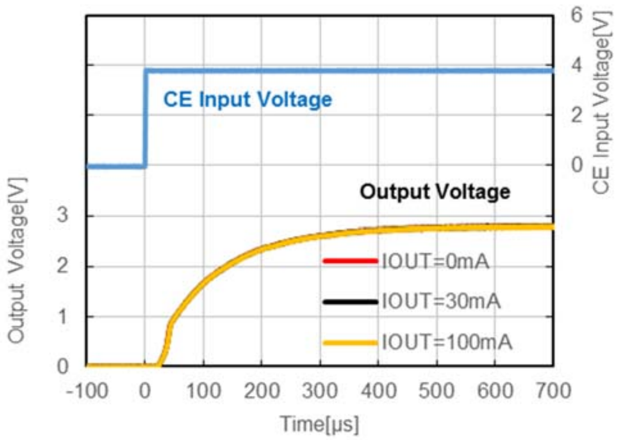
RP124x12xD, V_{IN} = 2.2 V, V_{CE} = 0 V => 2.2 V



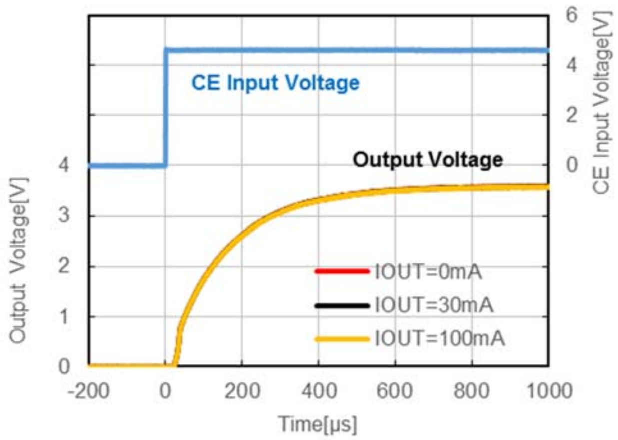
RP124x18xD, V_{IN} = 2.8 V, V_{CE} = 0 V => 2.8 V



RP124x28xD, V_{IN} = 3.8 V, V_{CE} = 0 V => 3.8 V

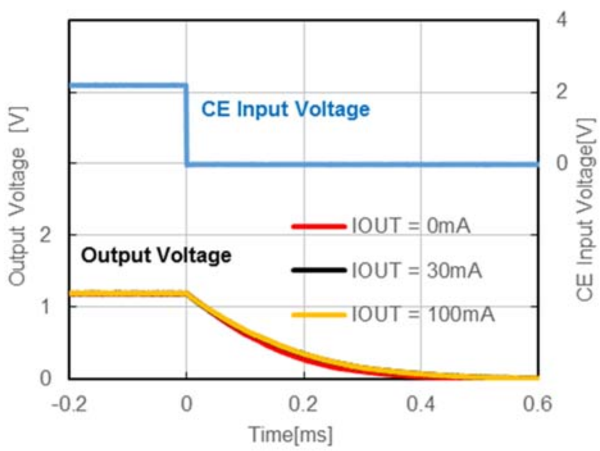


RP124x36xD, V_{IN} = 4.6 V, V_{CE} = 0 V => 4.6 V

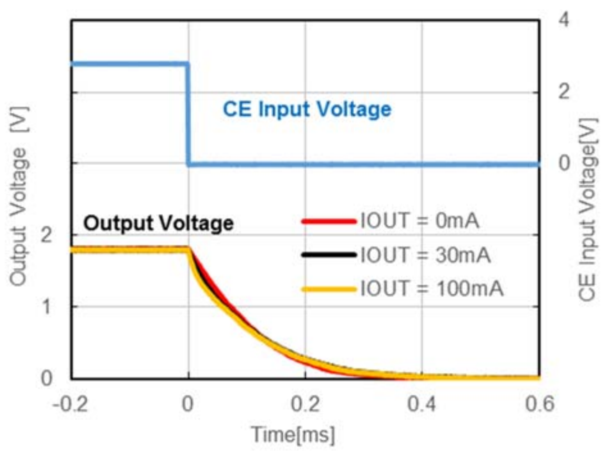


19) LDO Turning-off with CE Pin (C_{IN} = Ceramic 1.0 µF, C_{OUT} = Ceramic 1.0 µF, Ta = 25°C)

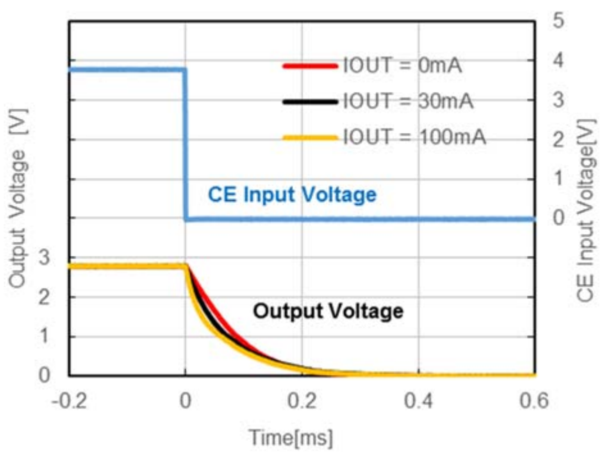
RP124x12xD, V_{IN} = 2.2 V, V_{CE} = 2.2 V => 0 V



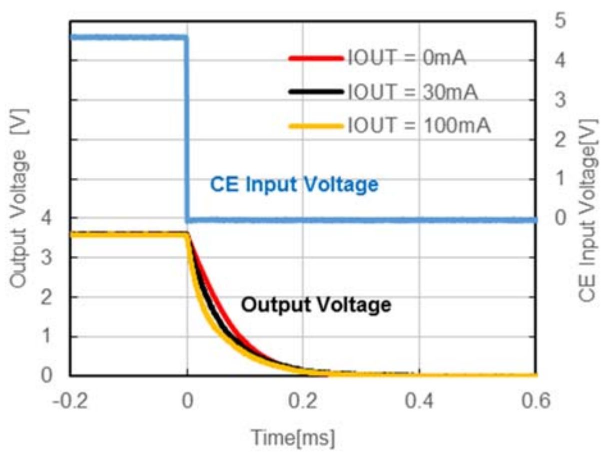
RP124x18xD, V_{IN} = 2.8 V, V_{CE} = 2.8 V => 0 V



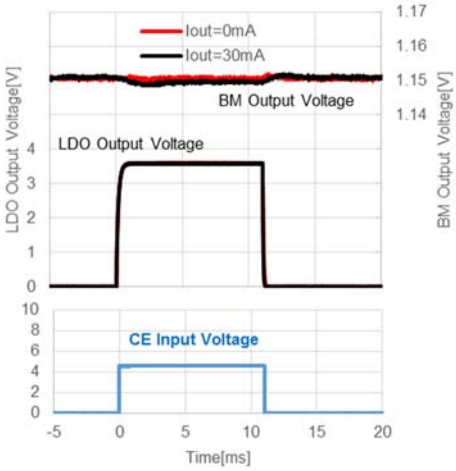
RP124x28xD, V_{IN} = 3.8 V, V_{CE} = 3.8 V => 0 V



RP124x36xD, V_{IN} = 4.6 V, V_{CE} = 4.6 V => 0 V

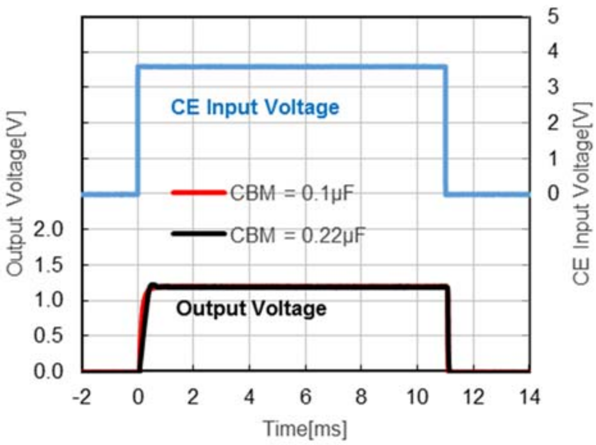


RP124x364D, V_{IN} = 4.6 V, V_{CE} = 0 V <=> 4.6 V

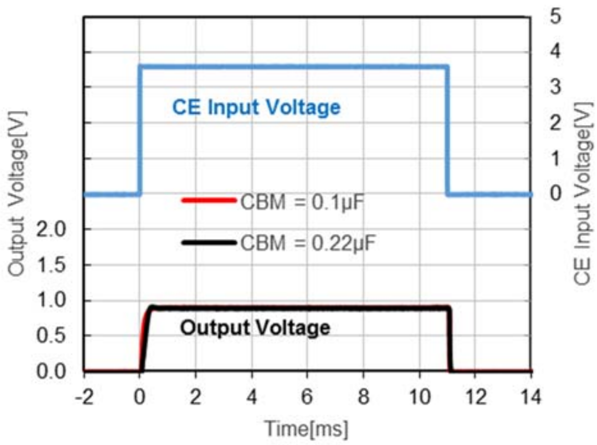


20) BM Turning-on/off with CE Pin (C_{IN} = Ceramic 1.0 μF, C_{BM} = Ceramic 0.1 μF, 0.22 μF, Ta = 25°C)

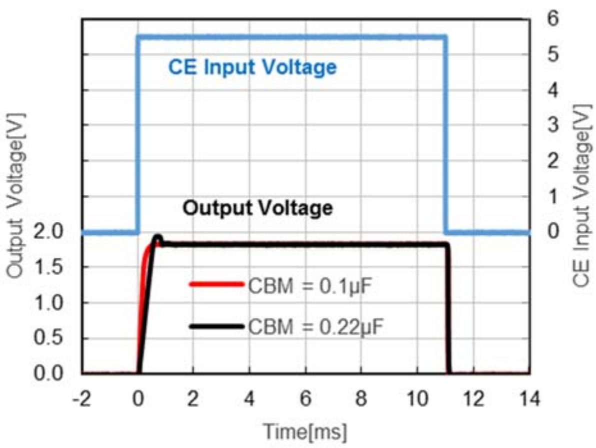
RP124xxx3x, V_{IN} = 3.6 V, V_{CE} = 0 V <=> 3.6 V



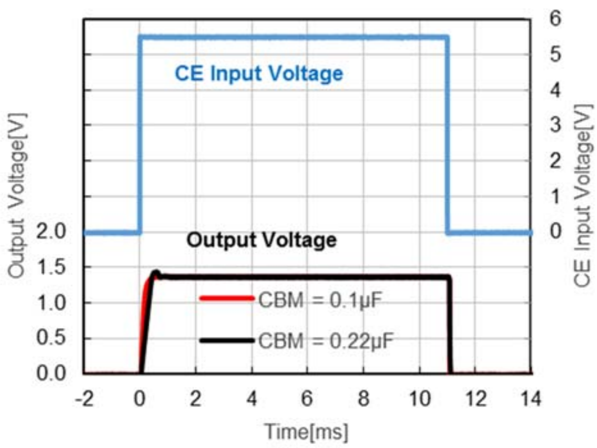
RP124xxx4x, V_{IN} = 3.6 V, V_{CE} = 0 V <=> 3.6 V



RP124xxx3x, V_{IN} = 5.5 V, V_{CE} = 0 V <=> 5.5 V

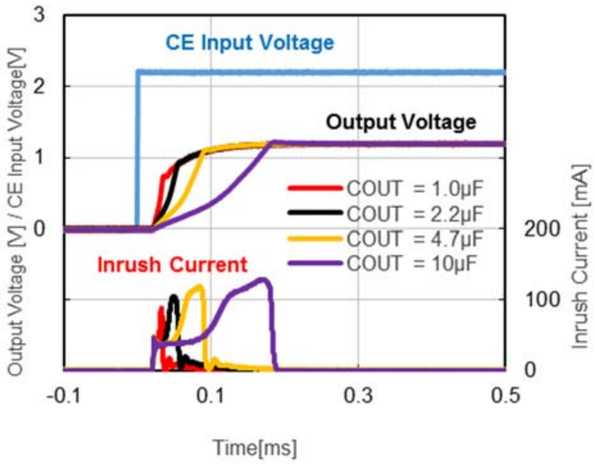


RP124xxx4x, V_{IN} = 5.5 V, V_{CE} = 0 V <=> 5.5 V

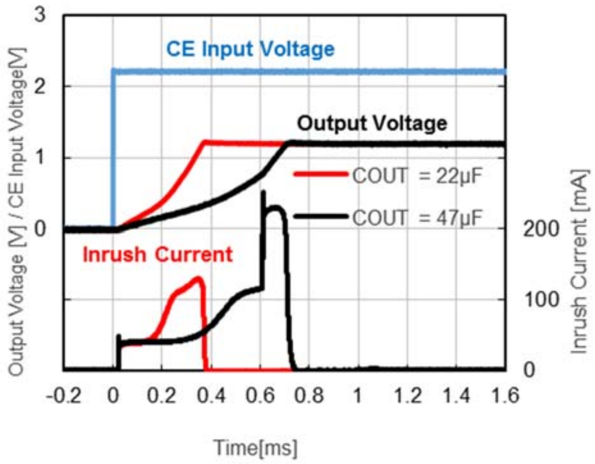


21) Inrush Current at CE Pin's Activation (C_{IN} = Ceramic 0.1 μF, Ta = 25°C)

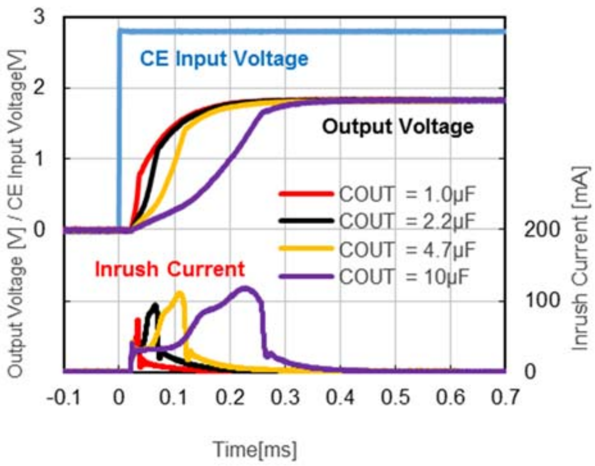
RP124x12xx, V_{IN} = 2.2 V, V_{CE} = 0 V => 2.2 V ①



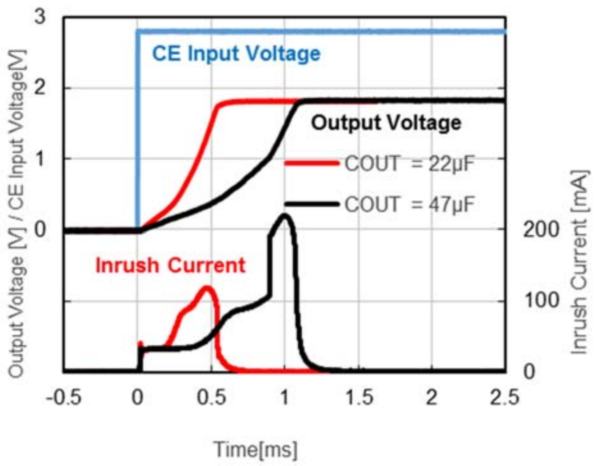
RP124x12xx, V_{IN} = 2.2 V, V_{CE} = 0 V => 2.2 V ②



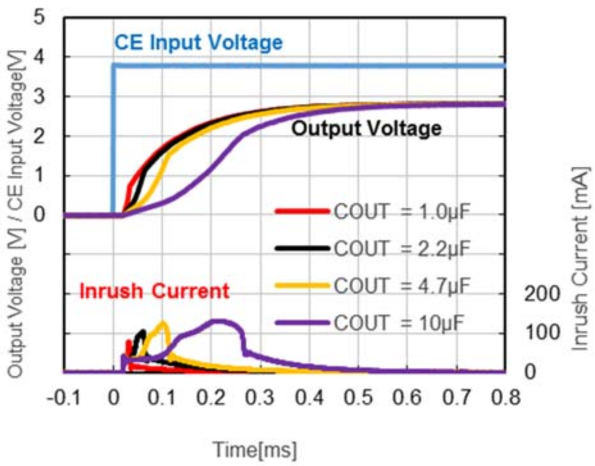
RP124x18xx, V_{IN} = 2.8 V, V_{CE} = 0 V => 2.8 V ①



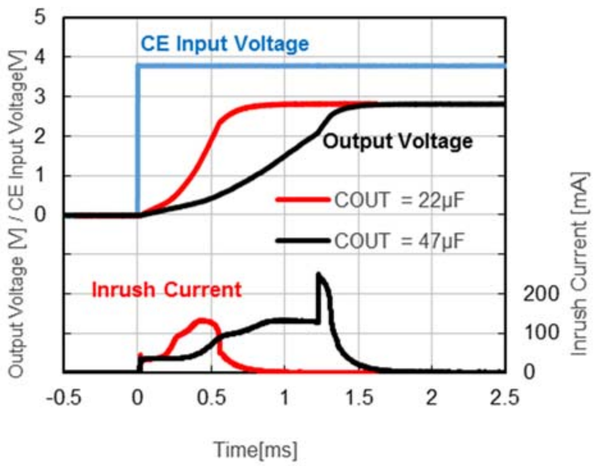
RP124x18xx, V_{IN} = 2.8 V, V_{CE} = 0 V => 2.8 V ②



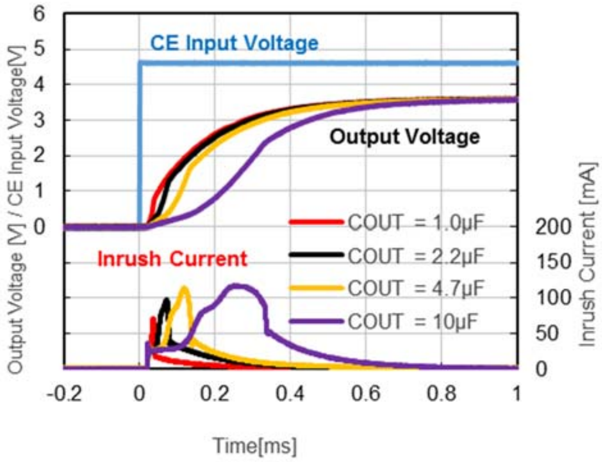
RP124x28xx, V_{IN} = 3.8 V, V_{CE} = 0 V => 3.8 V ①



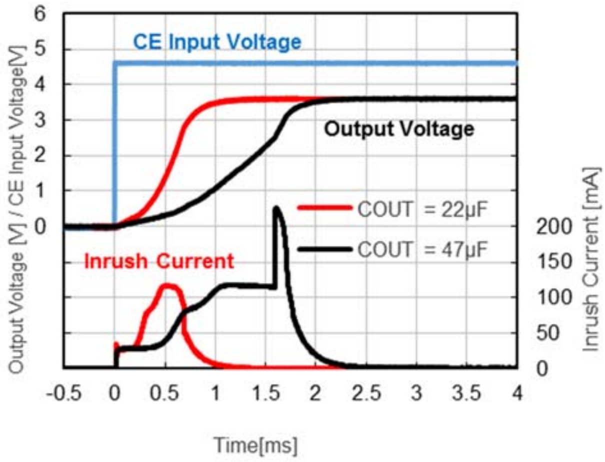
RP124x28xx, V_{IN} = 3.8 V, V_{CE} = 0 V => 3.8 V ②



RP124x36xx, V_{IN} = 4.6 V, V_{CE} = 0 V => 4.6 V ①

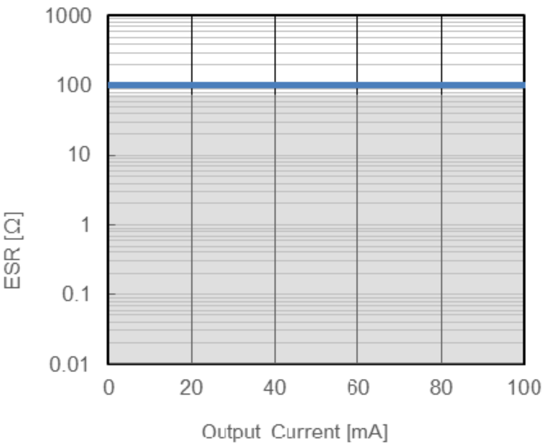


RP124x36xx, V_{IN} = 4.6 V, V_{CE} = 0 V => 4.6 V ②

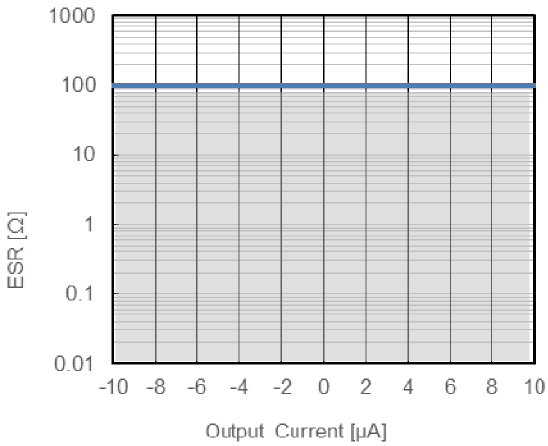


22) ESR vs. Output Current (C_{IN} = Ceramic 1.0 μF, C_{OUT} = Ceramic 1.0 μF, C_{BM} = Ceramic 0.1 μF)
Measuring Frequency：10 Hz to 2 MHz、Ambient Temperature：-40°C to 5°C

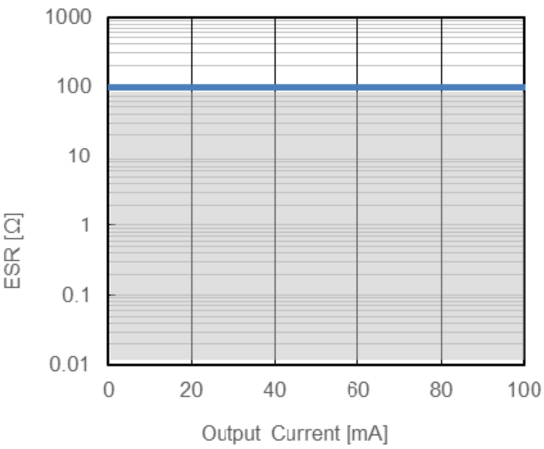
LDO
RP124x12xx, V_{IN}= 1.7V to 5.5V



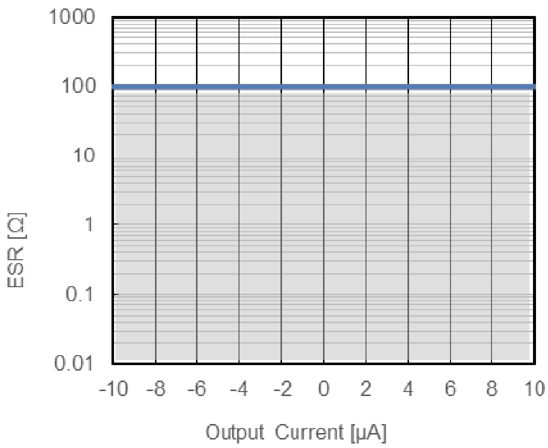
BM
RP124xxx3x, V_{IN}= 1.7V to 5.5V



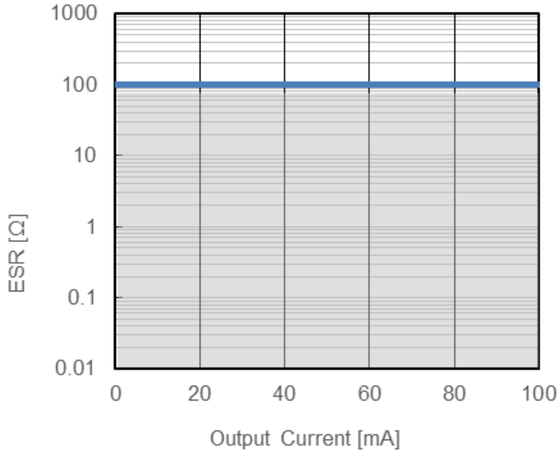
LDO
RP124x28xx, V_{IN} = 2.8 V to 5.5 V



BM
RP124xxx4x, V_{IN} = 2.4 V to 5.5 V



LDO
RP124x36xx, V_{IN} = 3.6 V to 5.5 V



The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

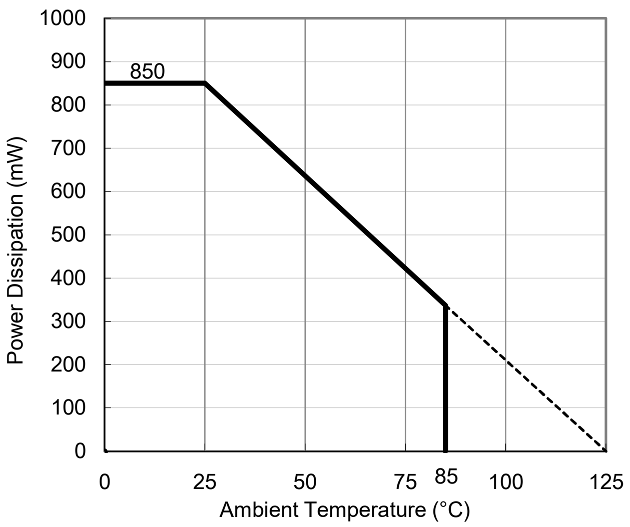
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.2 mm × 14 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

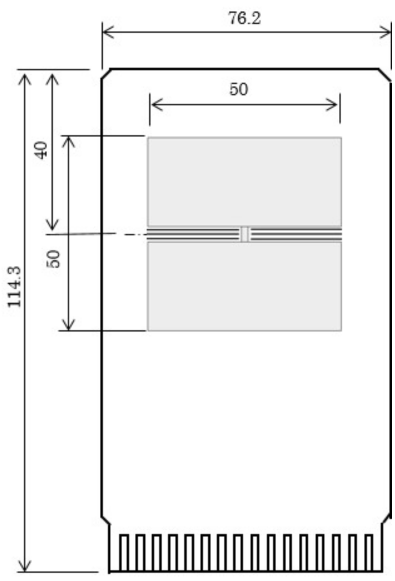
Item	Measurement Result
Power Dissipation	850 mW
Thermal Resistance (θja)	θja = 117°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 50°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter



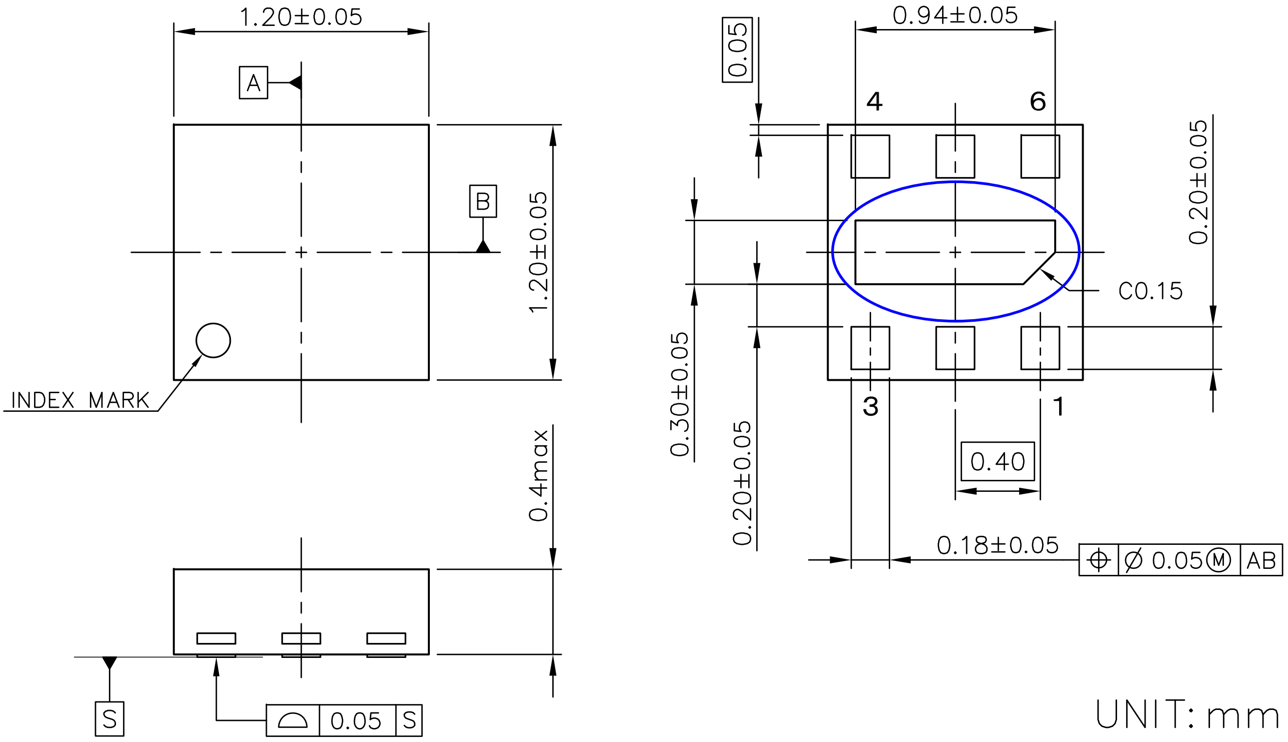
Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

RICOH

Ver. B



DFN1212-6 Package Dimensions

∗ The tab on the bottom of the package is substrate level (GND). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

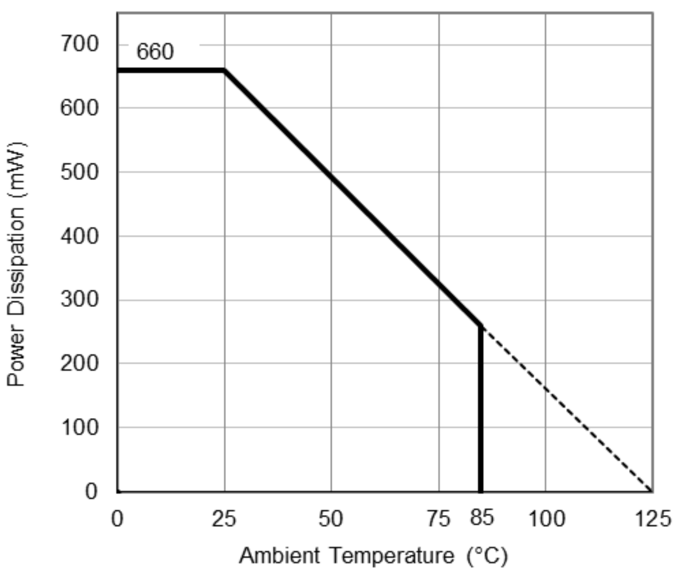
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 7 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

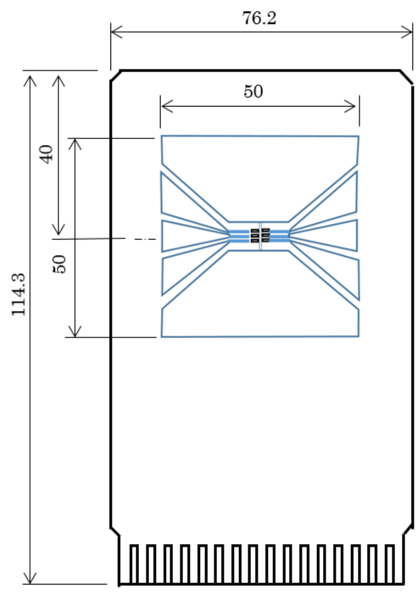
Item	Measurement Result
Power Dissipation	660 mW
Thermal Resistance (θja)	θja = 150°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 51°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter



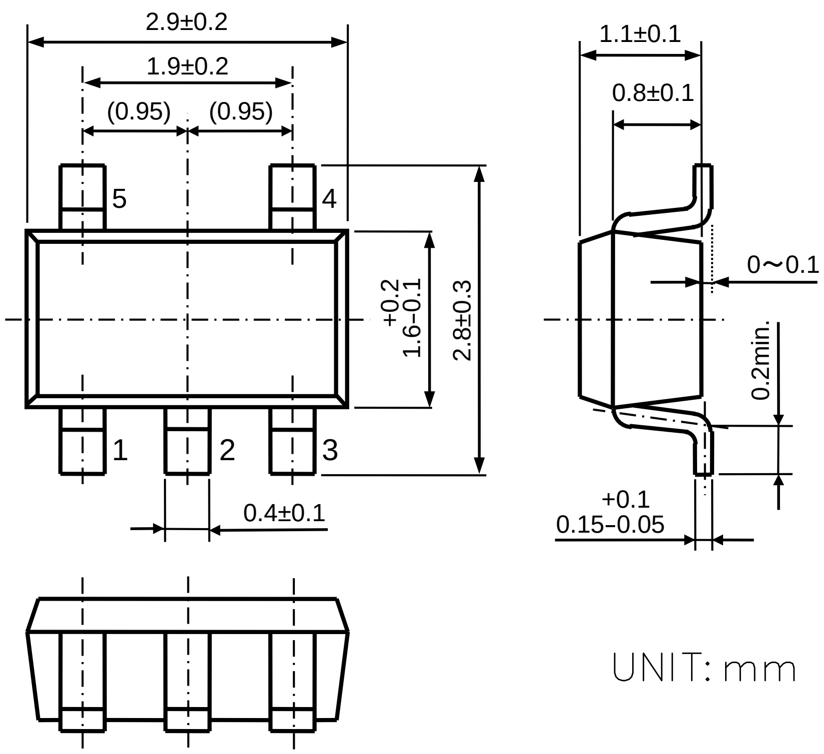
Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

RICOH

Ver. A



SOT-23-5 Package Dimensions

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