

42 V Input Power Management IC with Window Voltage Detector

No.EA-500-181128

OVERVIEW

The R5116x is a Power Management IC featuring input voltage range from 3.5 V to 42 V. This IC includes 500 mA Voltage Regulator and Window Voltage Detector in a single chip.

KEY BENEFITS

- Reducing components and improving functional safety
- High accuracy of the output voltage and the detector threshold: -1.25 % to 0.75 %
- Preventing the false detection of transient characteristic fluctuations by high-speed response Voltage Regulator

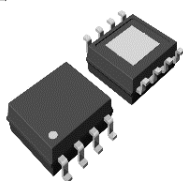
KEY SPECIFICATIONS

- Input Voltage Range (Max. Rating):
3.5 V to 42.0 V (50.0 V)
 - Supply Current: Typ. 25 μ A
- Voltage Regulator (VR)**
- Output Voltage Range: 3.3 V to 5.0 V
 - Output Voltage Accuracy: -1.25 % to 0.75 %
($-40^{\circ}\text{C} \leq T_a \leq 105^{\circ}\text{C}$)
 - Output Current: 500 mA
 - Protection:
Thermal shutdown (Detection Temp. Typ.175 $^{\circ}\text{C}$)
Output current (Typ.750 mA)
Output short-circuit (Typ.105 mA)

Voltage Detector (VD)

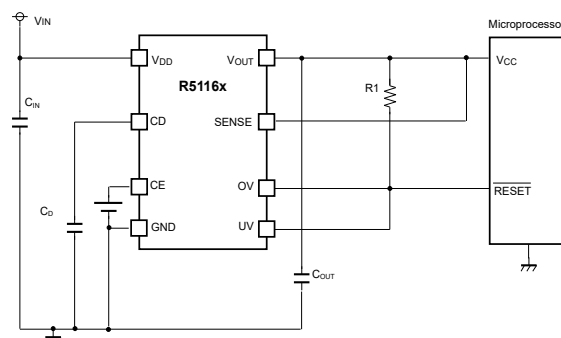
- Overvoltage (OV) Detector Threshold :
3.3 V to 5.5 V (in 0.01V step)
- Undervoltage (UV) Detector Threshold :
2.5 V to 5.0 V (in 0.01V step)
- Detector Threshold Accuracy:
-1.25% to 0.75% ($-40^{\circ}\text{C} \leq T_a \leq 105^{\circ}\text{C}$)
- Release hysteresis: max 0.7%

PACKAGES



HSOP-8E
5.20 x 6.20 x 1.45 (mm)

TYPICAL APPLICATIONS



- C_{IN} : 0.1 μ F, C_{OUT} : 10 μ F, Ceramic capacitors
- C_D : Ceramic capacitors for setting detection delay time

SELECTION GUIDE

Product Name	Package	Quantity per Reel
R5116SxxxA-E2-FE	HSOP-8E	1,000 pcs

xxx: Specify the set output voltage for VR (V_{VRSET}), the set OV detector threshold (V_{OVSET}) and the set UV detector threshold (V_{UVSET}) by using serial numbers starting from 001

Refer to ELECTRICAL CHARACTERISTICS for detail information.

APPLICATIONS

- Household electric appliances such as Refrigerators, Rice Cookers and Electric Kettles
- Laptop PCs, Digital Cameras, Digital TVs, Phones and LAN Systems

R5116x

No.EA-500-181128

SELECTION GUIDE

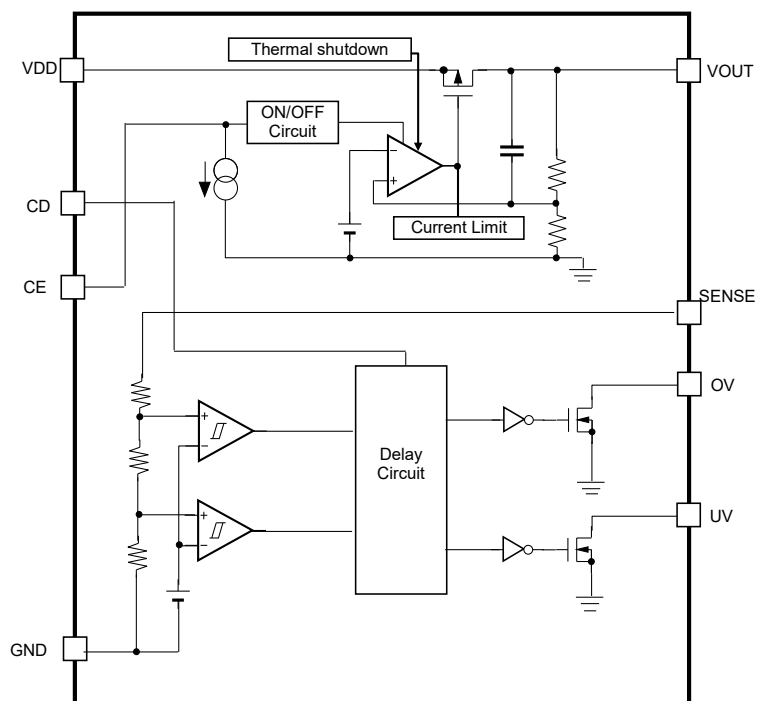
The set out voltages are user-selectable options.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5116SxxxA-E2-FE	HSOP-8E	1,000 pcs	Yes	Yes

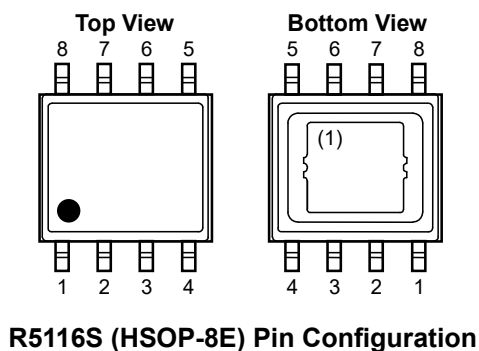
xxx: Specify the set output voltage for VR (V_{VRSET}), the set OV detector threshold (V_{OVSET}) and the UV detector threshold (V_{UVSET}) by using serial numbers starting from 001⁽¹⁾
Refer to ELECTRICAL CHARACTERISTICS for detail information

⁽¹⁾ The combinations of V_{VRSET} , V_{OVSET} and V_{UVSET} are following conditions;

- V_{VRSET} = 3.3 V to 5.0 V
- V_{OVSET} = 3.3 V to 5.5 V
- V_{UVSET} = 2.5 V to 5.0 V

BLOCK DIAGRAM**R5116xxx Block Diagram**

PIN DESCRIPTIONS



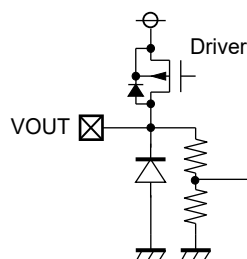
R5116S (HSOP-8E)

Pin No.	Symbol	Description
1	VDD	Supply Voltage Pin
2	CD	Pin for setting VD Release Output Delay Time (power-on reset time)
3	CE	Chip Enable Pin (Active-high)
4	GND	Ground Pin
5	UV	UV Detection Output Pin ("Low" at detection)
6	OV	OV Detection Output Pin ("Low" at detection)
7	SENSE	SENSE Pin
8	VOUT	Regulator Output Pin

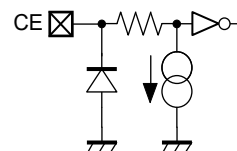
⁽¹⁾ The tab on the bottom of the package is substrate level (GND). It is recommended that the tab be connected to the ground plane on the board.

PIN EQUIVALENT CIRCUIT DIAGRAMS

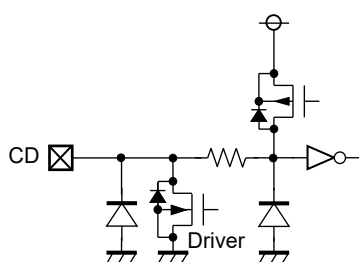
< VOUT Pin >



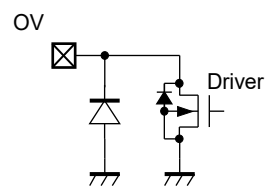
< CE Pin >



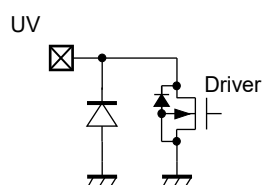
< CD Pin >



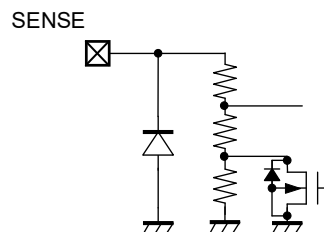
< OV Pin >



< UV Pin >



< SENSE Pin >



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{IN}	Input Voltage	-0.3 to 50	V
	Peak Input Voltage ⁽¹⁾	60	V
V_{CE}	CE Pin Input Voltage	-0.3 to 50	V
V_{OUT}	Output Voltage	-0.3 ~ $V_{IN} + 0.3 \leq 50$	V
V_{SENSE}	SENSE Pin Voltage	-0.3 to 50	V
V_{CD}	CD Pin Output Voltage	-0.3 to 50	V
V_{OVOUT}	OV Pin Output Voltage	-0.3 to 7.0	V
V_{UVOUT}	UV Pin Output Voltage	-0.3 to 7.0	V
P_D	Power Dissipation ⁽²⁾ (HSOP-8E, JEDEC STD. 51)	2900	mW
T_j	Junction Temperature	-40 to 125	°C
T_{stg}	Storage Temperature	-55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Rating	Unit
V_{IN}	Input Voltage	3.5 to 42	V
V_{CE}	CE Pin Input Voltage	0 to 42	V
V_{SENSE}	SENSE Pin Input Voltage	0 to 6.0	V
V_{OVOUT}	OV Pin Output Voltage	0 to 6.0	V
V_{UVOUT}	UV Pin Output Voltage	0 to 6.0	V
T_a	Operating Temperature	-40 to 105	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

⁽¹⁾ Duration time: 200 ms

⁽²⁾ Refer to POWER DISSIPATION for detail information

ELECTRICAL CHARACTERISTICS

$C_{IN} = 0.1 \mu F$, $C_{OUT} = 10 \mu F$, $V_{IN} = 14 V$, unless otherwise noted.

The specifications surrounded by are guaranteed by design engineering at $-40^{\circ}C \leq T_a \leq 105^{\circ}C$.

R5116xxxx

For All

($T_a = 25^{\circ}C$)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{SS}	Supply Current	$I_{OUT} = 0 \text{ mA}$		25	50	μA
$I_{standby}$	Standby Current	$V_{IN} = 42 V$, $V_{CE} = 0 V$		1.5	5.0	μA
I_{PD}	CE Pull-down Current			0.2	0.6	μA
V_{CEH}	CE Input Voltage, high		2.0		42	V
V_{CEL}	CE Input Voltage, low		0		1.0	V

All test items listed under Electrical Characteristics are done under the pulse load condition ($T_j \approx T_a = 25^{\circ}C$).

VR Section

($T_a = 25^{\circ}C$)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	$V_{IN} = 14 V$, $I_{OUT} = 1 \text{ mA}$	$T_a = 25^{\circ}C$	$\times 0.995$	$\times 1.005$	V
			$-40^{\circ}C \leq T_a \leq 105^{\circ}C$	$\times 0.9875$	$\times 1.0075$	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	$V_{IN} = V_{SET} + 3.0 V$	$1 \text{ mA} \leq I_{OUT} \leq 300 \text{ mA}$	-10	10	mV
			$1 \text{ mA} \leq I_{OUT} \leq 500 \text{ mA}$	-15	15	
V_{DIF}	Dropout Voltage	$I_{OUT} = 500 \text{ mA}$	$V_{SET} = 3.3 V$		1.1	V
			$V_{SET} = 5.0 V$		0.9	
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	$I_{OUT} = 1 \text{ mA}$	$8.0 V \leq V_{IN} \leq 16 V$	-10	10	mV
			$6.0 V \leq V_{IN} \leq 32 V$	-25	25	
I_{LIM}	Output Current Limit	$V_{IN} = 8.0 V$	500	750		mA
I_{SC}	Short Current Limit	$V_{OUT} = 0 V$	70	105	150	mA
T_{TSD}	Thermal Shutdown Temperature	Junction Temperature	165	175		$^{\circ}C$
T_{TSR}	Thermal Shutdown Release Temperature	Junction Temperature	125	145		$^{\circ}C$

All test items listed under Electrical Characteristics are done under the pulse load condition ($T_j \approx T_a = 25^{\circ}C$).

R5116x

No.EA-500-181128

ELECTRICAL CHARACTERISTICS (Continued) $C_{IN} = 0.1 \mu F$, $C_{OUT} = 10 \mu F$, $V_{IN} = 14 V$, unless otherwise noted.The specifications surrounded by are guaranteed by design engineering at $-40^{\circ}C \leq T_a \leq 105^{\circ}C$.**VD Section**

(Ta = 25°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OVDET}	OV Detector Threshold	Ta = 25°C	×0.995		×1.005	V
		$-40^{\circ}C \leq T_a \leq 105^{\circ}C$	×0.9875		×1.0075	
V_{UVDET}	UV Detector Threshold	Ta = 25°C	×0.995		×1.005	V
		$-40^{\circ}C \leq T_a \leq 105^{\circ}C$	×0.9875		×1.0075	
V_{OVHYS}	OV Detector Threshold Hysteresis		$\frac{V_{OVDET}}{\times 0.003}$	$V_{OVDET} \times 0.005$	$\frac{V_{OVDET}}{\times 0.007}$	V
V_{UVHYS}	UV Detector Threshold Hysteresis		$\frac{V_{UVDET}}{\times 0.003}$	$V_{UVDET} \times 0.005$	$\frac{V_{UVDET}}{\times 0.007}$	V
t_{DELAY}	Release Output Delay Time (Power-on Reset)	$C_D = 10 \text{ nF}$	2	4	8	ms
V_{UVLO}	UVLO Detector Threshold			1.8	2.8	V
$V_{UVLOHYS}$	UVLO Detector Threshold Hysteresis			0.1	0.2	V
V_{OVOUT}	OV Pull-up Current				6.0	V
V_{UVOUT}	UV Pull-up Current				6.0	V
I_{OUTOV}	Nch Output Current (OV Output Pin)	$V_{IN} = 3.0 V$, $V_{DS} = 0.1 V$	0.8	2.0		mA
I_{OUTUV}	Nch Output Current (UV Output Pin)	$V_{IN} = 3.0 V$, $V_{DS} = 0.1 V$	0.8	2.0		mA
I_{LEAKOV}	Nch Leakage Current (OV Output Pin)	$V_{OVOUT} = 5.5 V$			0.3	μA
I_{LEAKUV}	Nch Leakage Current (UV Output Pin)	$V_{UVOUT} = 5.5 V$			0.3	μA
R_{LCD}	C_D Pin Discharge Nch Tr.ON Resistance	$V_{CE} = 0 V$, $V_{CD} = 0.1 V$		1.2	3.0	kΩ

All test items listed under Electrical Characteristics are done under the pulse load condition ($T_j \approx T_a = 25^{\circ}C$).

ELECTRICAL CHARACTERISTICS (Continued)

The specifications surrounded by are guaranteed by design engineering at $-40^{\circ}\text{C} \leq T_a \leq 105^{\circ}\text{C}$

R5116S Product-specific Electrical Characteristics

Product Name	V _{OUT}			V _{OUT}		
	T _a =25°C			-40°C ≤ T _a ≤ 105°C		
	Min.	Typ.	Max.	Min.	Typ.	Max.
R5116S001A	4.975	5.000	5.025	4.938	5.000	5.037
R5116S002A	3.284	3.300	3.316	3.259	3.300	3.324

Product Name	V _{OVD}			V _{OVD}			V _{OVHYS}		
	T _a =25°C			-40°C ≤ T _a ≤ 105°C			T _a =25°C		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
R5116S001A	5.274	5.300	5.326	5.234	5.300	5.339	0.01590	0.02650	0.03710
R5116S002A	3.523	3.540	3.557	3.496	3.540	3.566	0.01062	0.01770	0.02478

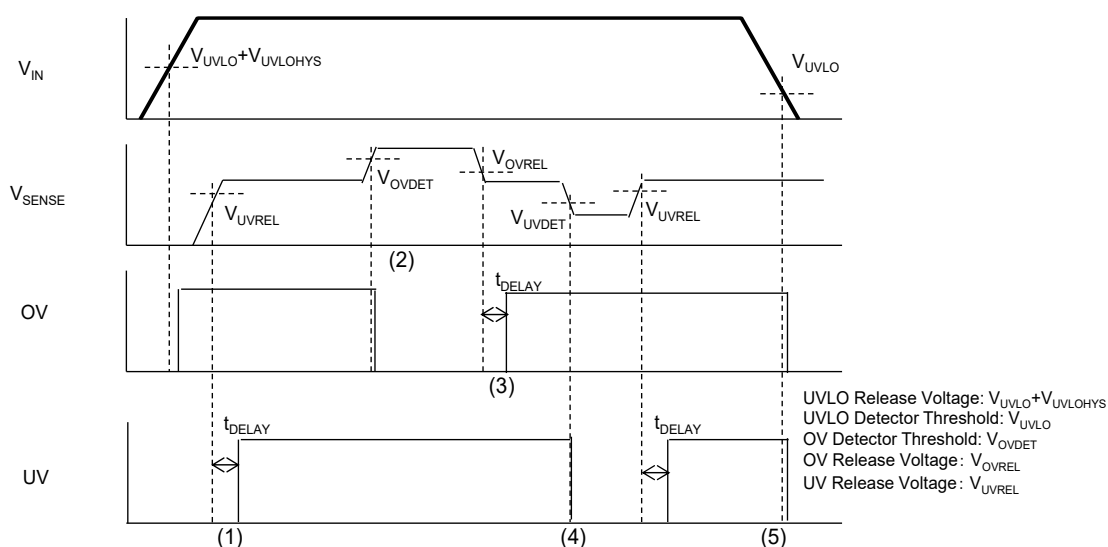
Product Name	V _{UVD}			V _{UVD}			V _{UVHYS}		
	T _a =25°C			-40°C ≤ T _a ≤ 105°C			T _a =25°C		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
R5116S001A	4.677	4.700	4.723	4.642	4.700	4.735	0.01410	0.02350	0.03290
R5116S002A	3.035	3.050	3.065	3.012	3.050	3.072	0.00915	0.01525	0.02135

THEORY OF OPERATION

Thermal Shutdown

When the junction temperature of this device exceeds 175°C (Typ.), the built-in thermal shutdown circuit stops the regulator operation. After that, when the temperature drops to 145°C (Typ.) or lower, the regulator restarts the operation. Unless eliminating the overheating problem, the regulator turns on and off repeatedly and a pulse shaped output voltage occurs as result.

R5116xxx Voltage Detector



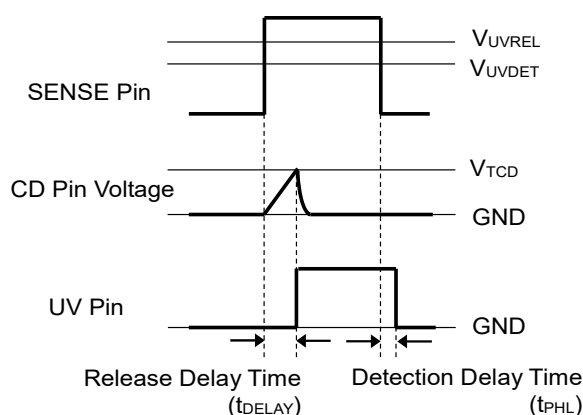
R5116xxx Voltage Detector Timing Chart

- (1) When the SENSE pin voltage (V_{SENSE}) exceed the UV release voltage (V_{UVREL}), the UV pin output becomes “High” after the release delay time (t_{DELAY}).
- (2) When V_{SENSE} exceed the OV detector threshold (V_{OVDET}) by increasing in voltage, the OV pin output becomes “Low” after the detection delay time (Typ.100 μ s) and enters the OV detecting state.
- (3) When V_{SENSE} decreases less than the OV release voltage (V_{OVREL}), the OV pin output becomes “High” after the release delay time (t_{DELAY}).
- (4) When V_{SENSE} decreases less than the UV detector threshold (V_{UVDET}), the UV pin output becomes “Low” after the detection delay time (Typ.100 μ s) and enters the UV detecting state.
- (5) When the input pin voltage (V_{IN}) decreases less than the UVLO detector threshold (V_{UVLO}), the OV and UV pins output become “Low”.

VD Delay Operation and Release Delay Time (t_{DELAY})

At Undervoltage Detection

When supplying a voltage higher than the UV release voltage (V_{UVREL}) to the SENSE pin, a charging to an external capacitor starts and the CD pin voltage (V_{CD}) increases. The UV pin voltage (V_{UV}) maintains “Low” until V_{CD} reaches the CD pin threshold voltage (V_{TCD}). When V_{CD} exceeds V_{TCD} , V_{UV} is inverted from “Low” to “High”. The release delay time (t_{DELAY}) is the period from the time the SENSE pin voltage (V_{SENSE}) exceeds V_{UVREL} to a rising edge of V_{UV} . When the output voltage turns from “Low” to “High”, a charge carrier of the external capacitor starts discharging. When supplying a voltage lower than the UV detector threshold (V_{UVDET}) to the SENSE pin, the detection delay time (t_{PHL}) remains constant independently of the external capacitor. t_{PHL} is the time V_{UV} is inverted from “High” to “Low”.



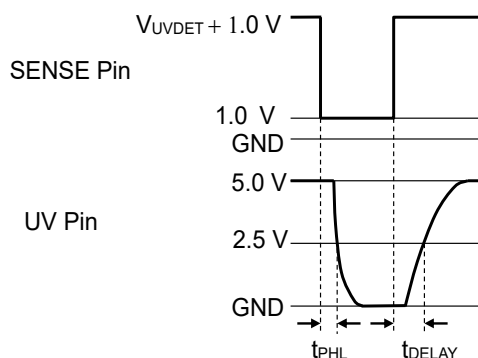
Undervoltage Release Delay Timing Diagram

Calculation of Undervoltage Release Delay Time

The following equation can calculate a typical value of the release delay time (t_{DELAY}) with using the external capacitor (C_{D}).

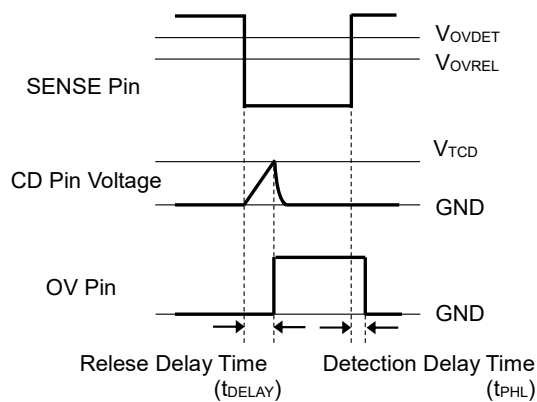
$$t_{\text{DELAY}} (\text{s}) = 0.72 \times C_{\text{D}} (\text{F}) / (1.8 \times 10^{-6})$$

t_{DELAY} is the period from supplying a pulse voltage of 1.0 V to ($V_{\text{UVDET}} + 1.0 \text{ V}$) to the SENSE pin to the UV pin reached 2.5 V after the UV pin is pulled up to 5V by connecting with a resistor of 100k Ω .



At Overvoltage Detection

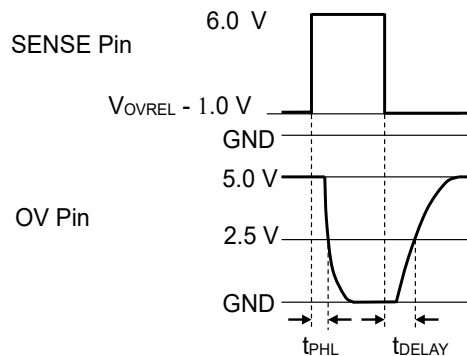
When supplying a voltage lower than the OV release voltage (V_{OVREL}) to the SENSE pin, a charging to an external capacitor starts and the CD pin voltage (V_{CD}) increases. The OV pin voltage (V_{OV}) maintains “Low” until V_{CD} reaches the CD pin threshold voltage (V_{TCD}). When V_{CD} exceeds V_{TCD} , V_{OV} is inverted from “Low” to “High”. The release delay time (t_{DELAY}) is the period from the time the SENSE pin voltage (V_{SENSE}) falls below V_{OVREL} to a rising edge of V_{OV} . When the output voltage turns from “Low” to “High”, a charge carrier of the external capacitor starts discharging. When the voltage higher than OV detector threshold (V_{OVDET}) is supplied to the SENSE pin, the detection delay time (t_{PHL}) remains constant independently of the external capacitor. t_{PHL} is the period that V_{OV} is inverted from “High” to “Low”.

**Overvoltage Release Delay Timing Diagram****Calculation of Overvoltage Release Delay Time**

The following equation can calculate a typical value of the release delay time (t_{DELAY}) with using the external capacitor (C_D).

$$t_{DELAY} (s) = 0.72 \times C_D (F) / (1.8 \times 10^{-6})$$

t_{DELAY} is the period from supplying a pulse voltage of 6.0 V to (V_{OVREL}) - 1.0 V to the SENSE pin to the OV pin reached 2.5 V after the OV pin is pulled up to 5V by connecting with a resistor of 100kΩ.



Voltage Setting of Voltage Regulator

The Window Voltage Detector (Window VD) detects the drop and rise of the Voltage Regulator (VR). When the UV release voltage (V_{UVREL}) is set to a voltage above the VR output voltage (V_{OUT}), the reset signal of Window VD is not released even if Window VD monitors the VR output voltage returns to the normal value after detecting the drop of VR. When the OV release voltage (V_{OVREL}) is set to a voltage under the VR output voltage (V_{OUT}), the reset signal of Window VD is not released even if Window VD monitors the VR output voltage returns to the normal value after detecting the rise of VR.

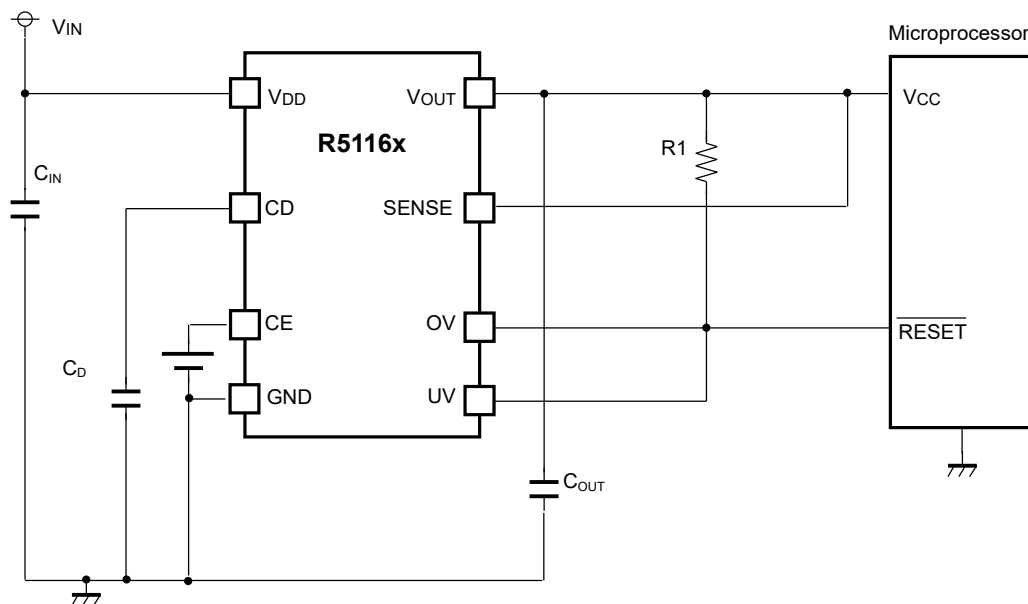
To prevent this issue, the following conditions are required between V_{OUT} and V_{UVREL} , and between V_{OUT} and V_{OVREL} .

$$(\text{VR Set Output Voltage}) \times 0.9875 - 15 \text{ mV}^* > (\text{UV Set Detector Threshold}) \times 1.0075 \times 1.007$$

$$(\text{OV Set Detector Threshold}) \times 0.9875 \times 0.993 > (\text{VR Set Output Voltage}) \times 1.0075 + 15 \text{ mV}^*$$

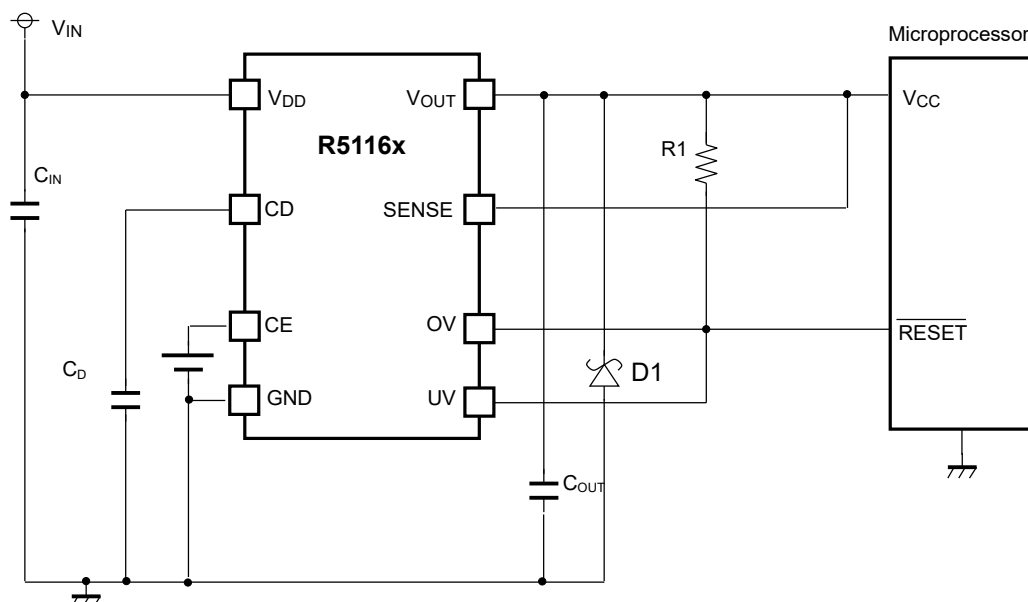
* 15mV is the worst value of load regulation

When using a device without the above conditions of V_{OUT} and V_{DET} , careful consideration must be given to the system operation before use.

APPLICATION INFORMATION**TYPICAL APPLICATIONS****R5116xxx TYPICAL APPLICATIONS****Recommended Components**

Symbol	Description
C _{IN}	Ceramic Capacitor, 0.1 μF or more, 50V Rated Voltage , CGA4J2X7R1H104K, TDK
C _{OUT}	Ceramic Capacitor, 10 μF or more, 50V Rated Voltage , CGA4J1X7R0J106K, TDK
C _D	A capacitor corresponding to setting of Release Output Delay Time
R1	A resistor covering the output current at Nch. driver ON and the leakage current at Nch. driver OFF. Refer to “Electrical Characteristic” providing the evaluation result with using a resistor of 100kΩ.

TYPICAL APPLICATION FOR IC CHIP BREAKDOWN PREVENTION



R5116xxx Typical Application for IC Chip Breakdown Prevention

When a sudden surge of electrical current travels along the VOUT pin and GND due to a short-circuit, electrical resonance of a circuit involving an output capacitor (C_{OUT}) and a short circuit inductor generates a negative voltage and may damage the device or the load devices. Connecting a schottky diode (D1) between the VOUT pin and GND has the effect of preventing damage to them.

TECHNICAL NOTES

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. A peripheral component or the device mounted on PCB should not exceed a rated voltage, a rated current or a rated power. When designing a peripheral circuit, please be fully aware of the following points.

Phase Compensation

Phase compensation is provided to secure stable operation even when the load current is varied by utilizing capacity of the output ceramic capacitor and Equivalent Series Resistance (ESR). For this purpose, be sure to use a capacitor with 10 μF or more (C_{OUT}) and wire it to the pin as short as possible.

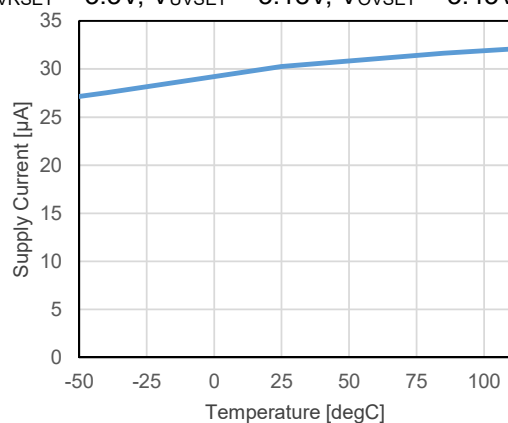
Evaluate the circuit with consideration of temperature and frequency characteristics, in case ESR value of the capacitor is large and the output is unstable. The capacitor with 0.1 μF or more (C_{IN}) connected in between VIN pin and GND pin must be wired the shortest.

TYPICAL CHARACTERISTICS

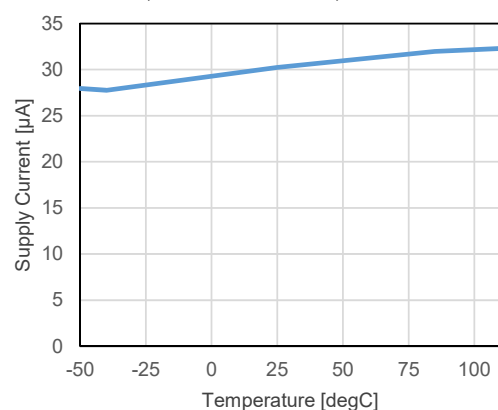
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Supply Current vs. Temperature ($V_{IN} = 14V$)

$V_{VRSET} = 3.3V$, $V_{UVSET} = 3.18V$, $V_{OVSET} = 3.43V$

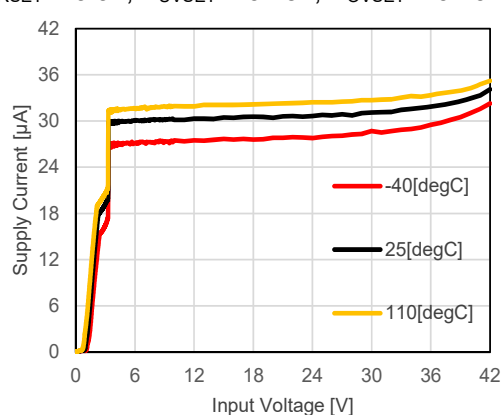


$V_{VRSET} = 5.0V$, $V_{UVSET} = 4.83V$, $V_{OVSET} = 5.17V$

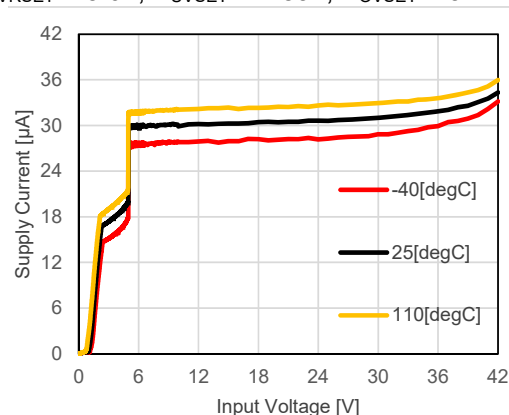


2) Supply Current vs. Input Voltage

$V_{VRSET} = 3.3V$, $V_{UVSET} = 3.18V$, $V_{OVSET} = 3.43V$

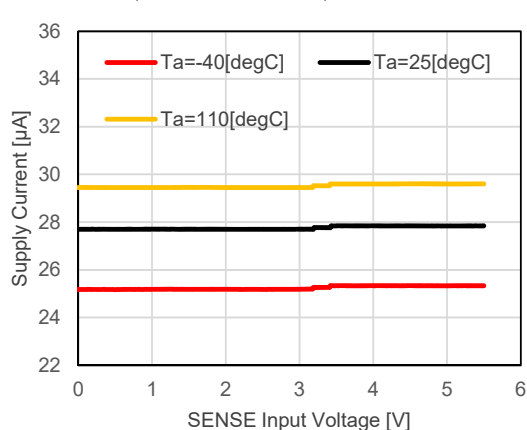


$V_{VRSET} = 5.0V$, $V_{UVSET} = 4.83V$, $V_{OVSET} = 5.17V$

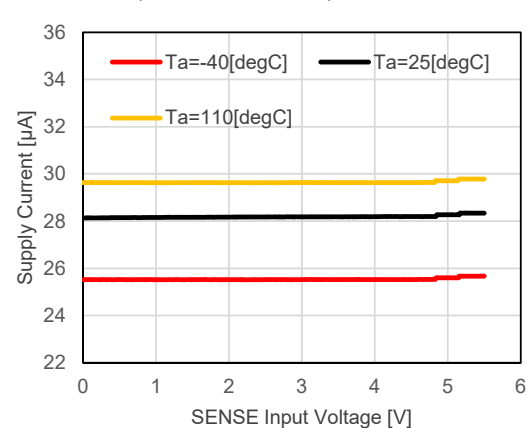


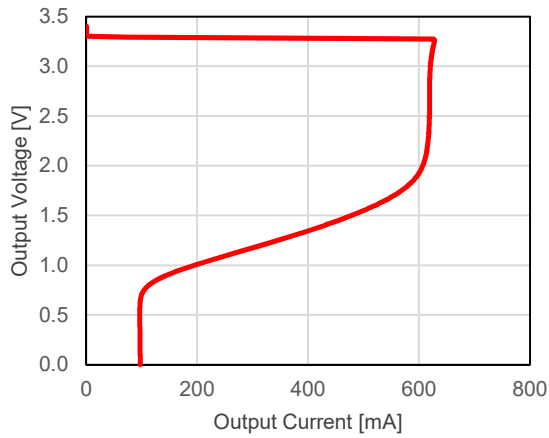
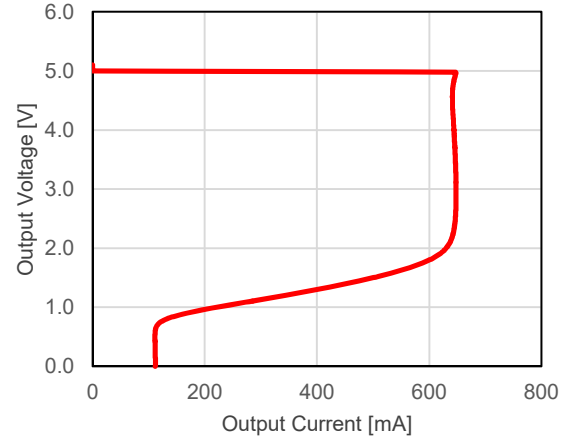
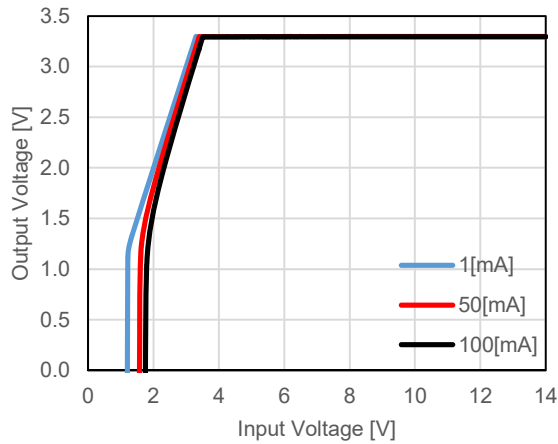
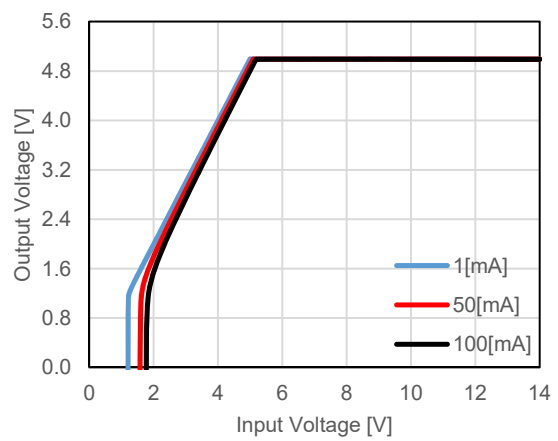
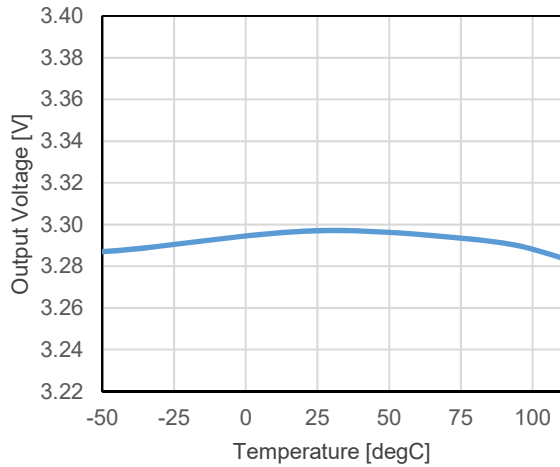
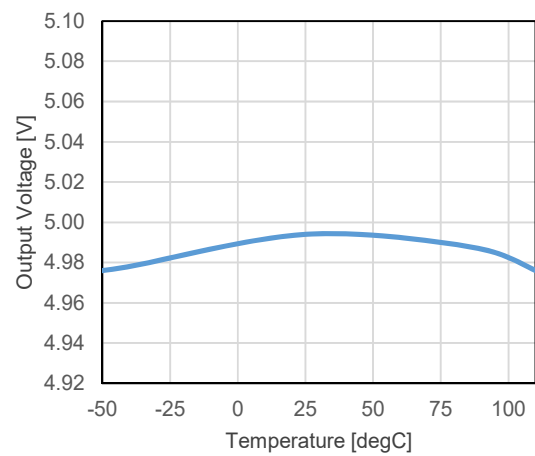
3) Supply Current vs. SENSE Voltage

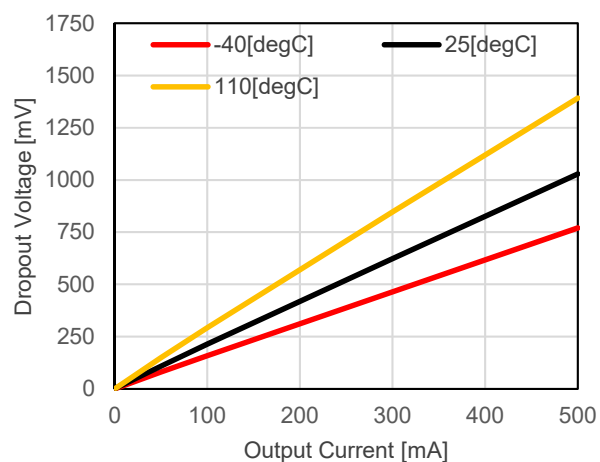
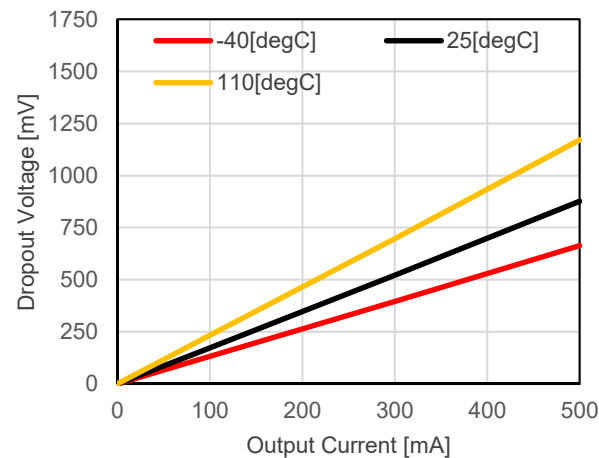
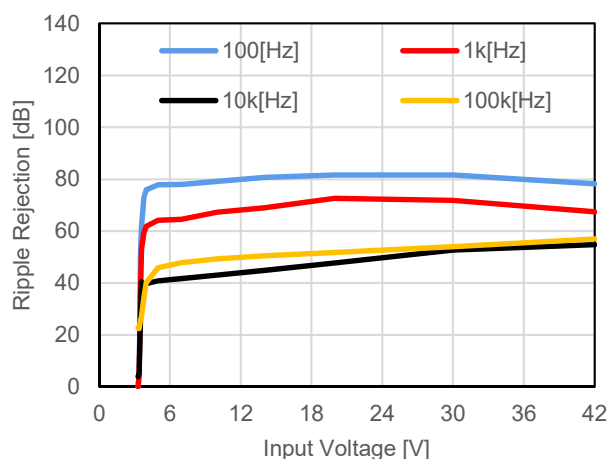
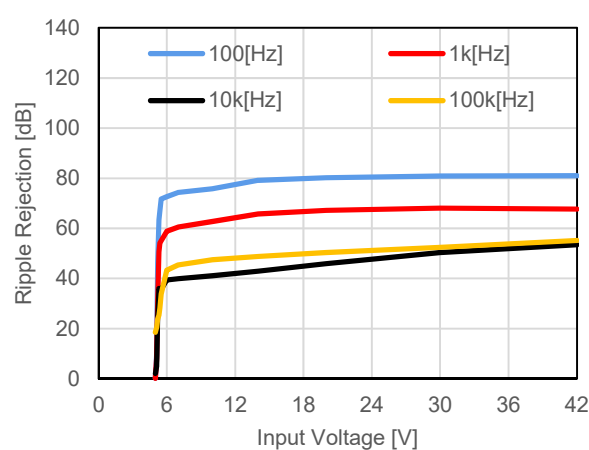
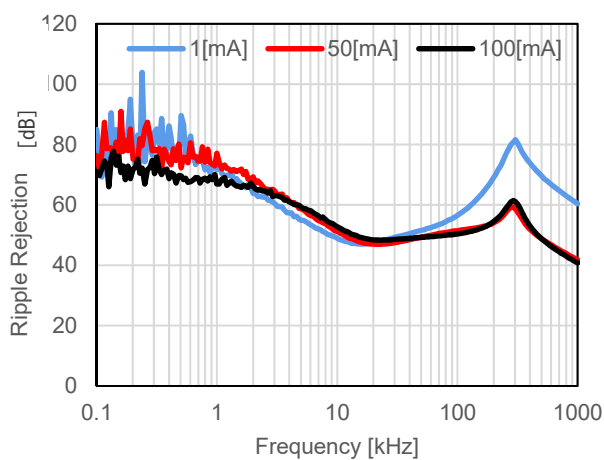
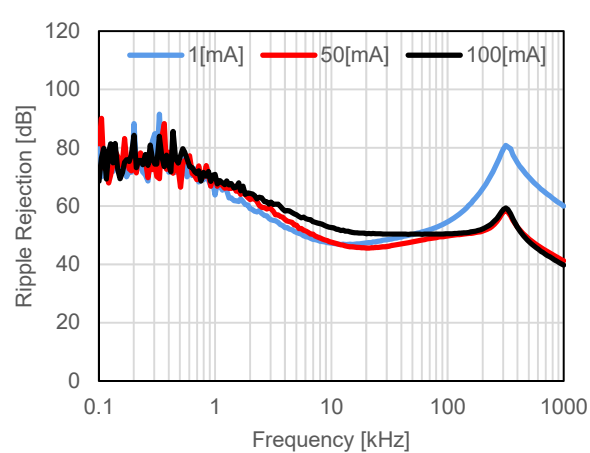
$V_{VRSET} = 3.3V$, $V_{UVSET} = 3.18V$, $V_{OVSET} = 3.43V$

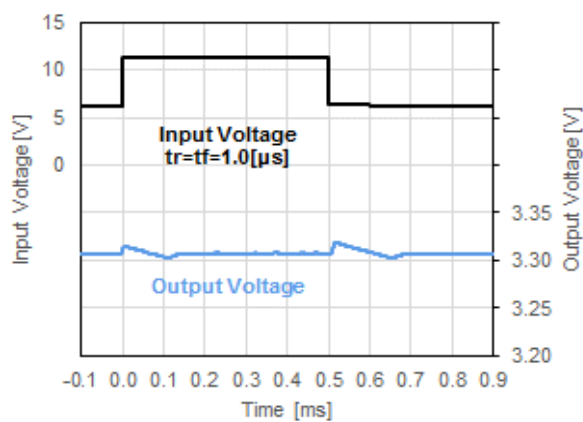
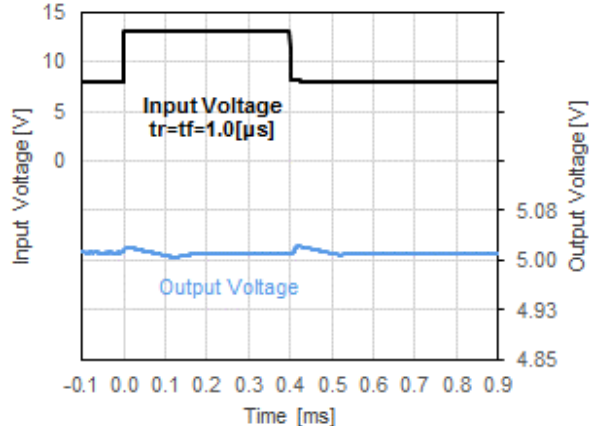
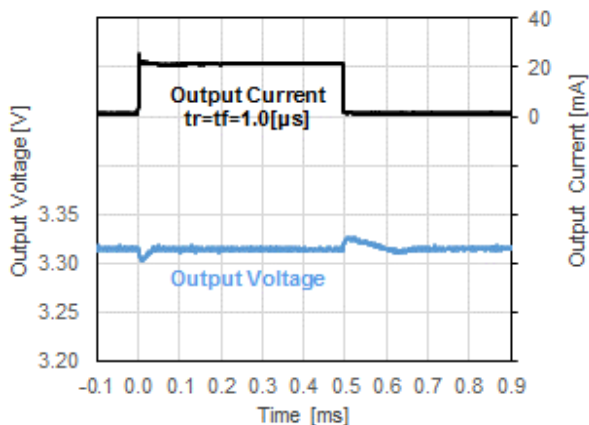
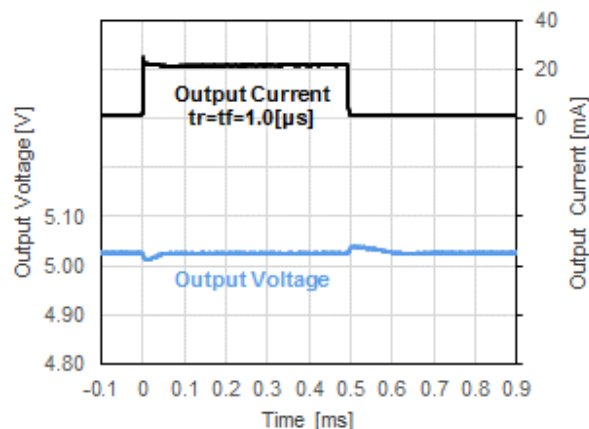
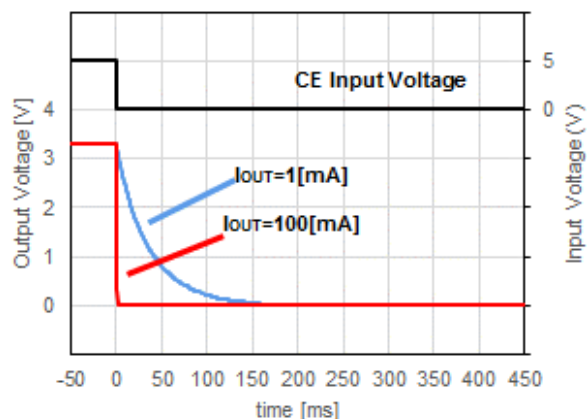
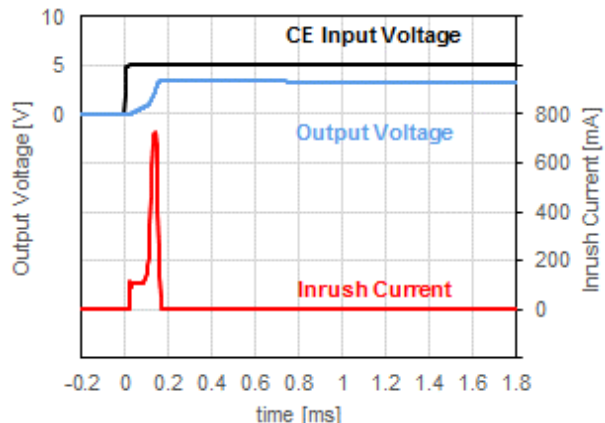


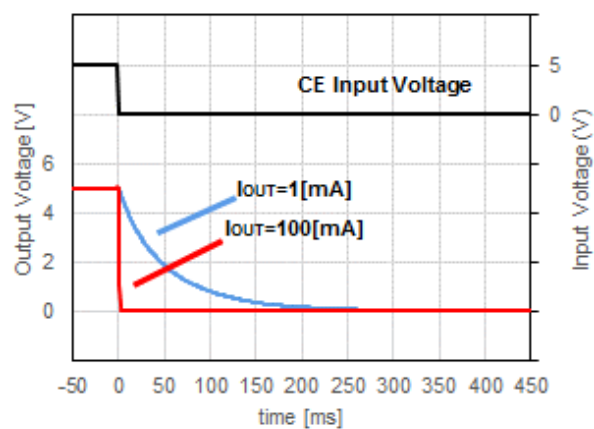
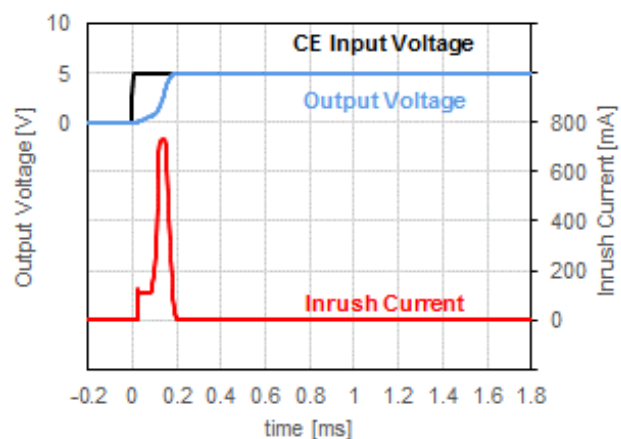
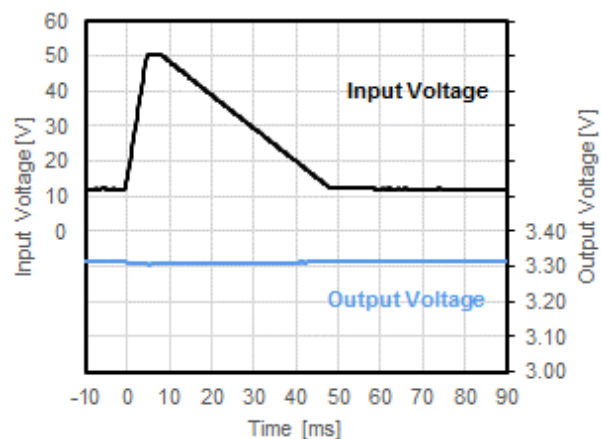
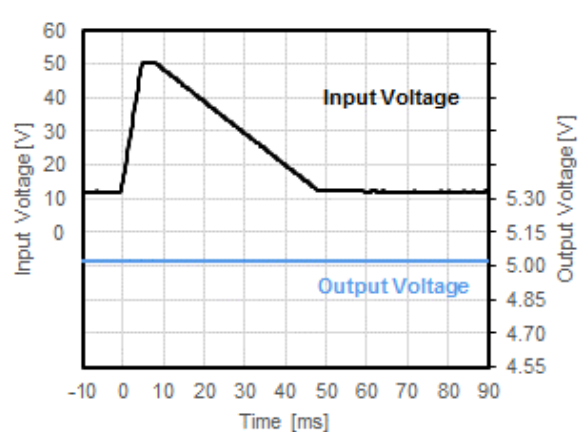
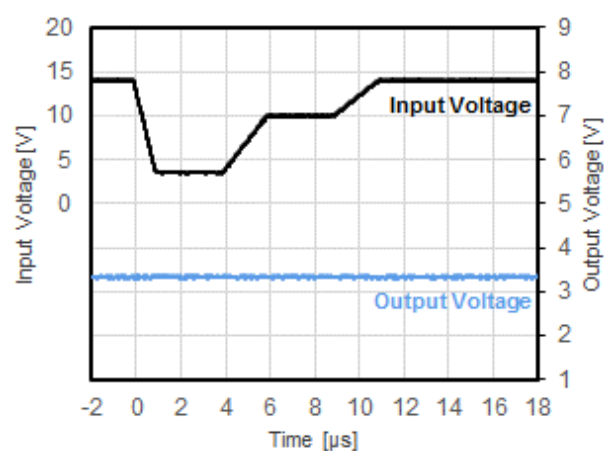
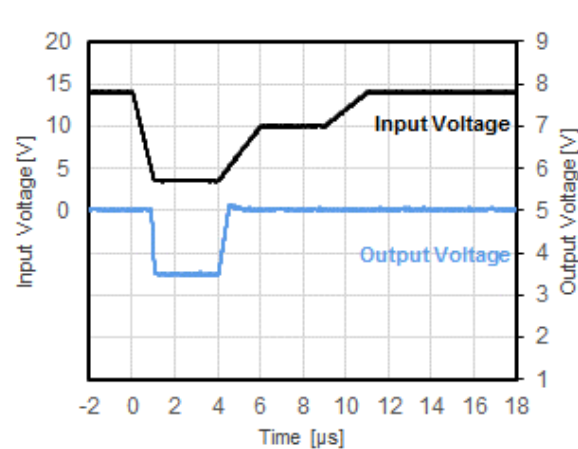
$V_{VRSET} = 5.0V$, $V_{UVSET} = 4.83V$, $V_{OVSET} = 5.17V$



4) Output Voltage vs. Output Current ($V_{IN} = V_{VRSET} + 3.0\text{ V}$, $T_a = 25\text{ }^{\circ}\text{C}$) $V_{VRSET} = 3.3\text{ V}$  $V_{VRSET} = 3.3\text{ V}$ **5) Output Voltage vs. Input Voltage ($T_a = 25\text{ }^{\circ}\text{C}$)** $V_{VRSET} = 3.3\text{ V}$  $V_{VRSET} = 5.0\text{ V}$ **6) Output Voltage vs. Temperature ($V_{IN} = 14\text{ V}$, $I_{OUT} = 1\text{ mA}$)** $V_{VRSET} = 3.3\text{ V}$  $V_{VRSET} = 3.3\text{ V}$ 

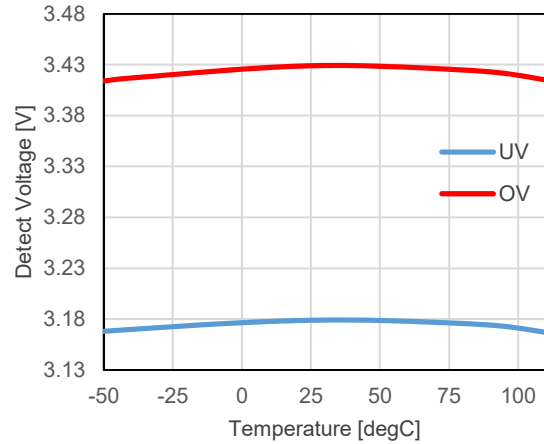
7) Dropout Voltage vs. Output Current $V_{VRSET} = 3.3V$  $V_{VRSET} = 5.0V$ **8) Ripple Rejection vs. Input Voltage ($T_a=25^\circ C$, $V_{ripple} = \pm 0.2V$)** $V_{VRSET} = 3.3V$  $V_{VRSET} = 5.0V$ **9) Ripple Rejection vs. Frequency ($T_a=25^\circ C$, $V_{IN} = 14V \pm 0.2V_{ripple}$)** $V_{VRSET} = 3.3V$  $V_{VRSET} = 5.0V$ 

10) Input Transient Response ($T_a=25^\circ\text{C}$, $V_{IN} = V_{VRSET} + 3.0\text{ V} \Leftrightarrow V_{VRSET} + 8.0\text{ V}$, $I_{OUT} = 1\text{ mA}$)
 $V_{VRSET} = 3.3\text{V}$

 $V_{VRSET} = 5.0\text{V}$

11) Load Transient Response ($T_a=25^\circ\text{C}$, $I_{OUT} = 1\text{ mA} \Leftrightarrow 20\text{mA}$, $V_{IN} = 14\text{V}$)
 $V_{VRSET} = 3.3\text{V}$

 $V_{VRSET} = 5.0\text{V}$

12) CE Transient Response ($T_a=25^\circ\text{C}$, $V_{IN} = 14\text{V}$, $I_{OUT} = 1\text{ mA}$)
 $V_{VRSET} = 3.3\text{V}$


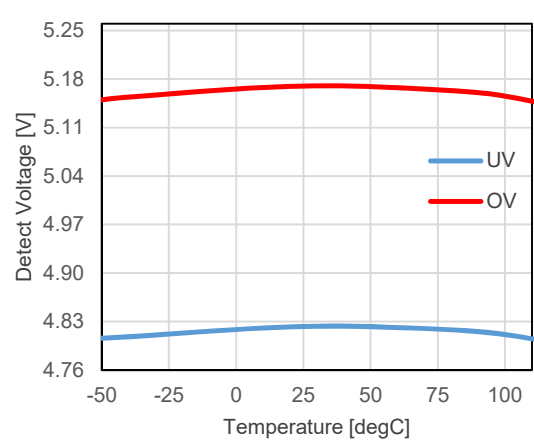
$V_{VRSET} = 5.0V$ **13) Load Dump ($T_a = 25^\circ C$, $I_{OUT} = 1 mA$)** $V_{VRSET} = 3.3V$  $V_{VRSET} = 5.0V$ **14) Cranking ($T_a = 25^\circ C$, $I_{OUT} = 1 mA$)** $V_{VRSET} = 3.3V$  $V_{VRSET} = 5.0V$ 

15) UV/OV Detection Voltage vs. Temperature

$V_{UVSET} = 3.18V$, $V_{OVSET} = 3.43V$

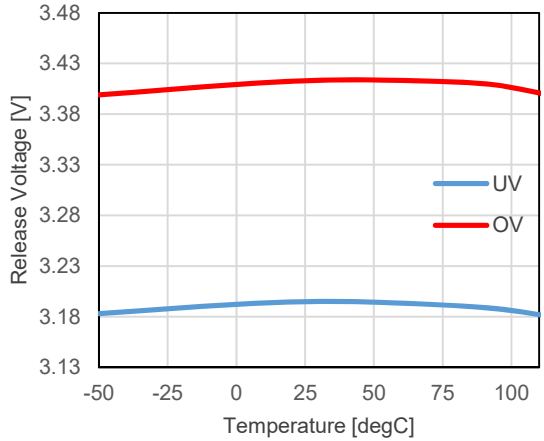


$V_{UVSET} = 4.83V$, $V_{OVSET} = 5.17V$

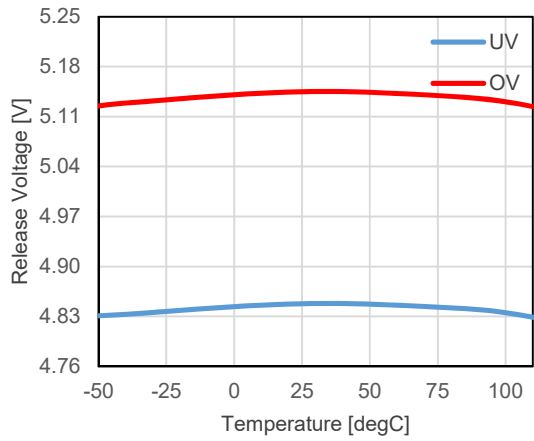


16) UV/OV Release Voltage vs. Temperature

$V_{UVSET} = 3.18V$, $V_{OVSET} = 3.43V$

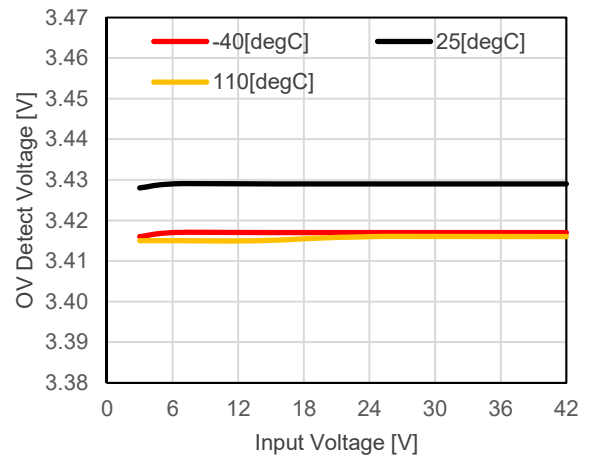
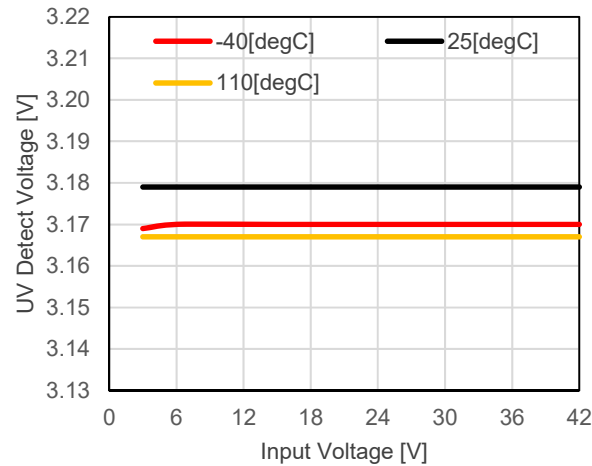


$V_{UVSET} = 4.83V$, $V_{OVSET} = 5.17V$

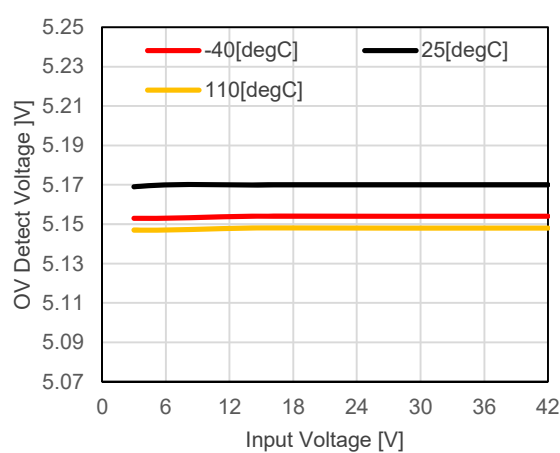
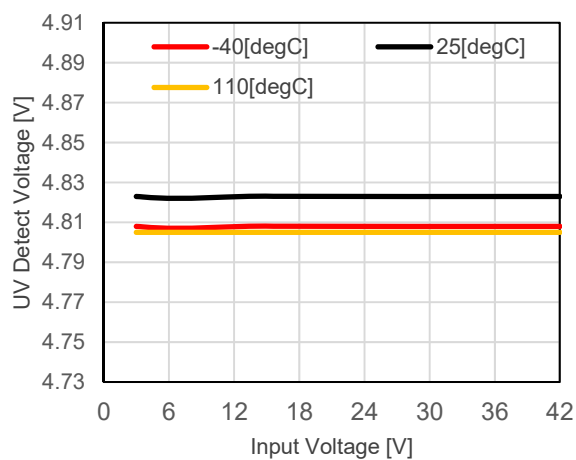


17) UV/OV Detection Voltage vs. Input Voltage

$V_{UVSET} = 3.18V$, $V_{OVSET} = 3.43V$

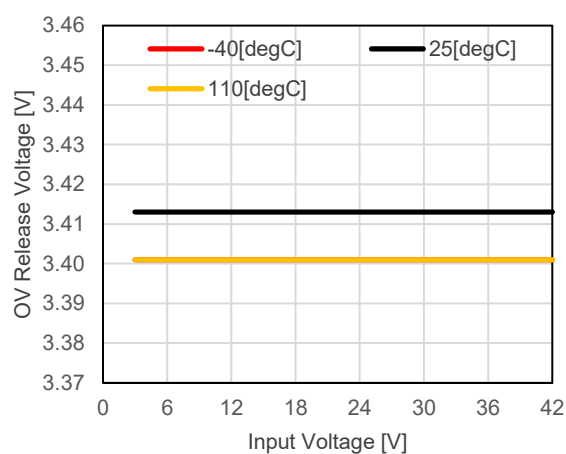
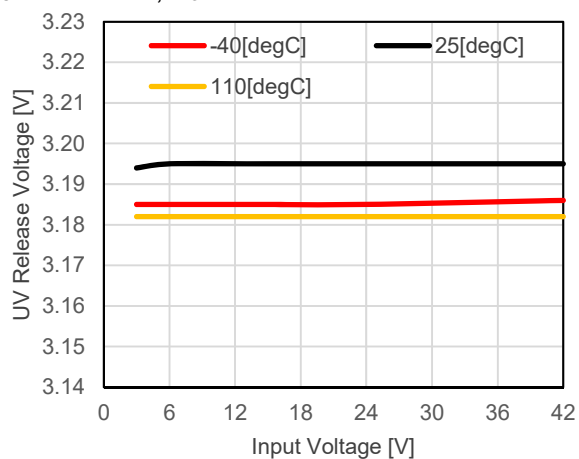


$V_{UVSET} = 4.83V$, $V_{OVSET} = 5.17V$

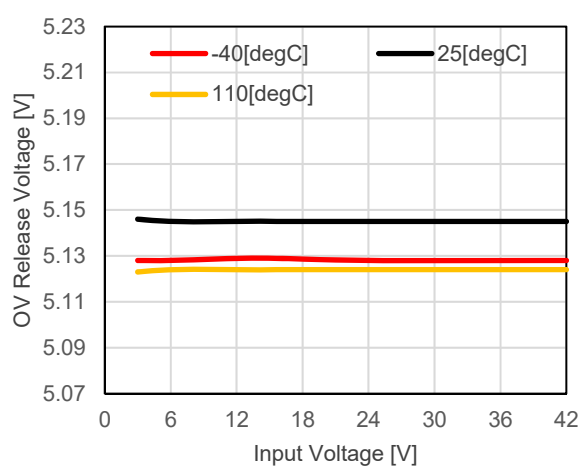
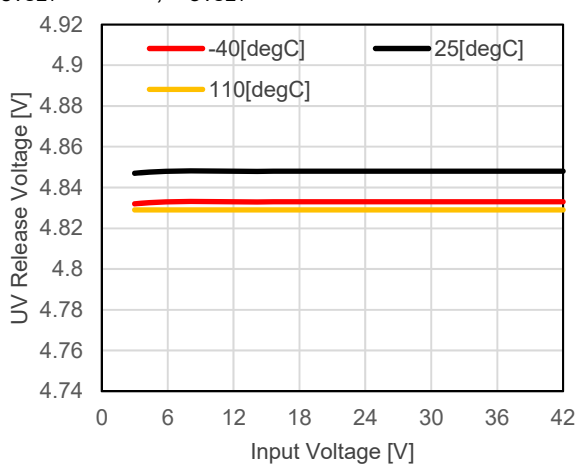


18) UV/OV Release Voltage vs. Input Voltage

$V_{UVSET} = 3.18V$, $V_{OVSET} = 3.43V$

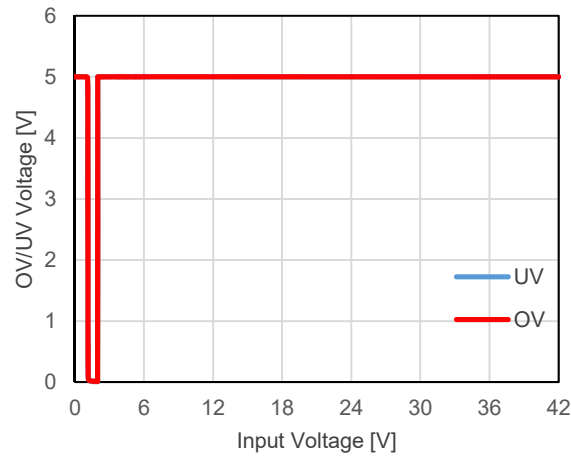


$V_{UVSET} = 4.83V$, $V_{OVSET} = 5.17V$

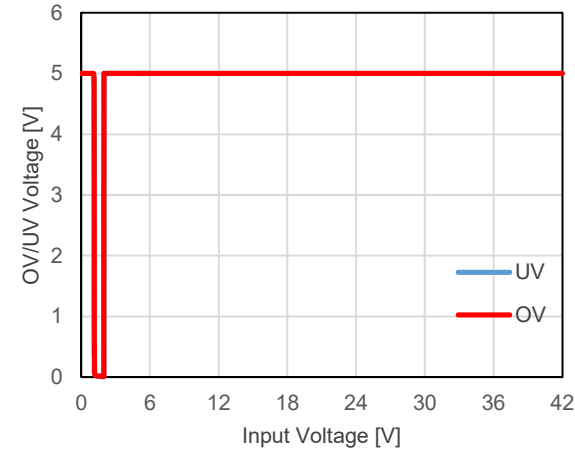


19) UV/OV Voltage vs. Input Voltage (Ta =25 °C)

V_{UVSET} = 3.18V, V_{OVSET} = 3.43V, Pull-up Voltage 5.0 V

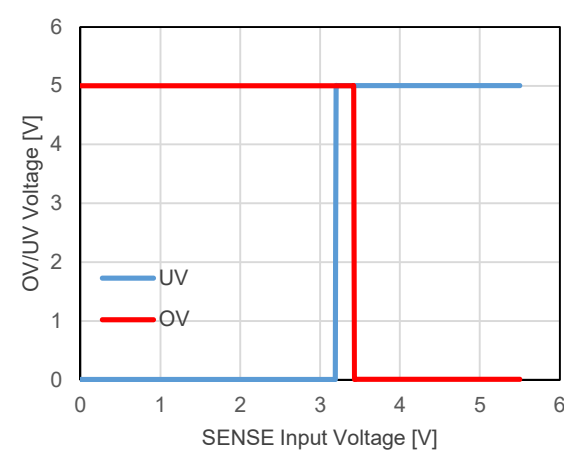


V_{UVSET} = 4.83V, V_{OVSET} = 5.17V, Pull-up Voltage 5.0 V

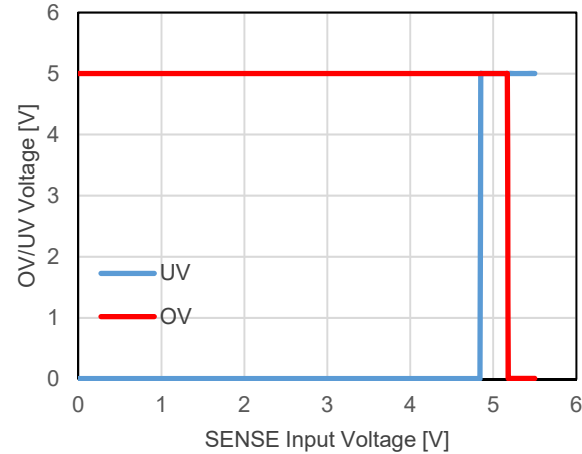


20) UV/OV Voltage vs. SENSE Voltage (Ta =25 °C)

V_{UVSET} = 3.18V, V_{OVSET} = 3.43V, Pull-up Voltage 5.0 V

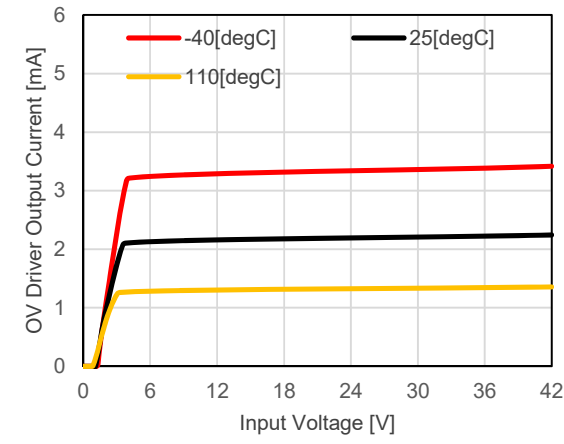
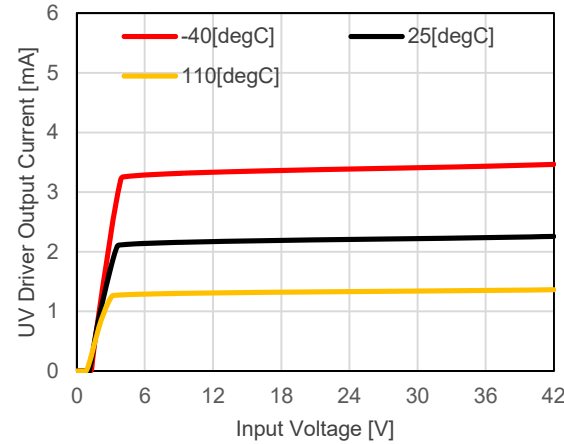


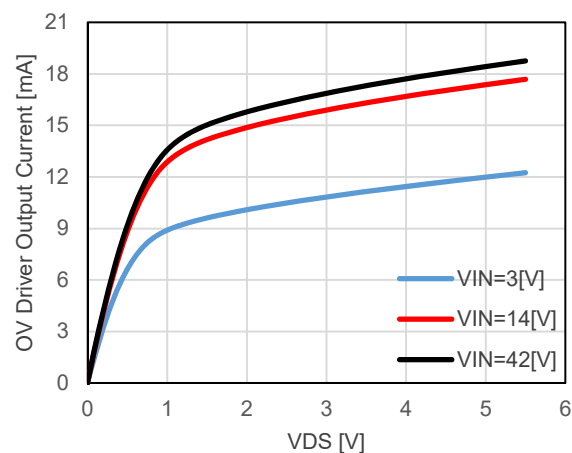
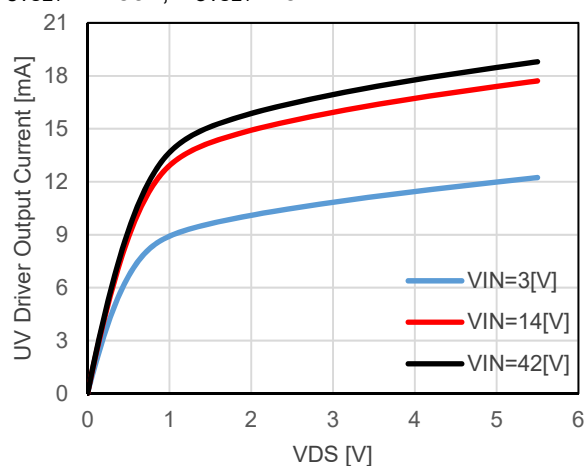
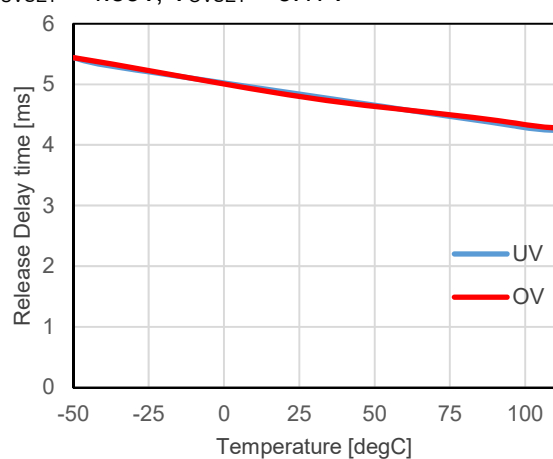
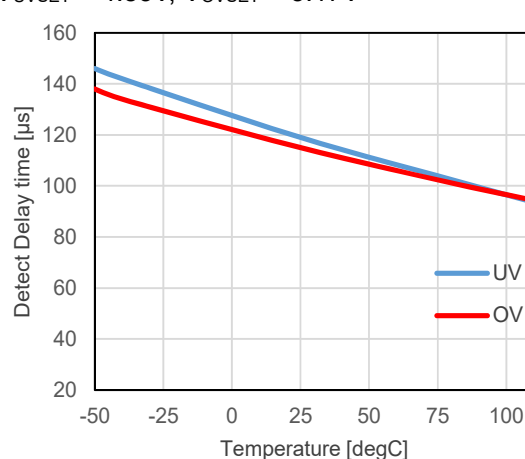
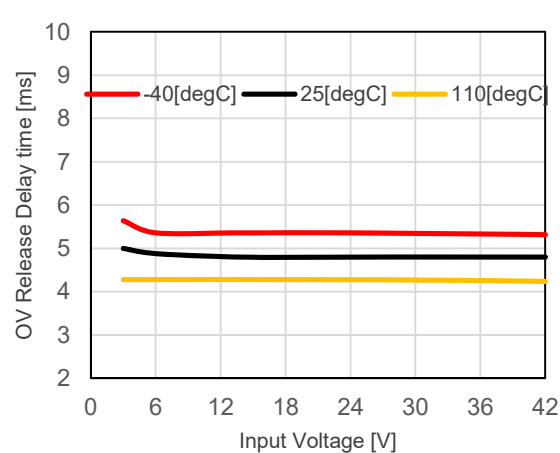
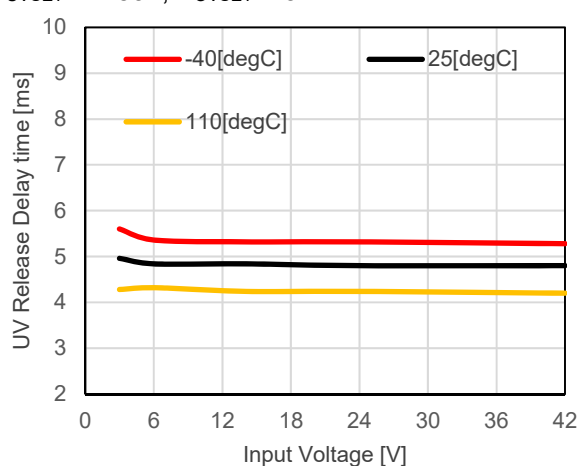
V_{UVSET} = 4.83V, V_{OVSET} = 5.17V, Pull-up Voltage 5.0 V



21) UV/OV Driver Output Current vs. Input Voltage

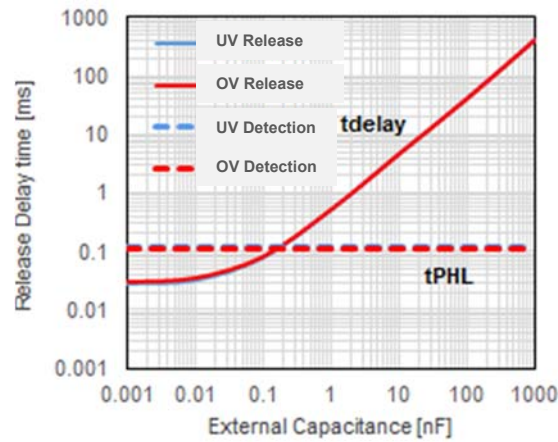
V_{UVSET} = 4.83V, V_{OVSET} = 5.17V



22) UV/OV Driver Output Current vs. V_{DS} ($T_a = 25^\circ\text{C}$) $V_{UVSET} = 4.83\text{V}$, $V_{OVSET} = 5.17\text{V}$ **23) Release Delay Time vs. Temperature** $V_{UVSET} = 4.83\text{V}$, $V_{OVSET} = 5.17\text{V}$ **24) Detection Delay Time vs. Temperature** $V_{UVSET} = 4.83\text{V}$, $V_{OVSET} = 5.17\text{V}$ **25) Release Delay Time vs. Input Voltage** $V_{UVSET} = 4.83\text{V}$, $V_{OVSET} = 5.17\text{V}$ 

26) Detection/Release Delay Time vs. External Capacitance for CD Pin (Ta =25 °C)

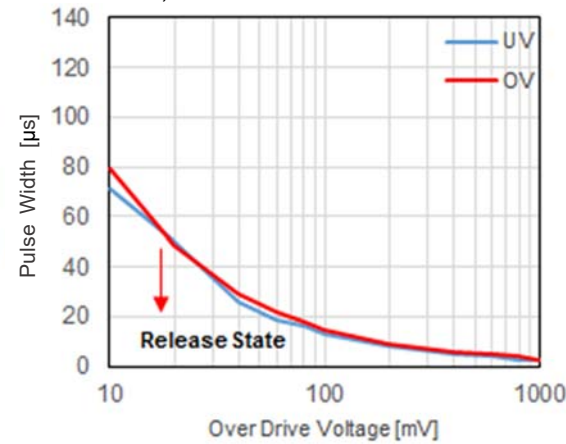
$V_{UVSET} = 4.83V$, $V_{OVSET} = 5.17V$



27) SENSE Pulse Width vs. SENSE Overdrive Voltage (Ta =25 °C)

Limit Pulse of Release State

$V_{UVSET} = 4.83V$, $V_{OVSET} = 5.17V$



The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.3 mm × 21 pcs

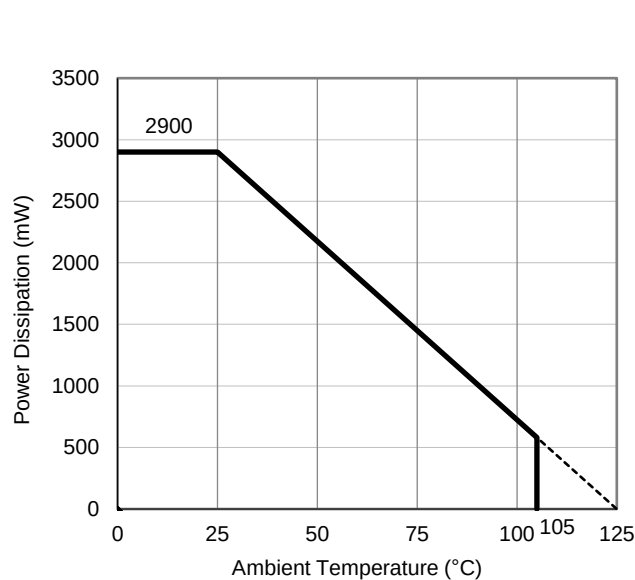
Measurement Result

(Ta = 25°C, Tjmax = 125°C)

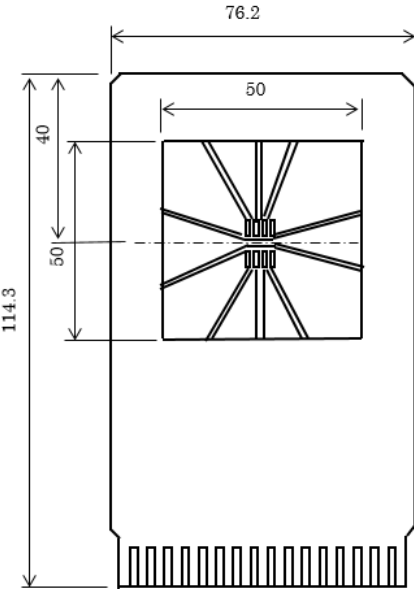
Item	Measurement Result
Power Dissipation	2900 mW
Thermal Resistance (θja)	θja = 34.5°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 10°C/W

θja: Junction-to–ambient thermal resistance.

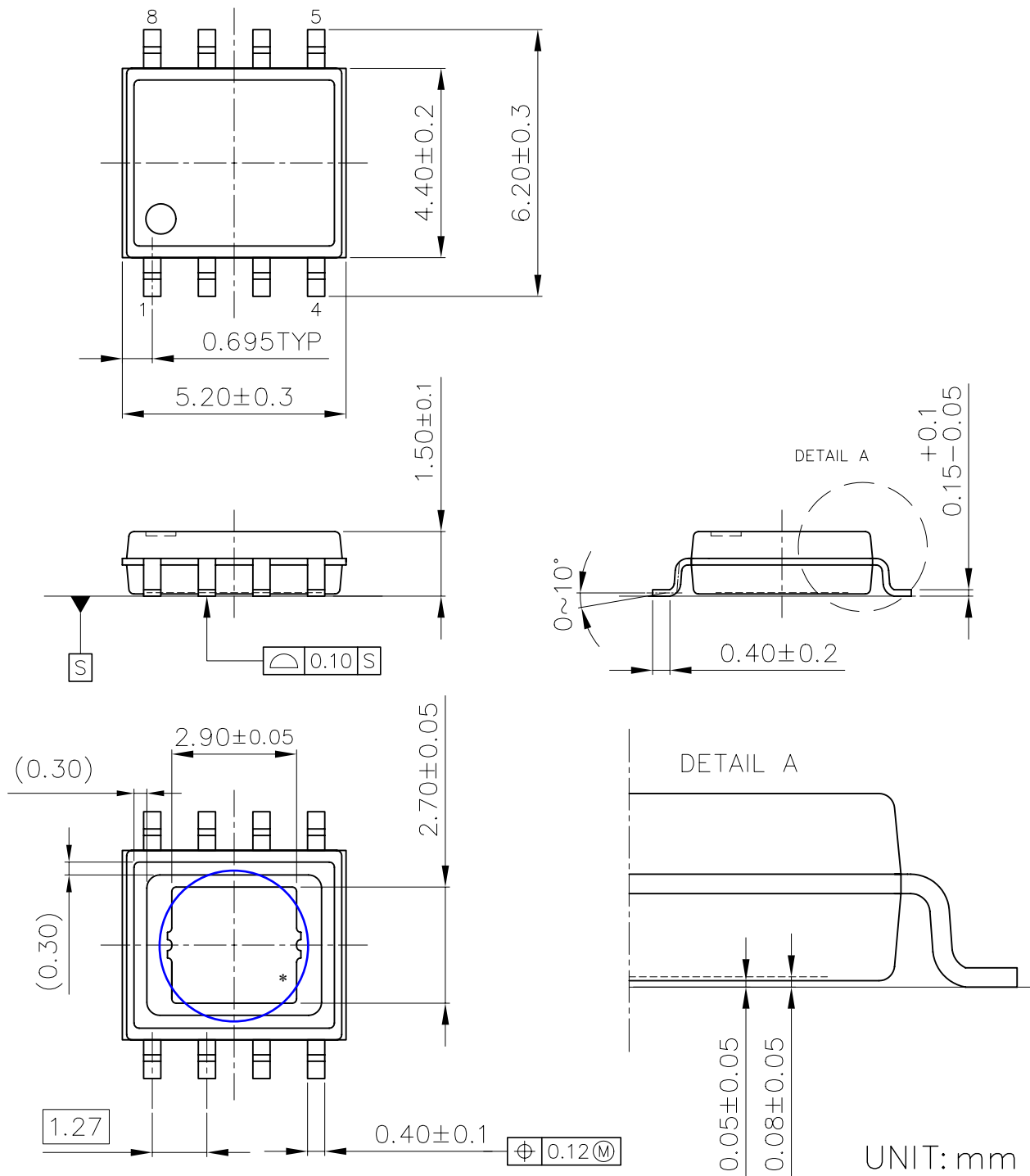
ψjt: Junction–to–top of package thermal characterization parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



HSOP-8E Package Dimensions

* The tab on the bottom of the package shown by blue circle is substrate potential (GND). It is recommended that this tab be connected to the ground plane on the board but it is possible to leave the tab floating.



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