



# **N-series Intel<sup>®</sup> Pentium<sup>®</sup> Processors and Intel<sup>®</sup> Celeron<sup>®</sup> Processors**

**Specification Update**

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*April 2015*

*Revision 001*



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# Revision History

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Revision	Description	Date
001	<ul style="list-style-type: none"><li>Initial Release.</li></ul>	April 2015

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# Preface

This document is an update to the specifications contained in the [Affected Documents](#) table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in [Nomenclature](#) are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

## Affected Documents

Document Title	Document Number
<i>N-series Intel® Pentium® Processors and Intel® Celeron® Processors Datasheet – Volume 1 of 3</i>	332092
<i>N-series Intel® Pentium® Processors and Intel® Celeron® Processors Datasheet – Volume 2 of 3</i>	332093
<i>N-series Intel® Pentium® Processors and Intel® Celeron® Processors Datasheet – Volume 3 of 3</i>	332094

## Related Documents

Document Title	Document Number/ Location
<i>AP-485, Intel® Processor Identification and the CPUID Instruction</i>	<a href="http://www.intel.com/design/processor/applnots/241618.htm">http://www.intel.com/design/processor/applnots/241618.htm</a>
<i>Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1: Basic Architecture</i> <i>Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A: Instruction Set Reference Manual A-M</i> <i>Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B: Instruction Set Reference Manual N-Z</i> <i>Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: System Programming Guide</i> <i>Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B: System Programming Guide</i> <i>Intel® 64 and IA-32 Intel Architecture Optimization Reference Manual</i>	<a href="http://www.intel.com/products/processor/manuals/index.htm">http://www.intel.com/products/processor/manuals/index.htm</a>
<i>Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes</i>	<a href="http://www.intel.com/content/www/us/en/processors/architectures-software-developer-manuals.html">http://www.intel.com/content/www/us/en/processors/architectures-software-developer-manuals.html</a>
<i>ACPI Specifications</i>	<a href="http://www.acpi.info">www.acpi.info</a>



## Nomenclature

**Errata** are design defects or errors. These may cause the processor behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**S-Spec Number** is a five-digit code used to identify products. Products are differentiated by their unique characteristics such as, core speed, L2 cache size, package type, etc. as described in the processor identification information table. Read all notes associated with each S-Spec number.

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

**Note:** Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, and so on).



# Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the processor. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations.

## Codes Used in Summary Tables

### Stepping

X: Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.

(No mark)  
or (Blank box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

### Page

(Page): Page location of item in this document.

### Status

Doc: Document change or update will be implemented.

Plan Fix: This erratum may be fixed in a future stepping of the product.

Fixed: This erratum has been previously fixed.

No Fix: There are no plans to fix this erratum.

### Row

Change bar to left of a table row indicates this erratum is either new or modified from the previous version of the document.

## Errata (Sheet 1 of 2)

Number	Steppings	Status	ERRATA
	C0		
CHP1	X	No Fix	The SoC May Not Detect a Battery Charger or May Fail to Connect to a USB Host
CHP2	X	No Fix	RGB666 Pixel Format Display Panel May Not Operate as Expected
CHP3	X	No Fix	LPDDR3 tINIT0 JEDEC* Duration May be Longer Than Specification Requirement
CHP4	X	No Fix	HDMI And DVI Displays May Flicker or Blank Out When Using Certain Pixel Frequencies
CHP5	X	No Fix	POPCNT Instruction May Take Longer to Execute Than Expected
CHP6	X	No Fix	LPSS UART Not Fully Compatible With 16550 UART
CHP7	X	No Fix	Accessing Undocumented Unimplemented MMIO Space May Cause a System Hang



## Errata (Sheet 2 of 2)

Number	Steppings	Status	ERRATA
	C0		
CHP8	X	No Fix	USB xHCI Controller May Not Re-Enter D3 State After a USB Wake Event
CHP9	X	No Fix	SoC PCIe* Gen 2 REFCLK Jitter Does Not Meet PCIe* Specification with SSC Enabled
CHP10	X	No Fix	SD Card / SDIO Controller PRESET_VALUE Does Not Change Transfer Frequency
CHP11	X	No Fix	Leakage Current on MIPI*-CSI Interface May Be Higher Than Specification
CHP12	X	No Fix	SATA Signal Voltage Level Violation
CHP13	X	No Fix	IA32_DEBUGCTL.FREEZE_PERFMON_ON_PMI is Incorrectly Cleared by SMI
CHP14	X	No Fix	Redirection of RSM to Probe Mode May Not Generate an LBR Record
CHP15	X	No Fix	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results
CHP16	X	No Fix	Reported Memory Type May Not Be Used to Access the VMCS and Referenced Data Structures
CHP17	X	No Fix	A Page Fault May Not be Generated When the PS bit is set to "1" in a PML4E or PDPTE
CHP18	X	No Fix	Some Performance Counter Overflows May Not be Logged in IA32_PERF_GLOBAL_STATUS When FREEZE_PERFMON_ON_PMI is Enabled
CHP19	X	No Fix	CS Limit Violations May Not be Detected After VM Entry
CHP20	X	No Fix	PEBS Record EventingIP Field May be Incorrect After CS.Base Change
CHP21	X	No Fix	MOVNTDQA From WC Memory May Pass Earlier Locked Instructions
CHP22	X	No Fix	Performance Monitor Instructions Retired Event May Not Count Consistently
CHP23	X	No Fix	LBR Stack And Performance Counter Freeze on PMI May Not Function Correctly
CHP24	X	No Fix	VM Exit May Set IA32_EFER.NXE When IA32_MISC_ENABLE Bit 34 is Set to 1
CHP25	X	No Fix	Machine Check Status Overflow Bit May Not be Set
CHP26	X	No Fix	LPDDR3 tINIT0 Duration May be Longer Than Specification Requirement
CHP27	X	No Fix	xHCI USB2.0 Split-Transactions Error Counter Reset Issue
CHP28	X	No Fix	SoC May Not Meet PCIe* Clock Jitter Specification
CHP29	X	No Fix	SATA Host Controller Does Not Pass Certain Compliance Tests
CHP30	X	No Fix	RTIT Trace May Contain FUP.FAR Packet With Incorrect Address
CHP31	X	No Fix	RTIT May Delay The PSB by One Packet
CHP32	X	No Fix	RTIT TraceStop Condition Detected During Buffer Overflow May Not Clear TraceActive
CHP33	X	No Fix	RTIT FUP.BuffOvf Packet May be Incorrectly Followed by a TIP Packet
CHP34	X	No Fix	RTIT CYC Packet Payload Values May be Off by 1 Cycle
CHP35	X	No Fix	First MTC Packet After RTIT Enable May be Incorrect





## Specification Changes

Number	SPECIFICATION CHANGES
	None for this revision of this specification update.

## Specification Clarifications

Number	SPECIFICATION CLARIFICATIONS
	None for this revision of this specification update.

## Documentation Changes

Number	DOCUMENTATION CHANGES
	None for this revision of this specification update.



# Identification Information

## Component Identification using Programming Interface

The processor stepping can be identified by the following register contents.

**Table 1. Processor Line Component Identification**

Reserved	Extended Family <sup>1</sup>	Extended Model <sup>2</sup>	Reserved	SoC Type <sup>3</sup>	Family Code	Model Number <sup>5</sup>	Stepping ID <sup>6</sup>
31:28	27:20	19:16	15:13	12	11:8	7:4	3:0
0000b	0000000b	0100b	000b	0b	0110b	1100b	0000b

**Notes:**

1. The Extended Family, Bits [27:20] are used in conjunction with the Family Code, specified in Bits[11:8], to indicate whether the processor belongs to the Intel386™, Intel486™, Pentium®, Pentium® 4, Intel® Core™ SoC family.
2. The Extended Model, bits [19:16] in conjunction with the Model Number, specified in bits [7:4], are used to identify the model of the SoC within the SoC family.
3. The SoC Type, specified in bits [13:12] indicates whether the SoC is an original OEM SoC, an OverDrive SoC, or a dual SoC (capable of being used in a dual SoC system).
4. The Family Code corresponds to bits [11:8] of the EDX register after RESET, bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
5. The Model Number corresponds to bits [7:4] of the EDX register after RESET, bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
6. The Stepping ID in bits [3:0] indicates the revision number of that model. See [Table 2](#) for the SoC stepping ID number in the CPUID information.

When EAX is initialized to a value of '1', the CPUID instruction returns the Extended Family, Extended Model, Processor Type, Family Code, Model Number and Stepping ID value in the EAX register. Note that the EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX and EDX registers after the CPUID instruction is executed with a 2 in the EAX register.

The processor can be identified by the following register contents.

**Table 2. Processor Identification by Register Contents**

Processor Line	Stepping	Vendor ID <sup>1</sup>	Host Device ID <sup>2</sup>	Processor Graphics Device ID <sup>3</sup>	Revision ID <sup>4</sup>
Intel® Pentium® processor Series and Intel® Celeron® processor Series	C-0	8086h	2280h	22B1h	8'h21

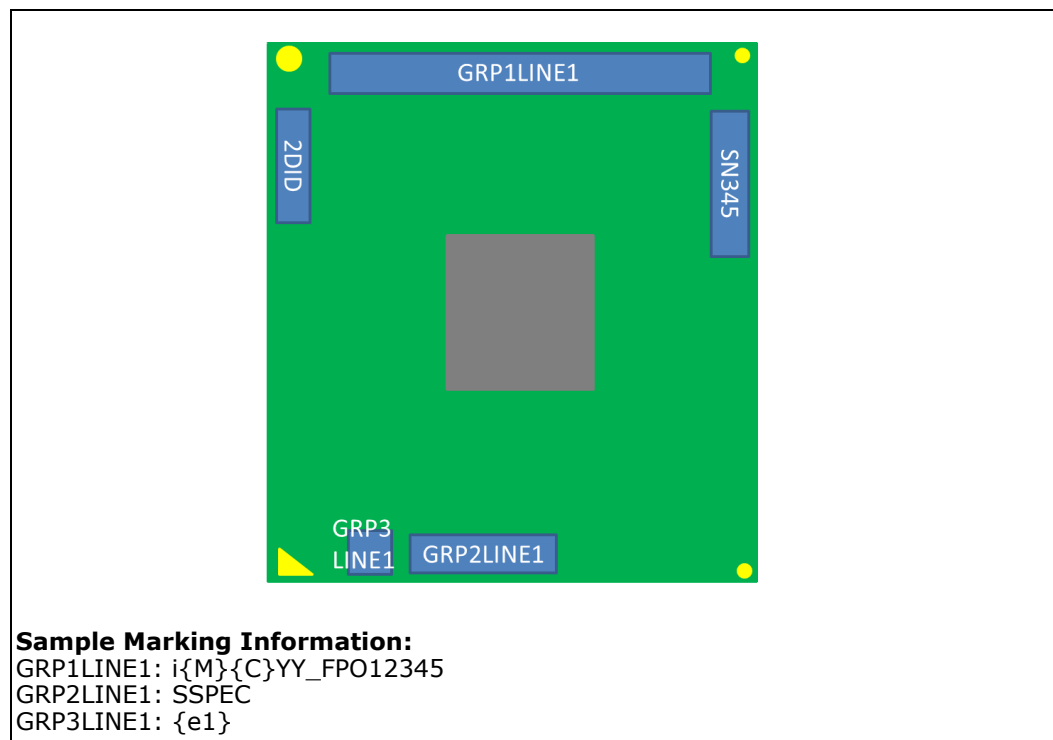
**Notes:**

1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00h–01h in the PCI function 0 configuration space.
2. The Host Device ID corresponds to bits 15:0 of the Device ID Register located at Device 0 offset 02h–03h in the PCI function 0 configuration space.
3. The Processor Graphics Device ID (DID2) corresponds to bits 15:0 of the Device ID Register located at Device 2 offset 02h–03h in the PCI function 0 configuration space.
4. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

## Component Marking Information

The processor stepping can be identified by the following component markings.

**Figure 1. Processor Family Top-Side Markings**



**Table 3. Processor Identification**

S-Spec #	MM Number	Processor #	Stepping	Cache Size (MB)	Functional Core	Graphic Freq. (MHz)	Graphic Burst Freq. (MHz)	Graphic Execution Units	Core Freq. (GHz)	Core Burst Freq. (GHz)	Mem. (MHz)	Therm. Design Power (W)
S-R29E	942599	Pentium® N3700	C0	2	4	400	700	16	1.6	2.4	1600	6
S-R2A7	943327 (Desktop sku)	Pentium® N3700	C0	2	4	400	700	16	1.6	2.4	1600	6
S-R29F	942600	Celeron® N3150	C0	2	4	320	640	12	1.6	2.08	1600	6
S-R2A8	943328 (Desktop sku)	Celeron® N3150	C0	2	4	320	640	12	1.6	2.08	1600	6
S-R29H	942602	Celeron® N3050	C0	2	2	320	600	12	1.6	2.16	1600	6
S-R2A9	943329 (Desktop sku)	Celeron® N3050	C0	2	2	320	600	12	1.6	2.16	1600	6
S-R29J	942603	Celeron® N3000	C0	2	2	320	600	12	1.04	2.08	1600	4

# Errata

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## **CHP1. The SoC May Not Detect a Battery Charger or May Fail to Connect to a USB Host**

**Problem:** During power-on, when the SoC is used in device mode instead of host mode, the USB D+ line may have a 2  $\mu$ sec glitch to 3.3 V.

**Implication:** Due to this erratum, the platform may not detect a battery charger (and hence not charge the battery) or the SoC may not successfully connect to an attached USB host.

**Workaround:** Power the SoC on before connecting to its USB port. Alternatively, manually disconnecting and re-connecting the USB cable restores operation after the erratum has occurred.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

## **CHP2. RGB666 Pixel Format Display Panel May Not Operate as Expected**

**Problem:** Due to this erratum, the RGB666 format support on the SOC has restrictions on the horizontal resolution. For single link MIPI\* DSI (Display Serial Interface), the horizontal resolution must be evenly divisible by 4. For dual link MIPI DSI, one-half the horizontal resolution plus the overlapping pixels must be evenly divisible by 4.

**Implication:** Due to this erratum, the RGB666 panel may not operate as expected.

**Workaround:** For dual link panels with overlap, choose the overlap so that one-half the horizontal resolution plus the overlapping pixels is evenly divisible by 4. For single link panels the horizontal resolution must be evenly divisible by 4

**Status:** For the steppings affected, see the *Summary Table of Changes*.

## **CHP3. LPDDR3 tINIT0 JEDEC\* Duration May be Longer Than Specification Requirement**

**Problem:** JEDEC Standard JESD209-3 requires a maximum power ramp duration tINIT0 of 20ms. Due to this erratum, the SoC may not comply with the tINIT0 specification.

**Implication:** Intel has not observed this erratum to impact the functionality or performance of any commercially available LPDDR3 parts. Intel has obtained waivers from vendors who provide commonly used LPDDR3 DRAM parts

**Workaround:** None identified.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

## **CHP4. HDMI And DVI Displays May Flicker or Blank Out When Using Certain Pixel Frequencies**

**Problem:** Due to this erratum, HDMI (High-Definition Multimedia Interface) and DVI (Digital Visual Interface) ports may send data out at an incorrect rate, that is different than the one requested when using certain pixel frequencies.

**Implication:** When this erratum occurs, panels may flicker or blank out. The impacted pixel frequencies are: 218.25MHz, 218.70MHz, 220.50MHz, 221.20MHz, 229.50MHz, 233.793MHz and 234.00MHz.

**Workaround:** Select a video mode that does not use an affected pixel frequency.

**Status:** For the steppings affected, see the *Summary Table of Changes*.



#### **CHP5. POPCNT Instruction May Take Longer to Execute Than Expected**

**Problem:** POPCNT instruction execution with a 32 or 64 bit operand may be delayed until previous non-dependent instructions have executed.

**Implication:** Software using the POPCNT instruction may experience lower performance than expected.

**Workaround:** None identified.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

#### **CHP6. LPSS UART Not Fully Compatible With 16550 UART**

**Problem:** Stick Parity bit, LCR[5], (Line Control Register, HSUART0\_BAR0, Offset 0CH; bit [5] for HSUART0 and HSUART1\_BAR0, Offset 0CH; bit [5] for HSUART1) does not follow the 16550 specified behavior, instead the parity bit is always logic 0.

**Implication:** LPSS (Low Power Sub-system) UARTs are not fully 16550 compatible and may cause an error when connected to a UART device that requires the Stick Parity feature.

**Workaround:** Do not use Stick Parity mode of UART.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

#### **CHP7. Accessing Undocumented Unimplemented MMIO Space May Cause a System Hang**

**Problem:** Access to undocumented unimplemented MMIO space should result in a software error. Due to this erratum, an access to undocumented unimplemented MMIO space may not complete.

**Implication:** When this erratum occurs, the system may hang.

**Workaround:** Do not access to undocumented unimplemented MMIO space.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

#### **CHP8. USB xHCI Controller May Not Re-Enter D3 State After a USB Wake Event**

**Problem:** After processing a USB wake event, the USB xHCI controller may not reenter D3 state.

**Implication:** When this erratum occurs, the affected USB xHCI controller may not recognize subsequent USB wake events. When this erratum occurs, PME status bit [15] of register Power Management Control/Status (PM\_CS) (Bus 0; Device 20; Function 20; Offset 74H) remains at 1.

**Workaround:** The software driver should set PMCTRL[28] (Bus 0; Device 14; Function 0; Offset 80A4H) after the xHCI controller enters D0 state following an exit from D3 state.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

#### **CHP9. SoC PCIe\* Gen 2 REFCLK Jitter Does Not Meet PCIe\* Specification with SSC Enabled**

**Problem:** SoC PCIe\* REFCLK does not meet PCIe\* jitter specification when SSC is enabled.

**Implication:** This issue only impacts PCIe\* interface when it is running at Gen 2 speed when SSC is enabled. No impact to PCIe\* Gen 1 operation. Intel has not observed any functional failures due to this erratum.

**Workaround:** There are no known issues with enabling SSC on PCIe interface that operates at Gen 1 speed. However, if SSC is enabled while PCIe\* interface is running at Gen 2 speed, system REFCLK will experience jitter would not meet PCIe specifications.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

### **CHP10. SD Card / SDIO Controller PRESET\_VALUE Does Not Change Transfer Frequency**

**Problem:** The PRESET\_VALUE (CMD12\_ERR\_STAT\_HOST\_CTRL\_2 CSR at Bus 0; Device 18; Function 0; Offset 3CH, bit 31) does not change the SD Card/ SDIO bus transfer frequency as required by the SD Host Controller Standard Specification Version 3.0.

**Implication:** Drivers that attempt to utilize PRESET\_VALUE may not obtain the maximum transfer rate of an attached UHS SD card or SDIO bus.

**Workaround:** Software should set the UHS\_MODE field (bits [18:16] of the CMD12\_ERR\_STAT\_HOST\_CTRL\_2 CSR) before setting the PRESET\_VALUE bit to reach the maximum transfer rate.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

### **CHP11. Leakage Current on MIPI\*-CSI Interface May Be Higher Than Specification**

**Problem:** The leakage current on the MIPI-CSI interface may exceed the specified limit of  $\pm 10\mu\text{A}$ .

**Implication:** Intel has not observed any functional or reliability failures due to this erratum.

**Workaround:** None identified.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

### **CHP12. SATA Signal Voltage Level Violation**

**Problem:** SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the SATA transmit signaling voltage levels may exceed the maximum motherboard Tx connectors and device RX connector voltage specifications as defined in Section 7.2.2.3 of Serial ATA specification, Rev3.1. This issue applies to Gen1 (1.5Gb/s).

**Implication:** None known.

**Workaround:** None identified.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

### **CHP13. IA32\_DEBUGCTL.FREEZE\_PERFMON\_ON\_PMI is Incorrectly Cleared by SMI**

**Problem:** FREEZE\_PERFMON\_ON\_PMI (bit 12) in the IA32\_DEBUGCTL MSR (1D9H) is erroneously cleared during delivery of an SMI (system-management interrupt).

**Implication:** As a result of this erratum the performance monitoring counters will continue to count after a PMI occurs in SMM (system-management Mode).

**Workaround:** None identified.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

### **CHP14. Redirection of RSM to Probe Mode May Not Generate an LBR Record**

**Problem:** A redirection of the RSM instruction to probe mode may not generate the LBR (Last Branch Record) record that would have been generated by a non-redirected RSM instruction.

**Implication:** The LBR stack may be missing a record when redirection of RSM to probe mode is used. The LBR stack will still properly describe the code flow of non-SMM code.

**Workaround:** None identified.

**Status:** For the steppings affected, see the *Summary Table of Changes*.



### **CHP15. Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results**

- Problem:** The act of one processor or system bus master writing data into a currently executing code segment of a second processor with the intent of having the second processor execute that data as code is called cross-modifying code (XMC). XMC that does not force the second processor to execute a synchronizing instruction prior to execution of the new code is called unsynchronized XMC. Software using unsynchronized XMC to modify the instruction byte stream of a processor can see unexpected or unpredictable execution behavior from the processor that is executing the modified code.
- Implication:** In this case the phrase "unexpected or unpredictable execution behavior" encompasses the generation of most of the exceptions listed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide including a General Protection Fault (GPF) or other unexpected behaviors. In the event that unpredictable execution causes a GPF the application executing the unsynchronized XMC operation would be terminated by the operating system.
- Workaround:** In order to avoid this erratum programmers should use the XMC synchronization algorithm as detailed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide Section: Handling Self- and Cross-Modifying Code.
- Status:** For the steppings affected, see the *Summary Table of Changes*.

### **CHP16. Reported Memory Type May Not Be Used to Access the VMCS and Referenced Data Structures**

- Problem:** Bits 53:50 of the IA32\_VMX\_BASIC MSR report the memory type that the processor uses to access the VMCS and data structures referenced by pointers in the VMCS. Due to this erratum, a VMX access to the VMCS or referenced data structures will instead use the memory type that the MTRRs (memory-type range registers) specify for the physical address of the access.
- Implication:** Bits 53:50 of the IA32\_VMX\_BASIC MSR report that the WB (write-back) memory type will be used but the processor may use a different memory type.
- Workaround:** Software should ensure that the VMCS and referenced data structures are located at physical addresses that are mapped to WB memory type by the MTRRs.
- Status:** For the steppings affected, see the *Summary Table of Changes*.

### **CHP17. A Page Fault May Not be Generated When the PS bit is set to "1" in a PML4E or PDPTE**

- Problem:** On processors supporting Intel® 64 architecture the PS bit (Page Size bit 7) is reserved in PML4Es and PDPTEs. If the translation of the linear address of a memory access encounters a PML4E or a PDPTE with PS set to 1 a page fault should occur. Due to this erratum, PS of such an entry is ignored and no page fault will occur due to its being set.
- Implication:** Software may not operate properly if it relies on the processor to deliver page faults when reserved bits are set in paging-structure entries.
- Workaround:** Software should not set bit 7 in any PML4E or PDPTE that has Present Bit (Bit 0) set to "1".
- Status:** For the steppings affected, see the *Summary Table of Changes*.

### **CHP18. Some Performance Counter Overflows May Not be Logged in IA32\_PERF\_GLOBAL\_STATUS When FREEZE\_PERFMON\_ON\_PMI is Enabled**

- Problem:** When enabled, FREEZE\_PERFMON\_ON\_PMI bit 12 in IA32\_DEBUGCTL MSR (1D9H) freezes PMCs (performance monitoring counters) on a PMI (Performance Monitoring Interrupt) request by clearing the IA32\_PERF\_GLOBAL\_CTRL MSR (38FH). Due to this erratum, when FREEZE\_PERFMON\_ON\_PMI is enabled and two or more PMCs overflow within a small window of time and PMI is requested, then subsequent PMC overflows may not be logged in IA32\_PERF\_GLOBAL\_STATUS MSR (38EH).
- Implication:** On a PMI, subsequent PMC overflows may not be logged in IA32\_PERF\_GLOBAL\_STATUS MSR.
- Workaround:** Re-enabling the PMCs in IA32\_PERF\_GLOBAL\_CTRL will log the overflows that were not previously logged in IA32\_PERF\_GLOBAL\_STATUS.
- Status:** For the steppings affected, see the *Summary Table of Changes*.

### **CHP19. CS Limit Violations May Not be Detected After VM Entry**

- Problem:** The processor may fail to detect a CS limit violation on fetching the first instruction after VM entry if the first byte of that instruction is outside the CS limit but the last byte of the instruction is inside the limit.
- Implication:** The processor may erroneously execute an instruction that should have caused a general protection exception.
- Workaround:** When a VMM emulates a branch instruction it should inject a general protection exception if the instruction's target EIP is beyond the CS limit.
- Status:** For the steppings affected, see the *Summary Table of Changes*.

### **CHP20. PEBS Record EventingIP Field May be Incorrect After CS.Base Change**

- Problem:** Due to this erratum a PEBS (Precise Event Base Sampling) record generated after an operation which changes CS.Base may contain an incorrect address in the EventingIP field.
- Implication:** Software attempting to identify the instruction which caused the PEBS event may identify the incorrect instruction when non-zero CS.Base is supported and CS.Base is changed. Intel has not observed this erratum to impact the operation of any commercially available system.
- Workaround:** None identified.
- Status:** For the steppings affected, see the *Summary Table of Changes*.

### **CHP21. MOVNTDQA From WC Memory May Pass Earlier Locked Instructions**

- Problem:** An execution of MOVNTDQA that loads from WC (write combining) memory may appear to pass an earlier locked instruction to a different cache line.
- Implication:** Software that expects a lock to fence subsequent MOVNTDQA instructions may not operate properly. If the software does not rely on locked instructions to fence the subsequent execution of MOVNTDQA then this erratum does not apply.
- Workaround:** Software that requires a locked instruction to fence subsequent executions of MOVNTDQA should insert an LFENCE instruction before the first execution of MOVNTDQA following the locked instruction. If there is already a fencing or serializing instruction between the locked instruction and the MOVNTDQA, then an additional LFENCE is not necessary.
- Status:** For the steppings affected, see the *Summary Table of Changes*.





## **CHP22. Performance Monitor Instructions Retired Event May Not Count Consistently**

**Problem:** Performance Monitor Instructions Retired (Event C0H; Umask 00H) and the instruction retired fixed counter (IA32\_FIXED\_CTR0 MSR (309H)) are used to track the number of instructions retired. Due to this erratum, certain situations may cause the counter(s) to increment when no instruction has retired or to not increment when specific instructions have retired.

**Implication:** A performance counter counting instructions retired may over or under count. The count may not be consistent between multiple executions of the same code.

**Workaround:** None identified.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

## **CHP23. LBR Stack And Performance Counter Freeze on PMI May Not Function Correctly**

**Problem:** When FREEZE\_LBRS\_ON\_PMI flag (bit 11) in IA32\_DEBUGCTL MSR (1D9H) is set, the LBR (Last Branch Record) stack is frozen on a hardware PMI (Performance Monitoring Interrupt) request. When FREEZE\_PERFMON\_ON\_PMI flag (bit 12) in IA32\_DEBUGCTL MSR is set, a PMI request clears each of the ENABLE fields of the IA32\_PERF\_GLOBAL\_CTRL MSR (38FH) to disable counters. Due to this erratum, when FREEZE\_LBRS\_ON\_PMI and/or FREEZE\_PERFMON\_ON\_PMI is set in IA32\_DEBUGCTL MSR and the local APIC is disabled or the PMI LVT is masked, the LBR Stack and/or Performance Counters Freeze on PMI may not function correctly.

**Implication:** Performance monitoring software may not function properly if the LBR Stack and Performance Counters Freeze on PMI do not operate as expected. Intel has not observed this erratum to impact any commercially available system.

**Workaround:** None identified.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

## **CHP24. VM Exit May Set IA32\_EFER.NXE When IA32\_MISC\_ENABLE Bit 34 is Set to 1**

**Problem:** When "XD Bit Disable" in the IA32\_MISC\_ENABLE MSR (1A0H) bit 34 is set to 1, it should not be possible to enable the "execute disable" feature by setting IA32\_EFER.NXE. Due to this erratum, a VM exit that occurs with the 1-setting of the "load IA32\_EFER" VM-exit control may set IA32\_EFER.NXE even if IA32\_MISC\_ENABLE bit 34 is set to 1. This erratum can occur only if IA32\_MISC\_ENABLE bit 34 was set by guest software in VMX non-root operation.

**Implication:** Software in VMX root operation may execute with the "execute disable" feature enabled despite the fact that the feature should be disabled by the IA32\_MISC\_ENABLE MSR. Intel has not observed this erratum with any commercially available software.

**Workaround:** A virtual-machine monitor should not allow guest software to write to the IA32\_MISC\_ENABLE MSR.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

## **CHP25. Machine Check Status Overflow Bit May Not be Set**

**Problem:** The OVER (error overflow) indication in bit [62] of the IA32\_MC0\_STATUS MSR (401H) may not be set if IA32\_MC0\_STATUS.MCACOD (bits [15:0]) held a value of 0x3 (External Error) when a second machine check occurred in the MC0 bank. Additionally, the OVER indication may not be set if the second machine check has an MCACOD value of 0x810, 0x820 or 0x410, regardless of the first error.

**Implication:** Software may not be notified that an overflow of MC0 bank occurred.

**Workaround:** None identified.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

## **CHP26. LPDDR3 tINIT0 Duration May be Longer Than Specification Requirement**

**Problem:** JEDEC Standard JESD209-3 requires a maximum power ramp duration tINIT0 of 20ms. Due to this erratum, the SoC may not comply with the tINIT0 specification.

**Implication:** Intel has not observed this erratum to impact the functionality or performance of any commercially available LPDDR3 parts. Intel has obtained waivers from vendors who provide commonly used LPDDR3 DRAM parts.

**Workaround:** None identified.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

## **CHP27. xHCI USB2.0 Split-Transactions Error Counter Reset Issue**

**Problem:** The xHCI controller may not reset its split transaction error counter if a high-speed USB hub propagates a mal-formed bit from a low-speed or full-speed USB device exhibiting non-USB specification compliant signal quality.

**Implication:** The implication is device dependent.

- Full Speed and Low Speed devices behind the hub may be re-enumerated and may cause a device to not function as expected.

**Workaround:** Software driver can be modified to workaround this erratum.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

## **CHP28. SoC May Not Meet PCIe\* Clock Jitter Specification**

**Problem:** The SoC's PCIe REFCLK signals may not meet PCIe jitter specifications when operating at 5.0 GT/s with SSC (Spread Spectrum Clocking) enabled.

**Implication:** The platform may not meet REFCLK jitter specification. Intel has not observed any functional failures due to this erratum.

**Workaround:** None identified.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

## **CHP29. SATA Host Controller Does Not Pass Certain Compliance Tests**

**Problem:** The SoC SATA host controller OOB (Out of Band) Host Responses, OOB Transmit Gap, and OOB Transmit Burst Length do not pass Serial ATA Interoperability Program Revision 1.4.3, Unified Test Document Version 1.01 tests OOB-03[a/b], OOB-05, and OOB-06[a/b].

**Implication:** Intel has obtained a waiver for these tests. Intel has not observed any functional failures due to this erratum.

**Workaround:** None identified.



**Status:** For the steppings affected, see the *Summary Table of Changes*.

### **CHP30. RTIT Trace May Contain FUP.FAR Packet With Incorrect Address**

**Problem:** The FUP.FAR (Flow Update Packet for Far Transfer) generated by RTIT (Real Time Instruction Trace) on a far transfer instruction should contain the linear address of the first byte of the next sequential instruction after the far transfer instruction. Due to this erratum, far transfer instructions with more than 3 prefixes may incorrectly include an address between the first byte of the far transfer instruction and the last byte of the far transfer instruction.

**Implication:** The RTIT Trace decoder may incorrectly decode the trace due to an incorrect address in the FUP packet.

**Workaround:** The RTIT trace decoder can identify a FUP.FAR in the middle of a far transfer instruction and treat that FUP.FAR as if it was coming from the first byte of the following sequential instruction.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

### **CHP31. RTIT May Delay The PSB by One Packet**

**Problem:** After an RTIT (Real Time Instruction Trace) packet that exceeds the limit specified by Pkt\_Mask in RTIT\_PACKET\_COUNT (MSR 77Ch) bits [17:16], the PSB (Packet Stream Boundary) packet should be sent immediately. Due to this erratum, the PSB packet may be delayed by one packet.

**Implication:** The PSB packet may be delayed by one packet.

**Workaround:** None identified.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

### **CHP32. RTIT TraceStop Condition Detected During Buffer Overflow May Not Clear TraceActive**

**Problem:** If an RTIT (Real Time Instruction Trace) TraceStop condition is detected while RTIT\_STATUS.Buffer\_Overflow MSR (769H) bit 3 is set, the processor may not clear RTIT\_CTL.TraceActive MSR (768H) bit 13, and tracing will continue after the overflow resolves. Such a case will be evident if the TraceStop packet is inserted before overflow is resolved, as indicated by the FUP.BuffOvf (Flow Update Packet for Buffer Overflow) packet.

**Implication:** The RTIT trace will continue tracing beyond the intended stop point.

**Workaround:** None identified.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

### **CHP33. RTIT FUP.BuffOvf Packet May be Incorrectly Followed by a TIP Packet**

**Problem:** When RTIT (Real Time Instruction Trace) suffers an internal buffer overflow, packet generation stops temporarily, after which a FUP.BuffOvf (Flow Update Packet for Buffer Overflow) is sent to indicate the LIP that follows the instruction upon which tracing resumes. In some cases, however, this packet will be immediately followed by a FUP.TIP (Flow Update Packet for Target IP) which was generated by a branch instruction that executed during the overflow. The IP payload of this FUP.TIP will be the LIP of the instruction upon which tracing resumes.

**Implication:** The spurious FUP.TIP packet may cause the RTIT trace decoder to fail.

**Workaround:** The RTIT trace decoder should ignore any FUP.TIP packet that immediately follows a FUP.BuffOvf whose IP matches the IP payload of the FUP.BuffOvf.



**Status:** For the steppings affected, see the *Summary Table of Changes*.

#### **CHP34. RTIT CYC Packet Payload Values May be Off by 1 Cycle**

**Problem:** When RTIT (Real Time Instruction Trace) is enabled with RTIT\_CTL.Cyc\_Acc MSR (768H) bit 1 set to 1, all CYC (Cycle Count) packets have a payload value that is one less than the number of cycles that have actually passed. Note that for CYC packets with a payload value of 0, the correct value may be 0 or 1.

**Implication:** The trace decoder will produce inaccurate performance data when using CYC packets to track software performance.

**Workaround:** As a partial workaround, the trace decoder should add 1 to the payload value of any CYC packet with a non-zero payload.

**Status:** For the steppings affected, see the *Summary Table of Changes*.

#### **CHP35. First MTC Packet After RTIT Enable May be Incorrect**

**Problem:** When RTIT (Real Time Instruction Trace) is enabled, indicated by TriggerEn in bit 2 of the RTIT\_STATUS MSR (769H) transitioning from 0 to 1, the first MTC (Mini Time Counter) packet may be sent at the wrong time.

**Implication:** The RTIT trace decoder will make incorrect assumptions about the TSC value based on an asynchronous MTC packet.

**Workaround:** The RTIT trace decoder should ignore the first MTC that follows trace enabling.

**Status:** For the steppings affected, see the *Summary Table of Changes*.





# Specification Changes

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There are no new Specification Changes in this Specification Update revision.

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# Specification Clarifications

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There are no new Specification Clarifications in this Specification Update revision.

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# Documentation Changes

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There are no new Documentation Changes in this Specification Update revision.

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