

Op-Amp/Comparator Application Note

Operational amplifier ,Comparator (Tutorial)

This application note explains the general terms and basic techniques that are necessary for configuring application circuits with op-amps and comparators. Refer to this note for guidance when using op-amps and comparators.

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1 What is Op-Amp/Comparator?

1.1 What is op-amp?

An op-amp (operational amplifier) is a differential amplifier that has high input resistance, low output resistance, and high open loop gain. Its function is to amplify the differential voltage between the + input terminal (non-inverting terminal) and the - input terminal (inverting terminal).

Each op-amp circuit is composed of five terminals: a power supply terminal on the positive side, a power supply terminal on the negative side, a + input terminal, a - input terminal, and an output terminal. (There are no general terms for the terminals except classifications such as power source, input and output.)

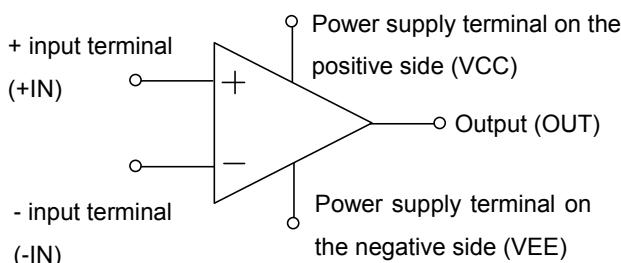


Figure 1.1.1. Op-amp/comparator symbol

Table 1.1.1. Examples of names for op-amp power supply terminals

	Bipolar type	CMOS type
Power supply terminal on the positive side	VCC	VDD
Power supply terminal on the negative side	VEE	VSS

Providing high input resistance (impedance) and low output resistance is a function required for the op-amps.

In Figure 1.1.2. Model of voltage controlled voltage source amplifier (op-amp), V_s is the input signal source, R_s is the signal source output resistor, R_i is the input resistor of the op-amp, R_o is the output resistor of the op-amp, R_L is the load resistor, and A_v is the amplification factor of the op-amp. The relation between the input and output voltages is described in the equation (1.1.1).

$$V_o = \frac{R_i}{R_i + R_s} V_s \times A_v \frac{R_L}{R_o + R_L} \quad (1.1.1)$$

As shown in Figure 1.1.2 and the equation (1.1.1), the signal voltage V_s is divided into resistance voltages by the signal source resistor R_s and the input resistor R_i of the op-amp. As a result, the input signal to the op-amp is attenuated. However, when the R_i is sufficiently larger than the R_s ($R_i = \infty$), the first term in the equation (1.1.1) can be approximated by 1 and it can be considered that $V_s = V_i$. Next, as for the second term, the amplified input voltage $A_v V_i$ is divided by the output resistor R_o of the op-amp and the load resistor R_L and output in Figure 1.1.2.

Here, the signal can be output without being attenuated if the R_o is sufficiently smaller than the R_L ($R_o=0$) because the second term can be approximated by 1. Such an op-amp is called an ideal op-amp. Usually, op-amps with high input resistance and low output resistance are preferred. The circuit configuration is designed to achieve an ideal op-amp as closely as possible.

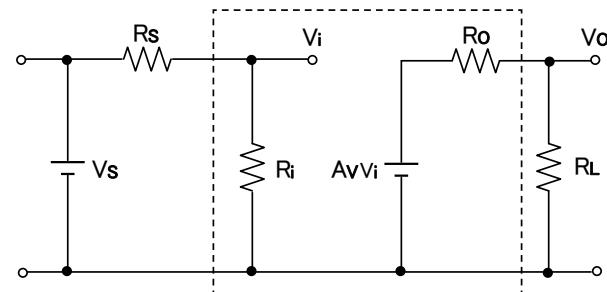


Figure 1.1.2. Model of voltage controlled voltage source amplifier

Table 1.1.2. Ideal input and output resistances required for op-amp

	Input resistance	Output resistance
Ideal op-amp (Voltage controlled voltage source)	∞	0

An op-amp amplifies a small differential voltage between the + input terminal and - input terminal and outputs the amplified voltage. For this purpose, an op-amp with a large amplification factor is preferred. The reason is explained using the voltage follower circuit in Figure 1.1.3.

A voltage follower circuit is a circuit in which the input and output voltages are equal. It is mainly used as a voltage buffer.

This circuit provides characteristics such as high input resistance and low output resistance, as mentioned above.

In Figure 1.1.3, the input voltage V_s and the V_{OUT} become identical.

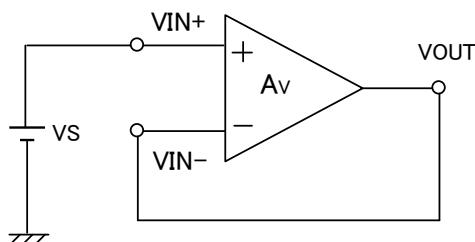


Figure 1.1.3. Voltage follower circuit

Since the op-amp amplifies the differential voltage between the terminals by the amplification factor of the op-amp, the output voltage is expressed with the equation (1.1.2).

$$V_{OUT} = A_V \times (V_{IN+} - V_{IN-}) = A_V \times (V_s - V_{OUT}) \quad (1.1.2)$$

The equation (1.1.2) is converted to the equation (1.1.3).

$$\frac{V_{OUT}}{A_V} = V_s - V_{OUT} \quad (1.1.3)$$

In the equation (1.1.3), when the open loop gain of the op-amp is sufficiently high, the left side can be approximated by 0 and the equation gives $V_s = V_{OUT}$. When the gain is low, the left side of the equation (1.1.3) cannot be approximated by 0 and the output voltage will contain an error.

An op-amp with a high open loop gain is desirable because the error in the output voltage can be minimized by the high gain.

From another point of view, the high open loop gain means that the difference in the potentials between the + input terminal and the - input terminal is minimized. Namely, the higher the open loop gain is, the better the relation $V_{IN+} = V_{IN-}$ holds. This relation in which the potentials of the + input terminal and the - input terminal become nearly equal is called a virtual short-circuit, imaginary short-circuit, or virtual

grounding. When configuring and using a negative feedback circuit, this relation is realized and application circuits are designed utilizing the characteristic of the virtual grounding.

1.2 What is comparator?

A comparator (voltage comparator) has the same terminal structure as an op-amp composed of five terminals: the + input terminal, the - input terminal, the positive side power supply terminal, the negative side power supply terminal, and the output terminal. When a comparator is used, the voltage is fixed at one of the input terminals as a reference terminal, and the difference between the reference voltage and the output voltage to the other terminal is amplified. The output voltage is either higher or lower than the reference voltage.

When the + input terminal potential > the - input terminal potential

→ High level output.

When the - input terminal potential > the + input terminal potential

→ Low level output.

The major difference between op-amps and comparators is whether or not the phase compensation capacitance exists. Since op-amps configure and utilize a negative feedback circuit, they require phase compensation capacitance to prevent oscillation inside the IC. On the other hand, since comparators will not configure the negative feedback circuit, they do not include the phase compensation capacitance. Since the phase compensation capacitance limits the response time between the input and the output, a comparator without the phase compensation capacitance provides a better responsiveness compared to an op-amp.

In contrast, if an op-amp is used as a comparator, since the phase compensation capacitance limits the response, it provides a very poor responsiveness compared with a comparator.

Therefore, care must be taken when using an op-amp as a comparator.

1.3 Internal circuit configuration of op-amp/comparator

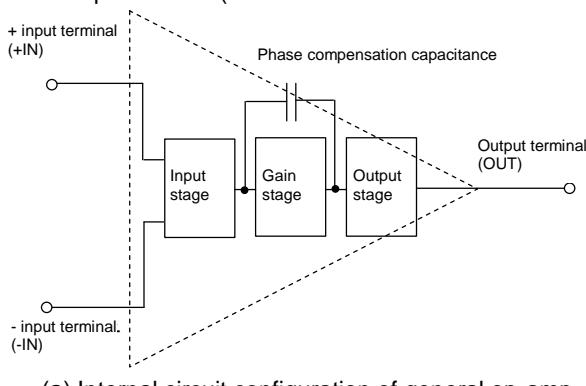
Figure 1.3.1 shows the internal circuit configuration of an op-amp. Generally, an op-amp is composed of three stages: the input stage, the gain stage, and the output stage.

The input stage is configured with a differential amplification stage that amplifies the differential voltage between the two terminals. In addition, it does not amplify the common-mode signal component (a condition where no difference in potential exists between the terminals and an equal voltage is input).

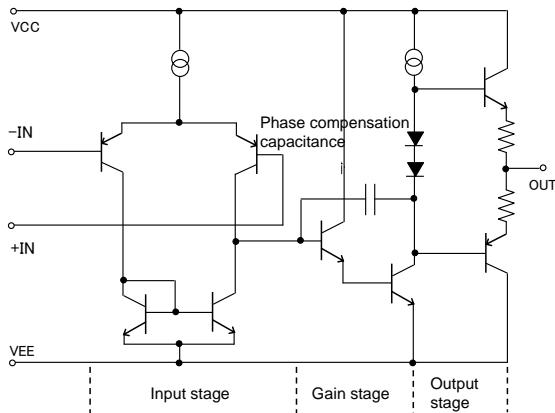
Since the gain is insufficient with the differential amplification circuit alone, the gain stage further increases the open loop gain in the op-amp.

In general op-amps, the phase compensation capacitance for oscillation prevention is connected over the gain stage.

The output stage is connected as a buffer so that the op-amp characteristics will not be affected by loads such as the resistance connected to the output terminal. The changes in the output characteristics due to the loads (such as distortion or voltage drop) mainly depend on the circuit configuration and the current capability of the output stage. The type of output stage, Class A and B, C, or AB push-pull output circuit, is classified according to the amount of drive current flowing in the output circuit (the difference in the bias voltage).



(a) Internal circuit configuration of general op-amp



(b) BA4558 Internal equivalent

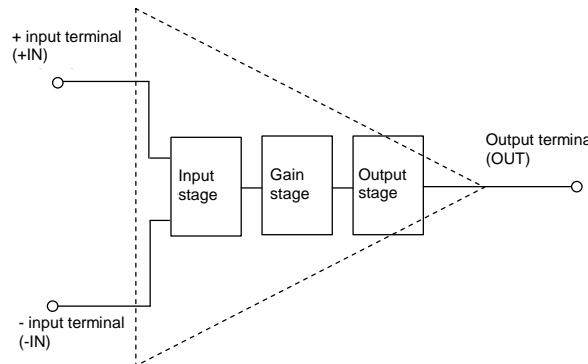
Figure 1.3.1. Internal circuit configuration of op-amp

The difference in the amount of drive current affects the distortion factor generated in the output stage. In general, the Class A output circuit has the lowest distortion factor, followed by Classes AB, B, and C.

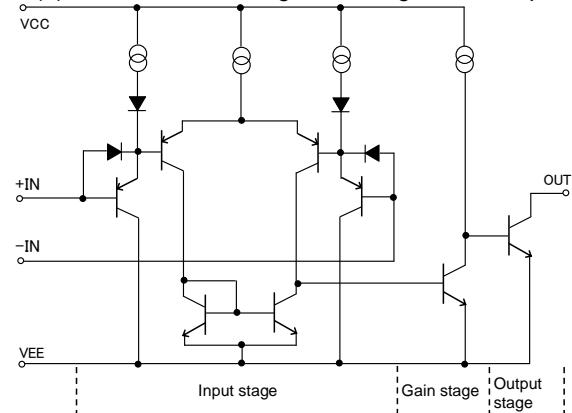
Figure 1.3.2 shows the internal circuit configuration of a comparator. Although the circuit configuration is nearly identical to that of an op-amp, the phase compensation capacitance for oscillation prevention is not included in the comparator since it is not supposed to be used in a negative feedback configuration. Since the phase compensation capacitance limits the operating speed between the input and the output, the response time is remarkably better compared with op-amps.

The type of output circuit for comparators is classified into the open collector (open drain) type or the push-pull type.

Figure 1.3.2 (b) shows the internal equivalent circuit of the BA2903. The BA2903 is an output circuit of the open collector type.



(a) Internal circuit configuration of general comparator



(b) BA2903 Internal equivalent

Figure 1.3.2. Internal circuit configuration of comparator

2 Absolute Maximum Rating

The absolute maximum rating is specified in the data sheet for op-amps/comparators. The absolute maximum rating provides the condition that must not be exceeded even instantaneously. The application of a voltage above the absolute maximum rating or use in a temperature environment outside the environment specified by the absolute maximum rating may cause the deterioration of characteristics or destruction of the internal circuit. The absolute maximum ratings for the following items are explained.

- 2.1. Power supply voltage/operating range of power supply voltage
- 2.2. Differential input voltage
- 2.3. Input common-mode voltage
- 2.4. Input current
- 2.5. Operating temperature range
- 2.6. Maximum junction temperature, storage temperature range
- 2.7. Power dissipation (total dissipation)

2.1 Power supply voltage/operating range of power supply voltage

For the power supply voltage, the absolute maximum rating refers to the maximum power supply voltage that can be applied between the positive side power supply terminal (VCC terminal) and the negative side power supply terminal (VEE terminal) of the op-amp without causing the deterioration of characteristics or destruction of the internal circuit. Figure 2.1.1 shows examples of the power supply voltage that can be applied to an op-amp/comparator that has an absolute maximum rating for the power supply voltage of 36 V. The absolute maximum rating for the power supply voltage specifies the difference in voltage between the VCC and VEE terminals. The op-amp/comparator must be used

with the value of (VCC-VEE) never exceeding the absolute maximum rating for the power supply voltage. Therefore, when 24 V and -12 V are applied to the VCC and VEE terminals, respectively, the difference in voltage between the terminals is 36 V and the deterioration of characteristics or destruction does not occur. It should be noted that the absolute maximum rating for the power supply voltage has a different meaning from the operating power supply voltage. The absolute maximum rating for the power supply voltage indicates the maximum value of the power supply voltage that will not cause the characteristics deterioration or destruction of the IC. It does not provide the voltage range in which the specifications and characteristics that are described in the data sheet are maintained. To obtain the characteristics that are guaranteed in the specifications, the op-amp/comparator must be used with the voltage value within the operating range of the power supply voltage. However, the absolute maximum rating for the power supply voltage of some products may be identical to the maximum value of the operating power supply voltage. Op-amps are sometimes called dual power supply or single power supply op-amps. In other words, an op-amp may be suited for the usage as a dual power supply or single power supply. Dual power supply op-amps have a voltage range in which either the input voltage or the output voltage cannot be output due to the circuit configuration on the positive power supply (VCC) side and the negative power supply (VEE) side. Therefore, the dual power supply op-amps are often used while applying a positive power supply and a negative power supply with the ground being the middle point. On the other hand, the single power supply op-amps are used while applying the positive power supply with reference to the ground and the input/output can be performed nearly at the ground level.

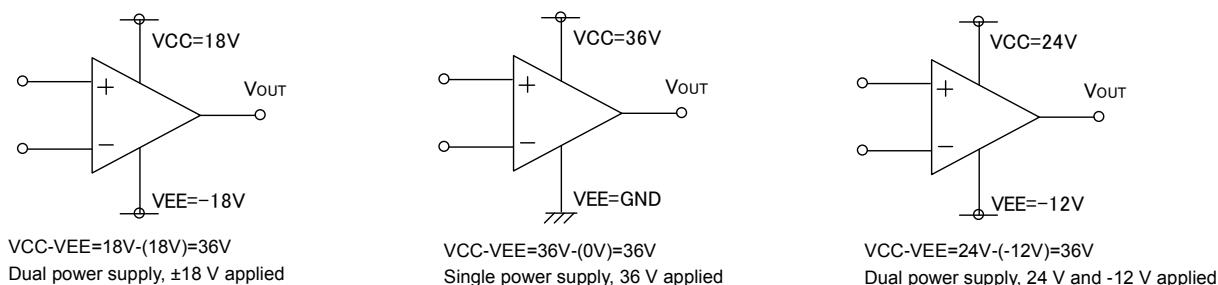


Figure 2.1.1. Examples of the power supply voltage that can be applied to an IC that has an absolute maximum rating for the power supply voltage of 36 V

Note: Dual power supply refers to the application of a power supply voltage to op-amps using two voltage power supplies (positive and negative). Single power supply refers to the application of a power supply voltage to op-amps with reference to the ground.

2.2 Differential input voltage

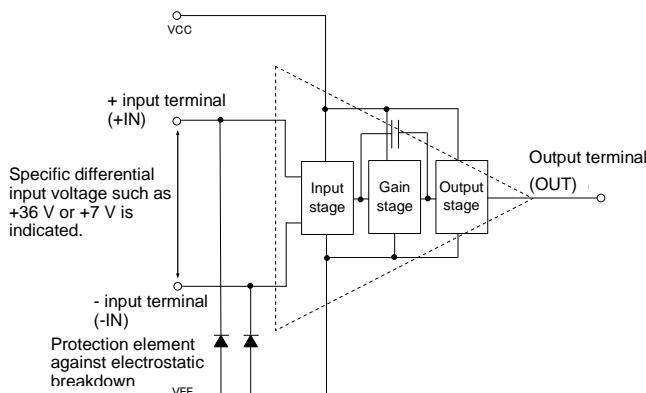
Differential input voltage indicates the maximum value of the voltage that can be applied between the + input terminal (non-inverting input terminal) and the - input terminal (inverting input terminal) without causing the characteristic deterioration or destruction of the IC. This voltage is the difference in voltage between the + input terminal and the - input terminal, and either of the terminals can be used as the reference. The polarity is not very important.

However, the potential of each input terminal is required to be higher than that of the VEE terminal. The reason for this requirement is that the current may flow out of the input terminal via the electrostatic protection element when the potential of the input terminal is lower than that of the VEE terminal, leading to deterioration or destruction.

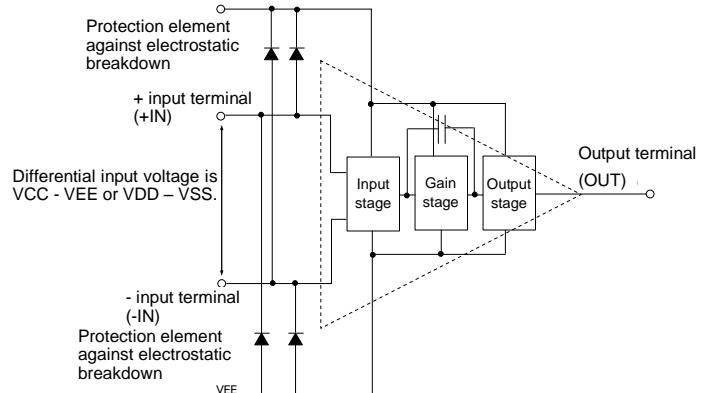
Two types of protection element are available: the elements are connected between the input terminals and the VEE

(ground) as in Figure 2.2.1(a), or the elements are connected between the input terminals and both the VCC and VEE (ground) as in Figure 2.2.1(b).

In the former, since there is no current path on the VCC side, the differential voltage does not depend on the VCC value and is determined by factors such as the breakdown voltage of the transistors (e.g., NPN and PNP transistors) that are connected to the input terminals. In the latter, since a protection element is located on the VCC side as well and the potential of the input terminals must be lower than that of the VCC, the differential input voltage is determined by $VCC - VEE$ or $VDD - VEE$. Some op-amps use an NPN differential input stage and the clamp diodes for the protection between the base and emitter of these transistors are connected between the input terminals. The differential voltage in such products may be specified to several volts (Figure 2.2.2).

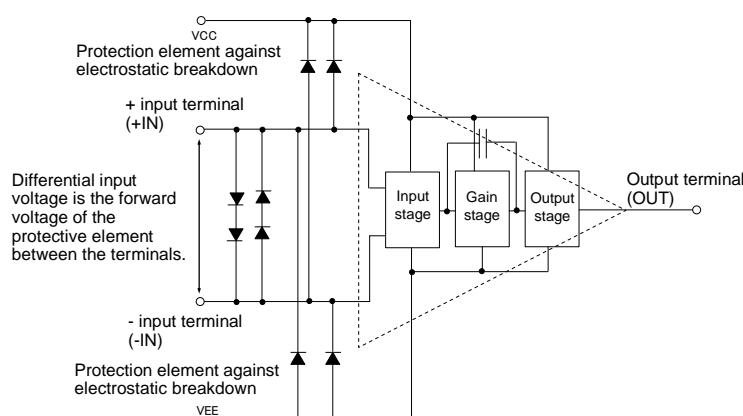


(a) When the electrostatic protection element is located only on the VEE (ground) side
(potential of input terminal must be higher than that of VEE)



(b) When the electrostatic protection elements are located on both the VCC and VEE (ground)
(potential of input terminal must be higher than that of VEE and lower than that of VCC)

Figure 2.2.1. Differential input voltage



When the diodes for the overvoltage protection are connected between the + input terminal and the - input terminal

Figure 2.2.2. Differential input voltage (with the protection between the terminals)

2.3 Input common-mode voltage

For the input common-mode voltage, the absolute maximum rating indicates the maximum voltage that can be applied without causing the characteristic deterioration or destruction of the IC when the potentials of the + input terminal and - input terminal are set to the same value. Unlike the input common-mode voltage range in the electrical characteristics specifications, the absolute maximum rating for the input common-mode voltage does not guarantee the normal operation of the IC.

If normal operation of the IC is expected, the voltage must follow the input common-mode voltage range in the electrical characteristics items. Generally, the absolute maximum rating for the input common-mode voltage is -0.3 V and +0.3 V for the VEE and VCC, respectively. However, as mentioned in section 2.2 Differential input voltage, the voltage can be applied up to the absolute maximum rating for the power supply voltage (e.g., +36 V for the VEE) in some products in which the protection element is not present on the VCC side.

In summary, the input common-mode voltage is determined by the protection circuit configuration and the parasitic element of the input terminals as well as the breakdown voltage of the input transistors among other factors. Figure 2.3.1 shows the absolute maximum rating for the input common-mode voltage.

In addition, the value of 0.3 V indicated in "VEE-0.3V" or "VCC+0.3V" represents the voltage range in which the electrostatic protection elements (diodes) are not activated when the forward voltage is applied to the protective element. For the protection method when a voltage outside the input voltage range is applied, refer to the next section, 2.4 Input current.

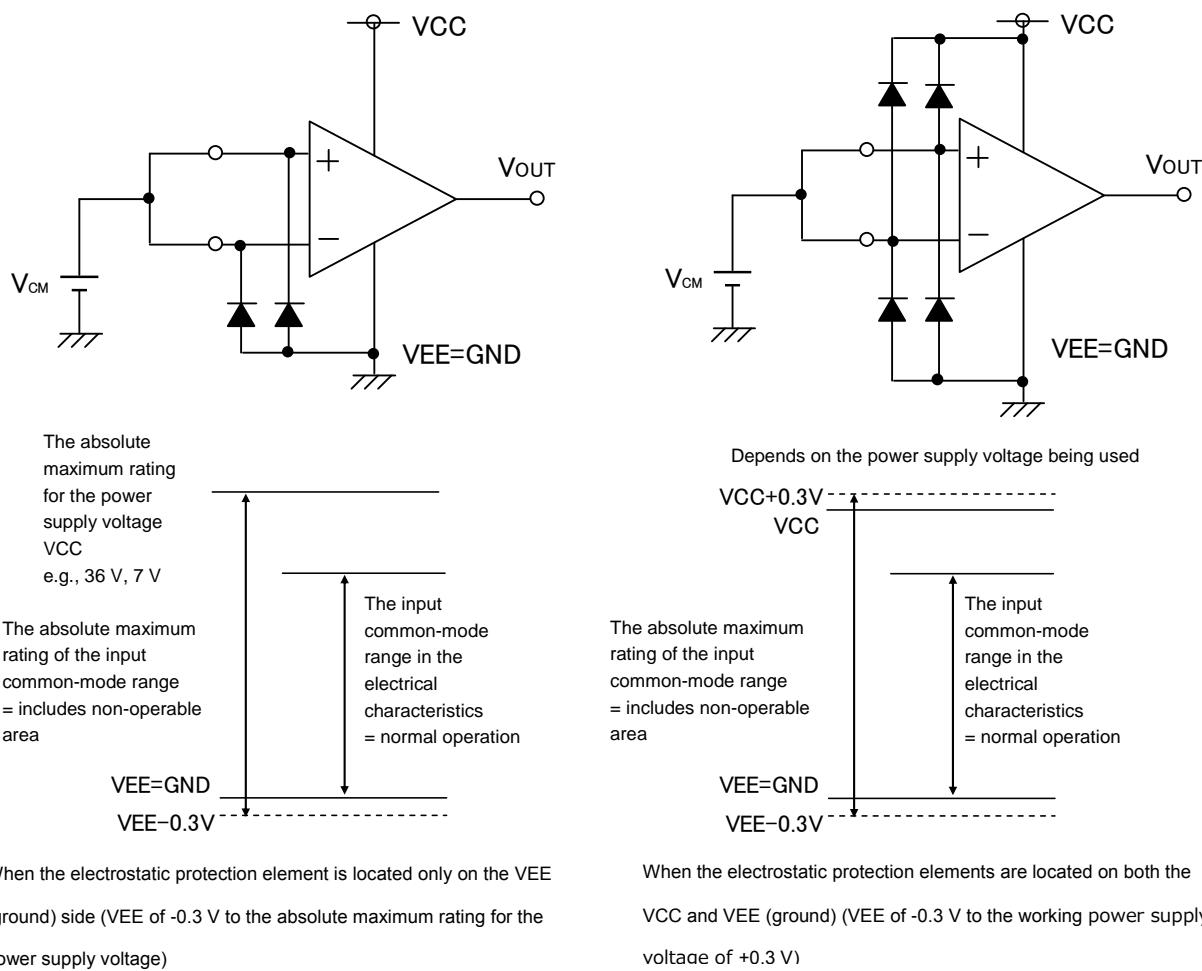


Figure 2.3.1. Absolute maximum rating for the input common-mode voltage

2.4 Input current

In sections 2.2 Differential input voltage and 2.3 Input common-mode voltage, it is explained that the current may flow into or out of the input terminals if a voltage is input at a value lower than the VEE of -0.3 V or higher than the VCC +0.3 V, leading to the characteristics deterioration or destruction.

As countermeasures, a small forward voltage diode for clamping can be provided on the input terminal, or the current flowing through the input terminal can be limited by inserting a resistor. The former is a method to limit the voltage that is input to the IC, while the latter is a method to limit the current. Set the resistor value so that the input current is 10 mA or less. Set the forward voltage of the diode (V_F in Figure 2.4.1) to approximately 0.6 V.

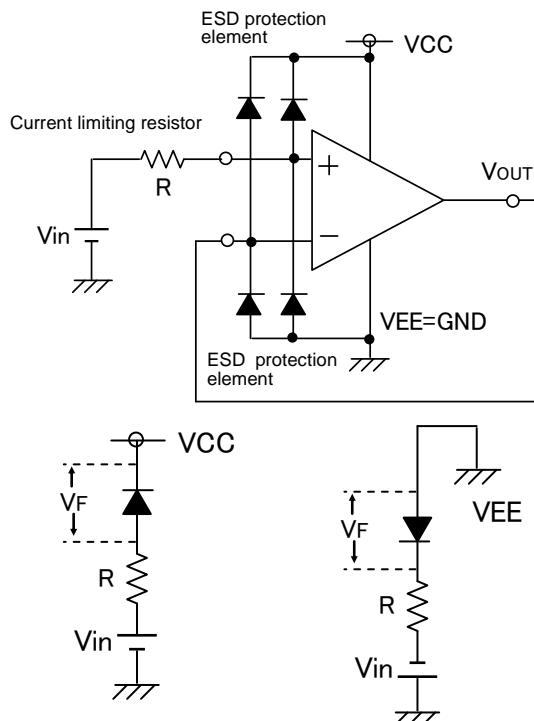


Figure 2.4.1. Connection of input current limiting resistor

2.5 Operating temperature range

Operation temperature range refers to the range in which the IC maintains the expected functions and operates normally.

The IC characteristics vary with temperature. Therefore, the standard values specified for 25°C are not necessarily guaranteed at other temperatures unless specified otherwise. There are some specification items that are guaranteed for all temperatures within the operating temperature range. The values for such items are standard ones that take into consideration the variation in IC characteristics within the operating temperature range indicated in the specifications. The data sheet lists the temperature characteristics data for the specification items. Refer to the data for using the IC.

2.6 Maximum junction temperature, storage temperature range

Maximum junction temperature is the maximum temperature at which the semiconductor can operate. The junction refers to the part where the chip and the package join. If the chip temperature exceeds the maximum junction temperature specified in the data sheet, a large number of electron-hole pairs will be generated in the semiconductor crystal, preventing the normal operation of the element. Therefore, the usage and thermal design should take into consideration the heat generation due to the power consumption by the IC and the ambient temperature. The maximum junction temperature is determined by the manufacturing process. The storage temperature range indicates the maximum temperature of the storage environment when the IC is not operating, i.e., without consumption power. Usually, this value is the same as the maximum junction temperature.

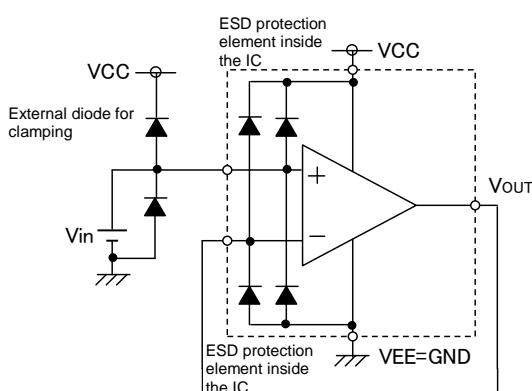


Figure 2.4.2. Connection of input protection diode

2.7 Power dissipation (total dissipation)

Power dissipation (total dissipation) or PD indicated in the data sheet refers to the power that the IC can consume at the ambient temperature $T_a = 25^\circ\text{C}$ (ordinary temperature). The power consumption by the IC causes self-heating, increasing the chip temperature so it is higher than the ambient temperature. The temperature that the chip can tolerate is determined by the maximum junction temperature. Therefore, the consumable power is limited by the thermal reduction curve (derating curve). The power dissipation at 25°C is determined by the temperature that the IC chip inside the package can tolerate (maximum junction temperature) and the thermal resistance (heat radiation property) of the package. In addition, the maximum value of the junction temperature is determined by the manufacturing process.

The heat generated by the IC power consumption is radiated through the mold resin or lead frame of the package.

The parameter to describe this heat radiation property (difficulty for the heat to escape) is called thermal resistance and is represented by the symbol θ_{j-a} [$^\circ\text{C}/\text{W}$]. The IC temperature (Junction temperature : T_j) inside the package can be estimated from the thermal resistance. Figure 2.5.1 shows the model for the thermal resistance of the package. θ_{j-a} is represented as the sum of the thermal resistance θ_{j-c} between the chip and the case (package) and the thermal resistance θ_{c-a} between the case (package) and the outside. When the thermal resistance θ_{j-a} [$^\circ\text{C}/\text{W}$], the ambient temperature T_a [$^\circ\text{C}$], and the consumption power P [W] are known, the junction temperature can be calculated with the following equation.

$$T_j = T_a + \theta_{j-a} \times P \quad (2.5.1)$$

Thermal resistance between the junction and the outside:

$$\theta_{j-a} = \theta_{j-c} + \theta_{c-a}$$

θ_{j-c} : Thermal resistance between the junction and the case [$^\circ\text{C}/\text{W}$]

θ_{c-a} : Thermal resistance between the case and the outside [$^\circ\text{C}/\text{W}$]

T_a : Ambient temperature [$^\circ\text{C}$]

T_j : Junction temperature [$^\circ\text{C}$]

The slope of the derating curve is the reciprocal of θ_{j-a}

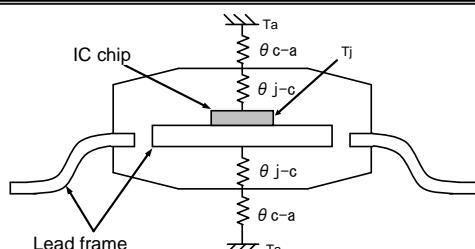


Figure 2.5.1. Thermal resistance of the package

Figure 2.5.2 shows examples of the thermal reduction curve (derating curve). This curve shows how much power the IC can consume at the ambient temperature. It indicates the power that can be consumed without exceeding the temperature that the IC chip can tolerate.

As an example, the chip temperature of the MSOP8 is considered. Since the storage temperature range for this IC is -55 [$^\circ\text{C}$] to 150 [$^\circ\text{C}$], the maximum allowable temperature is 150 [$^\circ\text{C}$]. The thermal resistance of the MSOP8 is $\theta_{j-a} \approx 212.8$ [$^\circ\text{C}/\text{W}$]. Therefore, the junction temperature when this IC consumes the power of 0.58 [W] at $T_a = 25$ [$^\circ\text{C}$] is calculated as follows.

$$T_j = 25 [^\circ\text{C}] + 212.8 [\text{^\circC}/\text{W}] \times 0.58 [\text{W}] \approx 150 [^\circ\text{C}] \quad (2.5.2)$$

The result shows that the junction temperature will reach the maximum allowable temperature of the chip, suggesting the possibility of deterioration or destruction if the power consumption is further increased.

For the thermal reduction curve, the amount of reduction per 1 [$^\circ\text{C}$] is determined by the reciprocal of the thermal resistance. In the figure, the reduction rate is as follows:

5.5 [$\text{mW}/^\circ\text{C}$] for the SOP8

5.0 [$\text{mW}/^\circ\text{C}$] for the SSOP-B8

4.7 [$\text{mW}/^\circ\text{C}$] for the MSOP8

Note: For calculation of the consumption power of op-amps, refer to the next section for the circuit current.

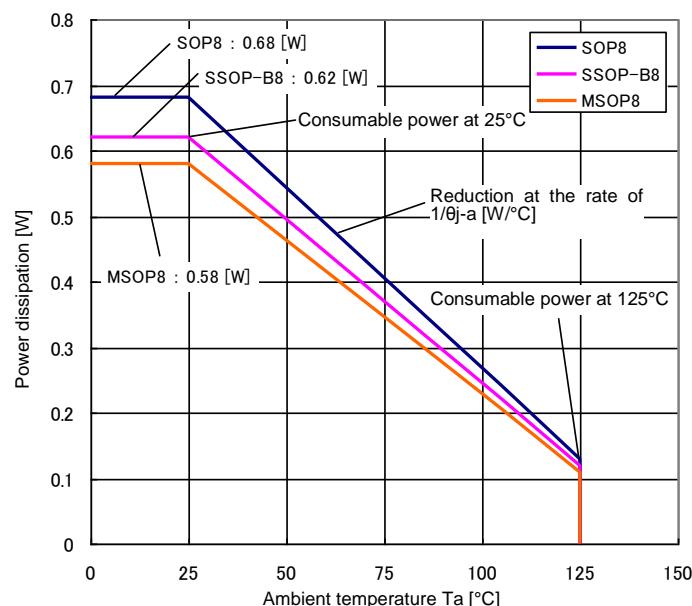


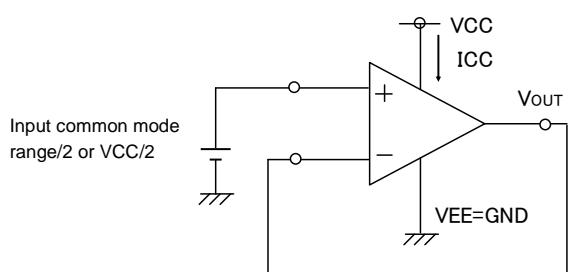
Figure 2.5.2. Examples of the thermal reduction curve
(When a 70 mm \times 70 mm \times 1.6 mm one-layer FR4 glass epoxy substrate is mounted)

3 Electrical Characteristics

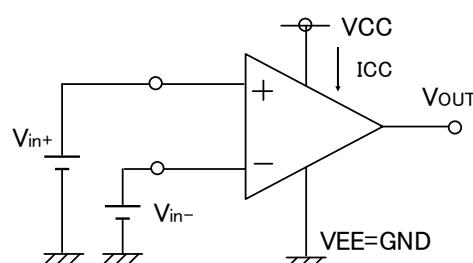
This technical note explains the electrical characteristics of op-amps and comparators as well as the precautions during actual use.

3.1 Supply current

The supply current of an op-amp/comparator represents a current flowing through the IC alone in the no-load and steady state as shown in Figure 3.1.1. Normally, the current flowing from the VCC terminal to the VEE terminal is monitored. The supply current is commonly called a no-signal supply current or quiescent current as well. The input range and the operating voltage range vary with the products, resulting in different measurement conditions. Normally, the measurement is performed by applying a voltage in the center of the input common-mode voltage range or in the middle between the supply voltages, VCC and VEE. In addition, the supply current of a comparator takes a different value either under the High or Low condition that is determined by the circuit structure. The value is specified under the condition that gives the higher supply current.



(a) Measurement circuit for the supply current of op-amps



(b) Measurement circuit for the supply current of comparators

Figure 3.1.1. Supply current of op-amp/comparator

Calculation of the power consumption of op-amps

When calculating the power consumption of an op-amp, it is necessary to consider the output current as well as the supply current.

We explain the calculation of the power consumption step by step. There are two types of power consumption by op-amps: the power consumption caused by the supply current or the output current. First, we show the calculation of the power consumption caused by the supply current. When P_{AMP} is the power consumed by an op-amp, Equation (3.1.1) becomes the supply current \times supply voltage based on $P = \text{current} \times \text{voltage}$.

This power consumption is always consumed as long as the supply voltage is applied on the op-amp.

$$P_{AMP} = I_{CC} \times (V_{CC} - V_{EE}) \quad (3.1.1)$$

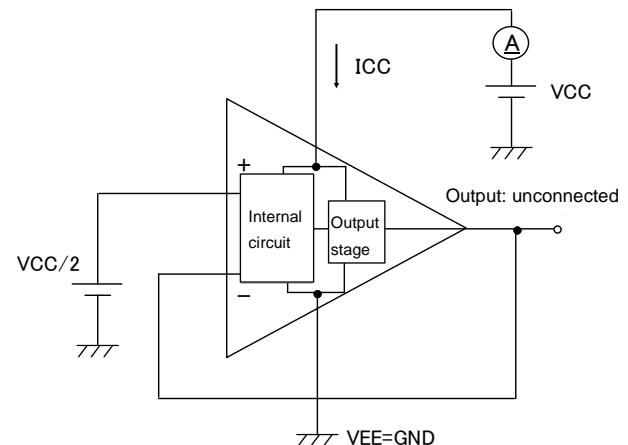


Figure 3.1.2. Power consumption caused by supply current

Next, we show the calculation of the power consumption caused by the output current.

The power is calculated for the case when an output sink current flows, as shown in Figure 3.1.3 (a).

The output sink current flows when V_o is lower than $V_{CC}/2$, with which the load resistance (R_L) is connected. The power consumption caused by this sink current is described by Equation (3.1.2). The power consumption is determined by the product of the current that flows into the inside of the IC and the difference in potentials between the OUT and VEE terminals.

$$P_{SINK} = I_{SINK} \times (V_o - V_{EE}) \quad (3.1.2)$$

The total power consumption of the op-amp when the sink current exists is represented as Equation (3.1.3).

$$P = P_{AMP} + P_{SINK} = I_{CC} \times (V_{CC} - V_{EE}) + I_{SINK} \times (V_o - V_{EE}) \quad (3.1.3)$$

Next, the power is calculated for the case when an output source current flows, as shown in Figure 3.1.3 (b).

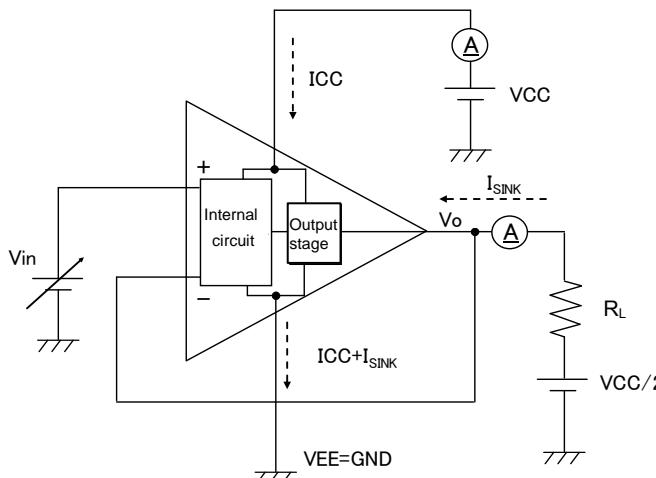
The output source current flows when the output voltage (V_o) is higher than $V_{CC}/2$, with which the load resistance (R_L) is connected. The calculation of the power caused by this source current is described by Equation (3.1.4). The power consumption is determined by the product of the current that flows from the inside of the IC and the difference in potentials between the VCC and OUT terminals.

$$P_{SOURCE} = I_{SOURCE} \times (V_{CC} - V_o) \quad (3.1.4)$$

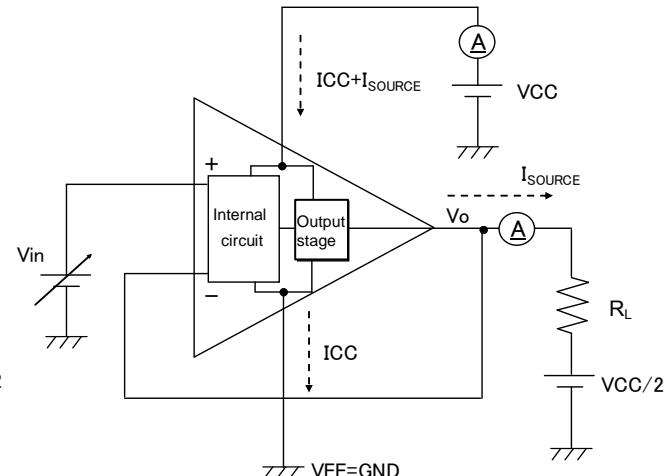
The total power consumption of the op-amp when the source current exists is represented as Equation (3.1.5).

$$P = P_{AMP} + P_{SOURCE} = I_{CC} \times (V_{CC} - V_{EE}) + I_{SOURCE} \times (V_{CC} - V_o) \quad (3.1.5)$$

When estimating the power consumption, the larger value of the sink or source current is used.



(a) Output sink current



(b) Output source current

Figure 3.1.3. Power consumption caused by output current

3.2 Input offset voltage

The input offset voltage represents the error voltage of an op-amp or comparator. An ideal op-amp or comparator has the input offset voltage of 0 V. When a common mode (identical) voltage is input to the input terminal of an op-amp or comparator, no output voltage is output in an ideal op-amp. However, when the input offset voltage exists, an output voltage is output in response to the input offset voltage. The difference in potential between the input terminals that is required to make this output voltage 0 V is referred to as the input offset voltage. This value is the input conversion value. One advantage of expressing the value as the input conversion is as follows: since op-amps and comparators are utilized with various amplification factors and circuit configurations, the influence on the output voltage can be easily estimated by using the input conversion.

The unit of the input offset voltage is usually [mV] or [μ V]. The ideal condition is approached when the value is closer to 0. When the voltage is out of the input common-mode voltage range, the input offset voltage rapidly increases and the circuit cannot be operated as an op-amp or comparator. When the frequency of appearance of the input offset voltage is observed, the observed values follow a normal distribution around 0 V. In other words, the values stochastically distribute within the range specified in the data sheet. While the standard values are described as absolute values, the input offset voltages actually have both + and - polarities. The specific effects of the input offset voltage are explained in the next section.

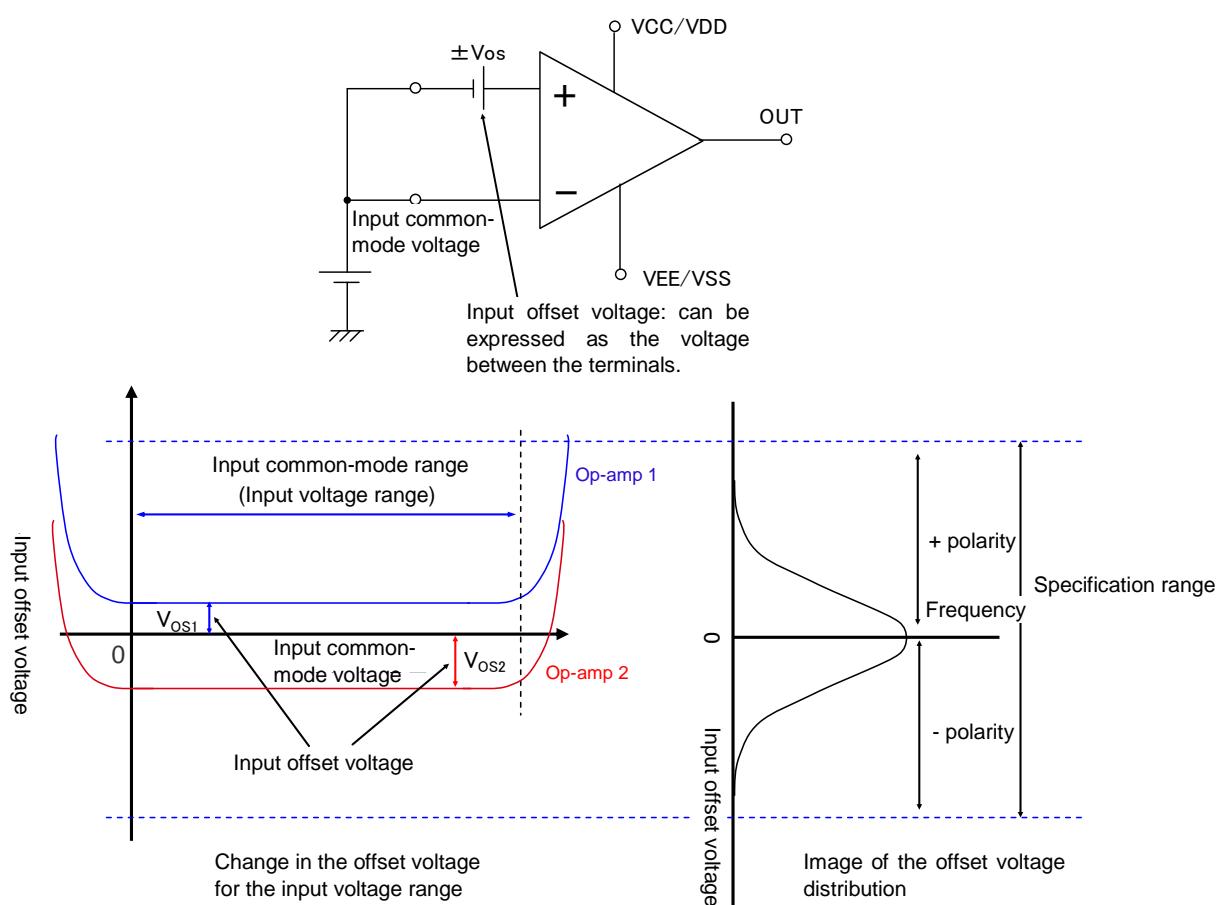


Figure 3.2.1. Image of input offset voltage

Effect of input offset voltage

Op-amp

This section explains the effect of the input offset voltage when an amplifier circuit is configured with an op-amp.

For the non-inverting amplifier circuit in Figure 3.2.2 (a), the effect of the input offset voltage is calculated as in Equation (3.2.1).

The input offset voltage is multiplied by the gain and the product is added to the output voltage. When the input offset voltage has the + polarity, the output voltage is higher than the expected value. Conversely, the - polarity results in a lower output voltage than the expected value.

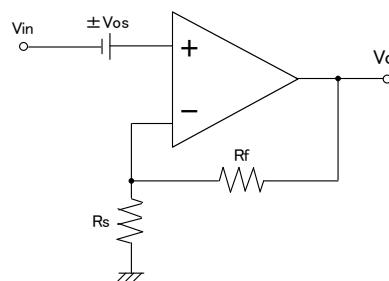
$$V_O = \left(1 + \frac{R_f}{R_s}\right)V_{in} \pm \left(1 + \frac{R_f}{R_s}\right)V_{os} \quad (3.2.1)$$

Next, the effect of the input offset voltage is determined when the inverting amplifier circuit is configured as in Figure 3.2.2 (b).

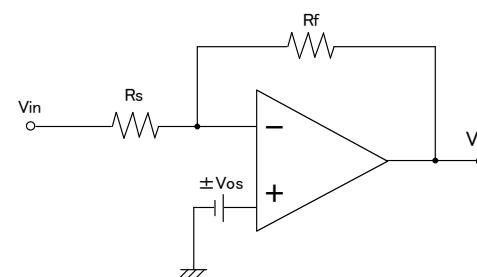
$$V_O = -\frac{R_f}{R_s}V_{in} \pm \left(1 + \frac{R_f}{R_s}\right)V_{os} \quad (3.2.2)$$

As described in Equation (3.2.2), the input offset voltage is multiplied by the amplification factor seen from the + terminal side (i.e., the amplification factor of the non-inverting amplifier circuit) and the product is added to the output of the inverting amplifier circuit. As in the previous case, the output voltage is shifted from the expected value by the product of the input offset voltage multiplied by the gain.

In Figure 3.2.3, the calculation is performed assuming that the input offset voltage is $\pm 5 \text{ mV}$. In either circuit, the center of the waveform is shifted by the product of the input offset voltage multiplied by the amplification factor ($5 \text{ mV} \times 16$). It is necessary to choose an op-amp with an appropriate value for the input offset voltage considering the desired circuit gain.

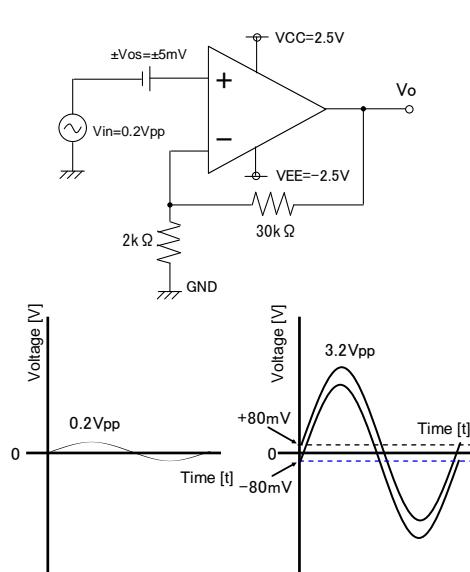


(a) Non-inverting amplifier circuit

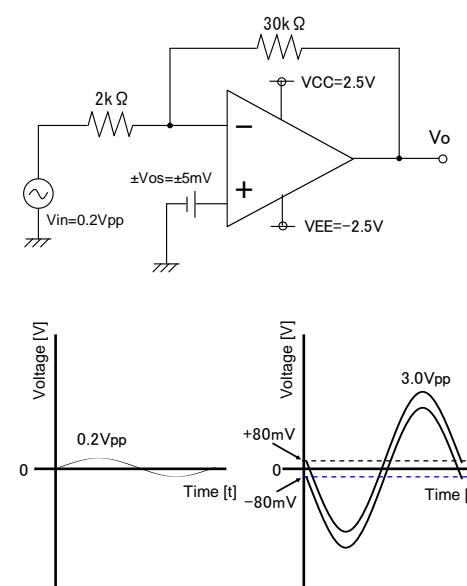


(b) Inverting amplifier circuit

Figure 3.2.2. Amplifier Circuit with Op-Amp



(a) Non-inverting amplifier circuit



(b) Inverting amplifier circuit

Figure 3.2.3. Example of effect of offset voltage

Comparator

Effect of the input offset voltage on the overdrive voltage

The difference between the voltage to be compared and the reference voltage (V_{ref}) is referred to as the overdrive voltage. When the difference is smaller, the response time tends to be longer. The response time is generally specified at 5 mV, 10 mV, 50 mV, and 100 mV. As an example, consider a comparator with the input offset voltage of 6 mV. In an ideal situation where no input offset voltage exists, the output voltage is switched even when the applied input is only slightly higher or lower than the reference voltage (V_{ref}).

However, when the input offset voltage is 6 mV, the comparator does not respond to the overdrive voltage of 5 mV. In other words, the input offset voltage appears to be added to the reference voltage V_{ref} . When the specification for the input offset voltage is $\pm V_{os}$, the individual circuits may output either High or Low outputs in the section between $V_{ref} + V_{os}$ and $V_{ref} - V_{os}$. Datasheet graphs of response time vs overdrive voltage are measured with compensating for input offset voltage.

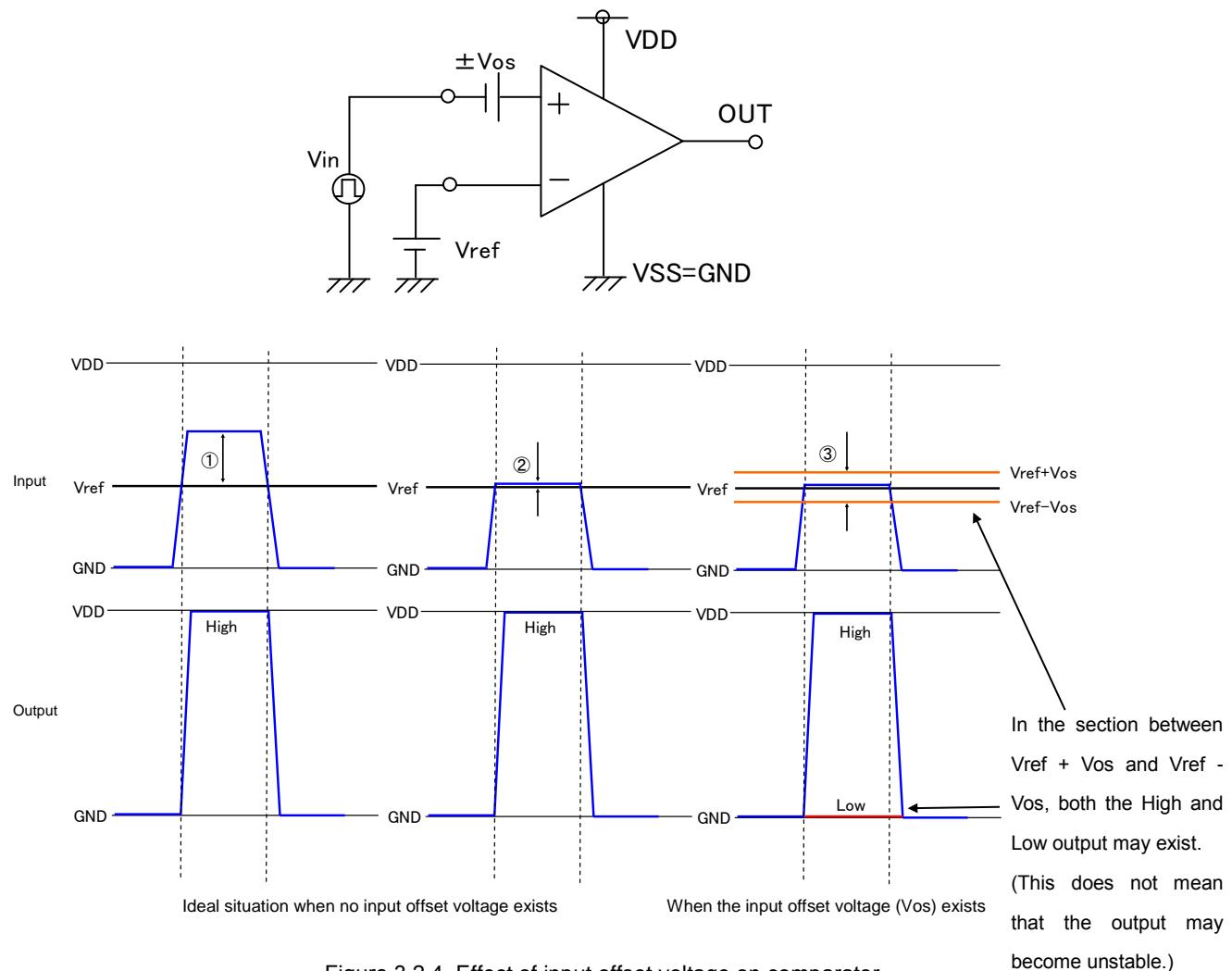


Figure 3.2.4. Effect of input offset voltage on comparator

Cause of the input offset voltage

Since the principle of generation is identical for the bipolar and CMOS types, the explanation is given for the bipolar type.

In Figure 3.2.5, the input offset voltage is generated by the difference in the characteristics between transistors Q1 and Q2 as well as between Q3 and Q4. More precisely, variations during the manufacturing process make the voltages between the base and emitter different between Q1 and Q2 as well as between Q3 and Q4. This causes the difference between collector currents I_{C3} and I_{C4} , which flow through Q3 and Q4, respectively. The difference between the collector currents contributes to the generation of the input offset voltage. (The base currents of Q3 and Q4 can also affect the input offset voltage through the variation in the center value. However, this effect is usually minimized by design and can be excluded from the consideration.)

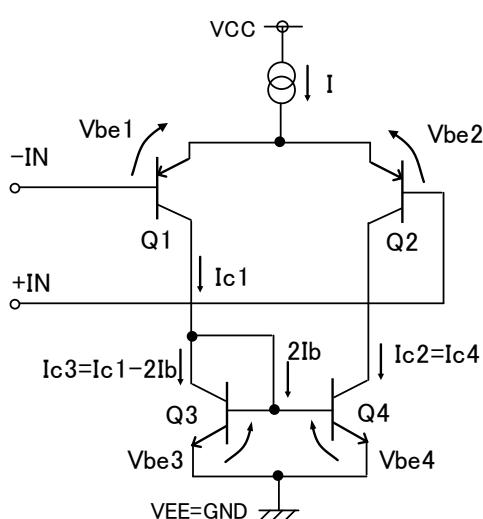


Figure 3.2.5. Differential input stage of op-amp

In addition, the effect of the stress from the package and the board is a cause of input offset voltage generation. This effect generally becomes more significant in the smaller packages. When the stress is received, the piezo-resistance effect is generated by the semiconductor element surface being pushed or the IC chip being bent. The piezoelectric effect caused by this piezo-resistance effect changes the characteristics of transistors.

In op-amps, mainly the differential input stage is subject to the stress effect and the input offset voltage may be changed by the stress from the board after the board is mounted. As a countermeasure, the op-amp should be placed on the center

of the board since the stress is larger in the edges. In addition, since a larger package is less susceptible to the stress, it is effective to choose a package with a larger size when precision is necessary.

Temperature drift of the input offset voltage

The input offset voltage varies with temperature. This variation is referred to as the temperature drift. As with the input offset voltage, the temperature drift value is not constant and follows a normal distribution. For some products, the standard values may be described in the data sheet. It should be noted that the input offset voltage may be observed as if drift has been caused by the piezo-resistance effect as mentioned above when the degree of bending of the mounted board changes with the temperature.

Increase of the input offset voltage caused by the input bias current

When configuring an amplifier circuit with a bipolar op-amp, it is necessary to take a countermeasure against the input bias current. The input offset voltage is increased by the product of the input bias current and the parallel combined resistor value of the resistors that constitute the amplifier circuit.

A countermeasure is to connect the same combined resistance to the other input terminal. This will be explained in more detail in the section for the input bias current.

3.3 Input bias current and input offset current

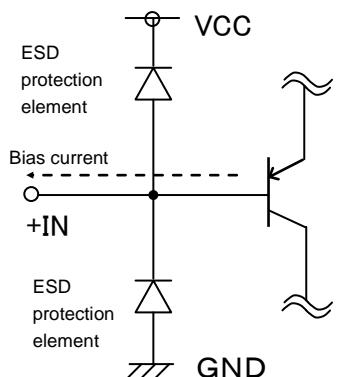
A current flowing from or into the input terminal of op-amps is referred to as the input bias current. In op-amps of the bipolar type, the base current of the transistor connected to the input terminal is the input bias current. When the differential input stage is configured with PNP transistors, the current flows out. Conversely, when the differential input stage is configured with NPN transistors, the current flows in. Many products are designed so that the amount of current falls approximately in the order of nA (10^{-9} [A]) while some high-speed type products have a bias current in the order of μ A (10^{-6} [A]).

Ideally, op-amps are easier to use when the bias current is smaller. The CMOS type (FET input) op-amps are considered such op-amps. The bias current in the CMOS op-amp is very small and falls in the order of fA (10^{-15} [A]) to pA (10^{-12} [A]). Therefore, the CMOS op-amps are used as the sensor amplifiers of sensor elements and other elements with high impedance.

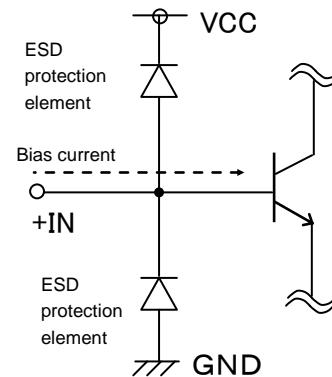
As shown in Figure 3.3.1 (a), the input bias current flows from the input terminal when the op-amp is configured with a PNP transistor as the input transistor.

In the case of the NPN input as shown in Figure 3.3.1 (b), the input bias current flows into the terminal. In the full swing op-amp of the bipolar type shown in Figure 3.3.1 (c), the direction of the input bias current changes depending on the operating range. In the range where only the PNP transistor operates, the input bias current flows from the terminal. In the range where both types of transistors operate, the differential current flows, and the polarity becomes the larger one. When only the NPN transistor operates, the input bias current flows into the terminal. Therefore, the polarity of the bias current changes within the input common-mode voltage range.

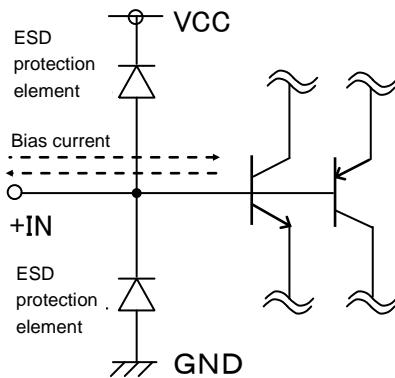
The input bias current in the CMOS op-amp shown in Figure 3.3.1 (d) is the terminal leakage current. The main cause is the electrostatic protection element connected to the inside of the IC. This current is very small compared with the bipolar type, providing an advantage when connecting op-amps of this type with high-impedance elements such as sensors. In addition, this type of op-amp has a characteristic in which the current tends to increase at a higher temperature since the leakage current increases with temperature.



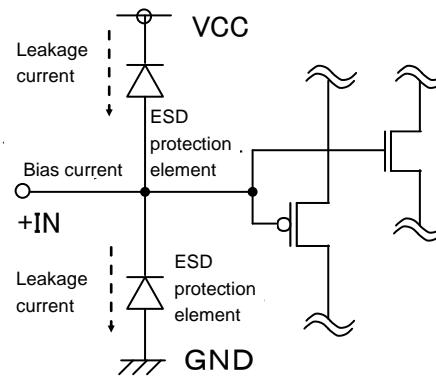
(a) Input ground sense (ground sense single/dual power supply)



(b) NPN input (VCC sense)



(c) PNP/NPN input (full swing)



(d) CMOS input (full swing)

Figure 3.3.1. Input bias current and input transistor

Effect of input bias current

The difference in the input bias currents in the + and - input terminals is referred to as the input offset current. Since the base current and the leakage current are affected by the performance variation in transistors, the values are not necessarily the same.

The input bias current (I_b) and the input offset current (I_{io}) are defined by Equations (3.3.1) and (3.3.2), respectively.

$$I_b = \frac{I_{b+} + I_{b-}}{2} \quad (3.3.1)$$

$$I_{io} = I_{b+} - I_{b-} \quad (3.3.2)$$

Cancel of the input bias current

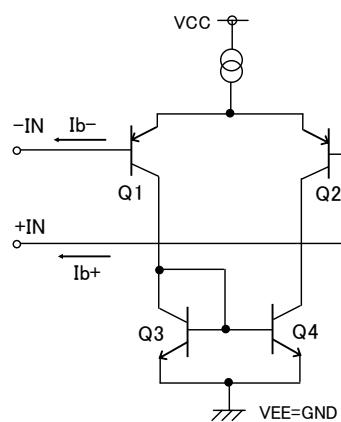
The effect of the input bias current in the inverting amplifier circuit in Figure 3.3.3 is described by Equation (3.3.3).

$$V_{out} = -\frac{R_2}{R_1}V_{in} - \left(1 + \frac{R_2}{R_1}\right) \left[\frac{R_1 R_2}{R_1 + R_2} I_{b-} - R_3 I_{b+} \right] \quad (3.3.3)$$

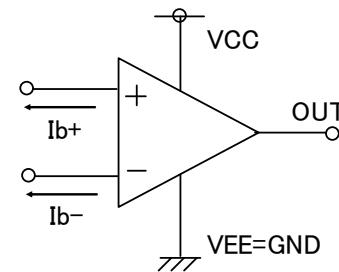
Arranging Equation (3.3.3) with Equations (3.3.1) and (3.3.2) gives Equation (3.3.4), where Equation (3.3.1) defines the input bias current and Equation (3.3.2) defines the input offset current.

In Equation (3.3.4), the effect of the input bias current can be removed if R_3 is set to the same value as the parallel combined impedance of R_1 and R_2 in order to nullify the I_b term. Equation (3.3.4) also shows that the presence of the input offset current affects the output voltage.

$$V_{out} = -\frac{R_2}{R_1}V_{in} - \left(1 + \frac{R_2}{R_1}\right) \left[\left(\frac{R_1 R_2}{R_1 + R_2} - R_3 \right) I_b - \left(\frac{R_1 R_2}{R_1 + R_2} + R_3 \right) \frac{I_{io}}{2} \right] \quad (3.3.4)$$



(a) Differential input stage



(b) Input bias current in op-amp

Figure 3.3.2. Input bias current

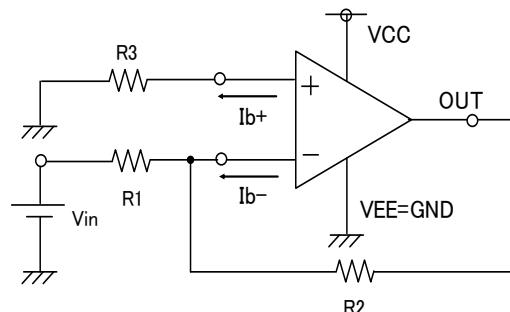


Figure 3.3.3. Input bias current in inverting amplifier circuit

3.4 Input common-mode voltage range

The input common-mode voltage range (V_{ICM}) refers to the range of input voltage within which an op-amp operates normally. When a signal outside the input common-mode voltage range is input, the input offset voltage is increased rapidly and the output voltage is saturated, disrupting the normal operation.

The input common-mode voltage range is determined by the circuit configuration of the differential amplifier circuit that is the input circuit of the op-amp.

Figures 3.4.1 and 3.4.2 show the differential input stages of the 4558 and 358/2904 series op-amps, respectively. Consider the input common-mode voltage ranges for these two types of op-amp.

The input common-mode voltage range of the 4558 series op-amp is described by Equation (3.4.1), where V_{ICM} is the input common-mode voltage. The lower limit of the input common-mode voltage range is the voltage that is required for transistors Q1 and Q2 to operate without being saturated. Conversely, the upper limit of the input common-mode voltage range is the voltage that is required for transistor Q0 to operate without being saturated.

Equation (3.4.2) shows that the 4558 series op-amp has both upper and lower limits between which the transistors can operate. The op-amps of this type are referred to as dual power supply op-amps. Normally, positive and negative power supplies are used with the ground being the middle point potential. However, this type of op-amp can also be used with a single supply if the bias voltage is appropriately adjusted.

Next, the input common-mode voltage range of the 358/2904 series op-amp shown in Figure 3.4.2 is described by Equation (3.4.3). In the 358/2904 series op-amps, level shift circuits Q1 and Q2 are employed so that the input voltage at the ground (VEE) level can be handled. In addition, this type of op-amp is designed so that the collector potentials at Q3 and Q4 can be made nearly equal due to the arrangement of the circuit configuration. This makes Q3 and Q4 saturated at nearly the same voltage.

Equation (3.4.4) shows that the lower limit of the input common-mode voltage is determined by V_{sat} and V_{be} . Since V_{sat} is generally lower than V_{be} , the input common-mode voltage range of the 358/2904 series op-amp can include VEE, allowing the signal input at the ground level.

$$V_{EE} + V_{be6} + V_{be5} + V_{sat2} - V_{be2} < V_{ICMR} < V_{CC} - V_{sat0} - V_{be2} \quad (3.4.1)$$

If we assume that all V_{be} and V_{sat} values are equal in Equation (3.4.1),

$$V_{EE} + (V_{be} + V_{sat}) < V_{ICMR} < V_{CC} - (V_{sat} + V_{be}) \quad (3.4.2)$$

$$V_{EE} + V_{be5} + V_{sat3} - V_{be3} - V_{be1} < V_{ICMR} < V_{CC} - V_{sat0} - V_{be3} - V_{be1} \quad (3.4.3)$$

If we assume that all V_{be} and V_{sat} values are equal in Equation (3.4.3),

$$V_{EE} + (V_{sat} - V_{be}) < V_{ICMR} < V_{CC} - (V_{sat} + 2V_{be}) \quad (3.4.4)$$

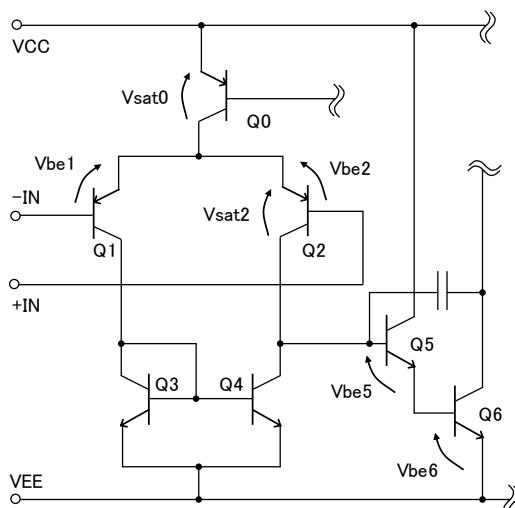


Figure 3.4.1. Differential input stage of 4558 series op-amp

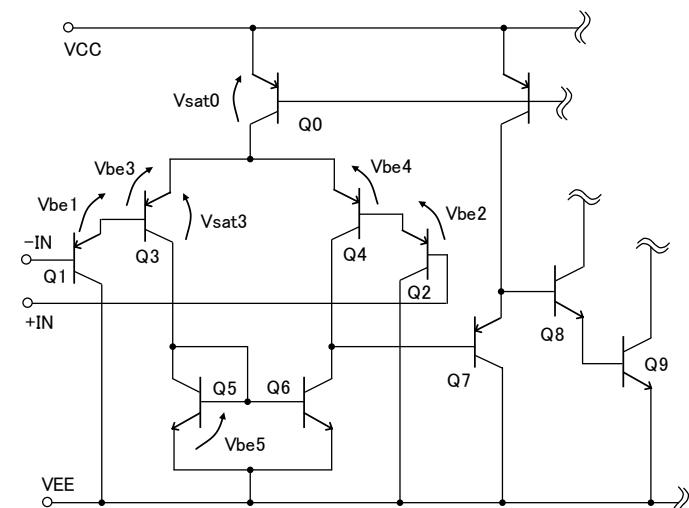


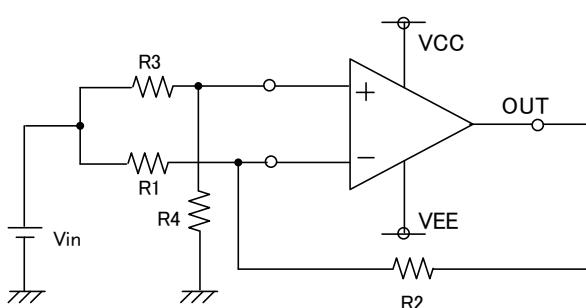
Figure 3.4.2. Differential input stage of 358/2904 series op-amp

Next, we explain examples of the characteristics and the measurement method of the input common-mode voltage.

Figure 3.4.3 (a) shows the measurement circuit for the input common-mode voltage. The input voltage is varied with the input terminal of the differential amplifier circuit being used as the common terminal.

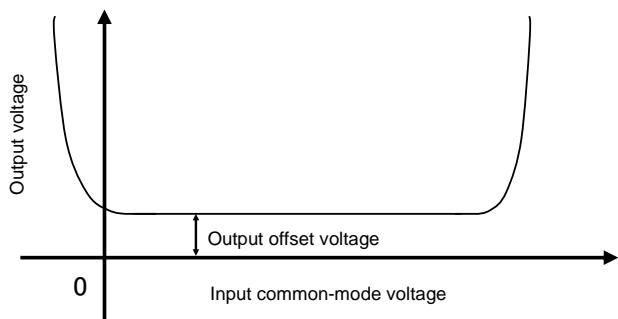
Since the common-mode voltage is input, the output voltage should ideally be 0. However, since the input offset voltage actually exists, the output offset voltage is output with the input offset voltage multiplied by the amplification factor as shown in Figure 3.4.3 (b).

Next, we present images of the input common-mode voltage ranges for the 358/2904 and 4558 series op-amps, which we considered in the previous section for the input common-mode voltage range.



(a) Measurement circuit diagram

As in Figures 3.4.4 and 3.4.5, the input common-mode voltage range limits the input voltage. Therefore, it is necessary to choose an op-amp with an input range adequate for the application to be used. So far, we have explained that the input common-mode voltage range and the input offset voltage are closely related. Regardless of whether the op-amp type is the CMOS (FET input) type or the bipolar type, there are commercially available op-amps of the full swing input type in which the input common-mode voltage range is extended from VEE to VCC . Since such op-amps can secure the input dynamic range even with a low supply voltage, they are ideal for applications operated at a low voltage, such as mobile devices.



(b) Input common-mode voltage vs. output voltage

Figure 3.4.3. Measurement circuit for input common-mode voltage

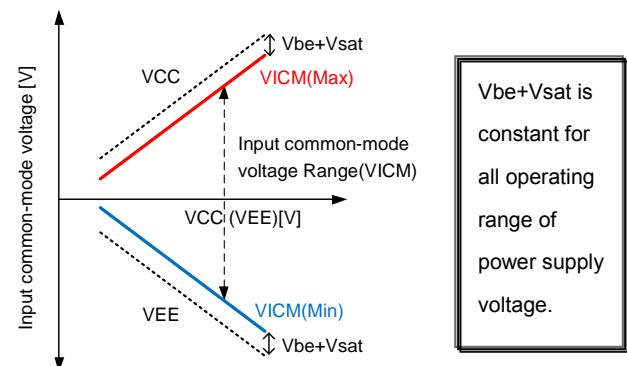
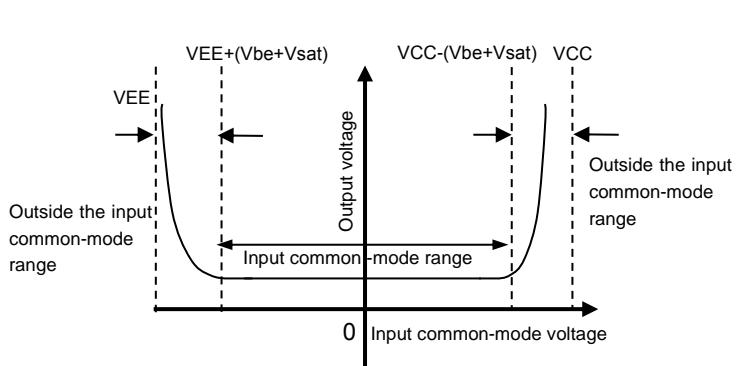


Figure 3.4.4. Input common-mode voltage range of 4558 series op-amp

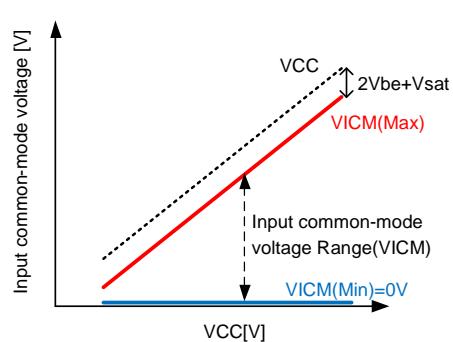
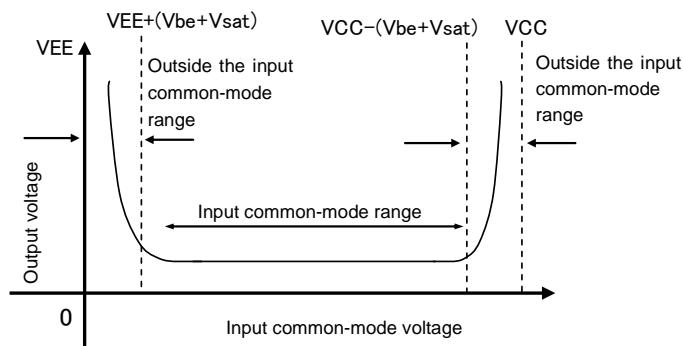


Figure 3.4.5. Input common-mode voltage range of 358/2904 series op-amp

3.5 Maximum output voltage (High/Low level output voltage)

The maximum output voltage (output voltage range) refers to the voltage range within which an op-amp can output. The voltage values can be separated into the maximum output voltage High (High level output voltage) and the maximum output voltage Low (Low level output voltage).

The output voltage range is limited by the output circuit configuration, the supply voltage, and the load condition (the amount of output current).

Next, we explain the output voltage range of the 4558 series low noise op-amp, which is the most standard dual power supply op-amp.

As we mentioned, the output voltage range depends on the output circuit configuration. The limit is imposed because a certain voltage is required for the elements that constitute the circuit, such as transistors, to operate normally.

Figure 3.5.1 shows the output equivalent circuit diagram for the 4558 series op-amp. First, we consider the maximum output voltage High. There are transistors Q1 and Q2 and output protection resistor R1 along the path from the output terminal to the VCC terminal. The voltage necessary for the normal operation is determined by the voltage between the collector and emitter of Q1 (V_{ce1}), the voltage between the base and emitter of Q2 (V_{be2}), and when the output source current (I_{source}) flows, the voltage drop from the Q2 emitter by $R1 \times I_{source}$. The output voltage range is reduced when the load (RL) is higher (the resistor value is smaller) and a larger source current flows.

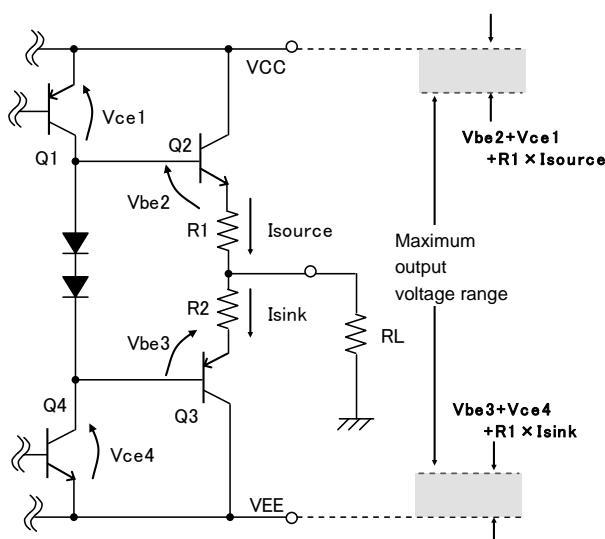


Figure 3.5.1. Output equivalent circuit diagram for 4558 series op-amp

The maximum output voltage High is described by the following equation.

Maximum output voltage High

$$= VCC - Vce1 - Vbe2 - (R1 \times I_{source}) \quad (3.5.1)$$

Next, we consider the maximum output voltage Low. There are transistors Q3 and Q4 and short circuit protection resistor R2 along the path from the output terminal to the VEE terminal. As in the case for the maximum output voltage High, the maximum output voltage Low is determined by the voltage between the collector and emitter of transistor Q4 (V_{ce4}), the voltage between the base and emitter of Q3 (V_{be3}), and when the output sink current (I_{sink}) flows, the voltage drop caused by protection resistor R2.

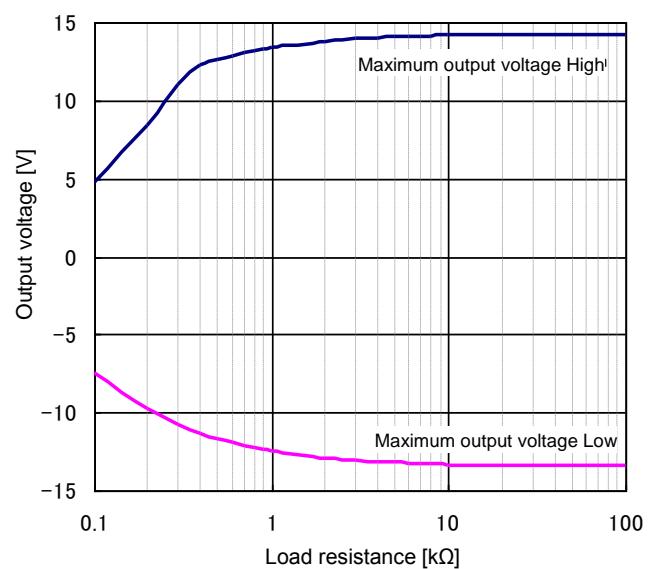
The maximum output voltage Low is described by the following equation.

Maximum output voltage Low

$$= VEE + Vce4 + Vbe3 + (R2 \times I_{sink}) \quad (3.5.2)$$

Figure 3.5.2 shows an example of the maximum output voltages for the 4558 series op-amp.

As shown in Figure 3.5.2, there exists dead zones on both the positive power supply (VCC) side and the negative power supply (VEE) side where the op-amp cannot operate.



VCC/VEE = +15 V/-15 V, Ta = 25°C, VRL = VCC/2

Figure 3.5.2. Example of maximum output voltage for 4558 series op-amp

Next, we consider the output voltage range of the 358/2904 series op-amp, which is the most standard single supply op-amp.

Figure 3.5.3 shows the output equivalent circuit diagram for the 358/2904 series op-amp. As for the maximum output voltage High, there are transistors Q1, Q2, and Q3, and current limit resistor R1 along the path from the output terminal to the VCC terminal. The voltage necessary for this circuit to operate is determined by the voltage between the collector and emitter of Q1 (V_{ce1}), the voltages between the base and emitter of Q2 (V_{be2}) and Q3 (V_{be3}), and the voltage drop due to the output source current (I_{source}) by $R1 \times I_{source}$. The output voltage range is reduced when the load (RL) is higher (the resistor value is smaller) and a larger source current flows.

The maximum output voltage High is described by the following equation.

Maximum output voltage High

$$= VCC - V_{ce1} - V_{be2} - V_{be3} - (R1 \times I_{source}) \quad (3.5.3)$$

Next, we consider the maximum output voltage Low. The 358/2904 series op-amps feature two routes from the output terminal to the VEE terminal. One is the path through transistors Q4 and Q5. The other is the path through Q6. The Q6 path has a structure in which a constant current of 40 μ A from the output terminal is always supplied by Q6 while the output voltage is Low. This constant current is referred to as the Low level sink current. When the output current is sufficiently smaller than 40 μ A, the output voltage Low is determined by the voltage between the collector and emitter of Q6 (V_{ce6}).

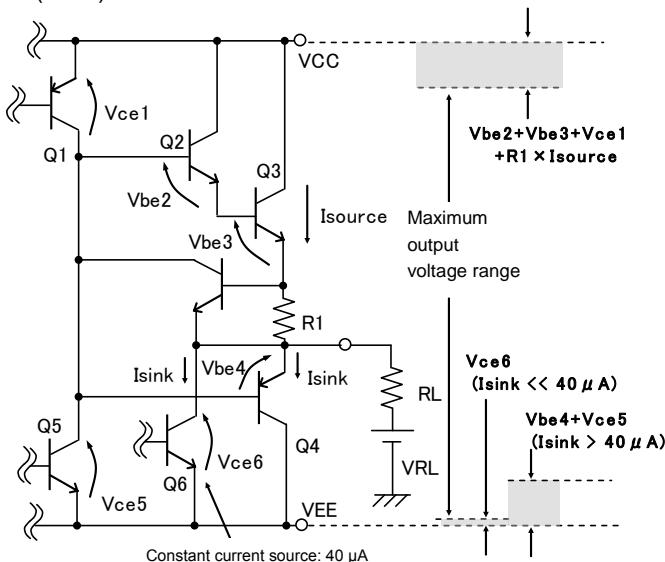


Figure 3.5.3. Output equivalent circuit for 358/2904 series op-amp

Since this Low level output voltage is very small (around 10 mV), the output voltage can be output nearly at the ground level. When the output sink current becomes larger than 40 μ A, the output sink current begins to flow into Q4. The voltage necessary for Q4 to operate is determined by the voltage between the collector and emitter of Q5 and the voltage between the base and emitter of Q4.

The maximum output voltage Low is described by the following equation.

Maximum output voltage Low

$$= VEE + V_{ce6} (Isink < 40 \mu A) \quad (3.5.4)$$

Maximum output voltage Low

$$= VEE + V_{ce5} + V_{be4} (Isink > 40 \mu A) \quad (3.5.5)$$

In this way, the different circuits operate in the 358/2904 series op-amps depending on the amount of the output sink current. Therefore, when the 358/2904 series op-amps are used with the load current value being near the Low level sink current of 40 μ A, the Low level voltage varies as the output circuits are switched, causing a distortion in the waveform.

This distortion is referred to as the crossover distortion. We explain this distortion in detail later.

Figure 3.5.4 shows an example of the maximum output voltages for the 358/2904 series op-amp. As shown in Figure 3.5.4, there exists a dead zone on the positive power supply (VCC) side where the op-amp cannot operate. On the negative power supply (VEE) side, the figure demonstrates that a voltage near VEE (ground) can be output in some conditions.

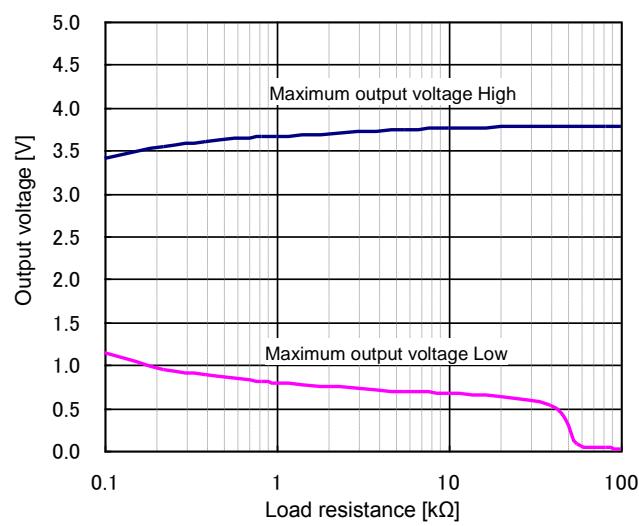


Figure 3.5.4. Example of maximum output voltage for 358/2904 series op-amp

3.6 Large signal voltage gain (open loop gain)

This refers to a gain with respect to the voltage difference between + and - input terminals of op-amps/comparators.

The standard values specified in the data sheet are the voltage gains with respect to a DC current. To minimize the gain error that is generated when a feedback circuit is configured, a high voltage gain (high open loop gain) is generally considered ideal. When the output voltage is V_{OUT} and the difference in input potentials is V_{IN_d} , the voltage gain (Av) is given by the following equation.

$$Av = \frac{V_{OUT}}{V_{IN_d}} \quad (3.6.1)$$

Take a non-inverting amplifier circuit shown in Figure 3.6.1 as an example to consider the gain error.

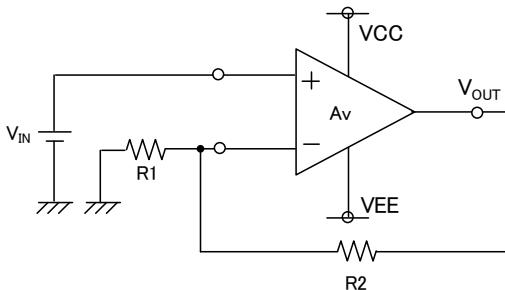


Figure 3.6.1. Non-inverting amplifier circuit

The output voltage (V_{OUT}) is given by the following equation.

$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right) \times \frac{1}{1 + \left(1 + \frac{R_2}{R_1}\right) \times \frac{1}{Av}} \times V_{IN} \quad (3.6.2)$$

In Equation (3.6.2), if we assume that Av is ∞ , the gain of the circuit is determined by $1 + R_2/R_1$. Therefore, a gain error occurs when the open loop gain (Av) has a finite value.

When $R_1 = 1 \text{ [k}\Omega\text{]}$, $R_2 = 10 \text{ [k}\Omega\text{]}$, $Av = 80 \text{ dB}$ (10,000 times), the amplification factor is 11 in an ideal situation.

$$V_{OUT} = (11) \times \frac{1}{1 + (11) \times \frac{1}{10000}} \times V_{IN} = \frac{11}{1.0011} \approx 10.988 \quad (3.6.3)$$

V_{OUT} is given by Equation (3.6.3), resulting in an amplification factor less than 11. The difference from the ideal situation is referred to as the gain error. Figure 3.6.2 shows the relation between the output voltage and the amplification factor of a large signal voltage gain.

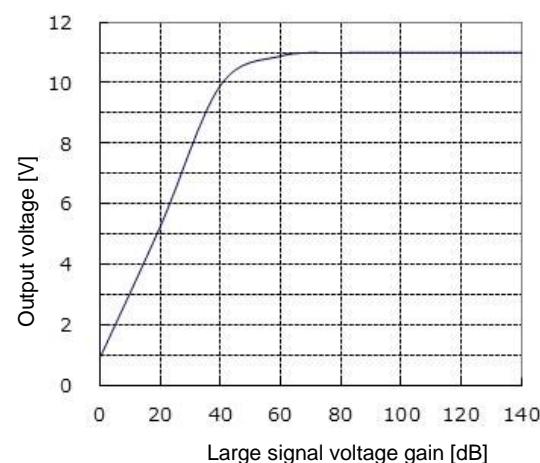


Figure 3.6.2. Relation between output voltage and large signal voltage gain

The voltage gain depends on the frequency. It is attenuated as the input signal frequency is increased. Therefore, the gain error increases at a higher frequency. Figure 3.6.3 shows an example of the frequency characteristic of the voltage gain in the circuit shown in Figure 3.6.1 (using a BA2904 op-amp).

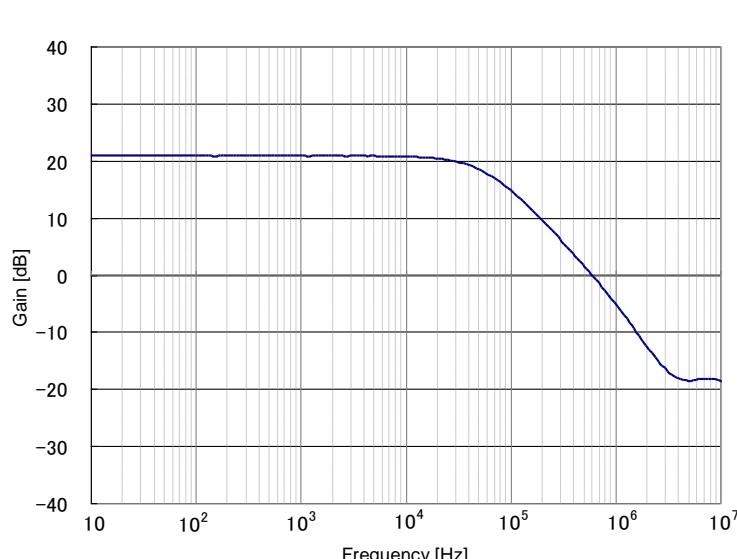


Figure 3.6.3. Frequency characteristic of the voltage gain

3.7 CMRR (Common Mode Rejection Ratio)

The common mode rejection ratio (CMRR_{AMP}) is the ratio of variation in the output voltage when the input common-mode voltage is varied, expressed in dB. Generally, the CMRR specified in the data sheet represents the ratio of the DC input common-mode voltage and the variation in the input offset voltage (ΔV_{IO}) when the DC input common-mode voltage is varied. This ratio expresses the value of the CMRR for the op-amp itself. We will explain the details in the next section.

$$CMRR_{AMP} = 20 \log \left(\frac{\Delta V_{ICM}}{\Delta V_{IO}} \right) \quad (3.7.1)$$

Next, we explain a view about the common mode rejection ratio when an amplifier circuit is configured.

When an amplifier circuit is configured with external resistors, an error in resistance (pair mismatch) causes an offset voltage in the amplifier circuit. This offset voltage due to the resistance error affects the common mode rejection ratio in the same way that the input offset voltage of op-amps does. The CMRR_{RES} due to the resistance error in the amplifier circuit can be calculated with the following equation. Here, we suppose that the CMRR of the op-amp is ideal (CMRR_{AMP} = ∞). The error mentioned here is a mismatch between R1 and R3 as well as between R2 and R4.

G is the gain (R_2/R_1) of the amplifier circuit. Suppose that $CMRR_{RES} = G_{DIFF}/G_{CM}$, where G_{DIFF} is the amplification factor for the differential voltage and G_{CM} is the amplification factor for the common-mode voltage (the derivation is omitted).

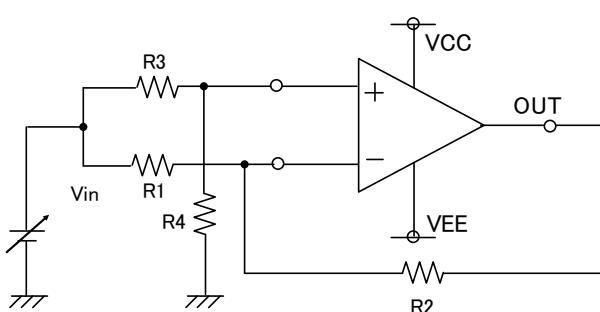
$$CMRR_{RES} = \frac{1+G}{1 - \frac{R_2 R_3}{R_1 R_4}} \quad (3.7.2)$$

In Figure 3.7.1 (a), the CMRR of the whole circuit (CMRR_{ALL}) is described by Equation (3.7.3).

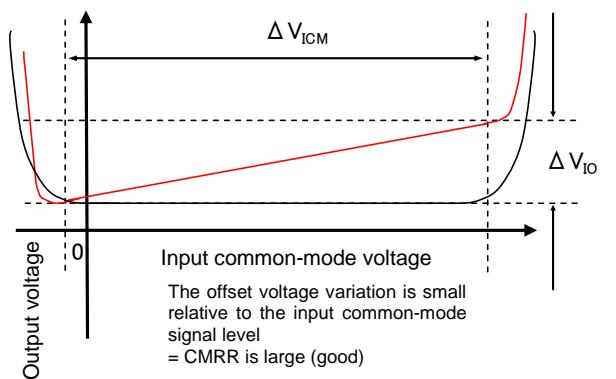
$$CMRR_{ALL} = \frac{1+G}{\frac{1+G}{CMRR_{AMP}} + \left(1 - \frac{R_2 R_3}{R_1 R_4} \right)} \quad (3.7.3)$$

Therefore, a resistance mismatch affects the common mode rejection ratio of an associated amplifier circuit. It can be seen that CMRR_{ALL} is limited even when an op-amp with a large CMRR (CMRR_{AMP}) is used.

In the next section, we further consider the meaning of the common mode rejection ratio of op-amps.



(a) Measurement circuit diagram



(b) Variation in the input offset voltage

Figure 3.7.1. Relation between input offset voltage and CMRR

Common mode rejection ratio of op-amps

Introductory books on circuit design define the CMRR of an op-amp itself as $CMRR = Ad/Ac$ expressed in dB, where Ad (the differential voltage gain) is the gain with respect to the difference in input voltages of the op-amp and Ac (the common-mode voltage gain) is the gain with respect to the input common-mode voltage. This definition corresponds to Equation (3.7.1).

Ideally, an op-amp should amplify the difference in voltages between its + and - input terminals by the gain of the amplifier. However, the differential voltage gain and the common-mode voltage gain are altered in an actual op-amp due to changes in the DC operating points (current and voltage) inside the circuit that are caused by a variation in the input common-mode voltage. As a result, the input offset voltage is varied and a variation in the output voltage is observed.

When the gain with respect to the difference in the input voltages is Ad (the differential voltage gain), the gain with respect to the input common-mode voltage is Ac (common-mode voltage gain), the potential of the + input terminal is V_{in_p} , and the potential of the - input terminal is V_{in_n} , the output voltage of the op-amp can be described by the following equations.

$$V_{OUT} = Ad \times (V_{in_p} - V_{in_n}) + Ac \times V_{ICM} \quad (3.7.4)$$

$$V_{OUT} = Ad \times \left((V_{in_p} - V_{in_n}) + \frac{Ac}{Ad} \times V_{ICM} \right) \quad (3.7.5)$$

V_{ICM} is the input common-mode voltage and equal to $(V_{in_p} + V_{in_n})/2$.

In Equation (3.7.5), the term, $(Ac/Ad) \times V_{IC}$, represents an error term due to the input common-mode voltage and can be considered the input offset voltage.

$$V_{IO} = \frac{Ac}{Ad} \times V_{ICM} \quad (3.7.6)$$

From Equation (3.7.6), a variation in the input offset voltage due to a variation in the input common-mode voltage is provided as follows.

$$\frac{\Delta V_{ICM}}{\Delta V_{IO}} = \frac{Ad}{Ac} = CMRR \quad (3.7.7)$$

Equation (3.7.7) shows that the ratio of the variations is equivalent to the ratio of the input common-mode voltage and

the input offset voltage as mentioned above.

As an example, we use Equation (3.7.7) to calculate the effect of a variation in the input common-mode voltage on the output.

We calculate V_{IO_10} when $V_{IO_0} = 1$ [mV] and $CMRR = 80$ [dB] = 10,000 [times], where V_{IO_10} is the input offset voltage when $V_{IC} = 10$ [V], V_{IO_0} is the offset voltage when $V_{IC} = 0$ [V], and V_{IC} is the input common-mode voltage.

$$CMRR = \frac{V_{IC_10} - V_{IC_0}}{V_{IO_10} - V_{IO_0}} \quad (3.7.8)$$

$$V_{IO_10} = \frac{10[V]}{CMRR[\text{times}]} + 1[mV] = 2[mV] \quad (3.7.9)$$

Therefore, when $CMRR = 80$ [dB], a variation of 10 [V] in the input common-mode voltage increases the input offset voltage by 1 [mV].

The next section explains the mechanism by which the input offset voltage is varied due to a variation in the input common-mode voltage.

Mechanism of the variation in the input offset voltage due to the input common-mode voltage (reference)

Figure 3.7.2 shows the equivalent circuit for a differential input stage. We explain the mechanism by which the input offset voltage is increased by a variation in the input common-mode voltage. First, we assume that the characteristics are identical between transistors M1 and M2 as well as between M3 and M4. This means that no input offset voltage is generated by the differential input stage or the active loads. Since the characteristics are identical, the voltages between the gate and source are equal and the currents flowing through differential input transistors M1 and M2 are equal. Next, since the characteristics of active loads M3 and M4 are identical, the currents flowing through the loads are equal. The identical currents and characteristics result in identical drain voltages between active loads M3 and M4. Therefore, we can consider that V_x and V_o is virtually short-circuited in small signal equivalent circuit 1 in Figure 3.7.2 (b). Based on this point, the small signal equivalent circuit is described as small signal equivalent circuit 2 in Figure 3.7.2 (c). Since we can consider that the transistor elements are connected in parallel to each other, it is possible to combine the circuits for simplification. The common-mode voltage gain is calculated with this circuit.

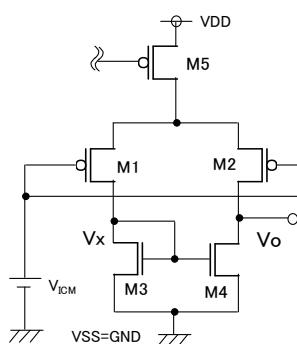
$$g_{d5}V + 2g_{m2}(V_{ICM} - V) + 2g_{d2}(V - V_o) = 0$$

$$2g_{m4}V_o + 2g_{d4}V_o + 2g_{m2}(V_{ICM} - V) + 2g_{d1}(V - V_o) = 0$$
(3.7.10)

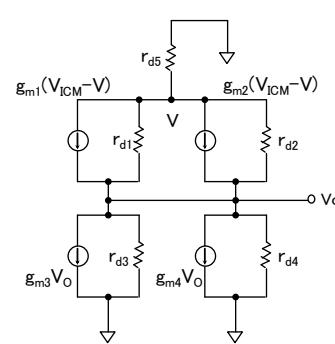
$$A_c = \frac{V_o}{V_{ICM}} = \frac{1}{2g_{m4}r_{d5}}$$
(3.7.11)

$$A_d = \frac{V_o}{V_{ind}} = g_{m1}(r_{d2} // r_{d4})$$
(3.7.12)

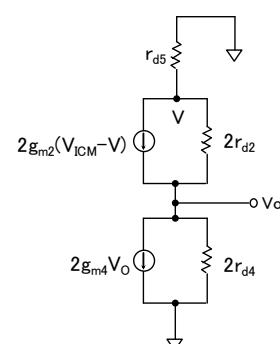
$$CMRR = \frac{A_d}{A_c} = \frac{V_{ICM}}{V_{ind}} = \frac{V_{ICM}}{V_{IO}} = 2g_{m4}g_{m1}r_{d5}(r_{d2} // r_{d4})$$
(3.7.13)



(a) Equivalent circuit for differential input circuit



(b) Small signal equivalent circuit 1



(c) Small signal equivalent circuit 2

For the calculation of common-mode voltage gain, g_m is the transconductance of transistors, r_d is the drain impedance, g_d is the drain conductance, V_{ICM} is the input common-mode voltage, and V is the drain voltage of M5.

In addition, $1/r_d = g_d$. Form an equation for nodes V_o and V . Arranging Equation (3.7.10) and using an approximation that $g_{m4}, g_{m2} \gg g_{d4}, g_{d2}$, Equation (3.7.11) is obtained (the derivation is omitted).

Equation (3.7.11) shows that the common-mode voltage gain (A_c) is determined by the impedance of transistor M5 and g_m of the active load. Next, the differential voltage gain can be described by Equation (3.7.12) (the derivation is omitted).

When the input offset voltage is V_{IO} , CMRR is calculated from Equations (3.7.11) and (3.7.12), resulting in Equation (3.7.13).

Thus, to obtain a smaller common-mode voltage gain (A_c), r_{d5} or g_{m4} needs to be larger. A larger r_{d5} means that the current flowing through transistor M5 is less likely to be affected by the input common-mode voltage. However, actual values of r_{d5} and g_{m4} are finite and CMRR is therefore limited. In other words, since CMRR is finite, the input offset voltage is varied due to the variation in the input common-mode voltage.

Figure 3.7.2. Equivalent circuit diagram for op-amp differential input stage

Next, we explain the frequency characteristic of the CMRR. The differential voltage gain shown in Equation (3.7.13) is the gain with respect to a given DC voltage. This gain actually has a frequency characteristic. As shown in Equation (3.7.13), the differential voltage gain of op-amps is closely related to the CMRR. The differential voltage gain of the op-amp is reduced at the rate of -6 dB/oct (= -20 dB/dec) as the frequency increases, due to the first pole of the differential input stage.

This causes a simultaneous reduction in the CMRR. Figure 3.7.3 shows the frequency characteristic of the CMRR. It is important to consider the frequency characteristic of the CMRR when actually using op-amps.

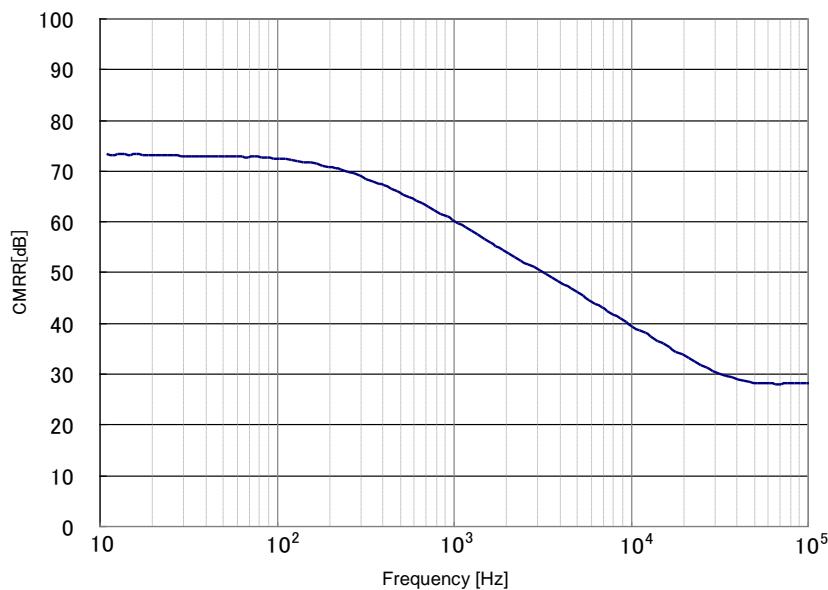


Figure 3.7.3. CMRR frequency characteristic

3.8 PSRR (Power Supply Rejection Ratio)

The power supply rejection ratio (PSRR) is the amount of variation in the input offset voltage when the power supply voltage is varied, expressed as a ratio. Generally, the standard values described in the data sheet are the ratio of variation in the input offset voltage when a DC voltage supply is varied.

$$PSRR = 20 \log \left(\frac{\Delta V_{CC}}{\Delta V_{IO}} \right) \quad (3.8.1)$$

PSRR is generally defined by $PSRR = Ad/Ap$, where Ad is the gain with respect to the difference in the input voltages of the amplifier (differential voltage gain) and Ap is the gain with respect to the power supply voltage. This definition has the same meaning as Equation (3.8.1).

Ideally, an op-amp should increase the difference in voltages between its + and - input terminals by the gain of the amplifier. However, the differential voltage gain and the power supply variation gain are altered in an actual op-amp due to changes in the DC operating points (current and voltage) inside the circuit that are caused by changing the power supply voltage. As a result, the input offset voltage varies and a variation in the output voltage is observed.

When the gain with respect to the difference in the input voltages is Ad (the differential voltage gain), the gain with respect to the power supply voltage is Ap (power supply voltage gain), the potential of the + input terminal is V_{in_p} , and the potential of the - input terminal is V_{in_n} , the output voltage of the op-amp can be expressed by the following equations.

$$V_{OUT} = Ad \times (V_{in_p} - V_{in_n}) + Ap \times VCC \quad (3.8.2)$$

$$V_{OUT} = Ad \times \left((V_{in_p} - V_{in_n}) + \frac{Ap}{Ad} \times VCC \right) \quad (3.8.3)$$

In Equation (3.8.3), the term, $(Ap/Ad) \times VCC$, represents an error term due to the power supply voltage and can be considered the input offset voltage.

$$V_{IO} = \frac{Ap}{Ad} \times VCC \quad (3.8.4)$$

From this relational expression, the variation in the input offset voltage with respect to the variation in the power supply voltage is described by Equation (3.8.5). Therefore, PSRR is

equivalent to the ratio of the variation in the input offset voltage with respect to the power supply voltage variation mentioned above.

$$\frac{\Delta V_{CC}}{\Delta V_{IO}} = \frac{Ad}{Ap} = PSRR \quad (3.8.5)$$

As an example, we use Equation (3.8.5) to calculate V_{IO_20} when $V_{IO_10} = 1$ [mV], where V_{IO_20} and V_{IO_10} are the input offset voltages when $VCC = 20$ [V] and 10 [V], respectively. Suppose that $PSRR = 80$ [dB] (= 10,000 times).

$$PSRR = \frac{V_{CC_20} - V_{CC_10}}{V_{IO_20} - V_{IO_10}} = 10000[\text{times}] \quad (3.8.6)$$

$$V_{IO_10} = \frac{10[\text{V}]}{10000[\text{times}]} + 1[\text{mV}] = 2[\text{mV}] \quad (3.8.7)$$

Therefore, when $PSRR = 80$ [dB], a variation of 10 [V] in the power supply voltage increases the input offset voltage by 1 [mV].

When an amplifier circuit is configured, the error voltage that is multiplied by the gain of the amplifier circuit is output as an error in the output voltage.

When a non-inverting amplifier circuit with a gain of 100 [times] is configured, a variation of 10 [V] in the power supply voltage causes a variation of 100 [mV] in the output voltage.

Mechanism of the variation in the input offset voltage due to the power supply voltage (reference)

Figure 3.8.1 shows the equivalent circuit for a differential input stage. Now we will explain the mechanism by which the input offset voltage is increased by a variation in the power supply voltage. First, we assume that the characteristics are identical between transistors M1 and M2 as well as between M3 and M4. This means that no input offset voltage is generated by the differential input stage or the active loads. Since the characteristics are identical, the voltages between the gate and source are equal and the currents flowing through differential input transistors M1 and M2 are equal. However, when considering the power supply voltage variation, the variation in the power supply also alters the input common-mode voltage range. Therefore, the input voltage level should always be adjusted to a value in the middle of the input common-mode voltage range.

Next, since the characteristics of active loads M3 and M4 are identical, the currents flowing through the loads are equal. The identical currents and characteristics result in identical drain voltages between active loads M3 and M4. Therefore, we can consider that V_x and V_o is virtually short-circuited in small signal equivalent circuit 1 in Figure 3.8.1 (b). Based on this point, the small signal equivalent circuit is described as small signal equivalent circuit 2 in Figure 3.8.1 (c).

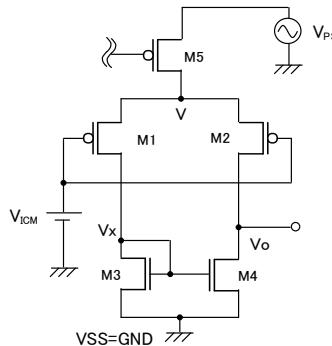
$$g_{d5}(V - V_{ps}) + 2g_{m1}(V_{ICM} - V) + 2g_{d1}(V - V_o) = 0$$

$$2g_{m4}V_o + 2g_{d4}V_o + 2g_{m1}(V_{ICM} - V) + 2g_{d1}(V - V_o) = 0$$

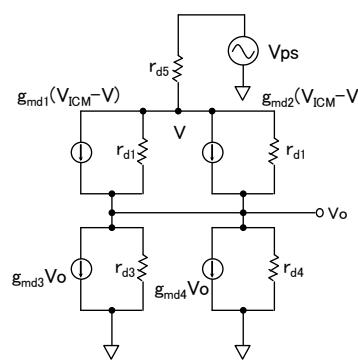
$$A_p = \frac{V_o}{V_{ds}} = \frac{g_{e5}}{2g_{m4}} = \frac{1}{2g_{m4}r_5}$$

$$A_d = \frac{V_o}{V_{ind}} = g_{m1}(r_{d2} // r_{d4})$$

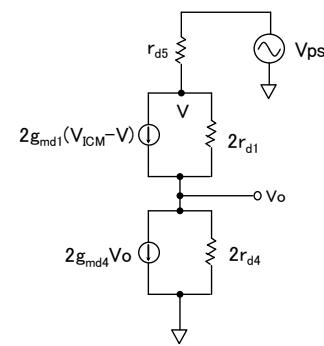
$$PSRR = \frac{A_d}{A_p} = \frac{V_{ds}}{V_{ind}} = \frac{V_{ds}}{V_{IO}} 2g_{m4}r_5g_{m1}(r_{d2} // r_{d4})$$



(a) Equivalent circuit for differential input circuit



(b) Small signal equivalent circuit 1



(c) Small signal equivalent circuit 2

Since we can consider that the transistor elements are connected in parallel to each other, it is possible to combine the circuits for simplification. The power supply voltage gain is calculated with this circuit. For the calculation of power supply voltage gain, g_m is the transconductance of transistors, r_d is the drain impedance, g_d is the drain conductance, V_{ICM} is the input common-mode voltage, and V is the drain voltage of M5. In addition, $1/r_d = g_d$. Form Equation (3.8.8) for nodes V_o and V .

Arranging Equation (3.8.8) and using approximations that $V - V_{ps} = V_{ds}$ and $g_{m4}, g_{m2} \gg g_{d4}, g_{d2}$, Equation (3.8.9) is obtained (the process is omitted).

Equation (3.8.9) shows that the power supply voltage gain (A_p) is determined by the impedance of transistor M5 and g_m of the active load. Next, the differential voltage gain can be described by Equation (3.8.10). (The derivation is omitted.)

When the input offset voltage is V_{IO} , PSRR is calculated from Equations (3.8.9) and (3.8.10), resulting in Equation (3.8.11). Thus, to obtain a smaller power supply voltage gain (A_p), r_{d5} or g_{m4} needs to be larger. A larger r_{d5} means that the current flowing through transistor M5 is less likely to be affected by the input common-mode voltage. However, actual values of r_{d5} and g_{m4} are finite and PSRR is therefore limited. In other words, since the PSRR is finite, the input offset voltage is varied due to the variation in the input common-mode voltage.

(3.8.8)

(3.8.9)

(3.8.10)

(3.8.11)

Figure 3.8.1. Equivalent circuit diagram for op-amp differential input stage

As with the CMRR, the value of the PSRR is reduced as the input signal frequency increases. As shown in Equation (3.8.11), the differential voltage gain of op-amps is closely related to the PSRR. The differential voltage gain of the op-amp is reduced at the rate of -6 dB/oct (= -20 dB/dec) as the frequency increases, due to the first pole of the differential input stage. This causes a simultaneous reduction in the PSRR.

Therefore, any ripple noise with a high frequency on the power supply line will alter the output voltage significantly, causing output noise. As a countermeasure against power supply noise, you can connect a bypass capacitor near the power supply terminal of op-amps. Figure 3.8.2 shows an example of the frequency characteristic of the power supply rejection ratio.

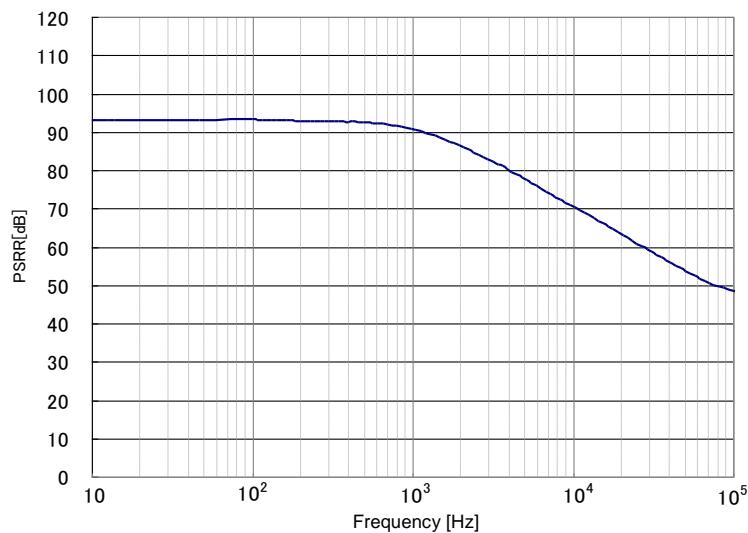


Figure 3.8.2. PSRR frequency characteristic

3.9 SR (Slew Rate)

The slew rate is a parameter that represents the operating speed of op-amps. This parameter describes the rate of variation that the output voltage can undertake per specified unit time. For example, 1 [V/μs] means that the voltage can be varied by 1 [V] in 1 [μs].

An ideal op-amp can exactly follow any input signal and output the output signal. However, the slew rate sets limits on the output in practice. The slew rate describes how much the output voltage can change per unit time when a rectangular wave pulse with a steep rise and fall is input. Equation (3.9.1) shows the definition of slew rate.

The slew rates for the rise and fall are calculated with Equation (3.9.1).

$$SR_r = \frac{\Delta V}{\Delta T_r} \quad SR_f = \frac{\Delta V}{\Delta T_f} \quad (3.9.1)$$

The slew rate specified in the data sheet is based on the rate for either "rise" or "fall", whichever is the slower. The slew rate represents the maximum slope of the op-amp output signal. When the signal has a steeper change, the output waveform cannot follow the signal and will be distorted. Since the slew rate is the rate of output change, it is not affected when an amplifier circuit is configured.

Consider the meaning of the slew rate when an op-amp is actually used. Op-amps are used for the amplification of both DC and AC signals. As mentioned above, since op-amps have a limit on their response speed, there are signals that op-amps cannot handle. We explain a voltage follower configuration shown in Figure 3.9.1. For a given DC voltage input, limits are set by the input and output voltage ranges. For an AC signal with a frequency, additional limits are set by the gain bandwidth product and the slew rate. Here, we consider the relation between the amplitude and frequency, namely the slew rate.

We calculate the maximum frequency that an op-amp can output. To determine the maximum frequency, we calculate the slew rate that is required to output a waveform as shown in Figure 3.9.2.

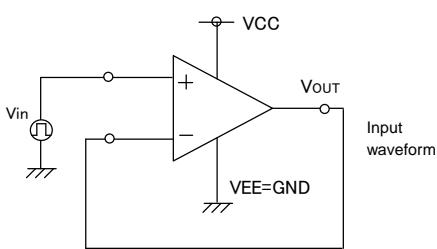


Figure 3.9.1. Example of slew rate measurement circuit and waveforms

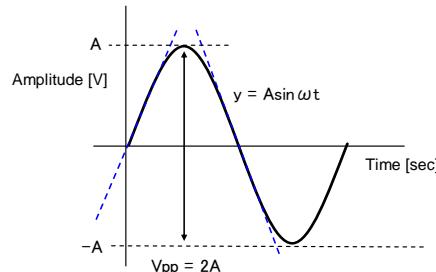


Figure 3.9.2 Waveform of a sine wave

$$y = A \sin \omega t \quad (3.9.2)$$

Since the slew rate is the slope of the tangent to the sine wave, we differentiate Equation (3.9.2).

$$\frac{dy}{dt} = A \omega \cos \omega t \quad \omega t = 0 \quad (3.9.3)$$

From Equation (3.9.3), the slew rate is described by

$$SR = A \omega \quad \omega = 2\pi f \quad (3.9.4)$$

In addition, since the amplitude of the sine wave is given by $V_{pp} = 2A$ (peak-to-peak), Equation (3.9.4) can be rearranged as follows.

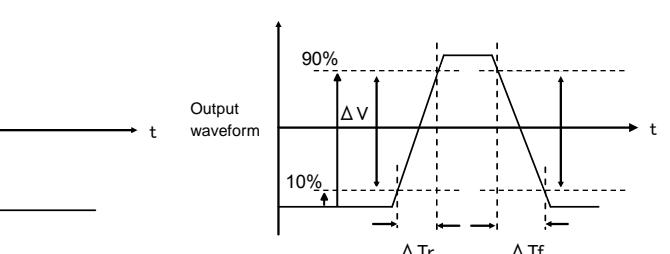
$$f = \frac{SR}{2\pi \times A} = \frac{SR}{\pi V_{pp}} [\text{Hz}] \quad V_{pp} = \frac{SR}{\pi f} [\text{V}] \quad (3.9.5)$$

This frequency f is referred to as the full power bandwidth. These are the relations between the frequency and the amplitude that an op-amp can output (within the output voltage range) when no amplification factor is set for the op-amp—in other words, when the op-amp is operated as a voltage follower.

Example: Calculate the frequency at which an op-amp with $SR = 1 \text{ V/μs}$ can output a signal of 1 Vpp.

$$f = \frac{SR}{\pi V_{pp}} = \frac{1}{10^{-6}} \times \frac{1}{\pi \times 1} = 318.4 \text{ kHz} \quad (3.9.6)$$

When the frequency increases such that it is higher than the frequency calculated with Equation (3.9.6) while the amplitude is kept constant, the slew rate restricts the waveform, distorting the sine wave into a triangular wave.



3.10 Frequency characteristics of op-amp

Term descriptions

- Gain frequency characteristic:

The gain of an amplifier circuit has a frequency characteristic.

This characteristic is determined by the phase compensation capacitance and terminal capacitance of the inside of the op-amp, the parasitic capacitance of the circuit board, and the circuit constant.

- Phase frequency characteristic:

This characteristic represents the difference in phase between the input and output waveforms of the op-amp. Similarly to the gain, it is affected by the characteristics, the circuit constant, and the parasitic capacitance of the op-amp.

- Open loop gain (A_v):

The open loop gain represents the voltage gain for direct current.

- Unity gain frequency (f_T):

The frequency at which the gain is 0 dB (1times) is referred to as the unity gain frequency.

- Gain bandwidth product (GBW):

The frequency characteristic of an amplifier circuit shows an attenuation at the rate of -6 dB/oct per pole. The product of the gain and frequency at an arbitrary point in the range

where the -6 dB/oct attenuation occurs is referred to as the gain bandwidth product. This product represents the frequency bandwidth within which the op-amp can be used for small signals.

Gain bandwidth product [Hz] = Frequency [Hz] \times Gain [times]

- First pole:

This is the first of several poles. The amplitude is attenuated at the rate of -6 dB/oct per single pole. Phase delay begins to increase when the frequency reaches 1/10 of the first pole frequency. The delay increases by 45deg at the first pole frequency and by 90deg when the frequency reaches 10 times that of the first pole frequency.

- Second pole:

This is the second of several poles. The attenuation rate increases to -12 dB/oct. In addition to the phase delay from the first pole, the phase delay further increases by 45deg at the second pole frequency and by 90deg when the frequency reaches 10 times that of the second pole frequency.

Note: -6 dB/oct = attenuation by -6 dB when the frequency is doubled. (oct = octave)

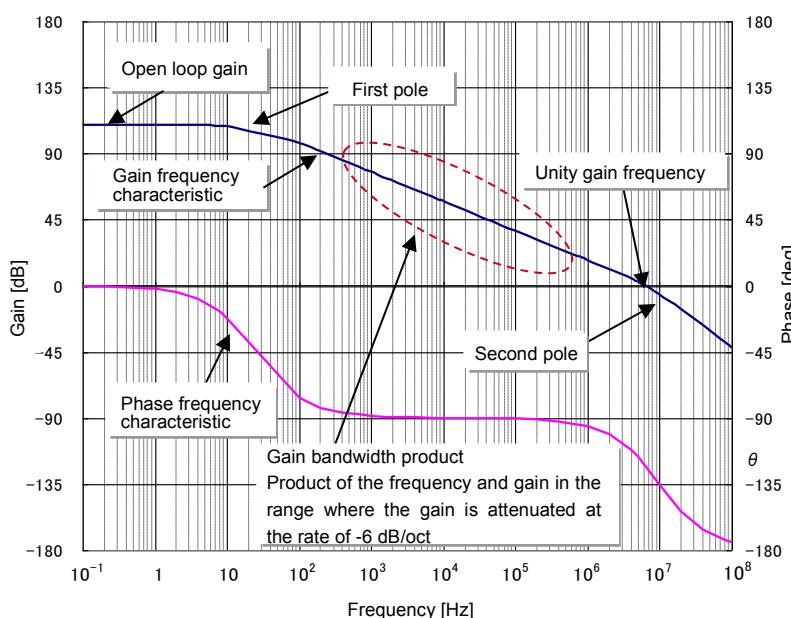


Figure 3.10.1. Example of open loop frequency characteristics of op-amp

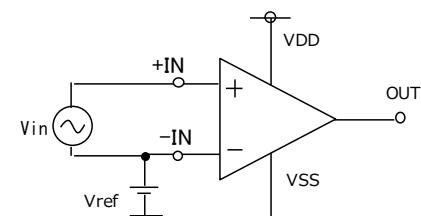


Figure 3.10.2. Measurement circuit
(schematic diagram)

- Phase margin:

The difference in phase between the input and output signals at the frequency where the gain is 0 dB (1times) is referred to as the phase margin. The phase margin is an indicator of the margin level and is designed to have a value between 40deg and 60deg.

In an inverting amplifier circuit, the difference in phase between the input and output θ_1 is the gain margin. The phase of an inverting amplifier circuit begins at 180deg.

Since the phase of a non-inverting amplifier circuit begins at 0deg, the gain margin is the margin level from 180deg, namely 180deg + θ_2

Phase margin of inverting amplifier circuit: θ_1

Phase margin of non-inverting amplifier circuit: 180deg + θ_2

- Gain margin:

The gain margin is the margin level for the gain to 0 dB at the frequency where the phase delay reaches 180deg. Typically, the gain margin is designed to be 7 dB or larger. The gain margin is used as an indicator of the margin level similarly to the phase margin.

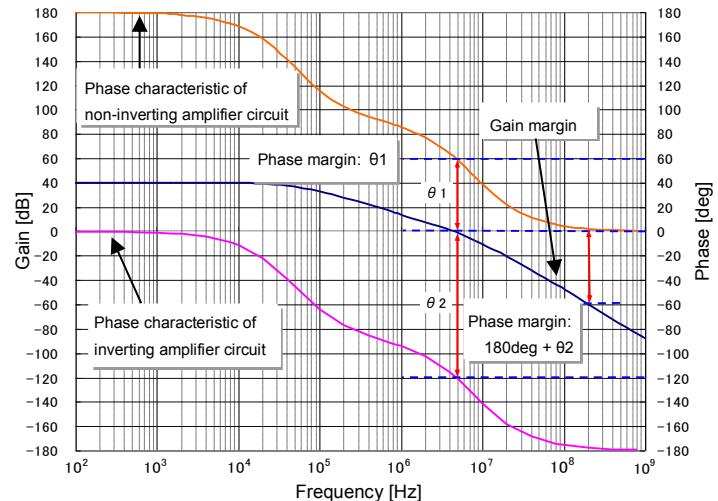


Figure 3.10.3. Example of frequency characteristics of inverting (non-inverting) amplifier circuit 40 dB* (100 times)

* The open loop gain of an op-amp is very large near a direct current (100 dB or larger). Applying a DC feedback from the output with a resistor stabilizes the output DC voltage. When measuring the gain frequency characteristics, the gain of the inverting or non-inverting amplifier circuit is set to about 40 dB in order to perform the measurement stably. Since the characteristics at frequencies higher than the first pole frequency range are equivalent, the phase and gain margins can be read from this graph.

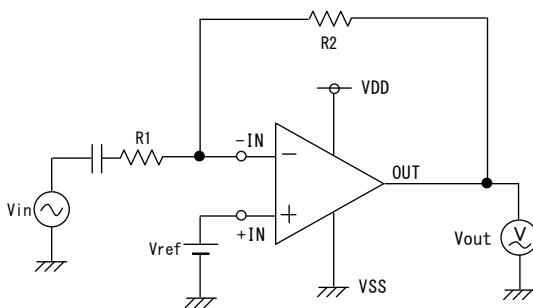


Figure 3.10.4. Inverting amplifier circuit

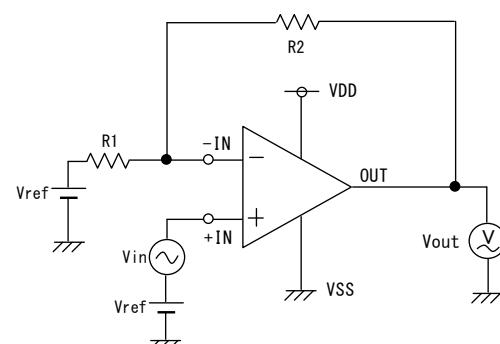


Figure 3.10.5. Non-inverting amplifier circuit

3.11 Phase delay and oscillation

This section describes one of the most general concepts for oscillations caused by Phase delay, the Barkhausen stability criterion.

The transfer function of a negative feedback circuit is determined in Figure 6.

$$A(s)(V_{in} - V_{in-}) = V_{out}$$

$$V_{in-} = \beta V_{out}$$

From the two equations above, the transfer function is determined as follows.

$$\frac{V_{out}}{V_{in}} = \frac{A(s)}{1 + \beta A(s)}$$

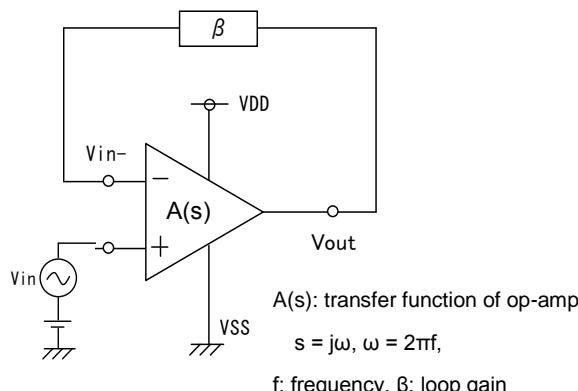


Figure 3.11.1. Negative feedback circuit

- When the phase is delayed by 180deg, the condition becomes identical to the state when a positive feedback is applied, causing an oscillation.

We focus on the denominator of the transfer function, $1 + \beta A(s)$.

When $\beta A(s) = -1$, the denominator is zero and the gain becomes infinity. This means that the transfer function diverges when $\beta A(s) = -1$.

In other words, $\beta A(s) = -1$ implies that the signal returned via a negative feedback is inverted (phase delay of 180deg), equivalent to the condition when a positive feedback is applied. Therefore, the circuit becomes unstable, causing an oscillation.

The following are a summary of oscillation conditions when the loop gain is 1times. (The loop gain of 1times represents an unity feedback.)

$$|\beta A(s)| = 1$$

$$\angle \beta A(s) = -180\text{deg}$$

Here $\angle \beta A(s)$ is the phase delay. When $s = j\omega_1$ and the loop gain $\beta A(\omega_1) = 1$, a phase delay of 180deg causes an oscillation with the angular frequency of ω_1 .

- There are two indicators of stability: the phase and gain margins. The phase margin indicates how much margin remains from the phase delay of 180deg when the gain is unity (0 dB). The gain margin indicates how much the gain is attenuated from unity when the phase delay is 180deg (phase margin of 0deg).

The phase delay is caused by the presence of the poles. We explain the reasoning using the frequency characteristics of an RC filter as an example.

Consider the transfer function of an RC filter as shown in Figure 3.11.2. Figure 3.11.3. shows that a pole is caused by capacitance in the transfer function (the first characteristic). This pole produces a phase delay of 45deg at the pole frequency f_c , and a phase delay of about 90deg when the frequency is about 10times that of the pole frequency.

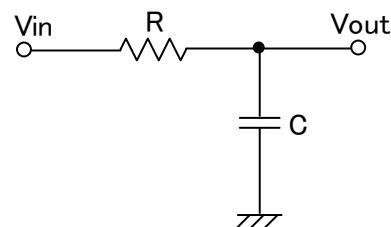


Figure 3.11.2. RC filter circuit

- One pole produces a phase delay of 90deg.
- The pole frequency depends on the capacitance value.
- Even with a high pole frequency, the phase begins to delay when the frequency reaches 1/10 of the pole frequency.

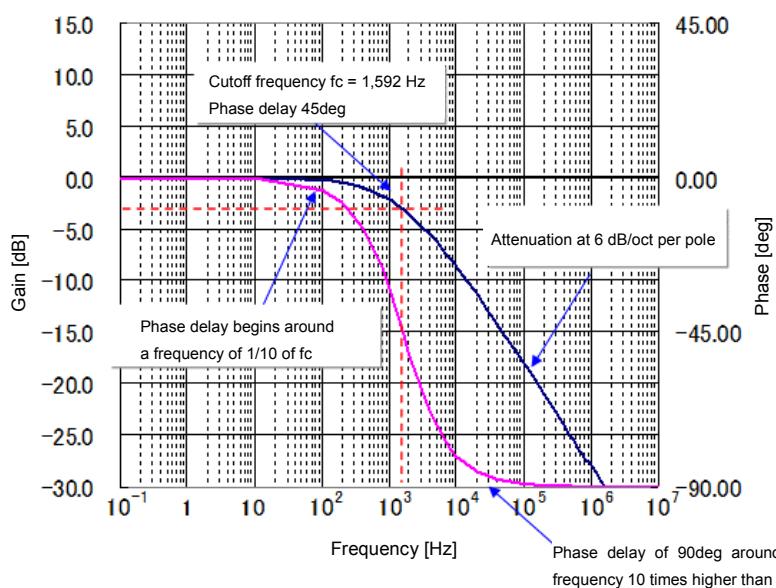


Figure 3.11.3. Frequency characteristics of RC filter

$$R = 1\text{k}\Omega, 0.1 \mu\text{F}, f_c = 1,592 \text{ Hz}$$

Transfer function of RC filter

$$\frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{1}{1 + j\omega RC}$$

Signal amplitude

$$H(\omega) = \frac{1}{\sqrt{1 + (\omega RC)^2}}$$

Phase

$$\theta = -\text{ArcTan}(\omega RC)$$

From the transfer function of the RC filter, the pole and cutoff frequencies are described as follows.

$$\omega_0 = \frac{1}{RC} \quad f_c = \frac{1}{2\pi RC}$$

3.12 Cause of phase delay in op-amp

We consider the causes of phase delay in op-amps, including the load capacitance.

From the transfer function of the circuit in Figure 9, we explain the cause of phase delay for an unity feedback circuit (voltage follower), which is most susceptible to oscillations.

$$A(s)(V_{in} - V_{o1}) = V_o$$

$$V_{o1} = \frac{1}{\frac{sC_p}{r_o + \frac{1}{sC_p}}} = \frac{1}{1 + r_o C_p s} V_o$$

From the equations above, the transfer function is described as follows when the output impedance (r_o) and the terminal capacitance are taken into account (C_p represents the total of parasitic capacitances).

$$\frac{V_{o1}}{V_{in}} = \frac{A(s)}{1 + r_o C_p s + A(s)} = \frac{1}{1 + \frac{1 + C_p r_o s}{A(s)}}$$

A pole is formed by C_p and r_o .

This effect is considered in the op-amp design.

In the equation above, assuming $C_p = C_p + C_L$ gives the transfer function when the load capacitance is connected.

$$\frac{V_{o1}}{V_{in}} = \frac{A(s)}{1 + r_o (C_p + C_L) s + A(s)} = \frac{1}{1 + \frac{1 + (C_p + C_L) r_o s}{A(s)}}$$

A pole is formed by $C_p + C_L$ and r_o .

C_p varies little since it is the parasitic capacitance inside the IC. However, the frequency where the pole occurs is reduced if the load capacitance C_L is large.

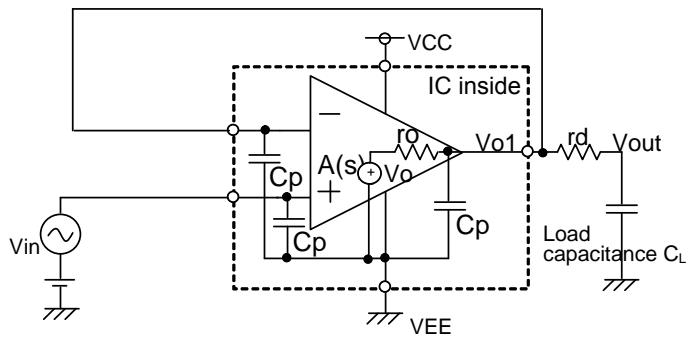


Figure 3.12.1. Unity feedback circuit

$A(s)$: transfer function of op-amp, $s = j\omega$, $\omega = 2\pi f$

f : frequency, r_o : output impedance,

C_p : parasitic capacitance of terminal, C_L : load capacitance

- Pole caused by the output impedance and the parasitic capacitance of the terminals
- Pole caused by the output impedance and the load capacitance
(intentionally provided)
- Pole caused by the feedback resistor and the parasitic capacitance of the input terminal when an amplifier circuit is configured

3.13 Stability confirmation method (amplifier circuit)

As an actual example, we show the variations in the phase and frequency characteristics according to the value of the load capacitance C_L for the BA2904.

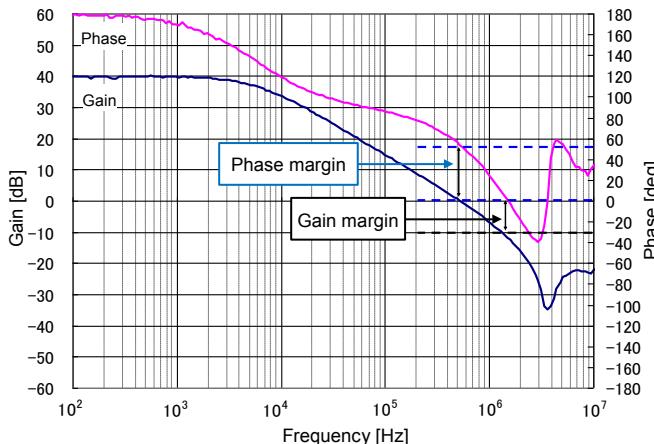


Figure 3.13.1. Frequency characteristics of BA2904 ($C_L = 25 \text{ pF}$)

- When $C_L = 25 \text{ pF}$

Phase margin: 55deg → the phase when the gain is 0 dB
Gain margin: -10 dB → the gain when the phase is 0deg

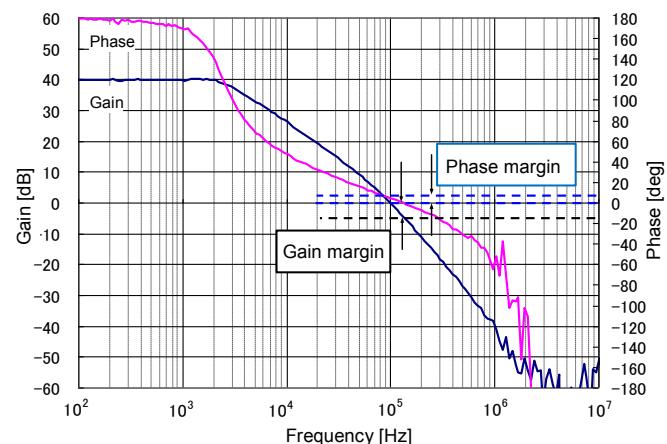


Figure 3.13.2. Frequency characteristics of BA2904 ($C_L = 0.01 \mu\text{F}$)

- When $C_L = 0.01 \mu\text{F}$

Phase margin: 7deg → the phase when the gain is 0 dB
Gain margin: -5 dB → the gain when the phase is 0deg
Although the phase margin is small, no oscillation occurs.

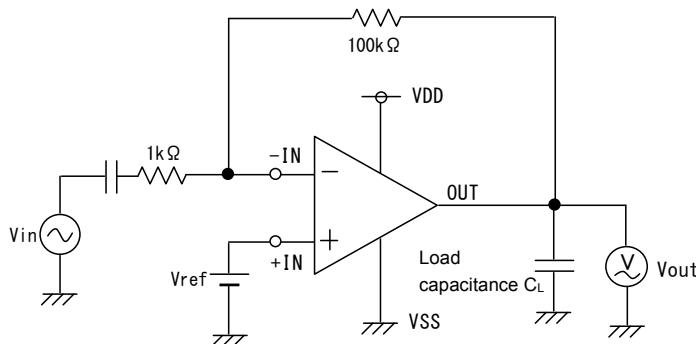


Figure 3.13.3. Inverting amplifier circuit of 40 dB (100 times)

- The oscillation stability of op-amps is confirmed with the phase and gain margins.
- In an inverting amplifier circuit, the phase margin is the phase when the gain is 0 dB since the phase begins from 180deg.
- In a non-inverting amplifier circuit, the phase margin is the difference between 180deg and the phase value when the gain is 0 dB since the phase begins from 0deg.
- Considering factors such as variations or temperature change, the phase margin is designed to be 35deg or larger, and the gain margin -7 dB or smaller.

3.14 Stability confirmation method (unity feedback circuit/voltage follower)

We review the idea of phase margin.

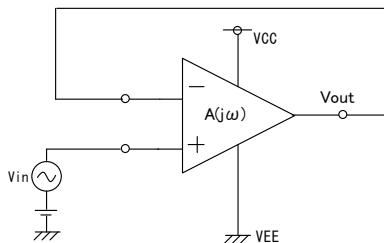


Figure 3.14.1. Overall feedback circuit

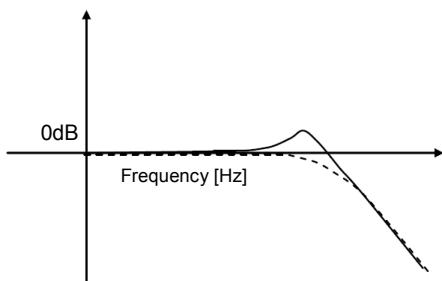


Figure 3.14.2. Measurement result

- The phase margin indicates how much margin remains from the phase delay of 180deg when the gain is unity (0 dB).
- The gain margin indicates how much the gain is attenuated from unity when the phase delay is 180deg (phase margin of 0deg).

The methods that we have explained so far cannot confirm the phase margin in an unity feedback circuit (gain of 0 dB). When the circuit becomes less stable, a peak gain appears in the frequency characteristic as shown in Figure 14. The phase margin is calculated from the size of the produced peak using the transfer function.

Transfer function of a voltage follower (unity feedback circuit)

$$\frac{V_{out}}{V_{in}}(j\omega) = \frac{A(j\omega)}{1 + \beta A(j\omega)}$$

$A(j\omega)$ is expressed in complex form and substituted in the transfer function.

$$A(j\omega) = \exp(j\theta)$$

$$\frac{V_{out}}{V_{in}}(j\theta) = \frac{\frac{1}{\beta} \exp(j\theta)}{\frac{1}{\beta} + \exp(j\theta)} = \frac{\frac{1}{\beta} (\cos \theta + j \sin \theta)}{\frac{1}{\beta} + \cos \theta + j \sin \theta}$$

Figure 3.14.3. shows the result of the calculation when the following values are substituted in the above equations.

$$\theta(\omega_1) = -175\text{deg} (5\text{deg}), \theta(\omega_2) = -135\text{deg} (45\text{deg}), \theta(\omega_3) = -120\text{deg} (60\text{deg}), \beta=1.$$

As the result shows in Figure 3.14.3, the phase margin of 60deg corresponds to a peak of 0 dB, giving an ideal condition

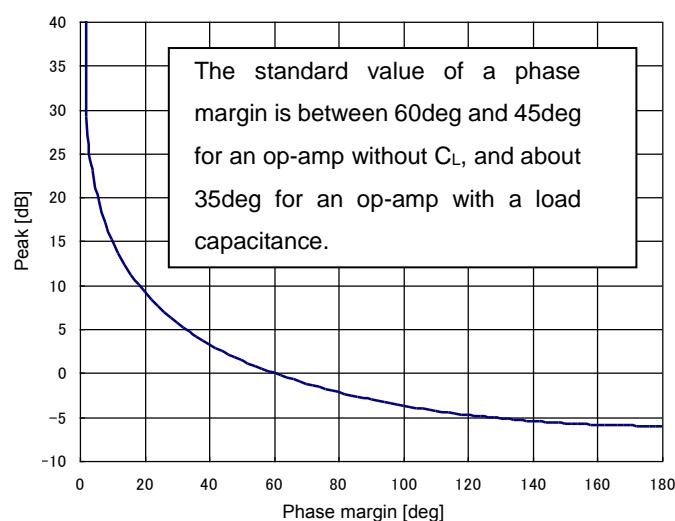


Figure 3.14.3. Result of gain peak calculation

Phase margin	Result of calculation [times]	Peak [dB]
5deg	11.5	21
45deg	1.3	2
60deg	1	0

- By measuring the frequency characteristics of a voltage follower, the phase margin can be calculated from the gain peak.
- This method is applicable to any types of general op-amps.
- When the phase margin is small, the occurrence of oscillation is actually confirmed using an oscilloscope or other instruments.

3.15 Summary of stability confirmation method

When an amplifier circuit is configured

- Oscillation in an amplifier circuit is confirmed by measuring the phase frequency characteristic and checking the phase and gain margins.
- In an inverting amplifier circuit, the reading of the phase margin is the phase when the gain is 0 dB since the phase begins from 180deg.
- In a non-inverting amplifier circuit, the phase margin is the difference between the phase when the gain is 0 dB and 180deg since the phase begins from 0deg.
- Considering factors such as variations or temperature change, the phase margin is designed to be 35deg or larger as a standard, and the gain margin -7 dB or smaller. (Generally, the phase margin is designed to be between 60deg and 40deg for an op-amp alone.)

3.16 Countermeasures against oscillation by load capacitance (output isolation resistor 1)

Basically, it is possible to prevent oscillation by satisfying the conditions to avoid oscillation as described in the previous sections. In this section, however, we explain countermeasures against oscillation when a capacitor with a large capacitance is connected to the output terminal.

We calculate the transfer function in Figure 3.16.1.

$$A(s)(V_{in} - V_{o1}) = V_o$$

$$V_{o1} = \frac{1}{r_o + \frac{1}{sC_p}} = \frac{1}{1 + r_o C_p s} V_o$$

$$\frac{V_{o1}}{V_{in}} = \frac{A(s)}{1 + r_o C_p s + A(s)} = \frac{1}{1 + \frac{1 + C_p r_o s}{A(s)}}$$

$$\frac{V_{out}}{V_{o1}} = \frac{1}{1 + r_d C_L s}$$

$$\frac{V_{o1}}{V_{in}} \frac{V_{out}}{V_{o1}} = \frac{A(s)}{1 + r_o C_p s + A(s)} \frac{1}{(1 + r_d C_L s)}$$

When an unity feedback circuit (voltage follower) is configured

- By measuring the frequency characteristics between the input and output and checking the gain peak, the phase margin can be estimated from Figure 15 of this document.
- Figure 15 is applicable to any types of general op-amps.
- When the phase margin is small, the occurrence of oscillation should actually be confirmed.
- Considering factors such as variations or temperature change, the phase margin is designed to be 35deg or larger as a standard.

Since the confirmation of oscillation with the calculations above is complicated, it is generally confirmed by experiment.

$$\frac{V_{out}}{V_{in}} = \frac{A(s)}{(1 + r_o C_p s + A(s)) (1 + r_d C_L s)}$$

While the transfer function without the isolation resistance calculated in Figure 3.12.1 is

$$\frac{V_{o1}}{V_{in}} = \frac{A(s)}{1 + r_o (C_p + C_L) s + A(s)}$$

When these two transfer functions are compared, it can be seen that the capacitance C_L that is connected to the output is separated into another transfer function with the dividing resistance r_d .

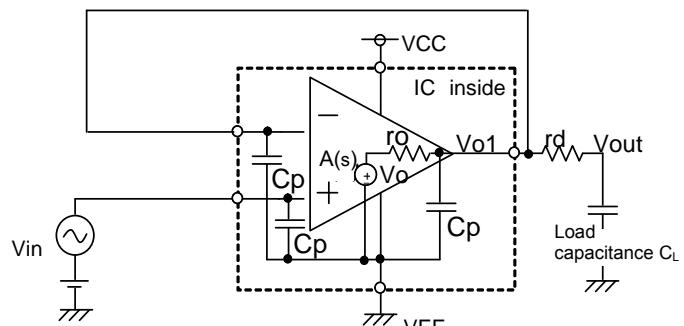


Figure 3.16.1. Example of output isolation resistor connection 1

- The value of the isolation resistor is set to between 50Ω to several hundred ohms, according to the capacitance and the required frequency bandwidth.
- Since a low pass filter is configured with r_d and C_L , the circuit bandwidth is reduced if the load capacitance is large.

3.17 Countermeasures against oscillation by load capacitance (output isolation resistor 2)

When using the method to insert an output isolation resistor as described in the previous section, the configuration of a low pass filter may be disadvantageous in some applications.

The peak gain is reduced by inserting a resistor in series to the capacitance.

We calculate the transfer function in Figure 3.17.1.

$$A(s)(V_{in} - V_{out}) = V_o$$

$$V_o = A(s)V_{in} - A(s)V_{out}$$

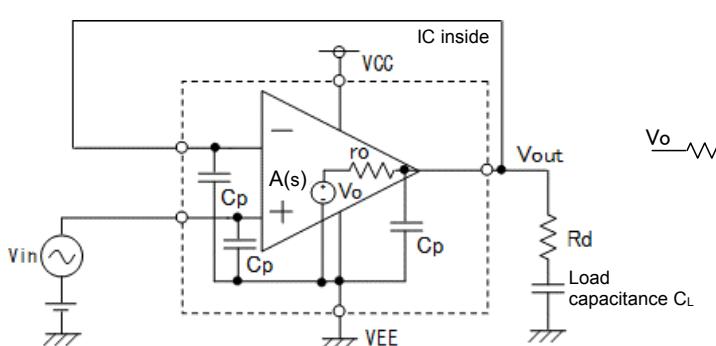
$$V_{out} = \frac{Z}{r_o + Z} V_o$$

$$(1 + \frac{r_o}{Z})V_{out} = A(s)V_{in} - A(s)V_{out}$$

$$(A(s) + 1 + \frac{r_o}{Z})V_{out} = A(s)V_{in}$$

$$\frac{V_{out}}{V_{in}} = \frac{A(s)}{A(s) + \frac{1}{Z}r_o + 1}$$

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + sC_p(R_d + \frac{1}{sC_L})} \frac{1}{A(s) + \frac{1}{R_d + \frac{1}{sC_L}}r_o + 1}$$



$$\frac{V_{out}}{V_{in}} = \frac{1}{A(s) + r_o \frac{C_L + C_p(sC_L + 1)}{sC_L R_d + 1} s + 1}$$

While the transfer function without the isolation resistance calculated in Figure 3.12.1. is

$$\frac{V_{o1}}{V_{in}} = \frac{A(s)}{1 + r_o(C_p + C_L)s + A(s)}$$

This part of the transfer functions is different.

We analyze the frequency characteristic of the underlined part in equation A. Suppose that $s = j\omega = j2\pi f$.

$$X = \frac{C_L + C_p(sC_L + 1)}{sC_L R_d + 1}$$

When $f \rightarrow 0$: $s \rightarrow 0$ and $X \rightarrow C_L + C_p$

When $f \rightarrow \infty$: $s \rightarrow \infty$, $sC_L R_d \gg 1$, $C_L \ll C_p$ ($sC_L + 1$), and $sC_L \gg 1$. Therefore, X is converged to C_p/R_d .

This result shows that the effect of the load capacitance C_L is removed.

- The value of the isolation resistor is set to between 50Ω to several hundred ohms, according to the capacitance and the required frequency bandwidth.

$$Z = \frac{1}{sC_p + \frac{1}{R_d + \frac{1}{sC_L}}}$$

$$Z = \frac{R_d + \frac{1}{sC_L}}{1 + sC_p(R_d + \frac{1}{sC_L})}$$

Figure 3.17.1. Example of output dividing resistor connection 2

3.18 THD+N (Total Harmonic Distortion + Noise)

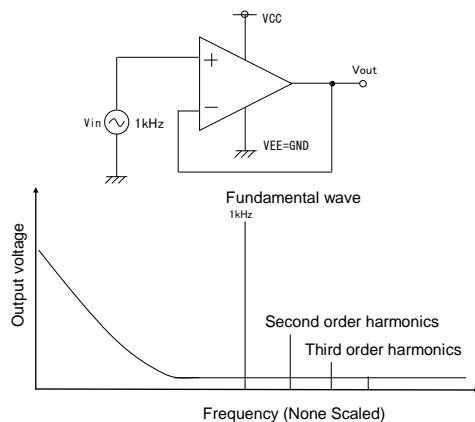
The value of THD+N (total harmonic distortion + noise) describes the percentage of the harmonic and noise components included in the output signal.

When the harmonic component or noise is included, the waveform of the output signal is not an exact reproduction of that of the input signal. In other words, the waveform of the output signal is distorted.

$$\text{THD+N} = (\text{Sum of harmonic and noise components}) / (\text{Output voltage})$$

The harmonic component arises from the non-linearity of op-amp circuits. For example, bipolar transistors have static current-voltage characteristics described by an exponential function. Therefore, the amplification factor is a non-linear function for the input voltage, causing the harmonic component.

We explain details of the noise in section 3.13 Input Referred Noise. Noise also arises from semiconductor elements inside the IC or from peripheral parts such as resistors.



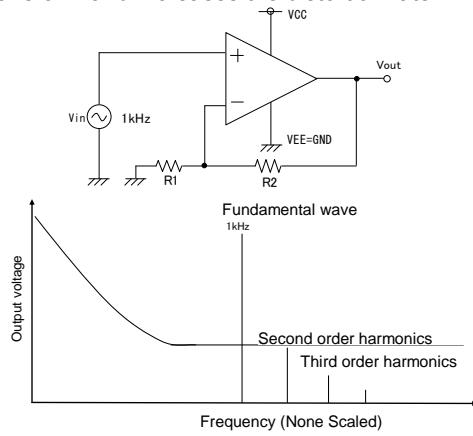
(a) Noise frequency spectrum of voltage follower

These components are mixed in the output signal of an op-amp, distorting the waveform.

We explain effects of the amplification factor and noise when an amplifier circuit is configured with an op-amp. An amplifier circuit amplifies not only the input signal but also the noise component. When you configure a circuit with a larger amplification factor to amplify the signal and the same magnitude of the output amplitude is obtained, the noise voltage is amplified by the gain and the distortion rate of the output signal becomes larger as the circuit gain increases (Figure 3.18.1).

When the amplification factor is constant, a smaller output amplitude results in a larger percentage of the noise voltage, exacerbating the distortion rate.

As we mentioned in the section for the slew rate, the amplitude that can be output becomes smaller as the signal frequency increases. Therefore, the slew rate limits the waveform and increases the distortion rate.

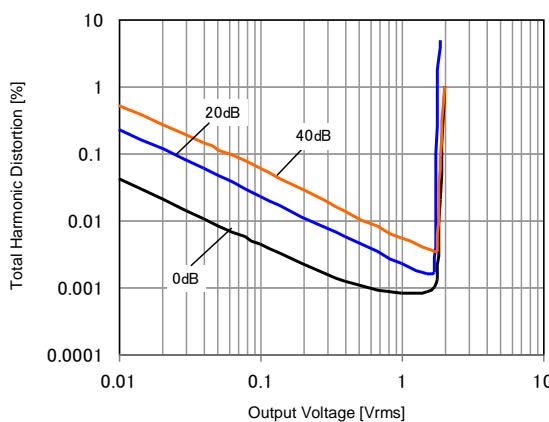


(b) Noise frequency spectrum of amplifier circuit

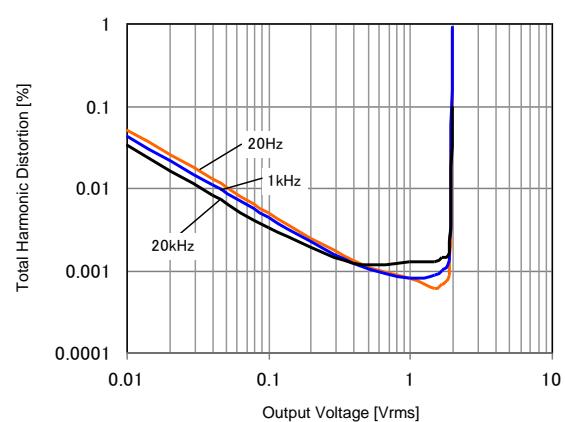
Figure 3.18.1. Noise frequency spectrum of THD+N

Next, Figure 3.18.2 shows examples of THD+N vs. the output voltage

characteristics.



(a) THD+N when the gain is varied



(b) THD+N when the frequency is varied

Figure 3.18.2. Examples of THD+N vs. output voltage characteristics

Next, we explain a cause of distortion in the output waveform of op-amps.

Input crossover distortion

Input full swing op-amps, especially op-amps equipped with two types (PMOS/NMOS or PNP/NPN) of differential input stage, have independent input offset voltages in the operating region of each differential input stage. Therefore, the input offset voltage varies within the input common-mode voltage range as shown in the figure. When the input signal passes over the step (crossover), a distortion is generated in the output signal.

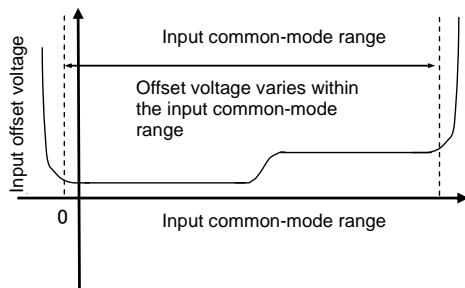


Figure 3.18.3. Offset voltage variation in input common mode range

Output crossover distortion and output circuit of op-amp

Output crossover distortion is generated as a result of the op-amp's output circuit configuration. It is also referred to as switching distortion. As we described in section 3.11 for the negative feedback system effect, you can restrain distortion generated in the output with a negative feedback effect. The distortion is restrained by the feedback amount when the open loop gain, $A(s)$, of the op-amp is large at lower frequencies, as shown in Equation (3.11.5). As $A(s)$ is decreased at higher frequencies, the restraining effect diminishes and the distortion gradually increases. However, as described in the next section for Class C operation, the output stage of 358/2904 series op-amps switches between Classes A and C operations according to the amount of the output sink current. Therefore, such distortions cannot be restrained by feedback.

The following sections explain how crossover distortion is generated as well as Classes A, B, C, and AB push-pull circuits for the types of op-amp output stages. Figure 3.18.4 shows an image of crossover distortion.

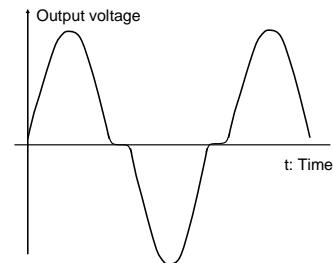


Figure 3.18.4. Output crossover distortion

Class A output circuit

A Class A output stage is an output stage through which a drive current flows at all times from a constant current source. One advantage of a constant current is that no crossover distortion is generated, since Q1 is always in the operating region. However, since the drive current keeps flowing even when there is no signal, power consumption increases. Since the output is driven by a constant current source, the capacity of the constant current source limits the source current, which flows from the amplifier, and a heavy load cannot be driven. (A heavy load distorts the waveform.)

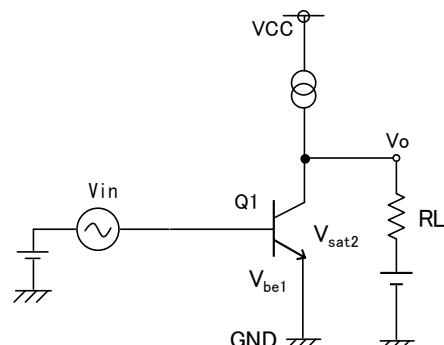


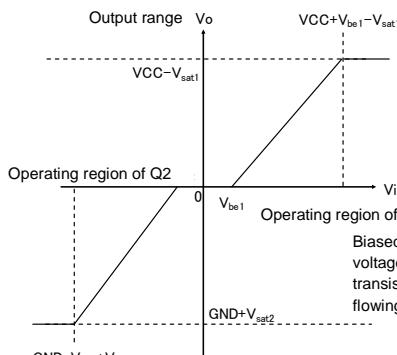
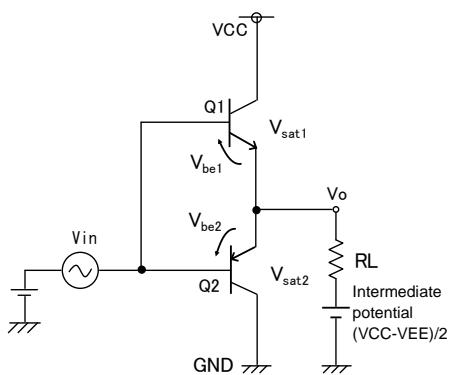
Figure 3.18.5. Class A output circuit

Class B push-pull output circuit

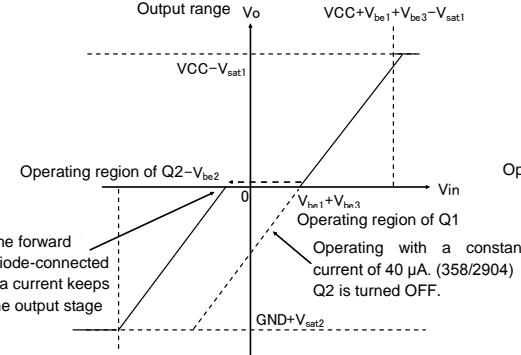
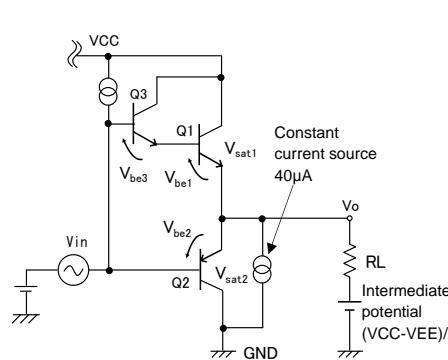
In Figure 3.18.6 (a) for Class B push-pull circuit, the vertical and horizontal axes are the output and input voltages, respectively. Since the operating regions for Q1 and Q2 are discontinuous, a distortion is generated in the output waveform. An output stage that has a discontinuous output characteristic with a gap of two V_{be} is called a Class B output stage. It features low current consumption, since no idling current flows in the output stage.

Class C push-pull output circuit

The Class C push-pull circuit shown in Figure 3.18.6 (b) is used for general single power supply op-amps, including 2904 and 358. When operating an op-amp with a single power supply, a bias voltage is applied to set the DC operating point of the circuit. In addition, when a load resistance is connected with the output of the op-amp—and especially if the voltage with which the load is connected is close to the bias voltage—no current flows into the output stage of the amplifier, since there is no potential difference between both ends of resistance RL . When the output voltage amplitude of the op-amp is varied from this condition, a potential difference between both ends of the resistance arises and a current flow into the amplifier. When this inflow current is 40 μA (value of the current from the constant current source) or less, the output stage operates as Class A.



(a) Class B push-pull circuit



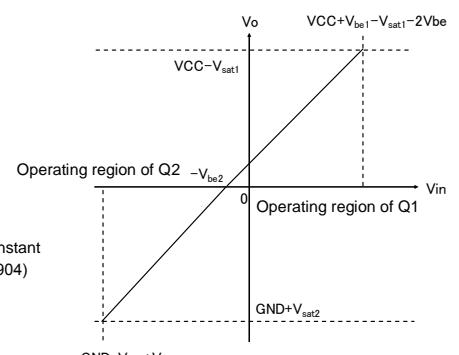
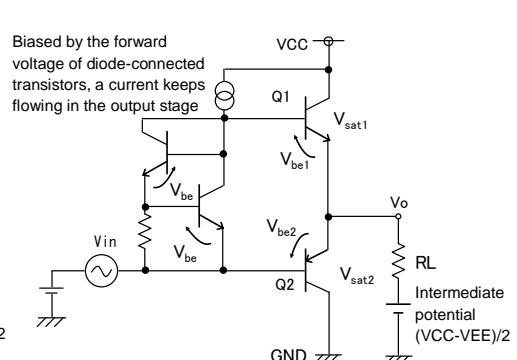
(b) Class C push-pull circuit

When the inflow current exceeds 40 μA , transistor Q2 starts to operate and the operation of the output stage transitions to Class C, causing discontinuous operation of the transistor.

This discontinuity contributes to crossover distortion. To reduce this distortion, you can decrease the amount of current flowing into the op-amp's output to the value of the current from the constant current source or below. It should also be noted that the feedback resistance serves as a load in addition to the load resistance that is connected with the output.

Class AB push-pull output circuit

The Class AB push-pull circuit shown in Figure 3.18.6 (c) is used for dual power supply low-noise op-amps, including 4558/4560. Class AB push-pull circuits are output stages that are modified so that a drive current flows in the output stage. The bias voltage is set so that transistors Q1 and Q2 are always ON by connecting two diode-connected transistors with a Class B push-pull circuit. Since the NPN and PNP transistors on the output stage are always operated by the drive current, switching operations are performed smoothly and crossover distortion is less likely to be generated. However, when a heavy load is connected—one that the current capacity of the output stage cannot drive—distortion may be generated even in a Class AB output stage.



(c) Class AB push-pull circuit

Figure 3.18.6. Op-amp output equivalent circuit

Output distortion with a heavy load

Connecting a load resistance or load capacitance with the output terminal of an op-amp may cause distortion, depending on the values of these variables. Here, we explain distortion generated when an RC filter is connected with the output. When a charge/discharge current to the capacitance exceeds the source and sink current capacities of the op-amp, distortion is generated. Figure 3.18.7 shows an RC filter circuit.

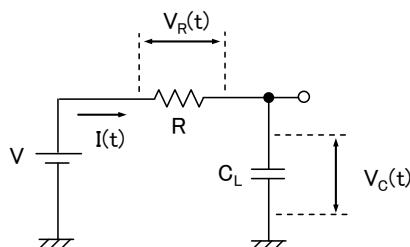


Figure 3.18.7. RC filter

Based on Figure 3.18.7, we calculate the initial value (maximum value) of the current that is charged in the capacitor. We assume that the capacitor has no electric charge initially.

The initial current that flows into the capacitor is given by Equation (3.18.1).

$$I(t) = \frac{V}{R} \exp\left(-\frac{1}{CR}t\right) \quad (3.18.1)$$

The above equation shows that the initial charge current is determined only by the resistance and current. Therefore, it is possible to check whether the maximum value of the charge current will exceed the output current capacity of the op-amp. The effect on the output voltage when an excessive current flows is also explained in section 3.5 for the maximum output voltage.

For example, consider the output current for 2904. When you configure a filter with $R = 100\Omega$, a current of 50 mA is required for outputting an amplitude of 5 Vpp. Since this current value exceeds the standard current capacity of 20 mA for 2904, it is expected that the output voltage range will be reduced and a distortion will be generated in the waveform. When $R = 10k\Omega$, the current value is 0.5 mA, which causes no distortion in the waveform. Discharge current can be viewed similarly. Figure 3.18.8 shows the relation between the output current and distortion. Figure 3.18.9 shows an example of waveform distortion.

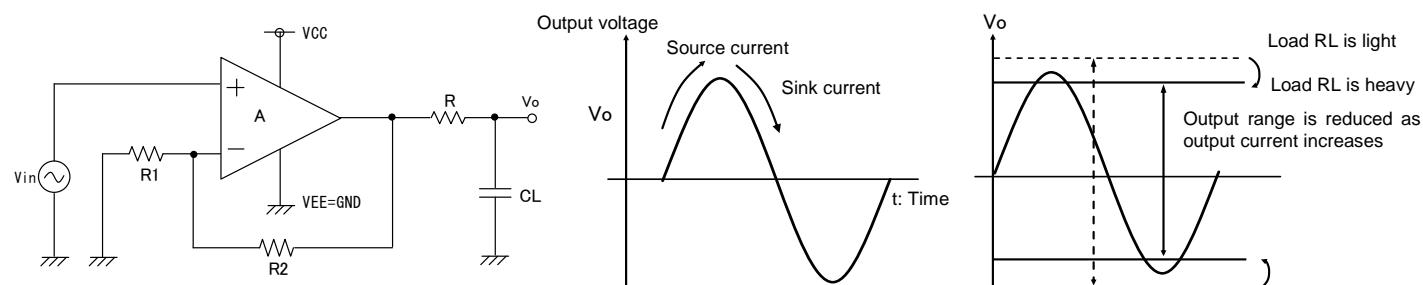


Figure 3.18.8. Relation between output current and distortion

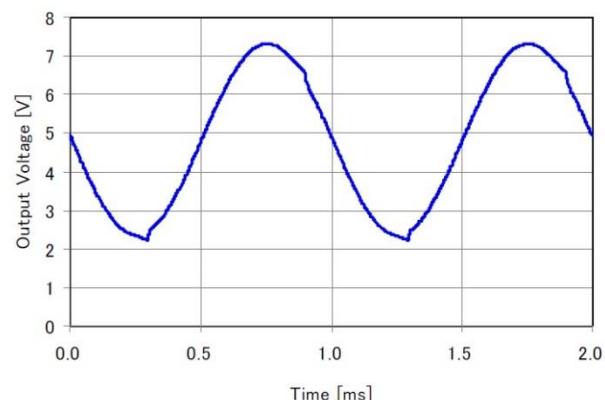
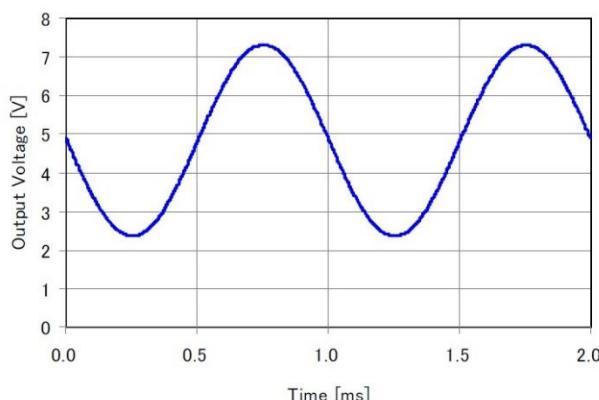


Figure 3.18.9. Example of waveform distortion for BA2904

3.19 Input referred noise

There are two types of noise: external and internal noise. Input referred noise in an op-amp—for example, thermal noise, 1/f noise, shot noise, and partition noise—is generated inside the electronic circuit and observed as noise at the op-amp's output stage. Output noise that is referred to input noise is termed input referred noise. Typically, the input referred noise voltage is described in a unit such as V_{RMS} , representing the magnitude of noise in the specified frequency bandwidth. The input referred noise voltage density is described in the unit of nV/\sqrt{Hz} , representing the noise voltage density per frequency. The product of the noise density multiplied by the noise bandwidth is the noise voltage. Op-amps are used in various circuit configurations with various amplification factors. Therefore, it is convenient to express the noise voltage as an input referred value in the same way as the input offset voltage.

Type of noise

Noise arises from the random motion of electrons, which is discontinuous in time. Primary noise generated from resistors and semiconductor elements includes thermal noise, shot noise, and 1/f noise (flicker noise). Primary mechanisms of noise generation are as follows:

Thermal noise

This noise arises from a random thermal motion of free electrons. Free electrons in a conductor move around randomly due to Brownian motion. This motion produces a tiny fluctuation in voltage, resulting in thermal noise. Thermal noise is distributed over a wide range of frequencies; it is also referred to as “white noise”. The amount of this noise depends not on the amount of current flowing through a conductor, but on variations in temperature.

Thermal noise V_{nT} generated with resistance R [Ω] is described by the following equation.

When k is the Boltzmann constant (1.38×10^{-23} [J/K]), T is the absolute temperature [K], and Δf is the bandwidth to estimate the noise [Hz],

$$\overline{V_{nT}^2} = 4kTR\Delta f \quad (3.19.1)$$

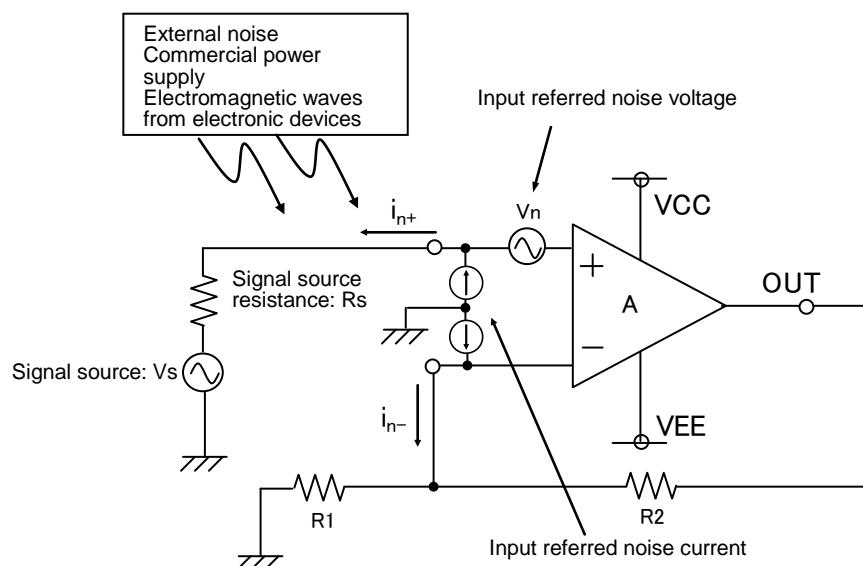


Figure 3.19.1. Op-amp noise

Shot noise

When a current flows inside a semiconductor, each carrier (electron or hole) passes through a depletion layer (PN junction) while moving randomly, causing a fluctuation in the current like waves on a river surface. The magnitude of the generated noise depends on the average current value flowing through the junction. It is also related to the traveling time of the carriers and is nearly constant in regions where the traveling time can be ignored. (It cannot be ignored at higher frequencies.)

This noise is distributed over a wide range of frequencies (white noise). When I_D is the current flowing through the junction, q is the elementary charge (1.6×10^{-19} [C]), and Δf is the bandwidth for estimating noise [Hz], i_{ns} (noise current of the generated shot noise) is described by Equation (3.19.2).

$$\overline{i_{ns}^2} = 2qI_D\Delta f \quad (3.19.2)$$

1/f noise (flicker noise)

When carriers are trapped by and released from uncombined bonds that are generated on a semiconductor interface, a current occurs that is different from the normal carrier travel.

This current is referred to as flicker noise. Since it is more frequently generated as the frequency decreases, it is also referred to as 1/f noise in the sense that the noise is inversely proportional to the frequency. In principle, this noise is said to arise from the presence of uncombined bonds referred to as dangling bonds on the interface between SiO_2 and silicon crystals. Since atomic bonds with which silicon molecules form covalent bonds are discontinuous at the SiO_2 interface, trapping and releasing occur as the carriers travel on the silicon interface. As a result, a fluctuation occurs in the current, generating noise.

When K_f is a constant determined by the manufacturing process, I is the DC current, f is the frequency, and Δf is the bandwidth for estimating noise [Hz],

$$\overline{i_{nf}^2} = K_f \frac{I}{f} \Delta f \quad (3.19.3)$$

There are other types of noise generated in semiconductors. For example, partition noise is generated when a current is split into different routes. Burst noise (popcorn noise) occurs in a low frequency region near the audio bandwidth.

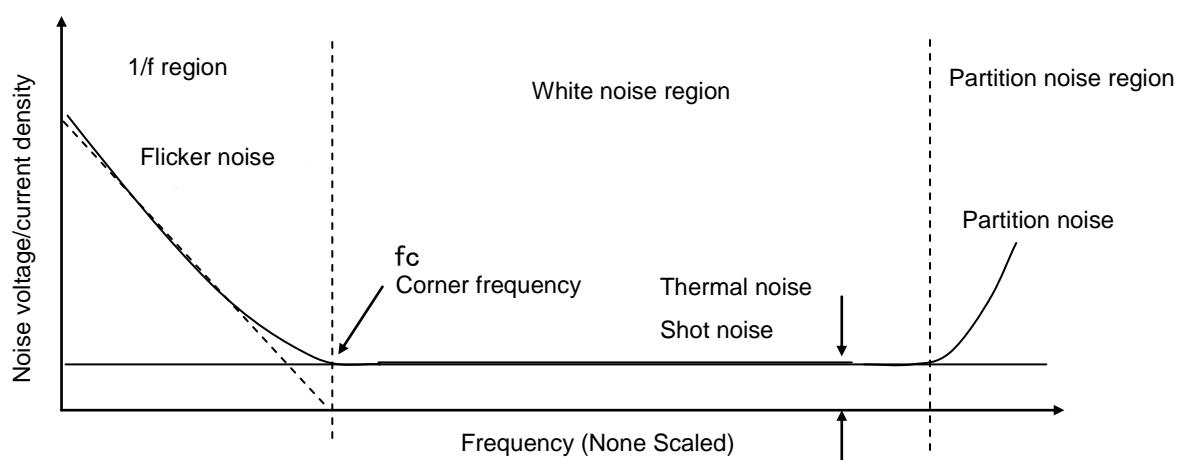


Figure 3.19.2. Image of frequency spectrum for input referred noise voltage

As mentioned above, various types of noise are generated in op-amps and appear as a noise in the output. Using a non-inverting amplifier circuit shown in Figure 3.19.3, we consider how the input referred noise of an op-amp affects an application circuit.

Input referred noise voltage/noise voltage density of op-amps

When the input circuit is short-circuited, noise generated inside an op-amp (primarily the differential amplification stage) is amplified and appears as noise in the output. Dividing this output noise by the amplification factor of the circuit provides the input referred noise voltage (V_n). Since it appears as if noise is input to the amplifier and amplified, it is termed input referred. However, the noise is actually generated inside the op-amp and no noise voltage is generated on the input terminal, as shown in Figure 3.19.3.

Input referred noise current/noise current density of op-amps

As mentioned above, the input referred noise current arises from a fluctuation in the transistor current or from noise caused by a split in the current.

This current is actually output from the input terminal to the outside. It is converted into voltage by external resistors or by signal source resistance, and it acts as a part of the input referred noise voltage. Its effect depends on factors in the external environment such as the circuit constant and circuit configuration. In Figure 3.19.3, a noise current is converted into a noise voltage by R_1 , R_2 , and R_s .

There is no correlation between the noise currents in the inverting terminal (i_-) and non-inverting terminal (i_+). Each noise current is generated at random. Therefore, they will not cancel each other out.

Thermal noise from external resistor and signal source resistance

External resistors and signal source can be sources of thermal noise. Thermal noise voltage is described as a noise voltage source connected in series to each resistance source.

The input referred noise voltage density is calculated based on these considerations. The thermal noise voltage density for the resistance is calculated by Equation (3.19.1). The noise voltage generated at each resistance source is calculated. The input referred noise current is converted into noise voltage at the external resistors. Since the noise is handled as power, its mean square is provided. In addition, it is assumed in Figure 3.19.3 that $i_{in+} = i_{in-} = i_{in}$. Since the noise is generated at random, each term has no polarity. When V_n is the input referred noise voltage density of the op-amp and "in" is the input referred noise current density of the op-amp, the input referred noise voltage density is described by Equation (3.19.4). This equation corresponds to a situation where all sources of noise are combined together and connected with a non-inverting input terminal, as shown in Figure 3.19.4.

$$V_{na}^2 = V_n^2 + [R_s^2 + (R_1 // R_2)^2]_{in}^2 + 4kT[R_s + (R_1 // R_2)] \quad (3.19.4)$$

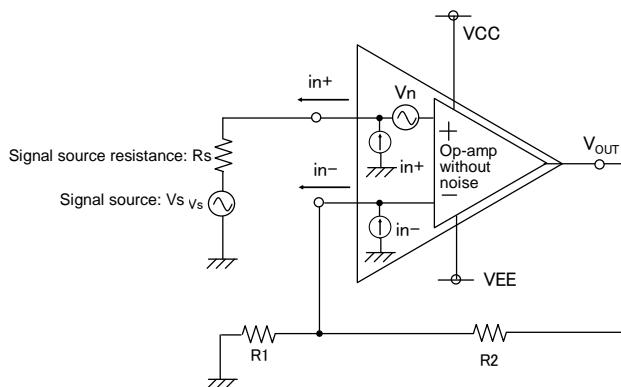


Figure 3.19.3. Equivalent circuit for non-inverting amplifier circuit noise

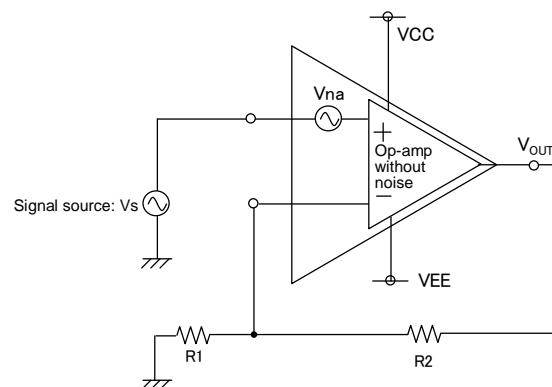


Figure 3.19.4. Equivalent circuit for non-inverting amplifier circuit noise
(Noise sources are combined together into IN+)

Next, we determine the output noise voltage of a non-inverting amplifier circuit.

Equation (3.19.5) shows the output noise voltage due to resistance.

Equation (3.19.6) shows the output noise voltage due to the input referred noise voltage of an op-amp.

Equation (3.19.7) shows the output noise voltage caused by the input referred noise current of an op-amp.

Suppose that the noise gain of a non-inverting amplifier circuit $(1 + R_2/R_1)$ is G_1 and (R_2/R_1) is G_2 and assume $i_{n+} = i_{n-} = i_n$.

The total output noise voltage is described by Equation (3.19.8).

The noise gain is the gain from the location of the noise source to the output. If you divide each term in Equation (3.19.7) by the square of the noise gain, it is equivalent to Equation (3.19.4) determined above for the input referred noise voltage.

As a measure to reduce noise in application circuits, you can use metal film resistors that do not generate flicker noise, avoid increasing the circuit constant (resistance value) excessively, or use low-noise op-amps. Products referred to as low-noise op-amps are designed so that the input referred noise voltage of the op-amp itself is small. They are mainly used for high-precision amplification applications, such as sensors, and audio applications.

$$V_{n2} = \sqrt{4kTR_2} \quad V_{n1} = \sqrt{4kTR_1} \left(\frac{R_2}{R_1} \right) \quad V_{ns} = \sqrt{4kTR_s} \left(1 + \frac{R_2}{R_1} \right) \quad (3.19.5)$$

$$V_{nOP} = V_n \left(1 + \frac{R_2}{R_1} \right) \quad (3.19.6)$$

$$V_{ni-} = i_{n-} (R_1 // R_2) \quad V_{ni+} = i_{n+} R_s \left(1 + \frac{R_2}{R_1} \right) \quad (3.19.7)$$

$$V_{no}^2 = (V_n G_1)^2 + (i_n R_s G_1)^2 + (i_n R_1 // R_2)^2 + 4kTR_2 + \left(\sqrt{4kTR_1} G_2 \right)^2 + \left(\sqrt{4kTR_s} G_1 \right)^2 \quad (3.19.8)$$

Items unique to comparators

3.20 Response time (rise/fall times and propagation delay time)

The response time of comparators is specified in terms of the rise time, fall time, rise propagation delay time, and fall propagation delay time.

The rise time refers to the time during which a signal is varied from 10% to 90% of the output signal amplitude. The fall time refers to the time during which a signal is varied from 90% to 10% of the output signal amplitude. The propagation delay time is specified in terms of the time during which the voltage is varied from the reference voltage to 50% of the output voltage amplitude. The propagation delay time is evaluated by varying the potential difference between the reference voltage and the signal level (overdrive voltage) as shown in Figure 3.20.1. The propagation delay time becomes longer as the overdrive voltage is reduced. In addition, an input signal at the TTL level (3.5 [V_{pp}]) may be supplied for evaluation. Figure 3.20.1 shows the input and output waveforms of a comparator.

There are two types of comparator: open-collector type (open drain CMOS) and push-pull type (CMOS).

As a feature of the open-collector (drain) type, the output stage of the comparator has no circuit for outputting at the High setting and external resistors are required to pull-up the output. By varying the value of the pull-up voltage (V_{RL}), you can adjust the High setting of the output voltage to a value different from that of the power supply of the comparator. It should also be noted that the rise time of an open-collector type comparator is affected by a time constant resulting from the external pull-up resistor and the load or from parasitic capacitance.

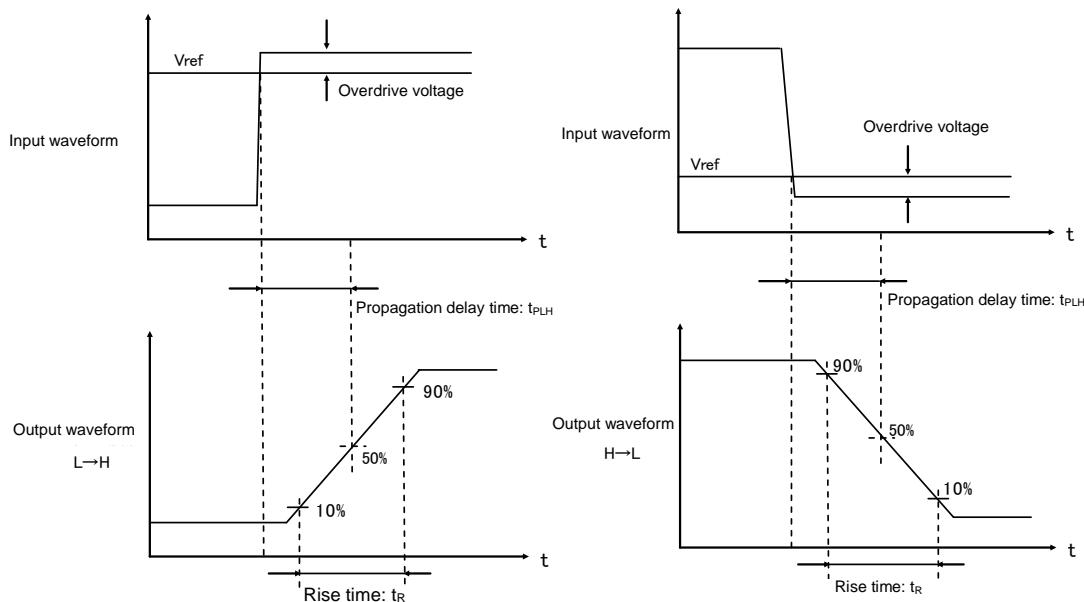


Figure 3.20.1. Response time of comparator

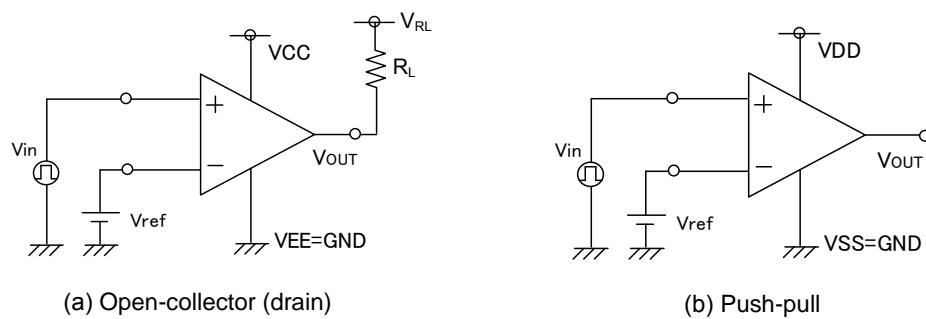


Figure 3.20.2. Measurement circuit for response time of comparator

Notes for using an op-amp as a comparator

In the output waveform of an op-amp in which phase compensation capacitance has been installed, the rise and fall times are limited by the slew rate. The slew rate is determined by the time for charging and discharging the phase compensation capacitance. Since comparators have no phase compensation capacitance, they can respond with faster rise and fall times compared with op-amps. In addition, some op-amps are not appropriate to use as comparators due to their inside circuit configuration.

In general, rise times and propagation delay times are not specified for op-amps. However, you can estimate rise and fall times based on the slew rate ($SR = [V/\mu s]$) if the output amplitude is known.

Since the propagation delay time is not specified, the use of comparators is also recommended when a high-speed response is required or when variations are of concern.

As we explained in section 2.2 for the differential breakdown voltage of the terminal structure, the protection diodes for clamping are connected between the terminals in some op-amps. Such op-amps cannot be used as comparators, since a current flow between the terminals. Equivalently, when a model whose differential input breakdown voltage is lower than the maximum rating for the power supply voltage is used as a comparator, care must be taken not to exceed the maximum rating.

4 Reliability Items

4.1 Electrostatic Breakdown Voltage (ESD Breakdown Voltage)

The breakdown resistance to static electricity is one of the reliability test items.

The following phenomena are examples of the breakdown when static electricity is applied to the IC.

- Dielectric breakdown of the oxide film

When the transistor has a MOS structure, this type of breakdown occurs when a high electric field is applied to the gate oxide film.

- Thermal breakdown of the PN junction

Static electricity causes an overcurrent through the PN junction inside the IC, resulting in thermal breakdown of the junction.

- Fusing in the wiring

Thermal breakdown in the wiring occurs if an overcurrent that exceeds the allowable current flows through the wiring.

The following are models for the electrostatic stresses that may be applied during the handling of semiconductor products.

- HBM (Human Body Model)

The human body model describes the discharge phenomenon that occurs when the electrically charged human body contacts semiconductor products. The values of capacitance and resistance are used for the modeling.

$$C_{ESD} = 100 \text{ [pF]}, R_{ESD} = 1.5 \text{ [k}\Omega\text{]}$$

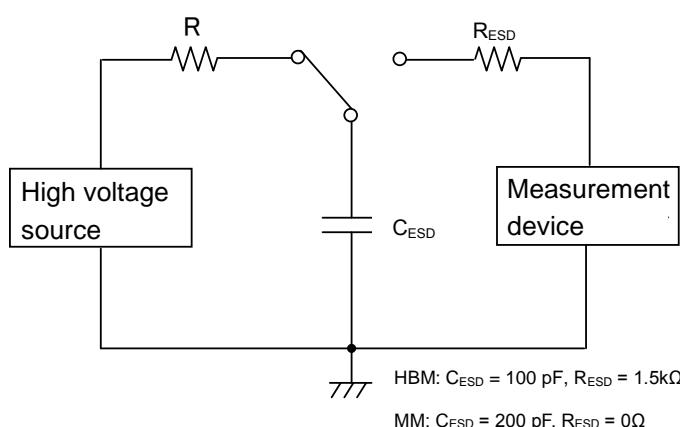


Figure 4.1.1. Simple test circuit for HBM and MM

- MM (Machine Model)

The machine model describes the discharge phenomenon that occurs when an electrically charged machine made of metal contacts the semiconductor products. The capacitance is larger while the resistance is lower than those used for the human body model.

$$C_{ESD} = 200 \text{ [pF]}, R_{ESD} = 0 \text{ [\Omega]}$$

This is an old standard and is currently slipping out of mainstream use.

- CDM (Charged Device Model)

This is a method to evaluate the resistance to the electrostatic discharge that occurs when the semiconductor itself is electrically charged and contacts metals or other materials.

Figure 4.1.1 shows a simple test circuit for the human body and machine models.

The capacitance of C_{ESD} is charged with a high voltage source, the charge is discharged through the resistance of R_{ESD} , and then the occurrence of destruction is checked.

The test is performed for both the positive and negative polarities. Generally, the common terminal for applying static electricity is the VEE terminal (ground terminal) or the VCC terminal. Usually, the IC is provided with a protection circuit against static electricity and a countermeasure is taken so that an overcurrent will not flow inside the circuit. The role of the protection circuit is to release the surge due to static electricity to the common terminal and a current path with low impedance is secured. Moreover, a resistor may be connected in series to the terminal in order to prevent the charging of hot carriers to the gate of the CMOS device.

Figure 4.1.2 shows an example of a protection circuit.

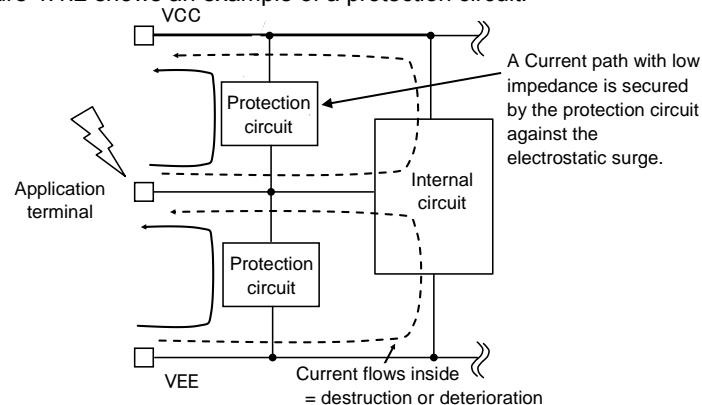


Figure 4.1.2. Example of an electrostatic protection circuit of an IC

Figure 4.1.3 shows the equivalent circuit diagram for the CDM test.

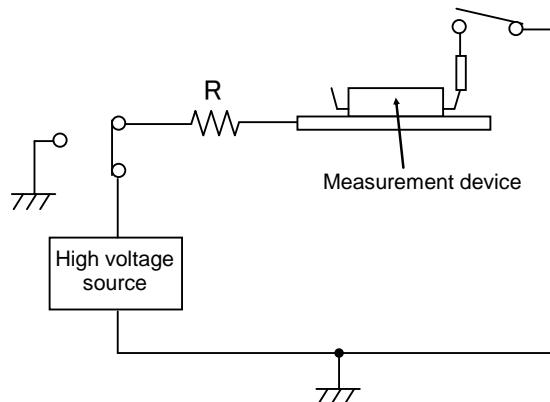


Figure 4.1.3. Equivalent circuit for the CDM test

4.2 Latch Up Test

The Latch up phenomenon occurs in an IC that is configured mainly with CMOS devices. The parasitic bipolar transistor that occurs between the elements is operated by the pulse current or voltage created by electrical noise or the electrostatic testing, causing abnormal operations.

This phenomenon shows various symptoms such as breakdown caused by a continued flow of overcurrent, or a fixed output voltage due to an increase of the circuit current. It also has a feature that enables the normal operation to be recovered by turning the power OFF and then ON again if a breakdown has not occurred. The occurrence of the latch up can be judged by monitoring the circuit current since the circuit current increases in all cases.

Usually, the latch up phenomenon is addressed using layout techniques during the design phase of the IC so that the capability of the parasitic element is restrained.

The following methods are available for evaluation of the IC resistance to the latch up.

- Current latch up test

A trigger by the current pulse is supplied to the IC and the occurrence of the latch up is checked.

A current with both negative and positive polarities is applied.

- Voltage latch up test

A trigger by the overvoltage pulse is supplied to the IC and the occurrence of the latch up is checked.

In both tests, the latch up is judged by monitoring the circuit current.

Figure 4.2.1 shows the latch up test circuit.

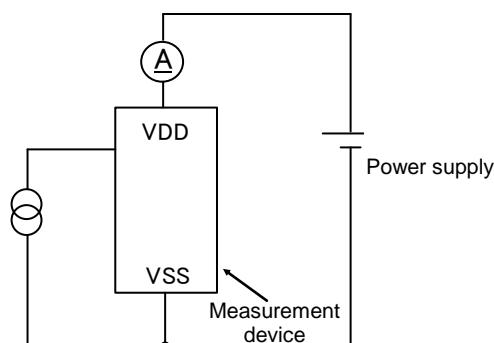


Figure 4.2.1. Latch up test circuit

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