AND9148/D

NCV7383 FlexRay® Bus Driver Application Note

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APPLICATION NOTE

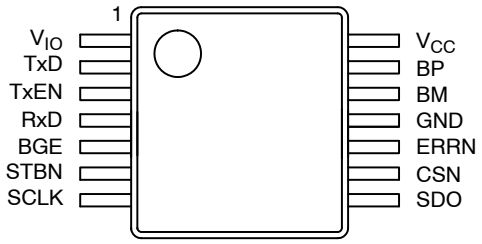
INTRODUCTION

NCV7383 is a single-channel FlexRay bus driver compliant with the FlexRay Electrical Physical Layer Specification Rev. 3.0.1, capable of communicating at speeds of up to 10 Mbit/s. It provides differential transmit and receive capability between a wired FlexRay communication medium on one side and a protocol controller and a host on the other side. NCV7383 mode control functionality is optimized for nodes without the need of extended power management provided by transceivers with permanent connection to the car battery as is on NCV7381. NCV7383 is primarily intended for nodes switched off by ignition.

This document provides additional information on following topics:

- Typical Application
- Optional ESD protection
- Example PCB layout
- Digital outputs DC characteristics
- Communication Controller interface termination
- Bus impedance in Power-off mode

PIN CONNECTIONS



(Top View)

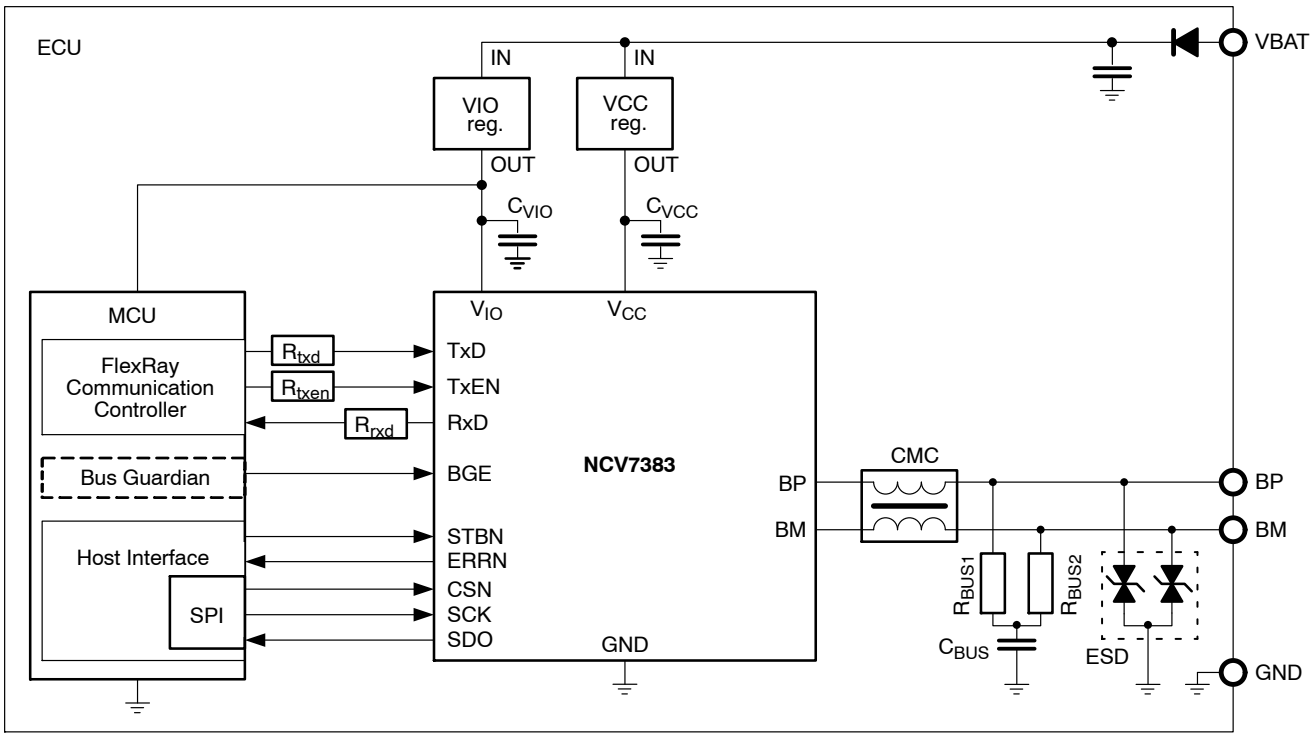


Figure 1. NCV7383 Application Diagram

TYPICAL APPLICATION

Table 1. NCV7383: RECOMMENDED EXTERNAL COMPONENTS

Component	Function	Value	Unit	Note
C_{VCC}	Decoupling capacitor on V_{CC} supply line, ceramic (X7R)	100	nF	Type 0603
C_{VIO}	Decoupling capacitor on V_{IO} supply line, ceramic (X7R)	100	nF	Type 0603
R_{BUS1}	Bus termination resistor	47.5	Ω	Type 0805, (Note 1)
R_{BUS2}	Bus termination resistor	47.5	Ω	Type 0805, (Note 1)
C_{BUS}	Common-mode stabilizing capacitor, ceramic	4.7	nF	Type 0805, ±20%
CMC	Common-mode chokes	100	μH	(Note 2)
ESD	Optional ESD protection	NUP2115	-	Type SOT-23
Rtxd	Optional TxD line series termination resistor	(Note 3)		Type 0603
Rtxen	Optional TxEN line series termination resistor	(Note 3)		Type 0603
Rrxd	Optional RxD line series termination resistor	(Note 3)		Type 0603

1. Tolerance ±1%; the value R_{BUS1}+R_{BUS2} should match the nominal cable impedance.
2. Recommended common-mode chokes:
   MURATA DLW43SH101XK2
   MURATA DLW43SH510XK2
   MURATA DLW43SH101XP2
   EPCOS B82799C0104N001
   TDK ACT45R-101-2P-TL001
3. See Communication Controller Interface Termination section.

Optional ESD Protection

In order to improve system reliability an additional external ESD protection may be used. As a result of the high speed nature, the FlexRay specification calls for a low capacitance protection of up to 20 pF and a tight deviation in capacitance between the signal pairs limited to 2%. The reason is that any additional ESD protection represents a capacitive load on the bus lines which can have undesired effects on electromagnetic emissions and immunity if the bus lines capacitive load does not match properly.

The NUP2115, dual line FlexRay Bus Protector, is designed for the highest possible signal integrity by limiting the stray capacitance to 10 pF max while having a nominal capacitance matching at 0.26% and achieving the ESD and other transient protection requirements.

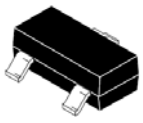


Figure 2. SOT−23 Package

System ESD measurement results are shown in the Table 2. Tested without external bus filter network, which is the worst case. The absolute values are from internal measurements. It indicates noticeable increase of the maximum possible discharge voltage. The values measured by external laboratory are visible in device datasheets [1][4].

Table 2. SYSTEM HBM ON PINS BP AND BM, per IEC 61000-4-2; 150 pF/330 Ω

	NCV7383	NCV7383 + NUP2115L
Requirement	±6 kV	
Pin	No failure up to:	
BP	±13 kV	±21 kV
BM	±13 kV	±21 kV

For more information on the device details, see the product datasheet [4].

Example PCB Layout

An example PCB layout is shown in the Figure 3. Modification of this layout is possible with the following recommendations:

- Place the NCV7383, the common mode choke and the optional ESD protection as near as possible to the BP and BM pins of the ECU connector.
- Route the BP and BM signal lines symmetrically.
- Keep the distance between the lines BP and BM minimal.
- Keep the decoupling capacitors close to the particular supply pins.
- Keep the ground plane uninterrupted if possible.

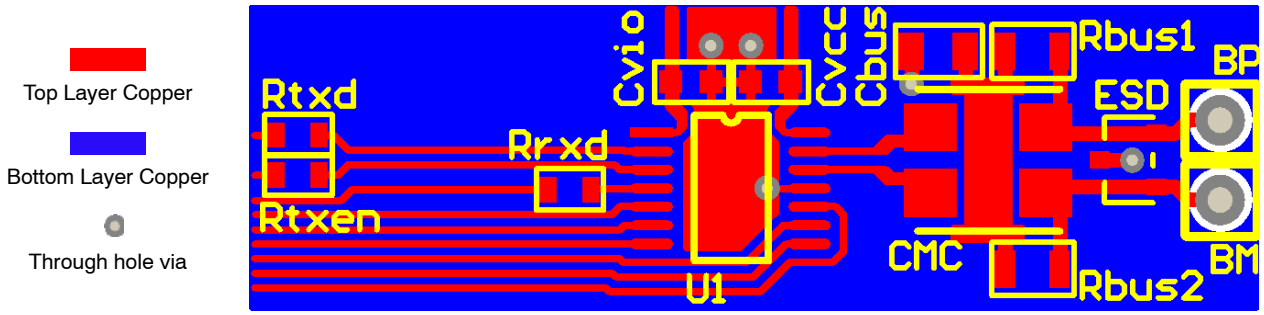


Figure 3. Example PCB Layout

Digital Outputs DC Characteristics

Typical digital outputs (RxD, ERRN and SDO) characteristics are shown in the Figure 6 to Figure 11. The characteristics were measured at room ambient temperature, in Normal mode (STBN and EN forced High), with no undervoltage and with supply voltages: VBAT = 12 V, VCC = 5 V, VIO = 3.3 V and 5 V.

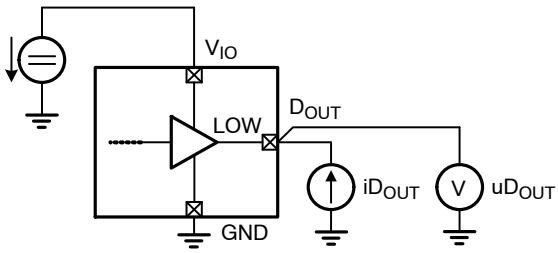


Figure 4. Test Setup for Output Low Characteristics on Digital Output Pins

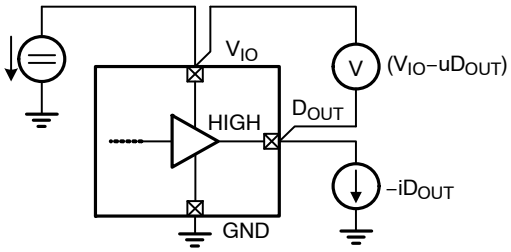


Figure 5. Test Setup for Output High Characteristics on Digital Output Pins

RxD Digital Output

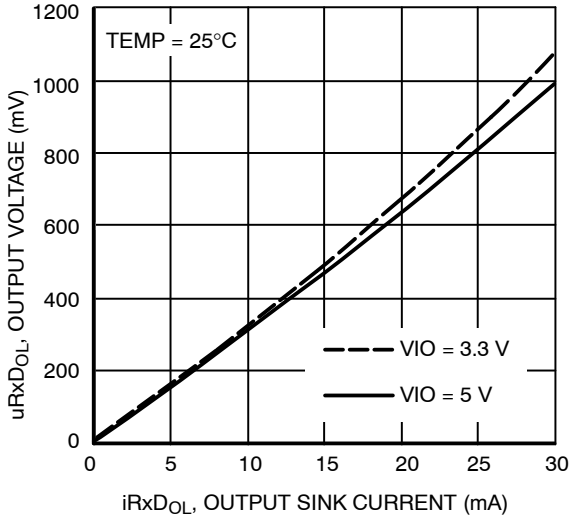


Figure 6. Typical RxD Output Sink Characteristics

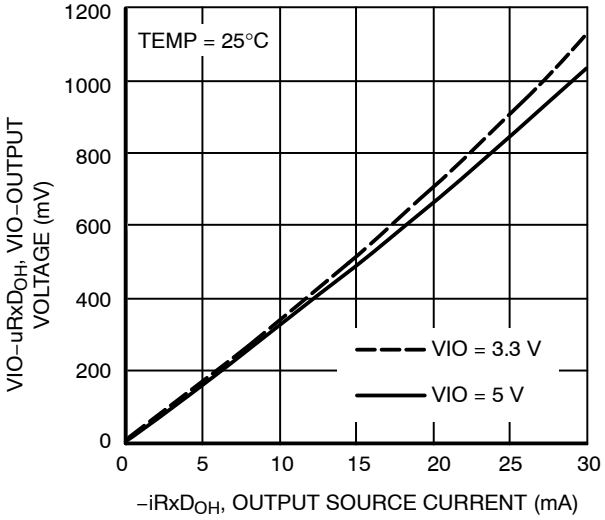


Figure 7. Typical RxD Output Source Characteristics

ERRN Digital Output

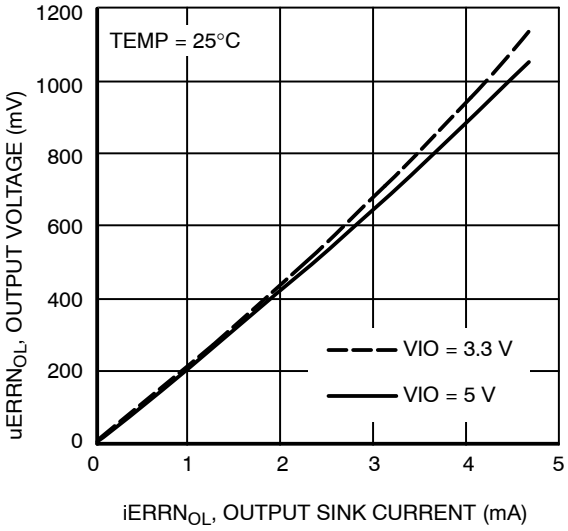


Figure 8. Typical ERRN Output Sink Characteristics

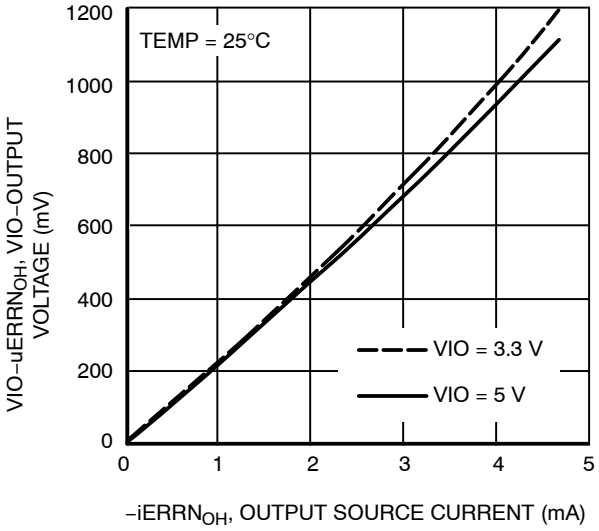


Figure 9. Typical ERRN Output Source Characteristics

SDO Digital Output

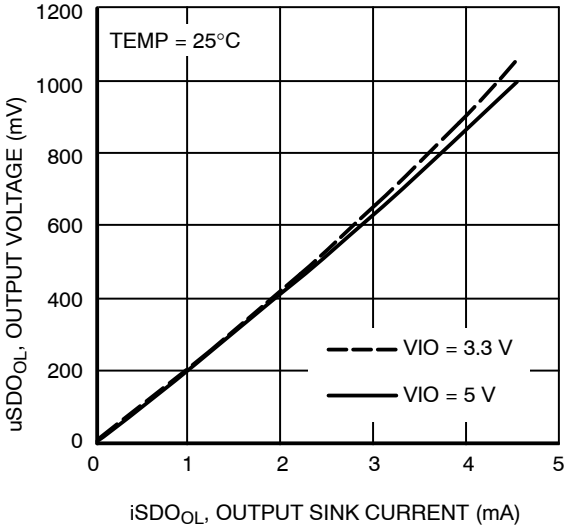


Figure 10. Typical SDO Output Sink Characteristics

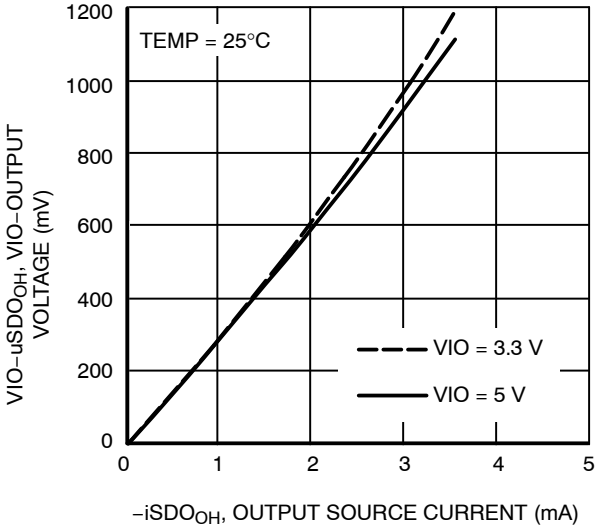


Figure 11. Typical SDO Output Source Characteristics

Communication Controller Interface Termination

The signals of the communication controller (CC) interface (TxD, TxEN and RxD) achieve high enough speed that the PCB connection should be considered a transmission line. The CMOS driver's impedance can be significantly lower than the PCB track characteristic impedance *Z0*, depending on the PCB configuration. The impedance mismatch at the ends of the line may cause reflections and thus all kinds of overshoots and undershoots. This may lead to signal integrity problems and increased electromagnetic emissions.

It is recommended to use a transmission line series termination in order to overcome these problems.

A series termination comprises of a resistor between the driver's output and the transmission line.

A typical PCB configuration is shown in the Figure 12 and Figure 13. An estimated characteristic impedance of the given 8 mils wide TOP layer trace is ca. 130 Ω at 2−Layer PCB (Figure 12) and ca. 72 Ω at 4-Layer PCB (Figure 13).

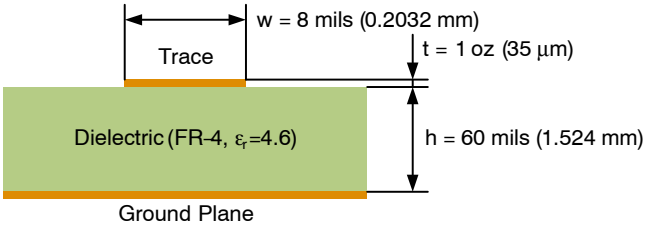


Figure 12. Example of 2−Layer PCB

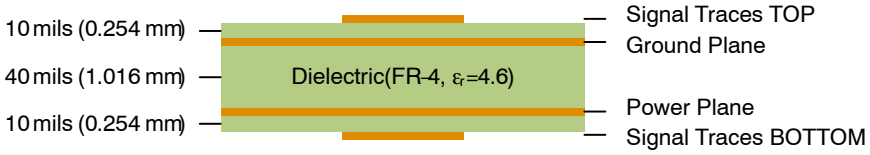


Figure 13. Example of 4−Layer PCB

The series termination resistor Rs should by calculated as follows:

$$Rs \approx \text{Line } Z0 - \text{Driver impedance} \quad \text{(eq. 1)}$$

The line characteristic impedance Z0 [Ω] depends on the PCB configuration. Typical RxD driver output impedance is shown in the Figure 14. The TxD and TxEN signals are driven by an MCU or communication controller. An example of the TxD output driver of Freescale MC9S12XF MCU is shown in the Figure 15.

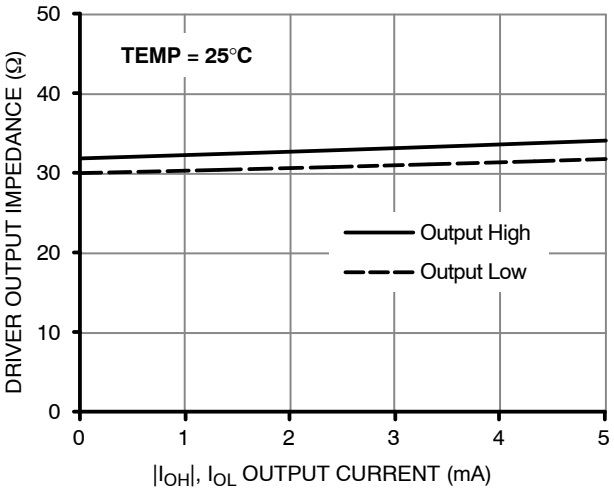


Figure 14. NCV7383 RxD Pin Output Impedance (typical)

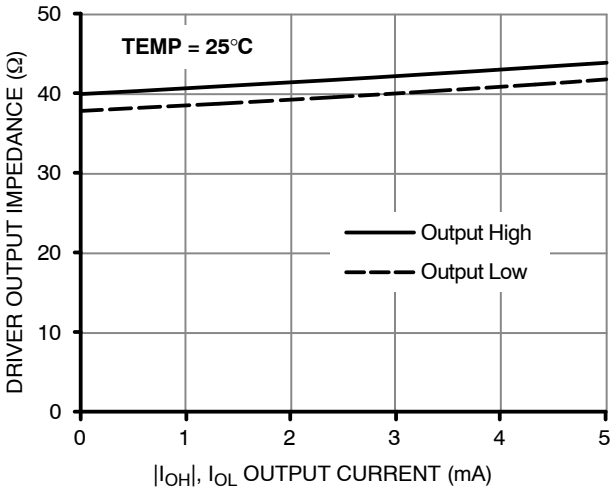


Figure 15. Freescale MC9S12XF MCU TxD Pin Output Impedance

Calculation example

Inputs:

- 4-Layer FR-4 PCB (Figure 13), 8 mils trace with estimated characteristic impedance 72 Ω.
- RxD driver output impedance 33 Ω.

Ideal Series termination resistor value ≈ 72 Ω - 33 Ω = = 39 Ω

Recommended value is 33 Ω.

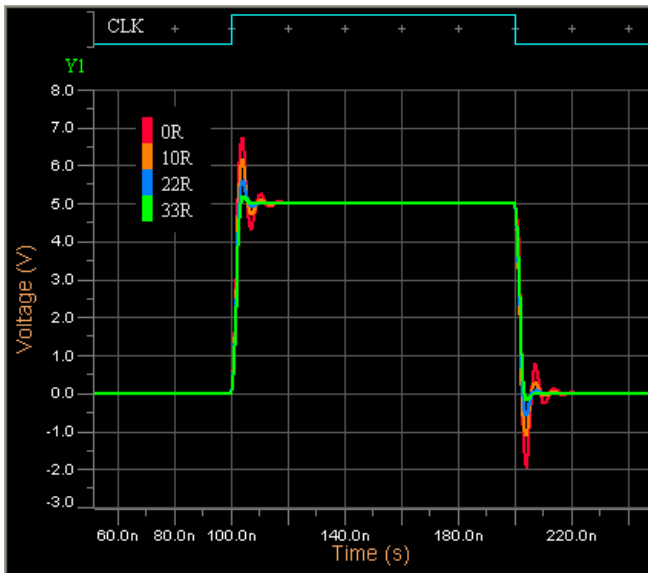


Figure 16. RxD Trace Impedance Mismatch Compensation (4−Layer PCB, ringing at MCU input pin)

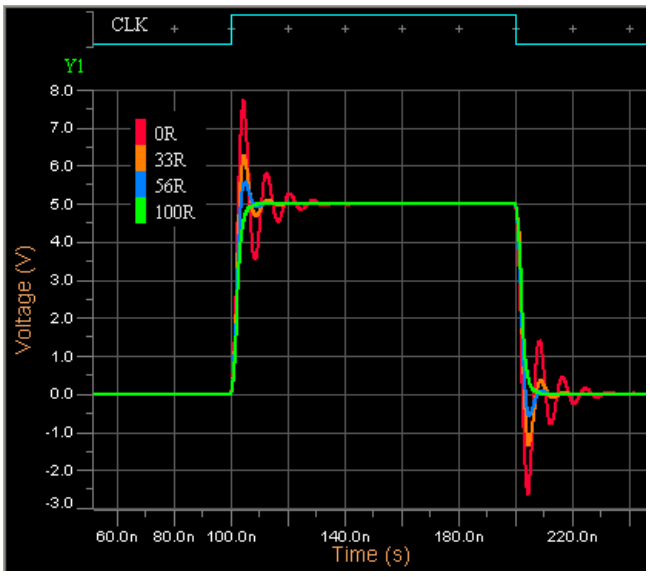


Figure 17. RXD Trace Impedance Mismatch Compensation (2−Layer PCB, ringing at MCU input pin)

Design recommendations:

- Place the RxD serial termination resistor close to transceiver.
- Place the TxD and TxEN serial termination resistor close to microcontroller / Communication Controller.
- Surface mount resistor is preferred in order to avoid additional serial inductance.
- Maximum value of series termination resistance is limited by required signal rise/fall time. Particularly values higher than 33 Ω should be carefully considered.

Bus Impedance in Power−off Mode

In order not to disturb the rest of the FlexRay network in case NCV7383 is unsupplied, the bus lines BP and BM remain High−Impedant with maximum leakage current of 5 μA (see the iBP_{LEAK} and iBM_{LEAK} parameter). This is valid for bus common mode voltage range uCM = 0 V to 5 V (See the Figure 18 and Figure 19).

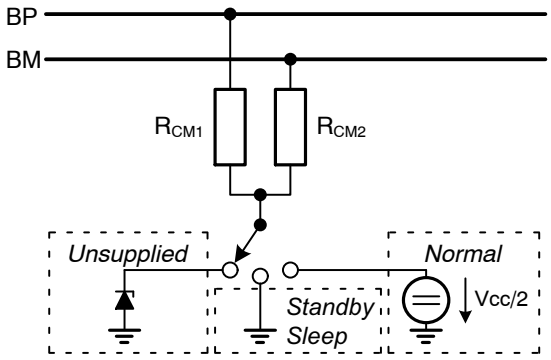


Figure 18. Simplified Bus Biasing Circuit

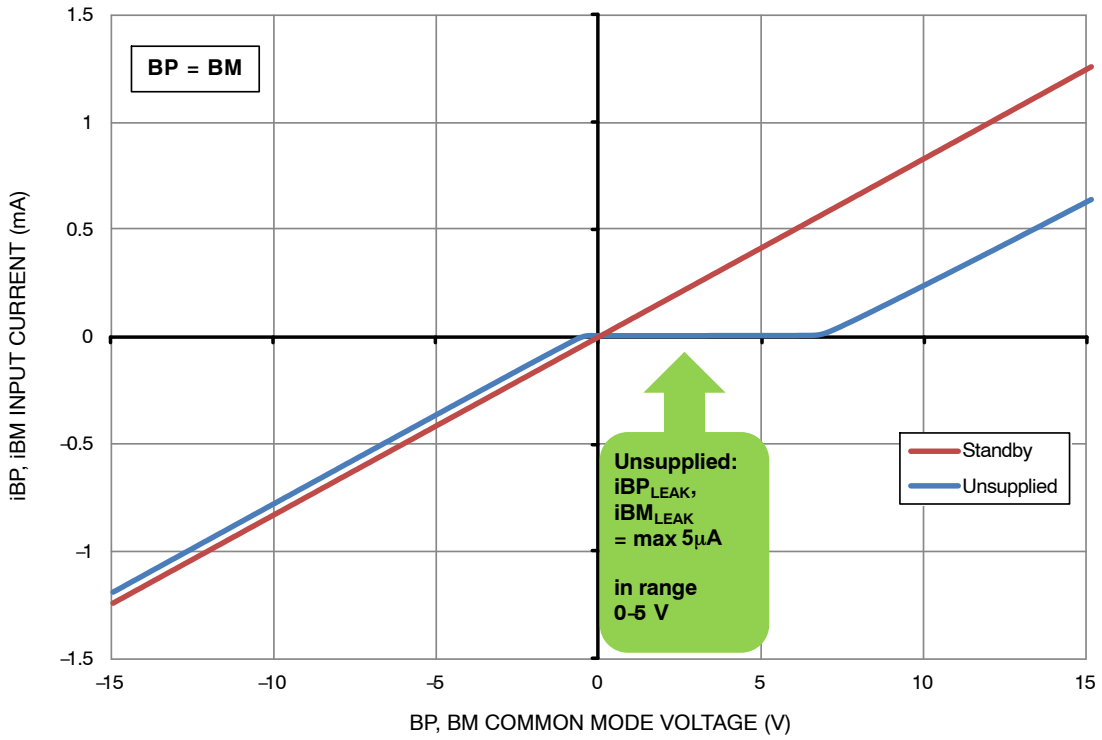


Figure 19. Bus Leakage Current versus Common Mode Voltage uCM

Table 3. EXTRACT FROM THE DEVICE DATASHEET [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{CM1}, R_{CM2}	Receiver common mode resistance		10	24	40	kΩ
iBP_{LEAK} iBM_{LEAK}	Absolute leakage current when driver is off	uBP = uBM = 5 V All other pins = 0 V			5	μA
$iBP_{LEAKGND}$ $iBM_{LEAKGND}$	Absolute leakage current, in case of loss of GND	uBP = uBM = 0 V All other pins = 16 V			1600	μA

REFERENCES

[1] ON Semiconductor, NCV7383/D Datasheet, Rev.P1, January 2013
[2] FlexRay Consortium. FlexRay Communications System − Electrical Physical Layer Specification, V3.0.1, October 2010
[3] FlexRay Consortium. FlexRay Communications System − Physical Layer EMC Measurement Specification, V3.0.1, October 2010
[4] ON Semiconductor, NUP2115L/D, Datasheet, Rev.0, April 2013

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