AND9081/D

NCV7381 FlexRay Bus Driver Application Note

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APPLICATION NOTE

Introduction

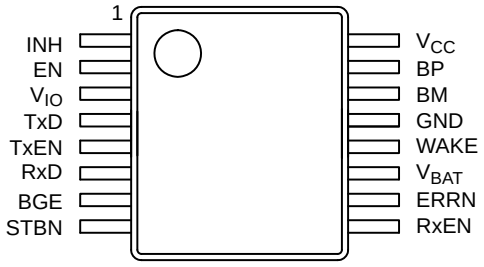
NCV7381 is a single-channel FlexRay bus driver compliant with the FlexRay Electrical Physical Layer Specification Rev. 3.0.1, capable of communicating at speeds of up to 10 Mbit/s.

It provides differential transmit and receive capability between a wired FlexRay communication medium on one side and a protocol controller and a host on the other side. The NCV7381 mode control functionality is optimized for nodes permanently connected to the car battery.

This document provides additional output characteristics for the digital output and INH pins, it gives PCB Layout recommendation and it analyzes the behavior of the NCV7381 in case of operating mode transition request.

- Digital outputs DC characteristics
- INH pin output characteristics
- Bus Driver PCB Layout
- Mode Transitions – STBN and EN Pin Filtering Time
- Optional ESD Protection

NCV7381 Pin Connections



(Top View)

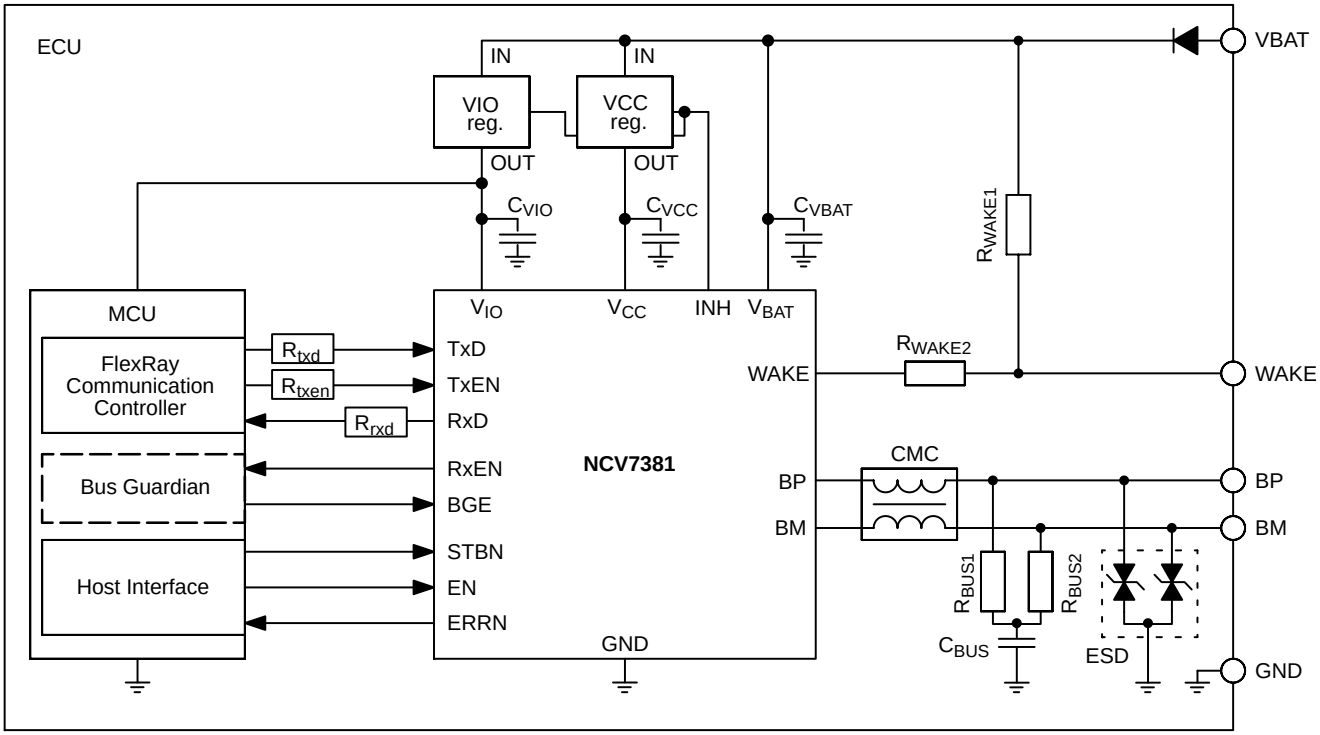


Figure 1. NCV7381 Application Diagram

Digital Outputs DC Characteristics

Typical digital outputs (RxD, RxEN and ERRN) characteristics are shown in the figures below. The characteristics are measured at room ambient temperature, in Normal mode (STBN and EN forced High), with no undervoltage and with supply voltages: V_{BAT} = 12 V, V_{CC} = 5 V, V_{IO} = 3.3 V and 5 V.

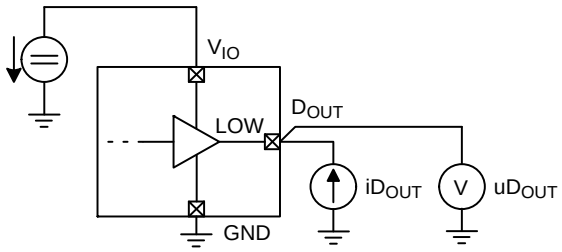


Figure 2. Test Setup for Output Low Characteristics on Digital Output Pins

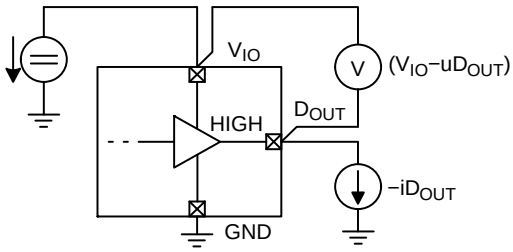


Figure 3. Test Setup for Output High Characteristics on Digital Output Pins

RxD Digital Output

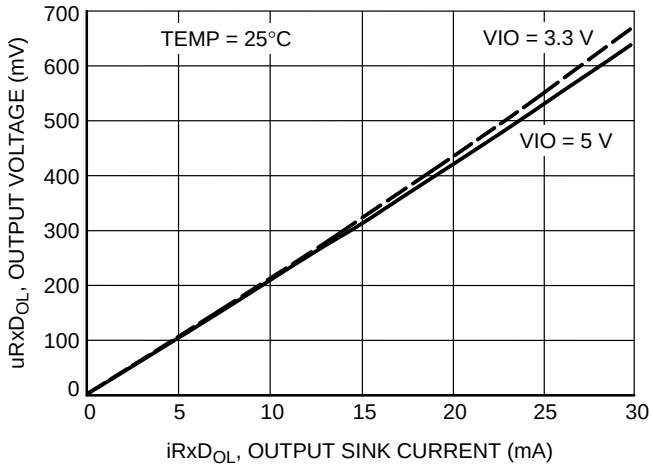


Figure 4. Typical RxD Output Sink Characteristics

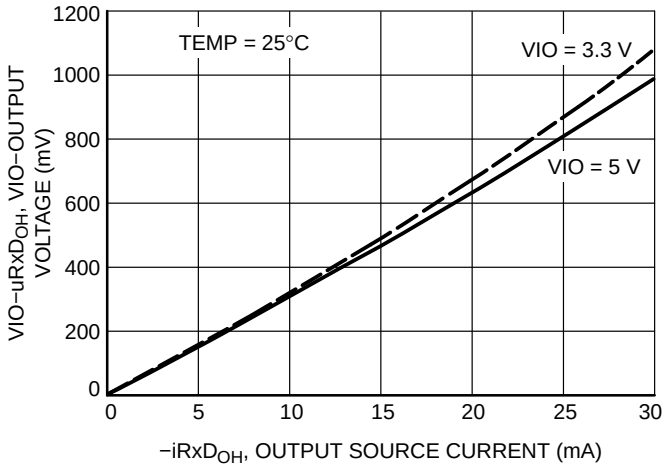


Figure 5. Typical RxD Output Source Characteristics

RxEN Digital Output

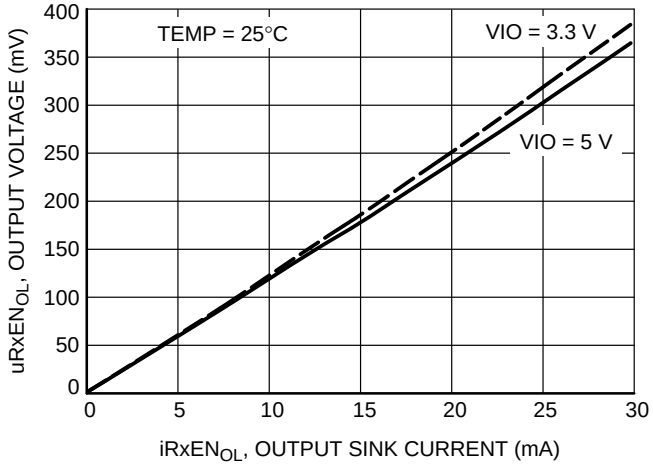


Figure 6. Typical RxEN Output Sink Characteristics

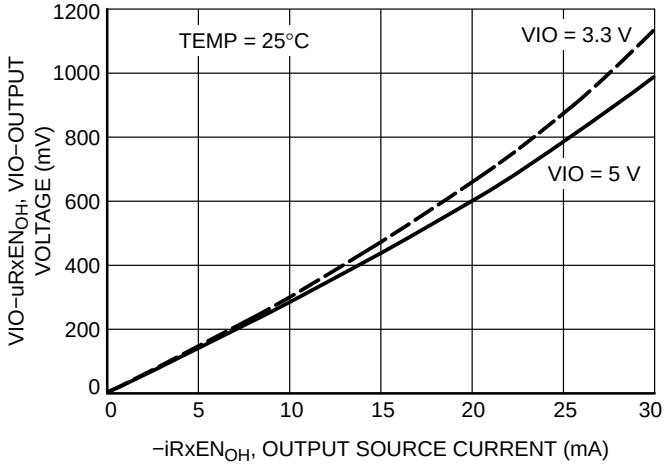


Figure 7. Typical RxEN Output Source Characteristics

ERRN Digital Output

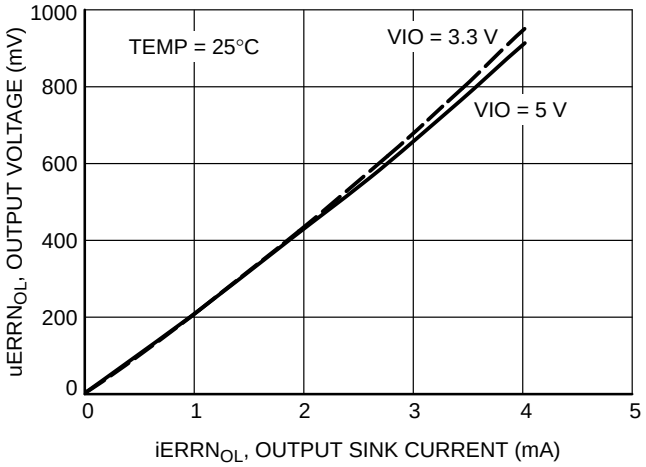


Figure 8. Typical ERRN Output Sink Characteristics

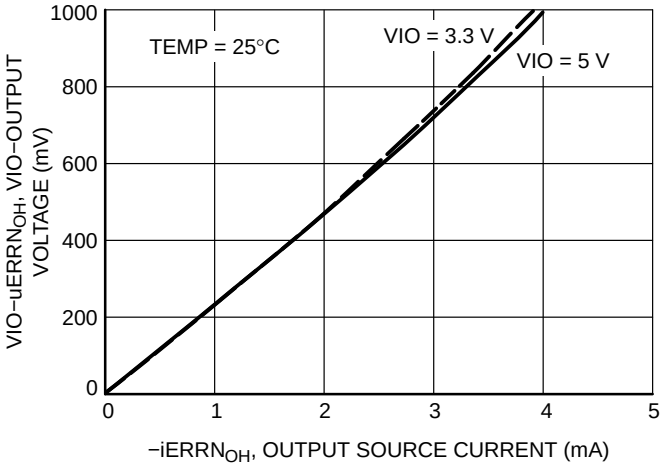


Figure 9. Typical ERRN Output Source Characteristics

INH Pin Output Characteristics

The NCV7381 provides a high-voltage output pin INH which can be used to control an external voltage regulator (see Figure 1). The pin INH is driven by a switch to V_{BAT} supply. In Normal, Receive-only, Standby and Go-to-Sleep modes, the switch is activated thus forcing a High level on the pin INH. In Sleep mode, the switch is open and INH pin remains floating. If a regulator is directly controlled by the INH, it is then active in all operating modes with an exception of the Sleep mode.

A typical INH switch voltage drop as a function of the INH pin output load current is shown in Figure 11. The characteristics are measured at room ambient temperature, in Normal mode (STBN and EN forced High), with no undervoltage and with V_{BAT} = 4.9 V and 14 V.

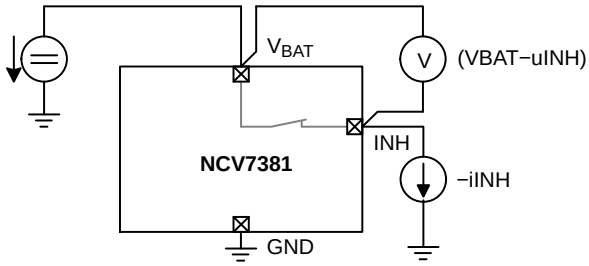


Figure 10. Test Setup for INH Output Characteristics

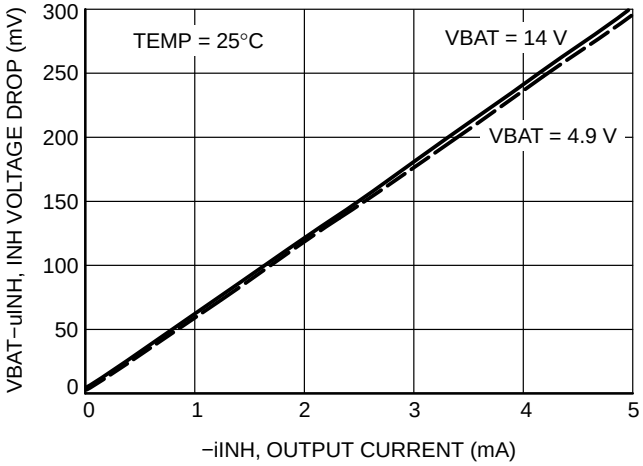


Figure 11. Typical INH Output Characteristic (INH signaling Not_Sleep)

Bus Driver PCB Layout

An example PCB layout is shown in the figure below. Modification of this layout is possible with the following recommendations:

- Place the NCV7381, the common mode choke and the optional ESD protection as near as possible to the BP and BM pins of the ECU connector.
- Route the BP and BM signal lines symmetric.
- Keep the distance between the lines BP and BM minimal.
- Keep the decoupling capacitors close to the particular supply pins.
- Keep the ground plane uninterrupted if possible.

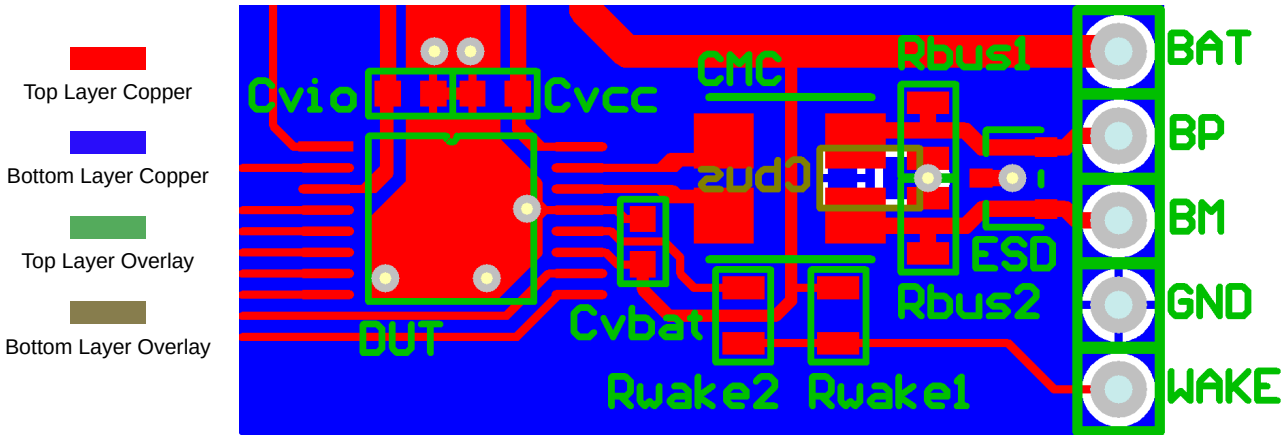


Figure 12. Example PCB Layout

Table 1. NCV7381: RECOMMENDED EXTERNAL COMPONENTS

Component	Function	Value	Unit	Note
C_{VBAT}	Decoupling Capacitor on Battery Line, Ceramic (X7R)	100	nF	Type 0603
C_{VCC}	Decoupling Capacitor on V_{CC} Supply Line, Ceramic (X7R)	100	nF	Type 0603
C_{VIO}	Decoupling Capacitor on V_{IO} Supply Line, Ceramic (X7R)	100	nF	Type 0603
R_{WAKE1}	Pull-up Resistor on WAKE Pin	33	kΩ	Type 0805
R_{WAKE2}	Serial Protection Resistor on WAKE Pin	3.3	kΩ	Type 0805
R_{BUS1}	Bus Termination Resistor	47.5	Ω	Type 0805, (Note 2)
R_{BUS2}	Bus Termination Resistor	47.5	Ω	Type 0805, (Note 2)
C_{BUS}	Common-mode Stabilizing Capacitor, Ceramic	4.7	nF	Type 0805, ±20%
CMC	Common-mode Chokes	100	μH	(Note 1)
ESD	Optional ESD Protection	NUP2115	−	Type SOT−23

1. Recommended common-mode chokes:
   MURATA DLW43SH101XK2
   MURATA DLW43SH510XK2
   MURATA DLW43SH101XP2
   EPCOS B82799C0104N001
   TDK ACT45R−101−2P−TL001
2. Tolerance ±1%; the value R_{BUS1} + R_{BUS2} should match the nominal cable impedance.

MODE TRANSITIONS – STBN AND EN PIN FILTERING TIME

The resulting operating mode is a function of the host signals STBN and EN, the state of the supply voltages and the wakeup detection.

During normal operation, the operating mode is directed by a host command – the host is directly driving pins STBN and EN to an appropriate logical state. In some cases these pins may be disconnected − usually during a microcontroller reset state, when the microcontroller's outputs may be put into a high-impedance state. In this case the resulting operating mode is determined by the NCV7381 EN and STBN pins internal pull-down resistors.

The STBN and EN pins are internally debounced and synchronized with the internal oscillator. The implemented debouncing time is 3 internal oscillator periods. Due to the synchronization, the actual delay between a change at the pin and a change of the internal signal may vary between 3 and 4 oscillator periods (parameter *dBDModeChange*, see the pictures below). The internal STBN and EN signal change is aligned with the internal oscillator rising edge.

Operating Mode Transition − Normal to Standby

A transition from Normal mode to Standby mode is initialized, when both STBN and EN, originally being High, are set Low (Figure 13). The STBN and EN falling edge do not need to occur exactly at the same time. However caution should be taken especially in case the EN falling edge is delayed too much with respect to the STBN falling edge, this could be considered as a Sleep mode transition request. Taking into account that the EN pin is ignored in Sleep mode, the original intention to enter Standby mode would not be completed (Figure 15).

If both STBN and EN go from High to Low at the same time (driven externally or driven by internal pull-down resistors), Standby mode is entered (Figure 13).

Even if the EN pin goes Low worst case 2 oscillator periods later than the STBN pin, the resulting operating mode is still Standby. Considering *dGo-To-Sleep* limiting values, the delay between STBN and EN pin falling edge should be less than 14 μs, in order to enter Standby mode successfully (Figure 14).

A delay between 14 μs and 51 μs leads to an uncertain mode transition – Standby mode or Sleep mode may be entered.

In case the delay STBN falling edge to EN falling edge is more than 51 μs, it is guaranteed that Sleep mode is entered.

In summary, the Standby mode is successfully entered if the delay between STBN and EN pin falling edges is less than 14 μs. Sleep mode is successfully entered if the delay between STBN and EN pin falling edges is more than 51 μs.

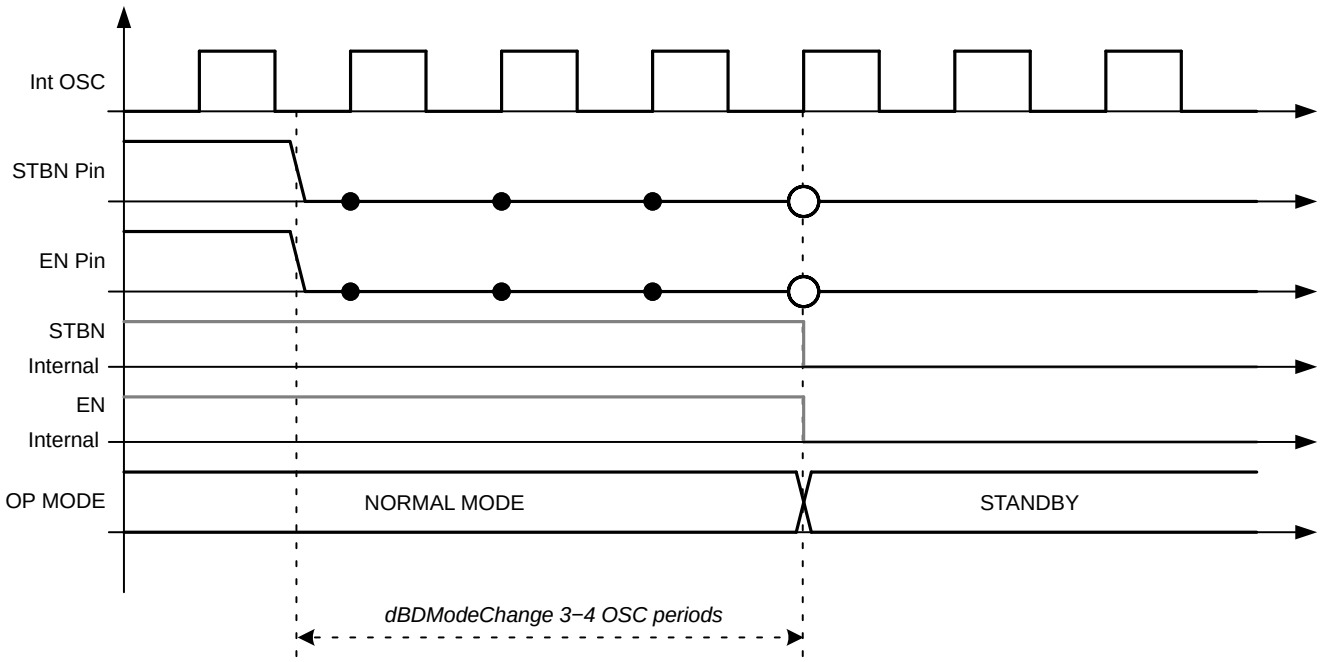


Figure 13. Mode Transition Example – STBN and EN Go Low at the Same Time

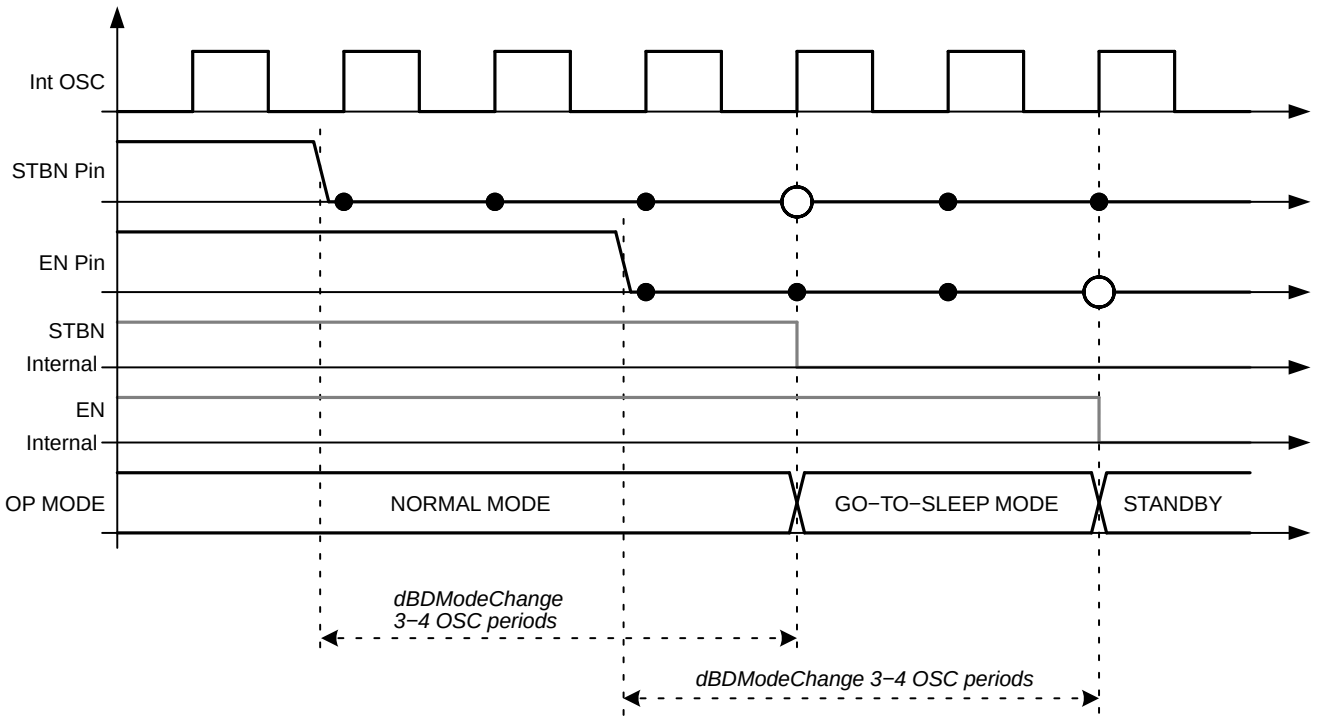


Figure 14. Mode Transition Example – EN goes Low max. 2 Osc. Period later than STBN

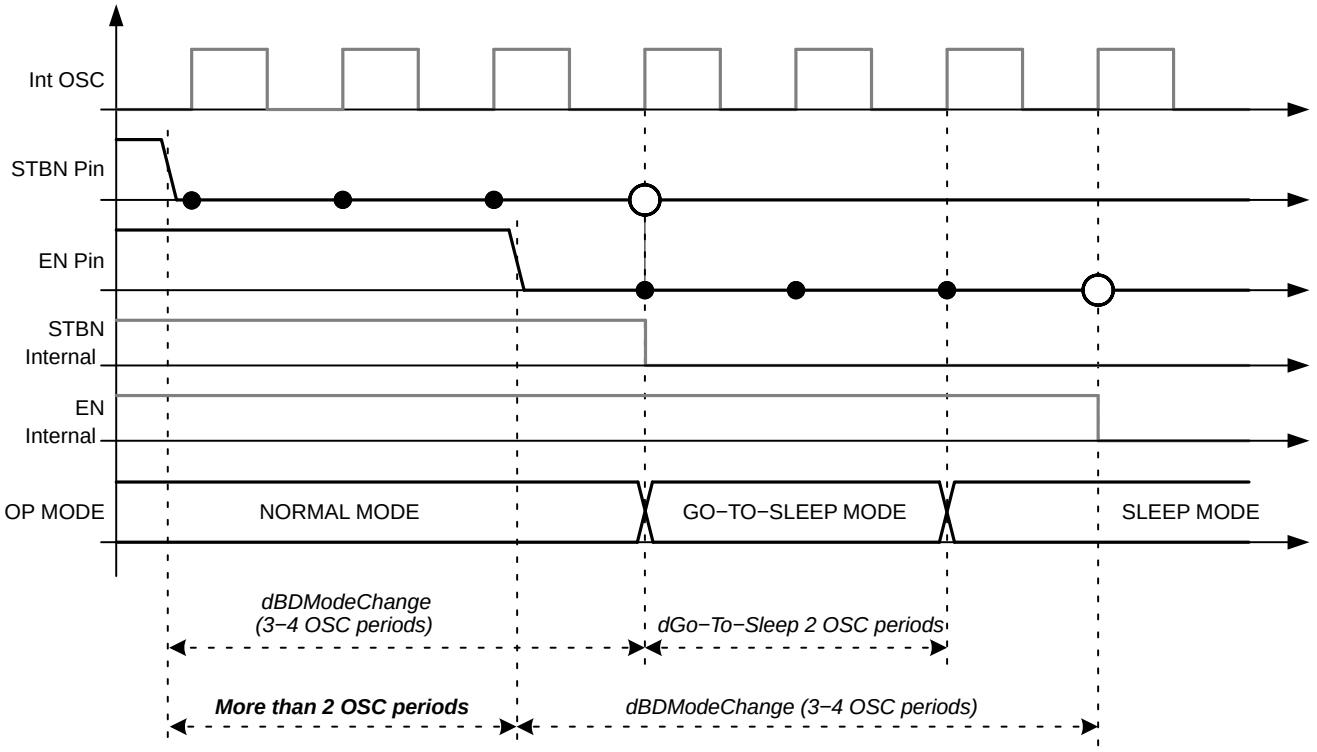


Figure 15. Mode Transition Example – EN goes Low more than 2 Osc. Period later than STBN

OPTIONAL ESD PROTECTION

In order to improve system reliability an additional external ESD protection may be used. As a result of the high speed nature, the FlexRay specification calls for a low capacitance protection of up to 20 pF and a tight deviation in capacitance between the signal pairs limited to 2%. The reason is that any additional ESD protection represents a capacitive load on the bus lines which can have undesired effects on electromagnetic emissions and immunity if the bus lines capacitive load does not match properly.

The NUP2115, dual line FlexRay Bus Protector, is designed for the highest possible signal integrity by limiting the stray capacitance to 10 pF max while having a nominal capacitance matching at 0.26% and achieving the ESD and other transient protection requirements.

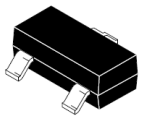


Figure 16. SOT−23 Package

System ESD measurement results are shown in the Table 2. Tested without external bus filter network, which is the worst case. The absolute values are from internal measurements. It indicates noticeable increase of the maximum possible discharge voltage. The values measured by external laboratory are visible in device datasheets [1][4].

Table 2. SYSTEM HBM ON PINS BP AND BM, per IEC 61000-4-2; 150 pF/330 Ω

	NCV7381	NCV7381 + NUP2115L
Requirement	±6 kV	
Pin	No failure up to:	
BP	±13 kV	±21 kV
BM	±13 kV	±21 kV

For more information on the device details, see the product datasheet [4].

REFERENCES

[1] ON Semiconductor, NCV7381/D Datasheet, Rev.0, May 2012

[2] FlexRay Consortium. FlexRay Communications System − Electrical Physical Layer Specification, V3.0.1, October 2010

[3] FlexRay Consortium. FlexRay Communications System − Physical Layer EMC Measurement Specification, V3.0.1, October 2010

[4] ON Semiconductor, NUP2115L/D, Datasheet, Rev.0, April 2013

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