



# MPM3695-25

## 16V, 20A, Scalable DC/DC Power Module with PMBus

### DESCRIPTION

The MPM3695-25 is a scalable, fully integrated power module with a PMBus interface. The MPM3695-25 offers a complete power solution that achieves up to 25A of peak output current with excellent load and line regulation over a wide input voltage range. It operates with high efficiency over a wide load range and can be paralleled to deliver a higher load current.

The MPM3695-25 adopts MPS's proprietary, multi-phase constant-on-time (MCOT) control, which provides ultra-fast transient response and simple loop compensation. The PMBus interface provides module configurations and monitoring of key parameters.

The MPM3695-25 features full protection features, including over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP). It requires a minimal number of readily available external components and is available in a QFN-59 (10mmx12mmx4mm) package.

### FEATURES

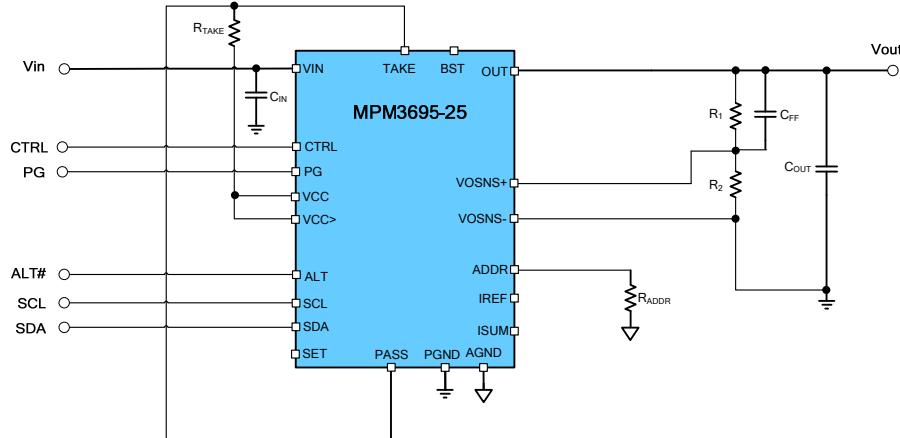
- Wide Input Voltage Range from 3V
  - 3V-16V Input Voltage with External  $V_{CC}$
  - 4V-16V Input Voltage with Internal  $V_{CC}$
- 0.5V to 5.5V Output Voltage Range
- 20A Continuous Output Current, Peak 25A
- Auto Interleaving for Multi-Phase Operation
- Auto Compensation with Adaptive MCOT for Ultra-Fast Transient Response
- 1% Reference Voltage Over 0°C to +70°C Junction Temperature Range
- True Remote Sense of Output Voltage
- PMBus 1.3 Compliant
- Telemetry Read-Back Including  $V_{IN}$ ,  $V_{OUT}$ ,  $I_{OUT}$ , Temperature, and Faults
- Programmable via PMBus
  - Current Limit
  - Selection of Pulse-Skip Mode or Continuous Conduction Mode (CCM)
  - Soft-Start Time
  - Switching Frequency
  - Fault Limits
- Available in a QFN-59 (10mmx12mmx4mm) Package

### APPLICATIONS

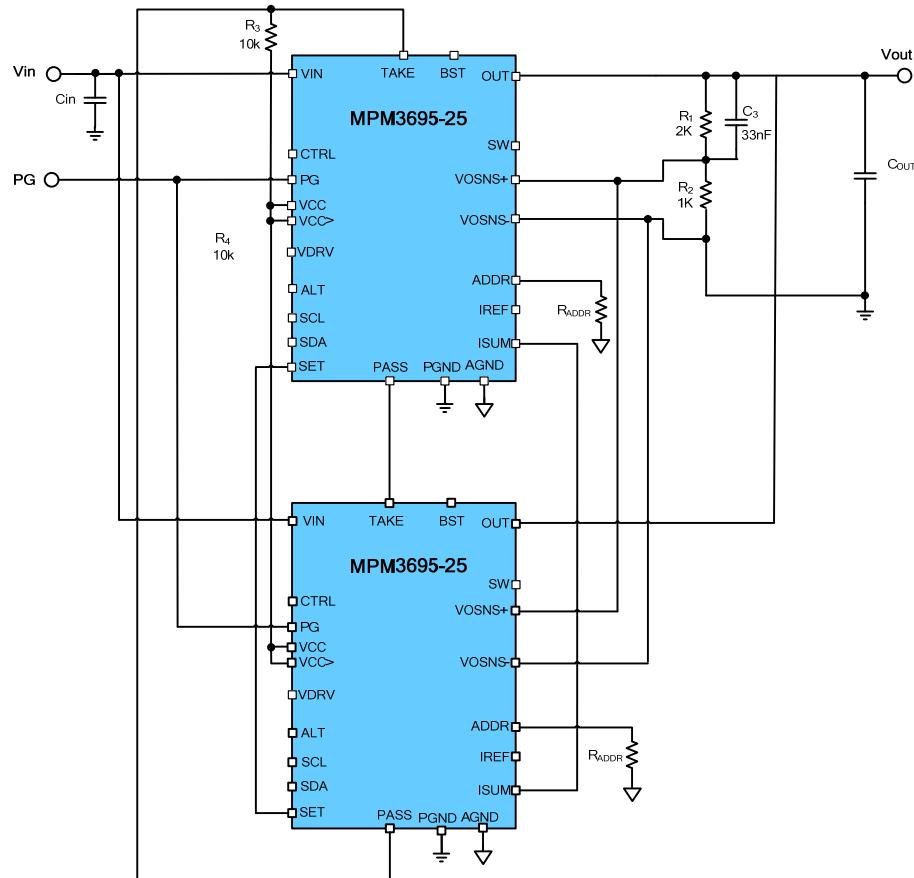
- Telecom and Networking Systems
- Industrial Equipment
- Servers and Computing
- FPGAs/ASIC AI and Data Mining

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## TYPICAL APPLICATION



Single Phase Operation



Dual Phase Operation

## ORDERING INFORMATION

| Part Number         | Package                   | Top Marking |
|---------------------|---------------------------|-------------|
| MPM3695GRF-25-xxxx* | QFN-59<br>(10mmx12mmx4mm) | See Below   |
| EVKT-MPM3695-25-A   | \                         | \           |

\* -xxxx is the configuration code identifier for the register settings stored in the MTP memory. Each “x” can be a hexadecimal value between 0 and F. The part number with default register setting is MPM3695GRF-25-0022. Please contact MPS to create a unique configuration identifier for customized design.

## TOP MARKING

**MPSYYWW**  
**MP3695**  
**LLLLLLLL**  
**25M**

MPS: MPS prefix

YY: Year code

WW: Week code

MP3695: Part number

LLLLLLLLL: Lot number

25: Suffix of part number

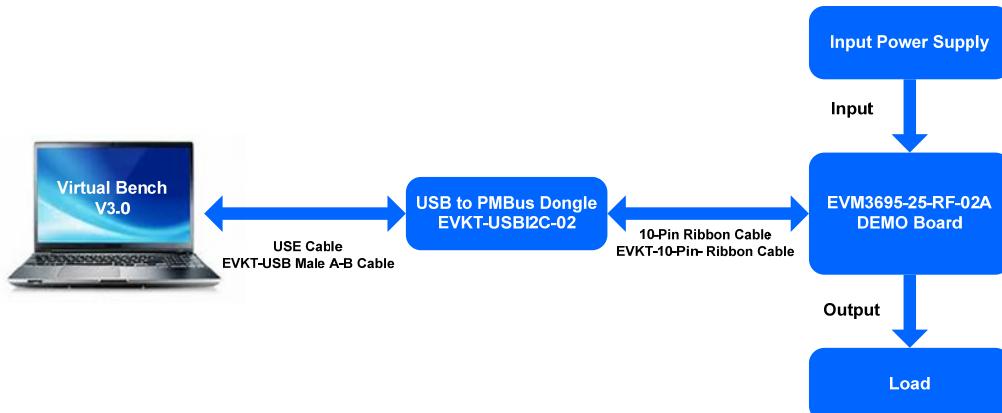
M: Module

## EVALUATION KIT EVKT-MPM3695-25-A

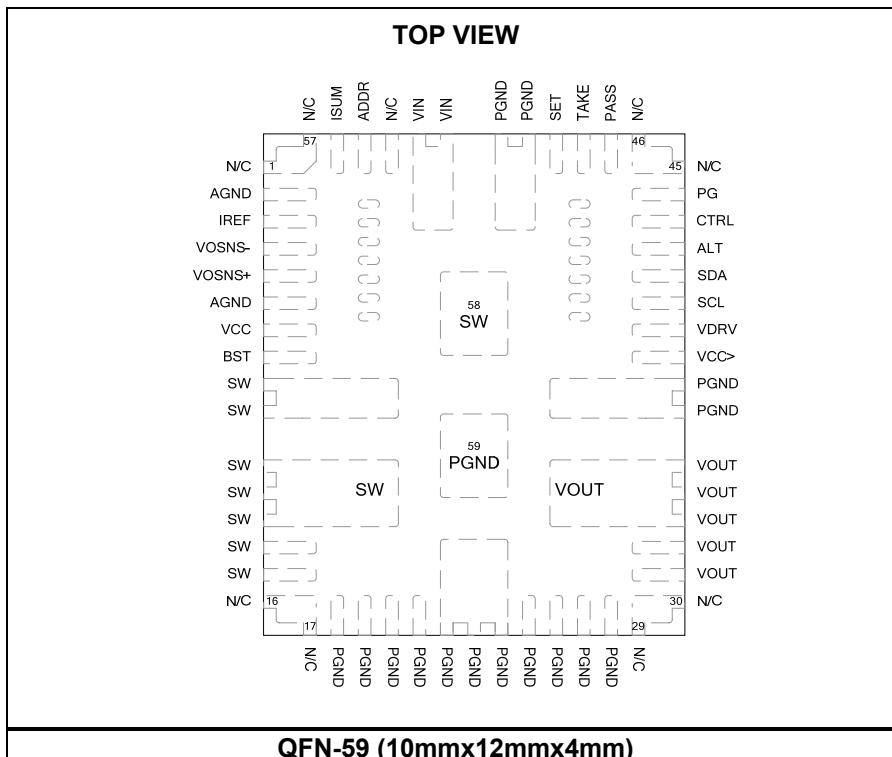
EVKT-MPM3695-25-A Kit Contents: (Items can be ordered separately).

| # | Part Number        | Item  | Quantity |
|---|--------------------|---|----------|
| 1 | EVM3695-25-RF-02A  | MPM3695-25 Single Phase Evaluation Board                            | 1        |
| 2 | MPM3695GRF-25-0022 | 1pcs MPM3695-25 Module  | 1        |
| 3 | EVKT-USBI2C-02*    | Includes One USB to I2C Dongle, One USB Cable, and One Ribbon Cable | 1        |

Order Directly from MonolithicPower.com or MPS distributors



## PACKAGE REFERENCE



## PIN FUNCTIONS

| PIN #                             | Name   | Description  |
|-----------------------------------|--------|--|
| 2,6                               | AGND   | <b>Analog ground.</b> Reference point of the control circuit.  |
| 3                                 | IREF   | <b>Current reference output.</b> Keep this pin floating.   |
| 4                                 | VOSNS- | <b>Output voltage sense negative return.</b> Connect directly to the GND sense point of the load. Short to GND if remote sense is not used.  |
| 5                                 | VOSNS+ | <b>Output voltage sense positive return.</b> Connect this pin to the positive sense point of the output voltage to provide feedback voltage to the system.   |
| 7                                 | VCC    | <b>Output of the internal 3.3V LDO.</b> The driver and control circuits are powered by this voltage. Must be connected to Pin 38.  |
| 8                                 | BST    | <b>Bootstrap.</b> Keep this pin floating.  |
| 9-15, 58                          | SW     | <b>Switch node.</b> Keep them floating.  |
| 31-35                             | VOUT   | <b>Module output voltage node.</b> Connect with wide PCB copper plane.   |
| 18-28, 36, 37, 50, 51, 59         | PGND   | <b>Power ground.</b> This pin is the reference point of the regulated output voltage. Connect with PCB copper planes as wide as possible.  |
| 38                                | VCC>   | <b>Input of driver circuit.</b> Must be connected to Pin 7.  |
| 39                                | VDRV   | <b>Decoupling pin for 3.3V driver power supply.</b>  |
| 40                                | SCL    | <b>PMBus serial clock.</b>   |
| 41                                | SDA    | <b>PMBus serial data.</b>  |
| 42                                | ALT    | <b>PMBus alert.</b> Open drain output, active low. A pull-up resistor must be connected to a 3.3V rail.  |
| 43                                | CTRL   | <b>Converter control.</b> CTRL is a digital input that turns the regulator on or off. Drive CTRL high to turn the regulator on, drive it low to turn it off. Do not float this pin.  |
| 44                                | PG     | <b>Multi-purpose power good output.</b> This pin can be configured as an output pin for single-phase operation or an input and output pin for multi-phase configuration. A pull-up resistor connected to a DC voltage is required to indicate high if the output voltage is higher than 90% of the nominal voltage. Refer to the application section for detailed configuration. |
| 47                                | PASS   | <b>Passes RUN signal to the next phase.</b> Refer to the applications section for connection details.  |
| 48                                | TAKE   | <b>Receives RUN signal from the previous phase.</b> Refer to the typical applications section for connection details.  |
| 49                                | SET    | <b>PWM signal.</b> The set signal turns on the HSFET when a RUN signal appears. For multi-phase operation, tie the SET pins of all the phases together.  |
| 52, 53                            | VIN    | <b>Supply voltage.</b> This pin provides power to the module. Decoupling capacitors are required to be connected between VIN and GND. Connect VIN with a wide copper plane.  |
| 55                                | ADDR   | <b>PMBus slave address setting pin.</b> Connect a resistor between this pin to AGND to set the address of this device.   |
| 56                                | ISUM   | <b>Reference current output.</b> For single-phase operation, keep this pin floating; for multi-phase operation, connect ISUM pins of all phases together.  |
| 1, 16, 17, 29, 30, 45, 46, 54, 57 | NC     | <b>No Internal Connection.</b>   |

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

|   |                          |
|---|--------------------------|
| Supply voltage ( $V_{IN}$ ) .....   | 18V                      |
| $V_{SW(DC)}$ .....  | -0.3V to $V_{IN}$ + 0.3V |
| $V_{SW(25ns)}$ <sup>(2)</sup> .....                                       | -3V to 25V               |
| $V_{SW(25ns)}$ .....  | -5V to 25V               |
| $V_{OUT}$ .....   | 5.5V                     |
| $V_{BST}$ .....   | $V_{SW}$ + 4V            |
| $V_{CC}$ .....  | 4.5V                     |
| CTRL current ( $I_{CTRL}$ ).....  | 2.5mA                    |
| All other pins .....  | -0.3V to 4.3V            |
| Continuous power dissipation ( $T_A = +25^\circ C$ ) <sup>(3)</sup> ..... | 5W                       |
| Junction temperature .....  | 170°C                    |
| Lead temperature.....   | 260°C                    |
| Storage temperature .....   | -65°C to +170°C          |

**Recommended Operating Conditions<sup>(4)</sup>**

|  |                 |
|--|-----------------|
| Supply voltage ( $V_{IN}$ ) .....      | 4V to 16V       |
| Output voltage ( $V_{OUT}$ ).....      | 0.5V to 5.5V    |
| External $V_{CC}$ bias .....           | 3.12V to 3.6V   |
| CTRL current ( $I_{CTRL}$ ).....       | 1mA             |
| Operating junction temp. ( $T_J$ ).... | -40°C to +125°C |

| <b><i>Thermal Resistance</i></b> <sup>(5)</sup> | $\theta_{JA}$ | $\theta_{JB}$ |
|---|---------------|---------------|
| QFN-59 (10x12x4mm) .....                        | 17            | 3.4 ... °C/W  |

**NOTES:**

- 1) Exceeding these ratings may damage the device.
- 2) Measured by using differential oscilloscope probe.
- 3) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX)- $T_A$ )/ $\theta_{JA}$ . Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 4) The device is not guaranteed to function outside of its operating conditions.
- 5) Measured on EVM3695-25-RF-02A Demo Board 6-LAYERS PCB.

**ELECTRICAL CHARACTERISTICS**
 **$V_{IN} = 12V$ ,  $T_J = -40^{\circ}C$  to  $125^{\circ}C$ , unless otherwise noted.**

| Parameters   | Symbol              | Condition                                   | Min  | Typ       | Max  | Units       |
|--|---------------------|---|------|-----------|------|-------------|
| <b><math>V_{IN}</math> Supply Current</b>                  |                     |   |      |           |      |             |
| Supply current (shutdown)                                  | $I_{IN}$            | $V_{CTRL} = 0V$                             |      | 2.5       | 4    | mA          |
| <b>Input Voltage</b>                                       |                     |   |      |           |      |             |
| Input voltage range  | $V_{IN}$            | No external VCC                             | 4    |           | 16   | V           |
|  |                     | With 3.3V External VCC                      | 3    |           | 16   |             |
| <b>Output Voltage</b>                                      |                     |   |      |           |      |             |
| Output voltage range <sup>(6)</sup>                        | $V_{OUT\_RANGE}$    |   | 0.5  |           | 5.5  | V           |
| Load regulation <sup>(6)</sup>                             | $V_{OUT\_DC\_Load}$ | $I_{OUT}$ from 0A to 25A                    |      | $\pm 0.5$ |      | % $V_{OUT}$ |
| Line regulation <sup>(6)</sup>                             | $V_{OUT\_DC\_Line}$ | $V_{IN}$ from 4V to 16V,<br>$I_{OUT} = 20A$ |      | $\pm 0.5$ |      | % $V_{OUT}$ |
| <b>Current Limit</b>                                       |                     |   |      |           |      |             |
| Valley current limit                                       | $I_{LIM}$           | Default setting                             |      | 27        |      | A           |
| Min valley current limit programmable value <sup>(6)</sup> |                     |   |      | 5         |      | A           |
| Max current limit programmable value <sup>(6)</sup>        |                     |   |      | 32        |      | A           |
| Low-side negative current limit in OVP                     | $I_{LIM\_NEG\_OVP}$ |   |      | -13       |      | A           |
| <b>CTRL</b>  |                     |   |      |           |      |             |
| CTRL ON threshold  | $CTRL_{ON}$         |   |      | 2.04      | 2.2  | V           |
| CTRL OFF threshold   | $CTRL_{OFF}$        |   |      | 1.66      |      | V           |
| <b>Frequency and Timer</b>                                 |                     |   |      |           |      |             |
| Switching frequency  | $f_{sw}$            | Default Value                               |      | 600       |      | kHz         |
| Minimum on time <sup>(6)</sup>                             | $T_{ON\_MIN}$       | $F_s = 1000\text{kHz}$ , $V_o = 0.6V$       |      | 50        |      | ns          |
| Minimum off time <sup>(6)</sup>                            | $T_{OFF\_MIN}$      | $V_{FB} = 580\text{mV}$                     |      | 220       |      | ns          |
| <b>Output Over-Voltage and Under-Voltage Protection</b>    |                     |   |      |           |      |             |
| OVP threshold  | $V_{OVP}$           | Default setting (D4h[1:0] = 00)             | 111% | 115%      | 119% | $V_{REF}$   |
| UV threshold   | $V_{UVP}$           | Default setting (D9h[3:2] = 10)             | 75%  | 79%       | 83%  | $V_{REF}$   |
| Max programmable OVP threshold                             | $V_{OVP\_max}$      | D4h[1:0] = 11                               | 126% | 130%      | 134% | $V_{REF}$   |
| Min programmable OVP threshold                             | $V_{OVP\_min}$      | D4h[1:0] = 00                               | 111% | 115%      | 119% | $V_{REF}$   |
| Max programmable UV threshold                              | $V_{UVP\_max}$      | D9h[3:2] = 11                               | 80%  | 84%       | 88%  | $V_{REF}$   |
| Min programmable UV threshold                              | $V_{UVP\_min}$      | D9h[3:2] = 00                               | 65%  | 69%       | 73%  | $V_{REF}$   |

**ELECTRICAL CHARACTERISTICS (continued)**

V<sub>IN</sub> = 12V, T<sub>J</sub> = -40°C to 125°C, unless otherwise noted.

| Parameters                                       | Symbol                  | Condition                          | Min | Typ   | Max  | Units            |
|--|-------------------------|------------------------------------|-----|-------|------|------------------|
| OSM threshold rising                             | V <sub>OSM_RISE</sub>   |                                    |     | 104%  |      | V <sub>REF</sub> |
| OSM threshold falling                            | V <sub>OSM_FALL</sub>   |                                    |     | 102%  |      | V <sub>REF</sub> |
| <b>ADC<sup>(6)</sup></b>                         |                         |                                    |     |       |      |                  |
| Voltage range                                    |                         |                                    | 0   |       | 1.28 | V                |
| ADC resolution                                   |                         |                                    |     | 10    |      | bits             |
| DNL  |                         |                                    |     | 1     |      | LSB              |
| Sample rate                                      |                         |                                    |     | 3     |      | kHz              |
| <b>DAC (Feedback Voltage)</b>                    |                         |                                    |     |       |      |                  |
| Range  |                         |                                    | 500 | 600   | 672  | mV               |
| Feedback accuracy                                | V <sub>FB</sub>         | T <sub>J</sub> = +25°C             | 594 | 600   | 606  | mV               |
| Feedback accuracy                                | V <sub>FB</sub>         | T <sub>J</sub> = -40°C to 125°C    | 591 | 600   | 609  | mV               |
| Resolution <sup>(6)</sup>                        |                         | Per LSB                            |     | 2     |      | mV               |
| Feedback voltage with margin high <sup>(6)</sup> | V <sub>FB_MG_HIGH</sub> |                                    |     | 672   |      | mV               |
| Feedback voltage with margin low <sup>(6)</sup>  | V <sub>FB_MG_LOW</sub>  |                                    |     | 500   |      | mV               |
| <b>Soft Start and Turn On/Off Delay</b>          |                         |                                    |     |       |      |                  |
| Soft-start time                                  | t <sub>SS</sub>         |                                    |     | 2     |      | ms               |
| Turn-on delay <sup>(6)</sup>                     | t <sub>ON_DELAY</sub>   | Default setting                    |     | 0     |      | ms               |
| Turn-off delay                                   | t <sub>OFF_DELAY</sub>  | Default setting                    |     | 0     |      | ms               |
| <b>Error Amplifier</b>                           |                         |                                    |     |       |      |                  |
| Feedback Current                                 | I <sub>FB</sub>         | V <sub>FB</sub> = V <sub>REF</sub> |     | 50    | 100  | nA               |
| <b>Soft Shutdown</b>                             |                         |                                    |     |       |      |                  |
| Soft shutdown discharge FET                      | R <sub>ON_DISCH</sub>   |                                    |     | 60    |      | Ω                |
| <b>Under-Voltage Lockout (UVLO)</b>              |                         |                                    |     |       |      |                  |
| VCC under-voltage lockout threshold rising       | V <sub>CVCVTH</sub>     | Default setting                    | 2.6 | 2.75  | 2.9  | V                |
| VCC under-voltage lockout threshold hysteresis   | V <sub>CCHYS</sub>      | Default setting                    |     | 200   |      | mV               |
| Min input programmable turn-on voltage           | V <sub>IN_ON_MIN</sub>  | V <sub>CC</sub> = 3.3V             |     | 3     |      | V                |
| Max input programmable turn-on voltage           | V <sub>IN_ON_MAX</sub>  |                                    |     | 15    |      | V                |
| Min input programmable turn-off voltage          | V <sub>IN_OFF_MIN</sub> | V <sub>CC</sub> = 3.3V             |     | 2.75  |      | V                |
| Max input programmable turn-off voltage          | V <sub>IN_OFF_MAX</sub> |                                    |     | 14.75 |      | V                |

**ELECTRICAL CHARACTERISTICS (continued)**

V<sub>IN</sub> = 12V, T<sub>J</sub> = -40°C to 125°C, unless otherwise noted.

| Parameters                                     | Symbol                           | Condition   | Min  | Typ   | Max | Units            |
|--|----------------------------------|---|------|-------|-----|------------------|
| <b>Power Good</b>                              |                                  |   |      |       |     |                  |
| Power good high threshold                      | P <sub>G</sub> <sub>Vth_Hi</sub> | FB from low to high, default setting (D9h[1:0] = 01)  |      | 92.5% |     | V <sub>REF</sub> |
| Power good low threshold                       | P <sub>G</sub> <sub>Vth_Lo</sub> | FB from high to low, default setting (D9h[3:2] = 10)  |      | 79%   |     | V <sub>REF</sub> |
| Power good low to high delay                   | P <sub>G</sub> <sub>Td</sub>     | Default setting (D1h[5:2] = 0000)   |      | 2.0   |     | ms               |
| Power good sink current capability             | V <sub>PG</sub>                  | I <sub>PG</sub> = 10mA  |      |       | 0.3 | V                |
| Power good leakage current                     | I <sub>PG</sub> _LEAK            | V <sub>PG</sub> = 3V  |      | 1.5   |     | μA               |
| Power good low-level output voltage            | V <sub>OL_100</sub>              | V <sub>IN</sub> = 0V, pull PGOOD up to 3.3V through a 100kΩ resistor, T <sub>J</sub> = 25°C |      | 600   | 720 | mV               |
|  | V <sub>OL_10</sub>               | V <sub>IN</sub> = 0V, pull PGOOD up to 3.3V through a 10kΩ resistor, T <sub>J</sub> = 25°C  |      | 700   | 820 |                  |
| <b>Thermal Protection (TP)</b>                 |                                  |   |      |       |     |                  |
| TP fault rising threshold <sup>(6)</sup>       | T <sub>SD_Rise</sub>             | Default setting   |      | 145   |     | °C               |
| TP fault falling threshold <sup>(6)</sup>      | T <sub>SD_Fall</sub>             | Default setting   |      | 125   |     | °C               |
| TP warning rising threshold <sup>(6)</sup>     | T <sub>WARN_Rise</sub>           | Default setting   |      | 130   |     | °C               |
| TP warning falling threshold <sup>(6)</sup>    | T <sub>WARN_Fall</sub>           | Default setting   |      | 110   |     | °C               |
| Min TP warning temp <sup>(6)</sup>             | T <sub>SD_WARN_MIN</sub>         |   |      | 35    |     | °C               |
| Max TP warning temp <sup>(6)</sup>             | T <sub>SD_WARN_MAX</sub>         |   |      | 160   |     | °C               |
| <b>Monitoring Parameters</b>                   |                                  |   |      |       |     |                  |
| Output voltage monitor accuracy                | M <sub>VOUT_ACC</sub>            | V <sub>O</sub> =0.6V  | -2%  | 0.6   | 2%  | V                |
| Output voltage bit resolution                  |                                  |   |      | 1.5   |     | mV               |
| Output current monitor accuracy <sup>(6)</sup> | M <sub>IOUT_ACC</sub>            | V <sub>O</sub> = 1.2V, fs = 600kHz, I <sub>O</sub> = 20A                                    | -10% | 20    | 10% | A                |
| Output current bit resolution <sup>(6)</sup>   |                                  |   |      | 62.5  |     | mA               |
| Input voltage monitor accuracy                 | M <sub>IN_ACC</sub>              |   | -2%  | 12    | 2%  | V                |
| Input voltage bit resolution <sup>(7)</sup>    |                                  |   |      | 25    |     | mV               |

**ELECTRICAL CHARACTERISTICS (continued)**

V<sub>IN</sub> = 12V, T<sub>J</sub> = -40°C to 125°C, unless otherwise noted.

| Parameters  | Symbol            | Condition                           | Min  | Typ  | Max  | Units |
|---|-------------------|-------------------------------------|------|------|------|-------|
| <b>PMBus DC Characteristics (SDA, SCL, ALERT)<sup>(6)</sup></b> |                   |                                     |      |      |      |       |
| Input high voltage  | V <sub>IH</sub>   |                                     |      |      | 2.1  | V     |
| Input low voltage   | V <sub>IL</sub>   |                                     | 0.8  |      |      | V     |
| Output low voltage  | V <sub>OL</sub>   | I <sub>OL</sub> = 1mA               |      |      | 0.4  | V     |
| Input leakage current   | I <sub>LEAK</sub> | SDA, SCL, ALERT = 3.3V              | -10  |      | 10   | µA    |
| Maximum voltage (SDA, SCL, ALERT, CTRL)                         | V <sub>MAX</sub>  | Transient voltage including ringing | -0.3 | 3.3  | 3.6  | V     |
| Pin capacitance on SDA,SCL                                      | C <sub>PIN</sub>  |                                     |      |      | 10   | pF    |
| <b>PMBus Timing Characteristics<sup>(7)</sup></b>               |                   |                                     |      |      |      |       |
| Min operating frequency   |                   |                                     |      | 10   |      | kHz   |
| Max operating frequency   |                   |                                     |      | 1000 |      | kHz   |
| Bus free time   |                   | Between stop and start condition    | 4.7  |      |      | µs    |
| Holding time  |                   |                                     | 4.0  |      |      | µs    |
| Repeated start condition set-up time                            |                   |                                     | 4.7  |      |      | µs    |
| Stop condition set-up time                                      |                   |                                     | 4.0  |      |      | µs    |
| Data hold time  |                   |                                     | 300  |      |      | ns    |
| Data set-up time  |                   |                                     | 250  |      |      | ns    |
| Clock low time out  |                   |                                     | 25   |      | 35   | ms    |
| Clock low period  |                   |                                     | 4.7  |      |      | µs    |
| Clock high period   |                   |                                     | 4.0  |      | 50   | µs    |
| Clock/data fall time  |                   |                                     |      |      | 300  | ns    |
| Clock/data rise time  |                   |                                     |      |      | 1000 | ns    |

**NOTE:**

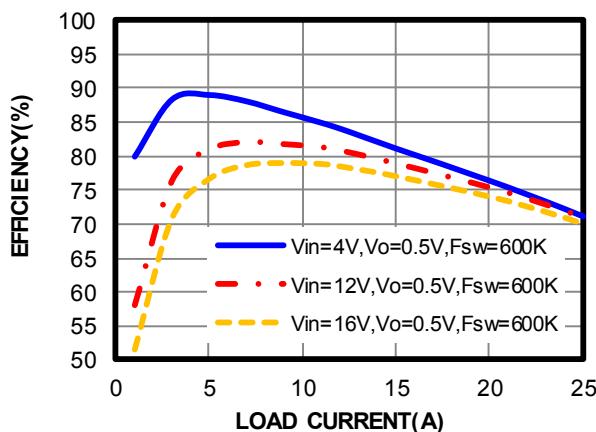
6) Guaranteed by design.

7) Guaranteed by design, not tested in production. The parameter is tested during parameters characterization.

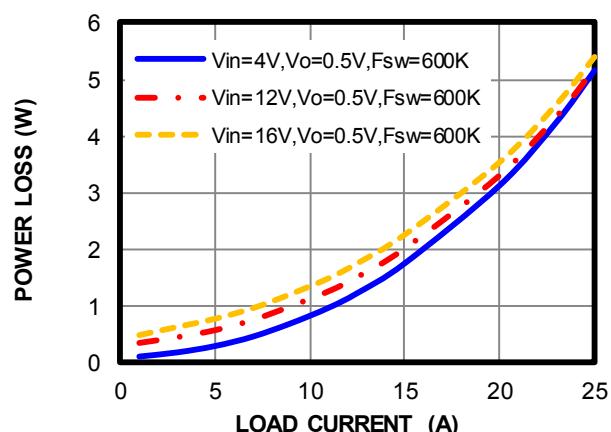
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}=12V$ ,  $V_{OUT}=1.8V$ ,  $F_{sw}=600\text{kHz}$ ,  $T_A=+25^\circ\text{C}$ , unless otherwise noted.

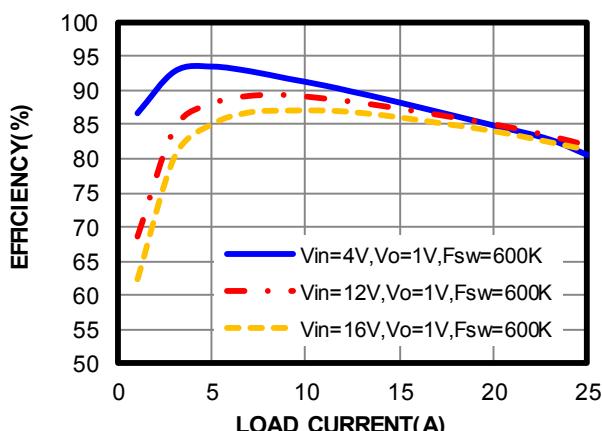
Efficiency vs. Load Current



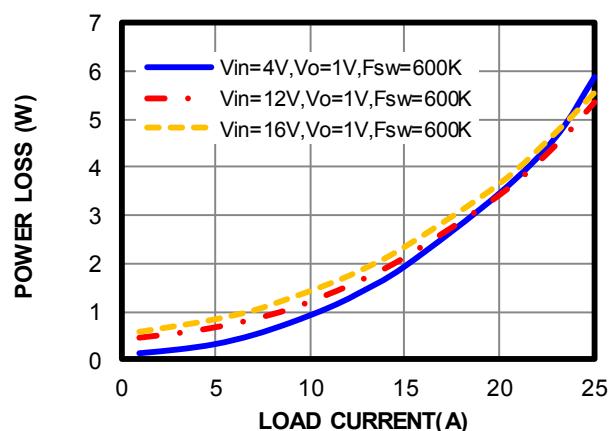
Power Loss vs. Load Current



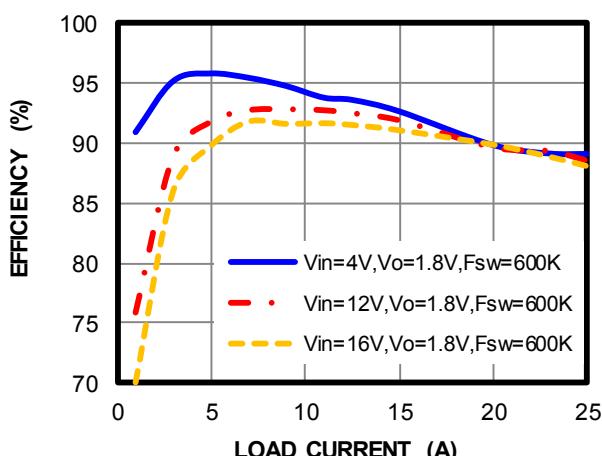
Efficiency vs. Load Current



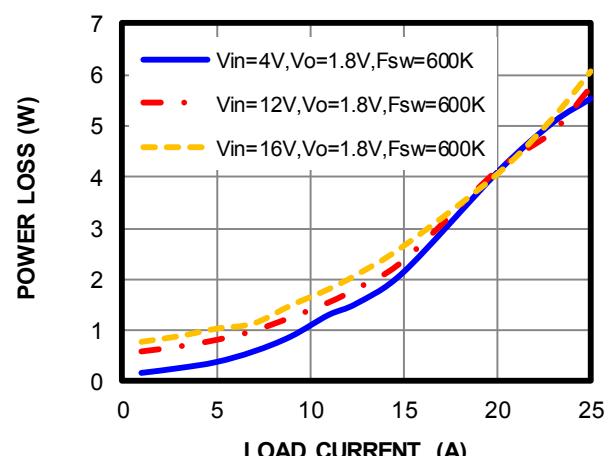
Power Loss vs. Load Current



Efficiency vs. Load Current



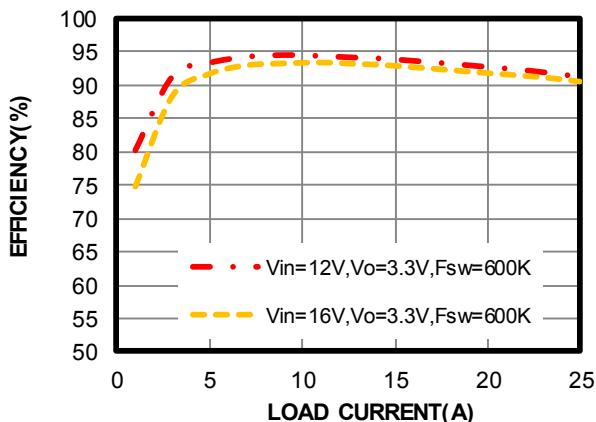
Power Loss vs. Load Current



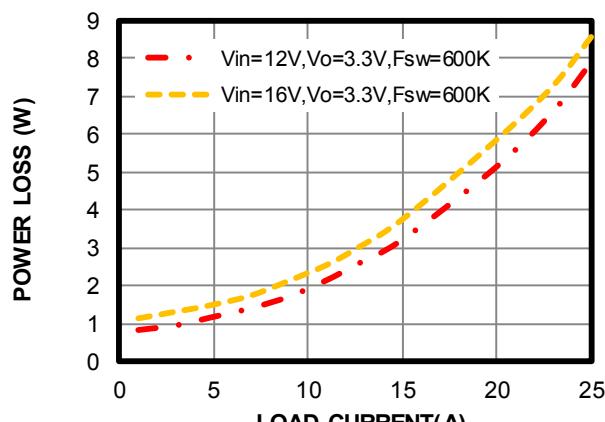
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

$V_{IN}=12V$ ,  $V_{OUT}=1.8V$ ,  $F_{sw}=600kHz$ ,  $T_A=+25^\circ C$ , unless otherwise noted.

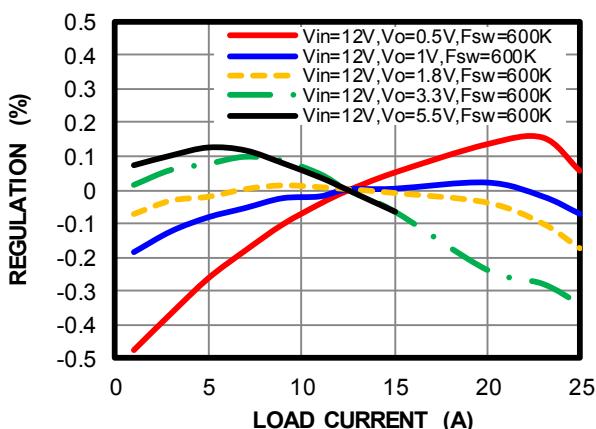
Efficiency vs. Load Current



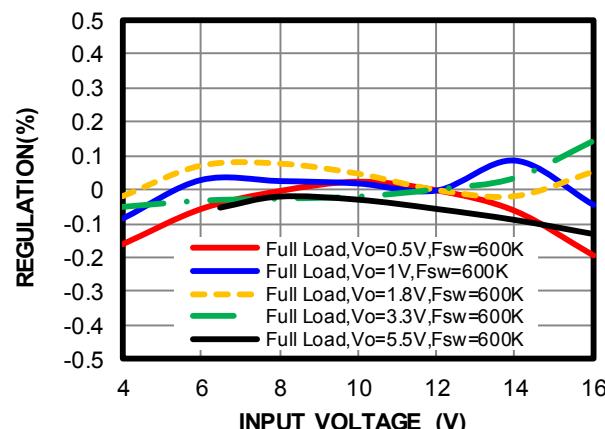
Power Loss vs. Load Current



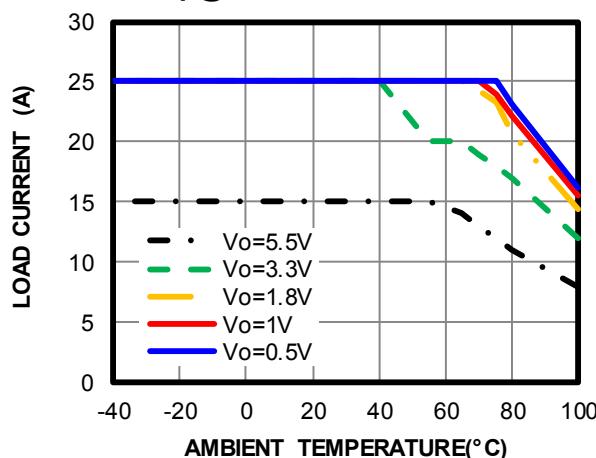
Regulation vs. Load Current



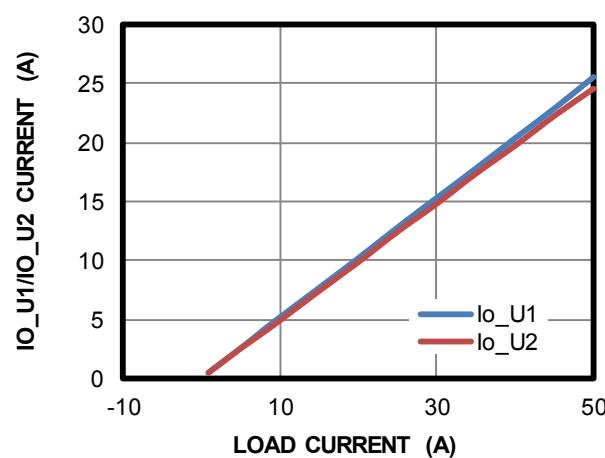
Regulation vs. Input Voltage



Thermal De-rating vs. Ambient Temp@200LFM Air Flow



Current Sharing

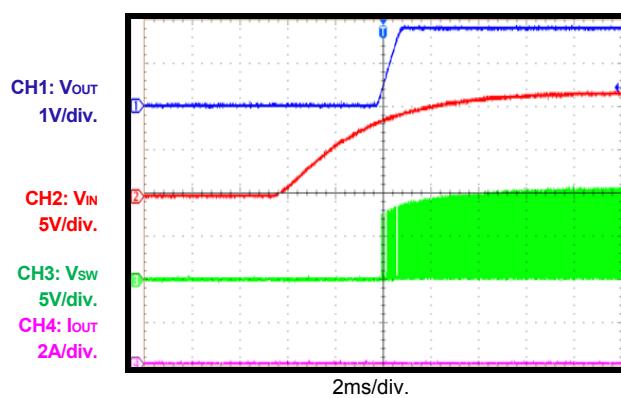


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Single Phase,  $V_{IN}=12V$ ,  $V_{OUT}=1.8V$ ,  $F_{sw}=600kHz$ ,  $T_A=+25^\circ C$ , unless otherwise noted.

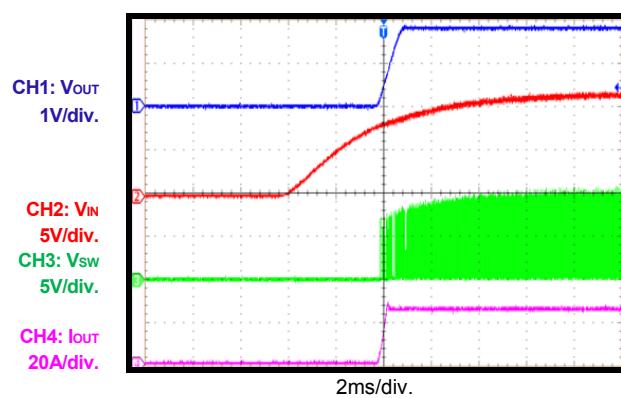
### VIN Start-Up

0A



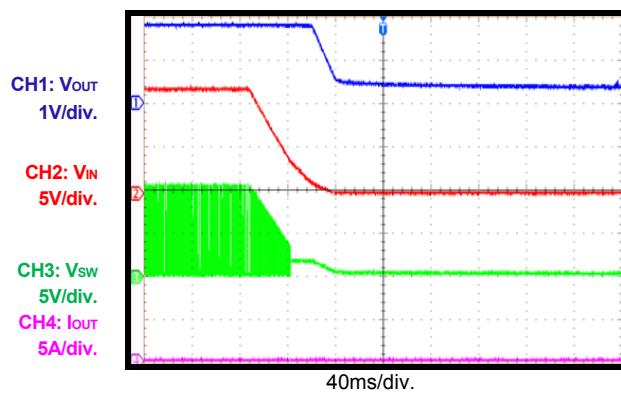
### VIN Start-Up

25A



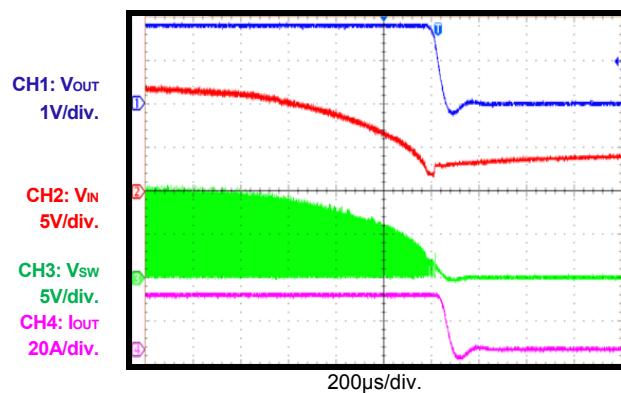
### VIN Shutdown

0A



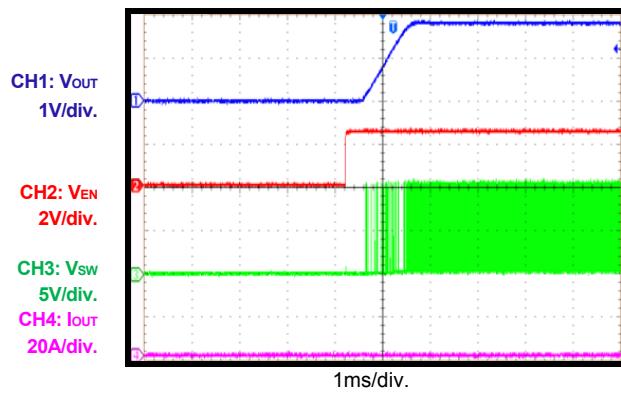
### VIN Shutdown

25A



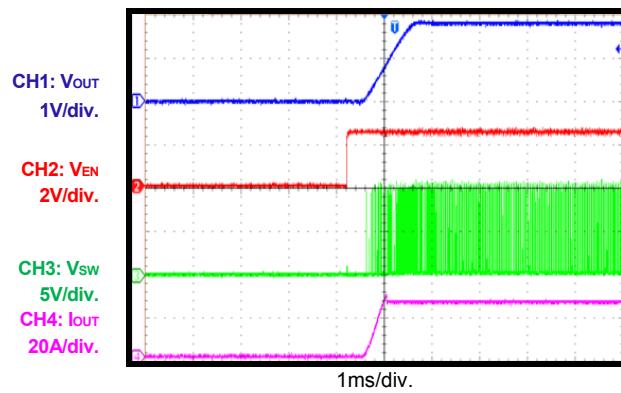
### EN Start-Up

0A



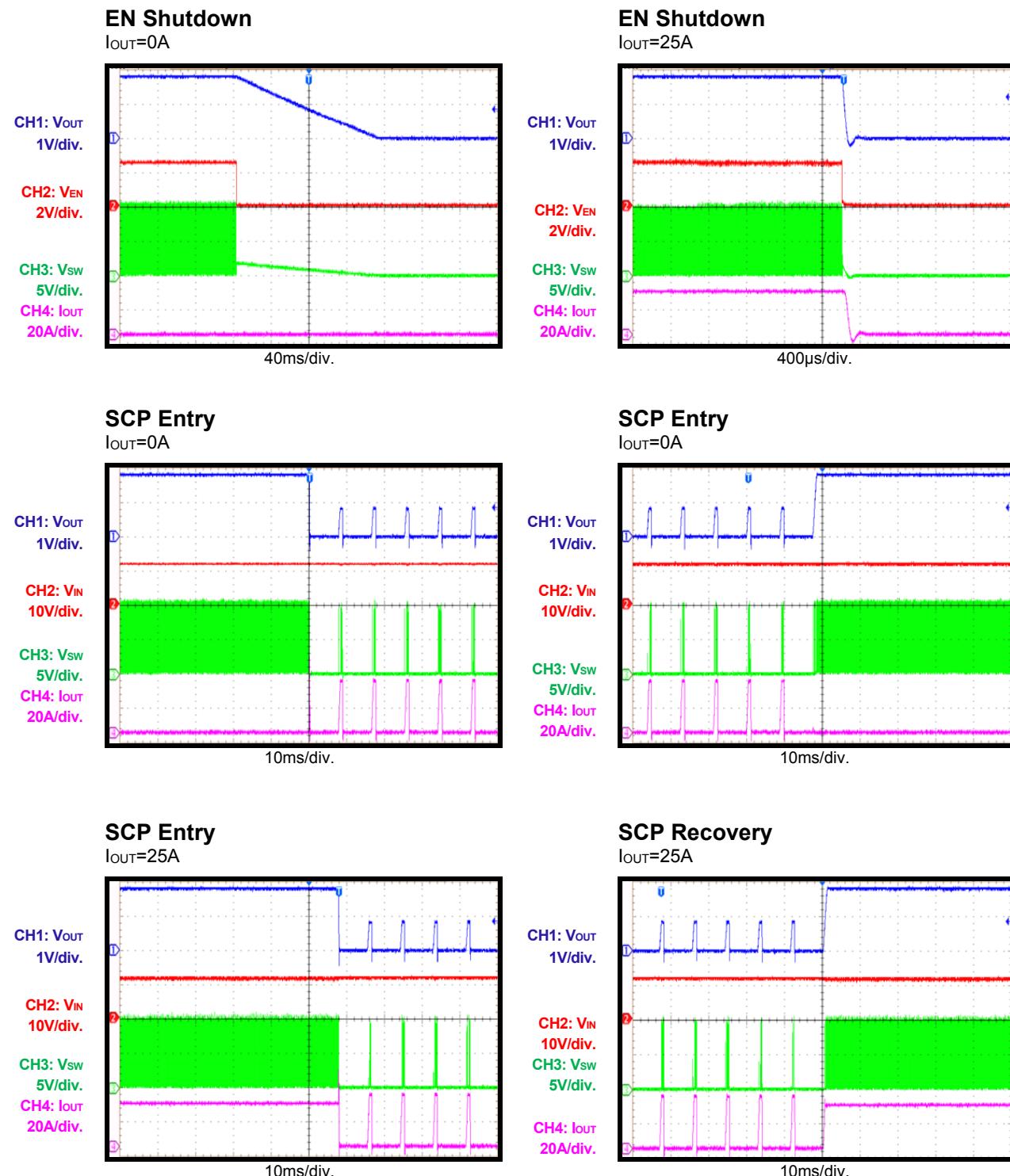
### EN Start-Up

25A



## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

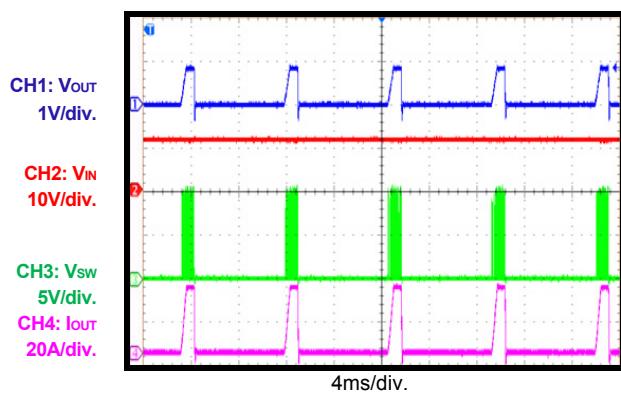
Single Phase,  $V_{IN}=12V$ ,  $V_{OUT}=1.8V$ ,  $F_{sw}=600kHz$ ,  $T_A=+25^\circ C$ , unless otherwise noted.



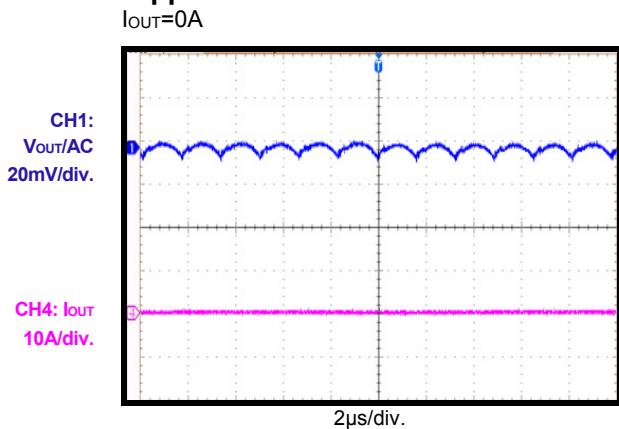
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Single Phase,  $V_{IN}=12V$ ,  $V_{OUT}=1.8V$ ,  $F_{sw}=600kHz$ ,  $T_A=+25^\circ C$ , unless otherwise noted.

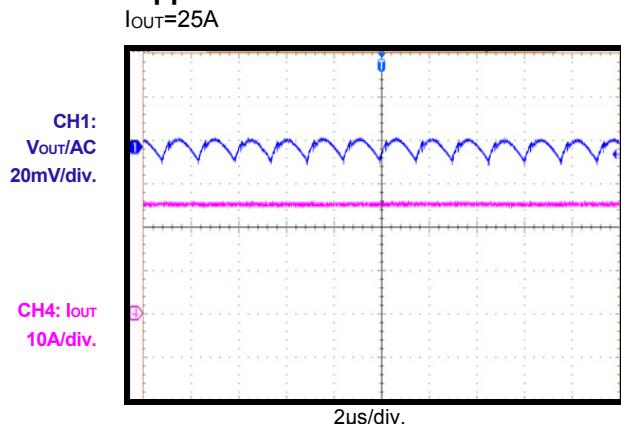
### SCP State Steady



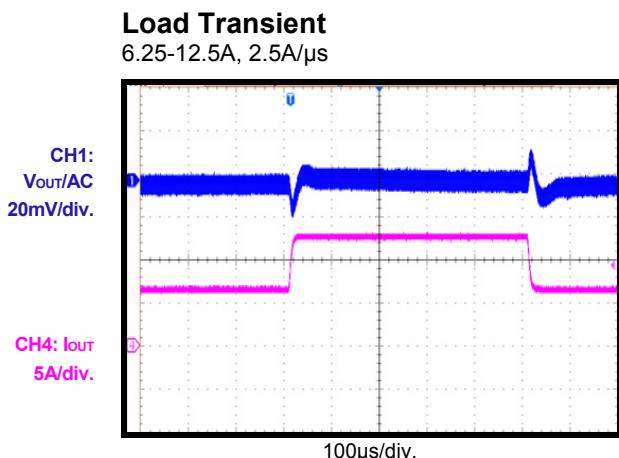
### Ripple



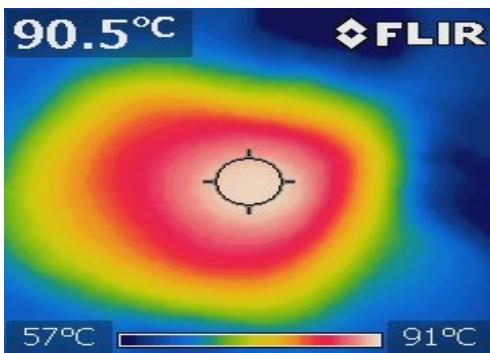
### Ripple



### Load Transient

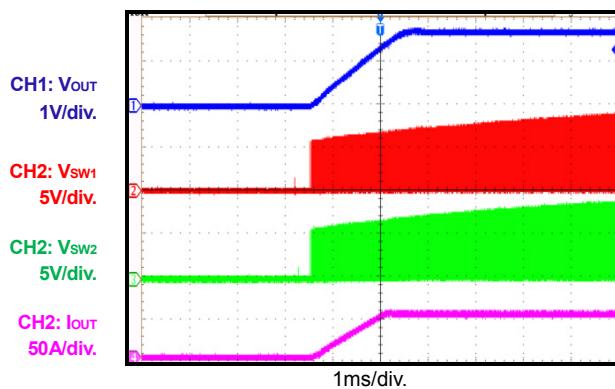
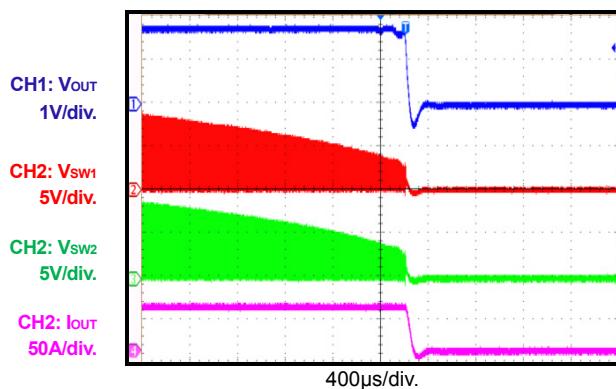
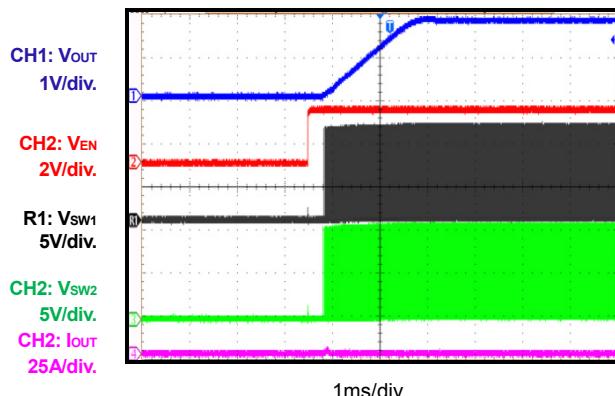
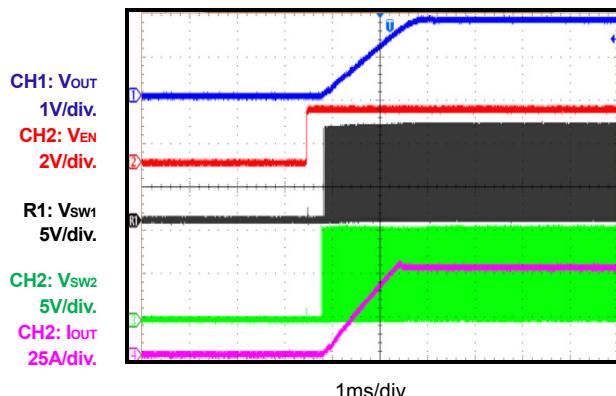
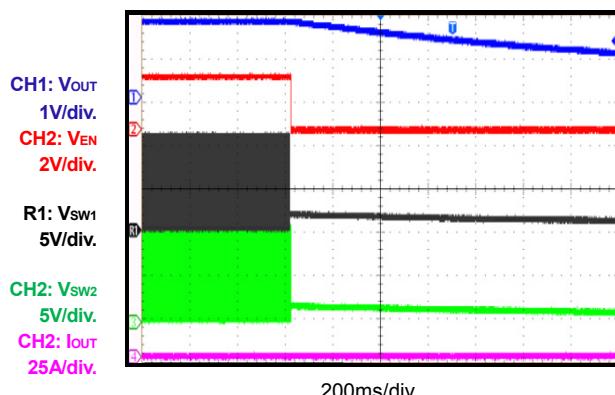
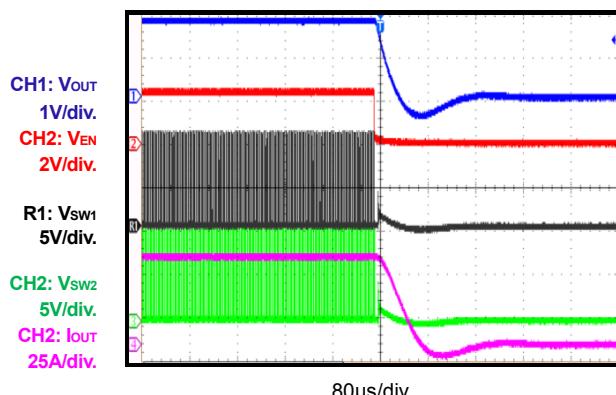


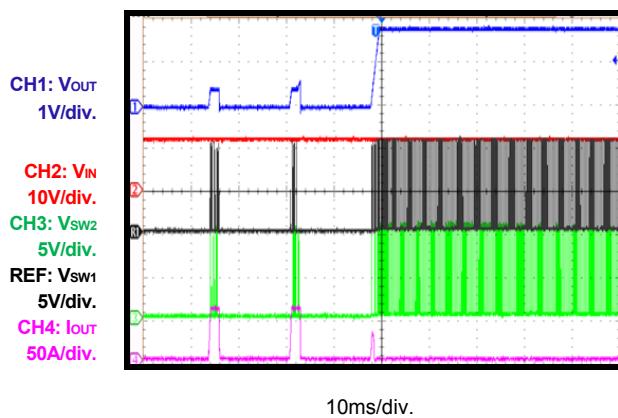
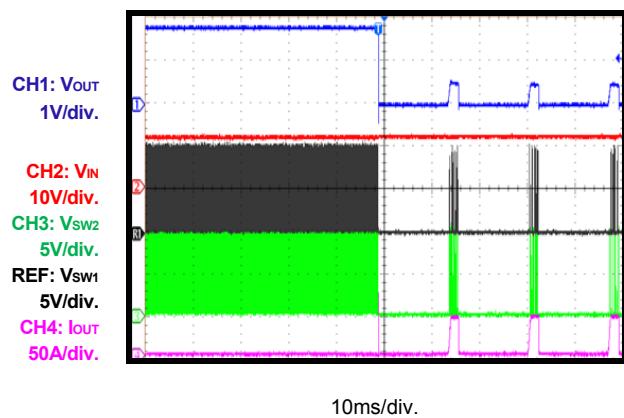
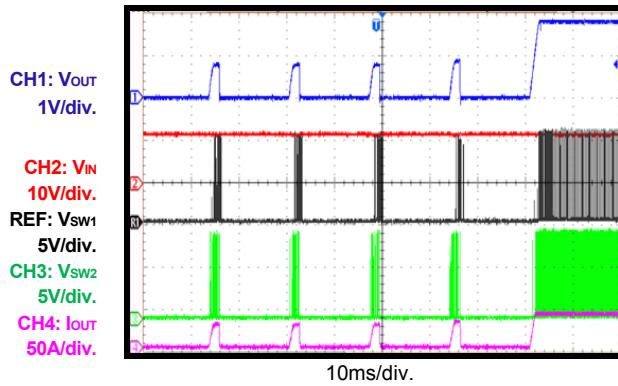
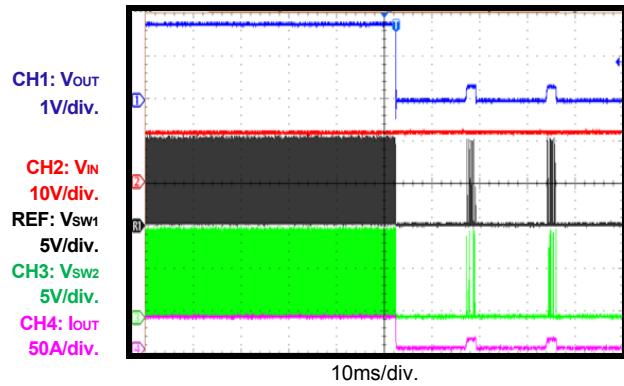
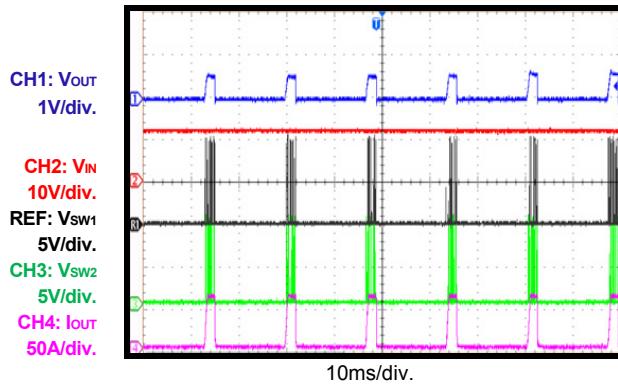
### Thermal 12V to 1.8V/20A



## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

2 Phase,  $V_{IN}=12V$ ,  $V_{OUT}=1.8V$ ,  $F_{sw}=600kHz$ ,  $T_A=+25^\circ C$ , unless otherwise noted.

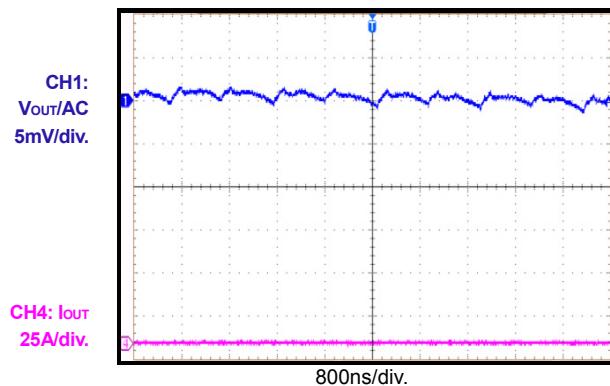
**VIN Start Up,  
Io=50A**

**VIN Shutdown,  
Io=50A**

**EN Start Up,  
Io=0A**

**EN Start Up,  
Io=50A**

**EN Shutdown,  
Io=0A**

**EN Shutdown,  
Io=50A**

**TYPICAL PERFORMANCE CHARACTERISTICS (Continued)**
**2 Phase,  $V_{IN}=12V$ ,  $V_{OUT}=1.8V$ ,  $F_{SW}=600kHz$ ,  $T_A=+25^{\circ}C$ , unless otherwise noted.**

**SCP Recovery**
 $I_{OUT}=0A$ 

**SCP Entry**
 $I_{OUT}=0A$ 

**SCP Recovery**
 $I_{OUT}=50A$ 

**SCP Entry**
 $I_{OUT}=50A$ 

**SCP State Steady**


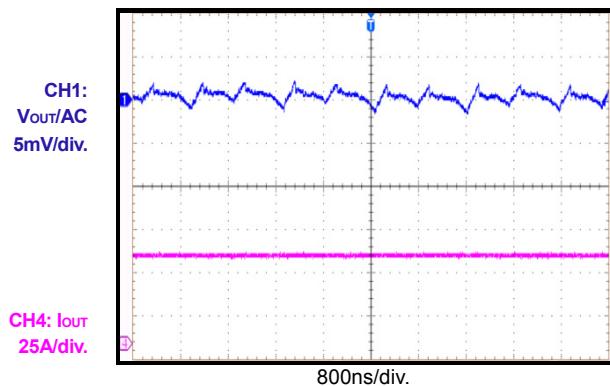
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

2 Phase,  $V_{IN}=12V$ ,  $V_{OUT}=1.8V$ ,  $F_{sw}=600kHz$ ,  $T_A=+25^{\circ}C$ , unless otherwise noted.

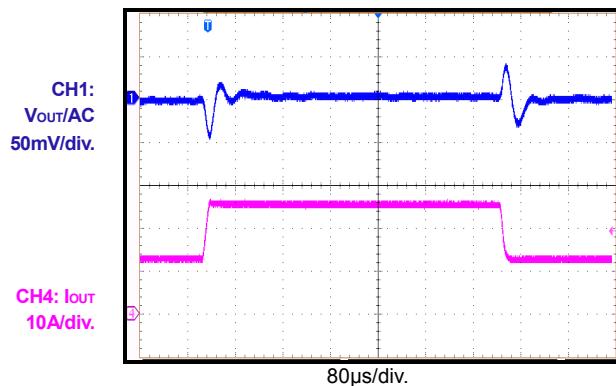
$V_{OUT}$  Ripple@ $V_{IN}=12V$ ,  $I_O=0A$



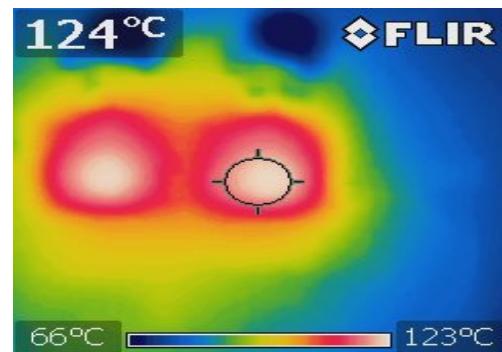
$V_{OUT}$  Ripple@ $V_{IN}=12V$ ,  $I_O=50A$



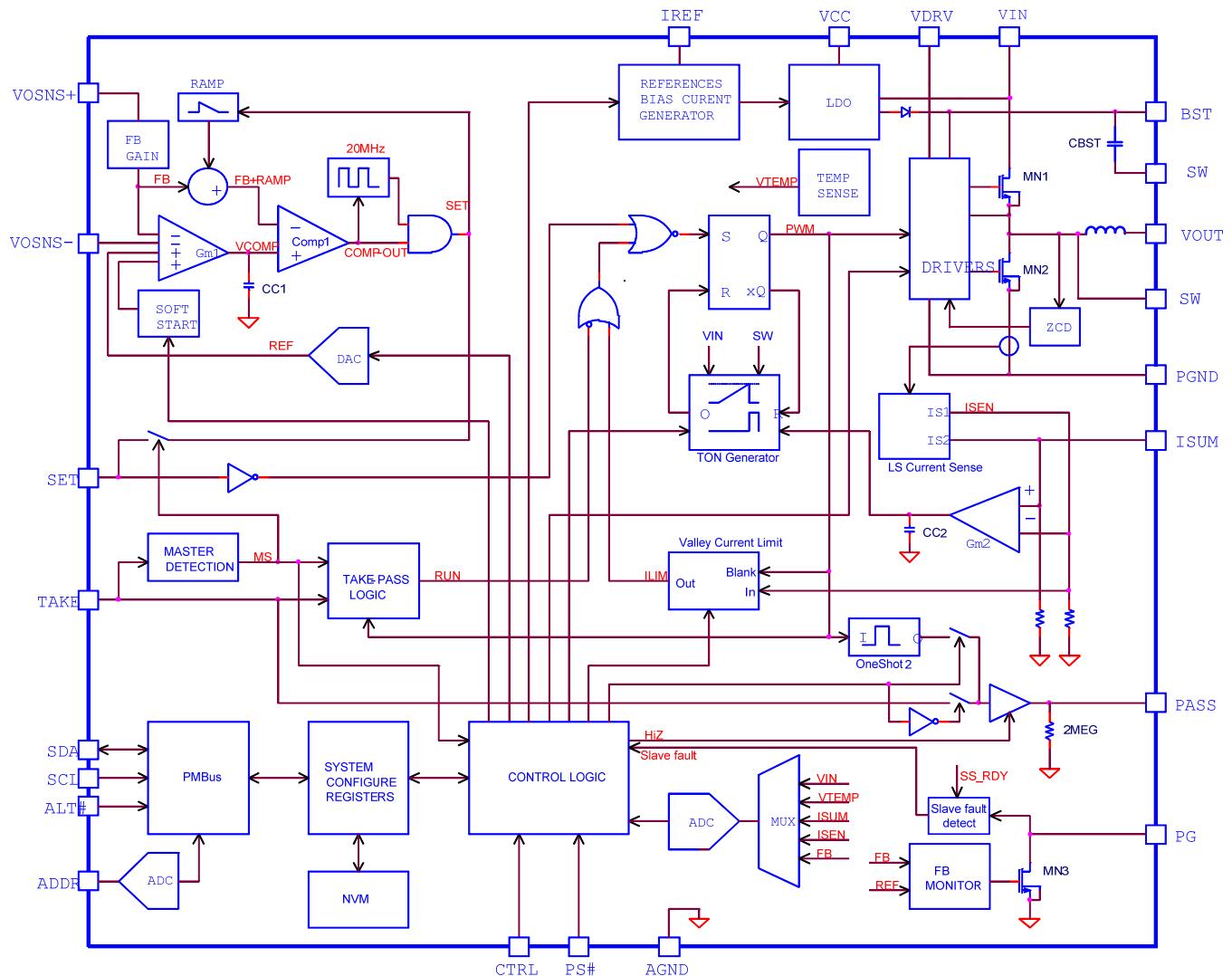
Load Transient @ 25%-50%, 2.5A/us

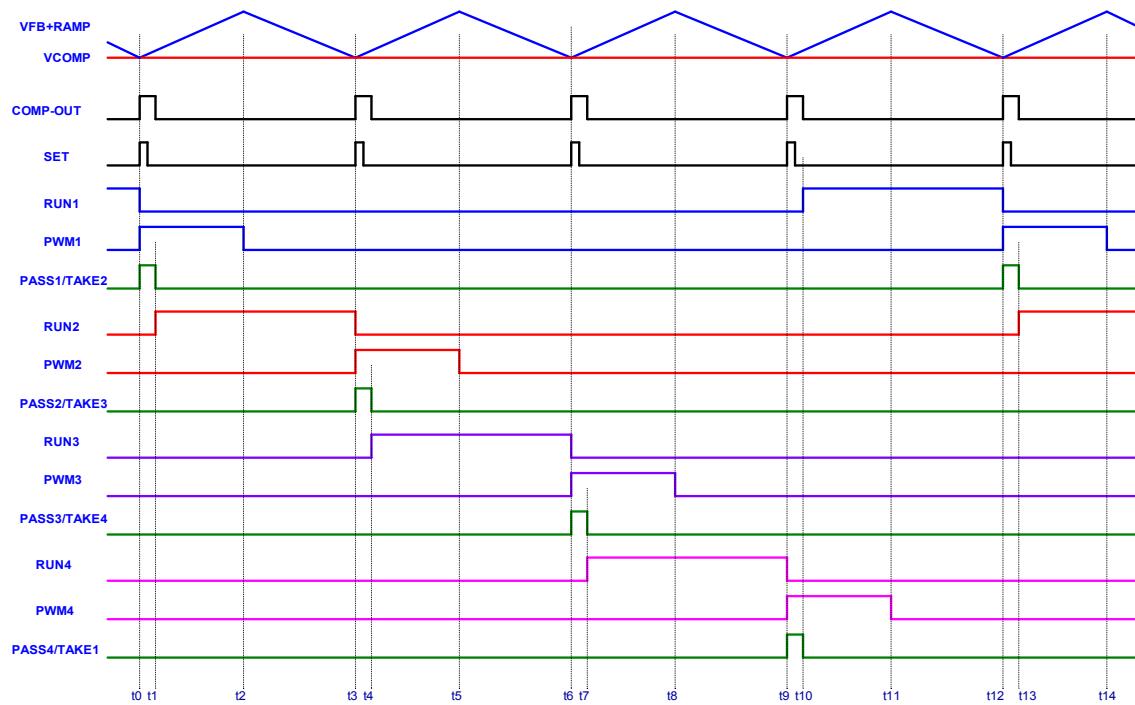


$V_{IN} = 12V$ ,  $V_{OUT} = 1.8V$ ,  $I_O=40A$ ,  $T_A = 25^{\circ}C$

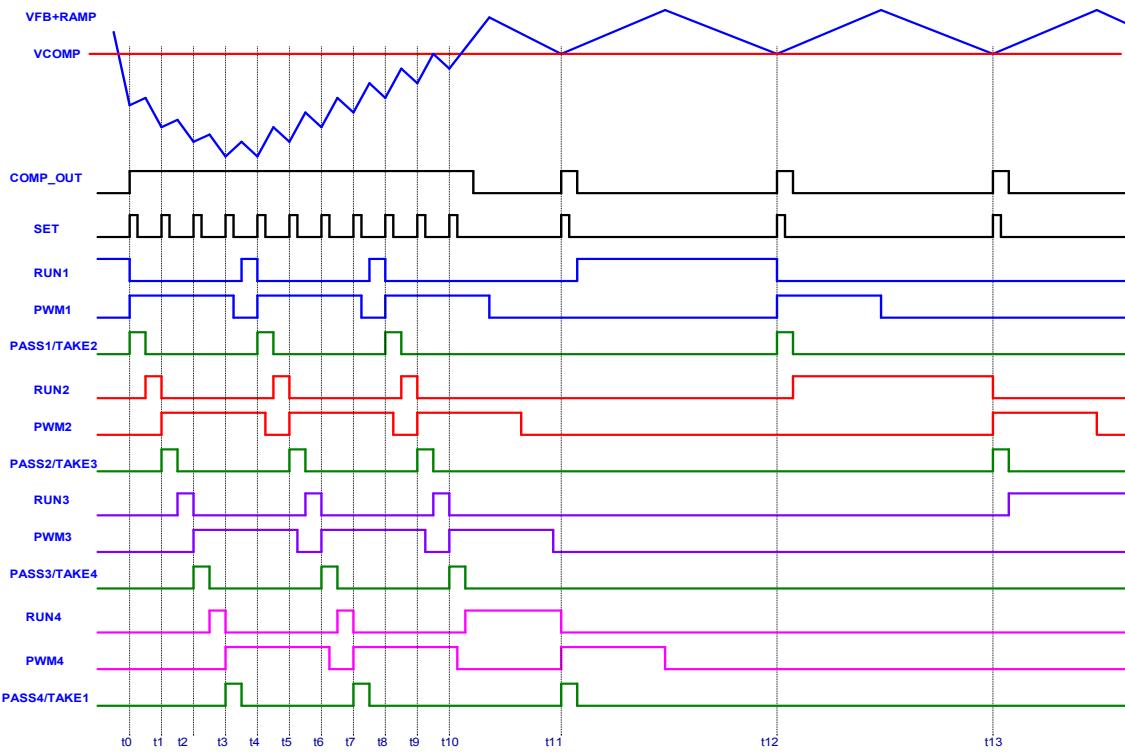


## BLOCK DIAGRAM





**Figure 1: Multi-Phase Operation Timing Diagram (Steady State)**



**Figure 2: Multi-Phase Operation Timing Diagram (Transient)**

## OPERATION

The MPM3695-25 is a fully integrated power solution with up to 25A output current in a 10x12x4mm QFN package. For applications that require more than 25A, the MPM3695-25 can be connected in parallel to provide a higher output current. The MPM3695-25 employs constant-on-time (COT) control to provide fast transient response. The internal ramp compensation guarantees stable operation for applications using zero-ESR ceramic output capacitors.

### Multi-Phase Operation

In a multi-phase configuration, one master phase and up to five slave phases are connected in parallel. The output current is shared equally among all phases. The typical application circuit illustrates four MPM3695-25s in a multi-phase configuration. The TAKE pin of the master phase is required to be pulled up to a voltage source through a resistor. The MPM3695-25 detects its master/slave configuration by monitoring the state of the TAKE pin during start-up. The PASS and TAKE pins of all phases are connected in a cascaded manner (See Typical Application circuit). The PASS pin of the last slave-phase is connected back to the TAKE pin of the master phase.

### MCOT Operation-Master Phase

A master phase performs the following functions:

- Accepts both write and read commands through PMBus from a host
- Generates the SET signal
- Manages the start-up, shut-off, and all the protections
- Monitors fault alerts from the slave phases through the PG pin
- Generates the first ON pulse
- Generates the ON pulse when receiving RUN and SET signals
- Dynamically adjusts its on-time to ensure equal current sharing
- Generates the PASS signal

### MCOT Operation-Slave Phases

The master phase performs the following functions:

- Accepts write commands through PMBus from a host
- Receives the SET signal from a master
- Sends an OV/UV/OT fault alert to a master phase through the PG pin
- Starts the ON pulse when receiving RUN and SET signals
- Dynamically adjusts its on-time to ensure equal current sharing with its own phase based on the per-phase and total current
- Generates the PASS signal

Figure 1 illustrates MCOT operation. At t0, a SET pulse is generated by the master phase when  $(VFB+RAMP)$  drops below the reference level (VCOMP). All the phases receive this SET signal, but only the phase (the MASTER) that has an active RUN signal will take action, so the MASTER turns on the High-Side-FET (HS-FET). Meanwhile, it generates a fixed width-pulse on the PASS pin, and passes it to the TAKE pin of SLAVE1.

At t1, the falling edge of the TAKE pin of SLAVE1 activates the RUN signal. This enables the SLAVE1 to wait for the SET signal to turn on its HS-FET.

At t2, the ON time of the PWM signal of the MASTER phase expires and the HS-FET is turned off. The ON time of the PWM signal is fixed for any given input voltage, output voltage and switching frequency. The ON time of each phase is fine-tuned based on the per phase and the total current to ensure equal current sharing among phases.

At t3, the  $(VFB+RAMP)$  drops below the reference level (VCOMP) in the MASTER phase again, only SLAVE1 has an active RUN signal, so it turns on its HS-FET. All other phases ignore this SET signal. Meanwhile, the SLAVE1 generates a pulse with fixed width on the PASS pin, and passes it to the TAKE pin of SLAVE2.

The MPM3695-25 keeps above operation and each phase turns on its HS-FET one by one for a fixed ON time. The operation is similar to a relay race and the RUN signal is like the baton. The relay is carried on through the PASS/TAKE loop. Only the phase that has the baton (RUN signal) will turn on the HS-FET when the SET signal is ready.

The MPM3695-25 benefits from MCOT control to achieve extremely fast load transient response. The SET signal is generated more frequently during a load transient compared to steady state (See Figure 2). Consequently, energy is delivered to the load at a higher rate, which minimizes the output deviation during a load transient event. With the MPM3695-25, the SET pulses are generated with a minimum 50ns interval, i.e., the next phase can be turned on as fast as 50ns after the turn-on of the previous phase.

### **RAMP Compensation**

The MPM3695-25 guarantees stable operation with zero-ESR ceramic output capacitors by using internal RAMP compensation. A triangular RAMP signal is generated internally and is superimposed on the FB signal. The triangular RAMP signal starts to rise once RAMP+FB drops below the REF signal, and a SET pulse is generated. The rise time of the RAMP signal is fixed. The amplitude of the RAMP compensation is selectable through the PMBus command of D0h[3:1] to support wide operation configurations. There is a trade-off between the stability and load transient response. A larger RAMP signal provides higher stability but a slower load transient response and vice versa. Consequently, it is necessary to optimize the RAMP compensation selection based on the design criteria for each application.

## APPLICATION INFORMATION

### Operation Mode Selection

The MPM3695-25 provides both forced CCM and pulse skip operations in a light-load condition. Four switching frequencies are available for the MPM3695-25. The selection of operation mode in a light-load condition and the switching frequency is done through the PMBus.

### Output Voltage Setting

A feedback resistor divider is required to set the proper feedback gain. The values of the feedback resistors are determined using equation 1:

$$R_2(k\Omega) = \frac{0.6}{V_o - 0.6} \times R_1(k\Omega) \quad (1)$$

where  $V_o$  is the output voltage. The output voltage feedback gain is determined with equation 2:

$$G_{FB} = \frac{R_2}{R_1 + R_2} \quad (2)$$

To optimize the load transient response, a feed-forward capacitor ( $C_{FF}$ ) is required to be placed in parallel with  $R_1$ . Table 1 lists the values of the feedback resistors and the feedforward capacitor for common output voltages.

**Table 1: Common Output Voltages**

| $V_o$ | $R_1(k\Omega)$ | $R_2(k\Omega)$ | $C_{FF}(nF)$ |
|-------|----------------|----------------|--------------|
| 0.9   | 0.5            | 1              | 33           |
| 1.2   | 1              | 1              | 33           |
| 1.8   | 2              | 1              | 33           |
| 3.3   | 4.53           | 1              | 4.7          |
| 5     | 7.32           | 1              | 4.7          |

The MPM3695-25 offers output voltage programmability through PMBus. In addition, the output voltage can be adjusted within a certain range through PMBus by adjusting the internal reference voltage of the PMW controller ( $V_{REF}$ ). The reference voltage, which has a default value of 0.6V, can be adjusted between 0.5V to 0.672V. For a given feedback resistor network, the upper and lower limits of the output voltage are determined with equation 3a and equation 3b:

$$V_{o,max} = \frac{0.672}{G_{FB}} \quad (3a)$$

$$V_{o,min} = \frac{0.5}{G_{FB}} \quad (3b)$$

Two steps need to be followed to program the output voltage through PMBus:

1. Write  $G_{FB}$  value determined by Equation 2 to register VOUT\_SCALE\_LOOP (29h)
2. Write the output voltage command to register VOUT\_COMMAND (21h)

$V_{REF}$  is updated automatically based on the output voltage command and  $G_{FB}$

Output voltage monitoring through PMBus is enabled by setting the register VOUT\_SCALE\_LOOP (29h) with a value that matches the  $G_{FB}$  calculated with Equation 2.

For applications where a PMBus interface is not required,  $V_{REF}=0.6V$  is used by default, and the MPM3695-25 operates in analog mode. The feedback resistors should be determined based on Equation 1.

### Soft Start

The soft start (SS) time can be programmed through PMBus. The default SS time is 2ms.

### Pre-Bias Start-Up

The MPM3695-25 is designed for monotonic startup into pre-biased loads. If the output voltage is pre-biased to a certain voltage during startup, both the high-side and low-side switches are disabled until the internal reference voltage exceeds the sensed output voltage at the FB pin.

### Output Voltage Discharge

The output voltage discharge mode will be enabled if the MPM3695-25 is disabled through the CTRL pin. In such a case, both the high-side and low-side switches are latched off. A discharge FET connected between SW and GND is turned on to discharge the output capacitor. A typical on-resistance of the discharge FET is 60Ω. Once the FB voltage drops below 10% of the reference output voltage, the discharge FET is turned off.

This feature can be enabled or disabled through the MFR\_CTRL\_VOUT (D1h) command.

## Current Sense and Over-Current Protection (OCP)

The MPM3695-25 features on-die current sense and a programmable positive current limit threshold.

The MPM3695-25 provides both inductor valley current limits (set by register D7h).

## Inductor Valley Over-Current Protection (D7h)

During the LS-FET ON state, the inductor current is sensed and monitored cycle-by-cycle. The HS-FET will only be allowed to turn ON if over-current is not detected during the LS-FET ON-state. If there are 31 consecutive cycles of an OC condition detected, OCP is triggered.

During an over-current condition or output short-circuit condition, if the output voltage drops below the under-voltage protection (UVP) threshold, the MPM3695-25 enters OCP immediately.

Once OCP is triggered, it either enters HICCUP mode or latch-off mode, depending on the register. It should be noted that a power-recycle of the Vcc or CTRL is required to re-enable the MPM3695-25 once it latches-off.

The inductor valley over-current limit can be programmed through register D7h, which sets the per-phase inductor valley current limit for both single and multi-phase operation.

## Negative Inductor Current limit

When the LS-FET detects a negative current lower than the limit set through register D5h[2], the part will turn off its LS-FET for a period of time to limit the negative current. The period is set through register D5h[3].

## Under -Voltage Protection (UVP)

The MPM3695-25 monitors the output voltage through the FB pin to detect an under-voltage condition. If the FB voltage drops below the UVP threshold (set through register VOUT\_UV\_FAULT\_LIMIT), the UVP is triggered. After UVP is triggered, the MPM3695-25 enters either HICCUP or latch-off mode, depending on the PMBus selection. Please note that a power-recycle of the Vcc or CTRL is required to re-enable the MPM3695-25 once it latches off.

## Over-Voltage Protection (OVP)

The MPM3695-25 monitors the output voltage using the FB pin connected to the tap of a resistor divider to detect an over-voltage condition. Please refer to the register VOUT\_OV\_FAULT\_RESPONSE section for additional information on OVP.

## Output Sinking Mode (OSM)

The MPM3695-25 enters the OSM when the output voltage is more than 5% higher than the reference and below the OVP threshold. Once the OSM is triggered, the MPM3695-25 runs in forced CCM. The MPM3695-25 exits OSM mode when the HS-FET turns back on.

## Over-Temperature Protection (OTP)

The MPM3695-25 monitors the junction temperature. If the junction temperature exceeds the threshold value (set by register OT\_FAULT\_LIMIT), the converter enters either HICCUP or latch-off mode depending on the PMBus selection. Please note that a power-recycle of the Vcc or CTRL is required to re-enable the MPM3695-25 once it latches off.

## Power Good (PG)

The MPM3695-25 has an open-drain power-good (PG) output. The PG pin can be configured as an output only or input and output pin by bit [0] of register MRF\_CTRL\_COMP (D0h). For single-phase configuration, the PG pin should be configured as output only. For multi-phase operation, the PG pin should be configured as an input and output pin to detect faults from the slave phases. The PG pin must be pulled high, to V<sub>CC</sub> or a voltage source, with less than 3.6V through a pull-up resistor (typically 100kΩ).

PG is pulled low initially once input voltage is applied to the MPM3695-25. After the FB voltage reaches the threshold set by register POWER\_GOOD\_ON, the PG pin is pulled high after a delay set by the register MFR\_CTRL\_VOUT.

PG is latched low if any fault occurs, and the relevant protection feature is triggered (e.g., UV, OV, OT, UVLO, etc.). After the PG is latched low, it cannot be pulled high again unless a new soft-start is initialized.

If the input supply fails to power the MPM3695-25, the PG is latched low. The relationship between the PG voltage and the pull-up current is shown in Figure 3.

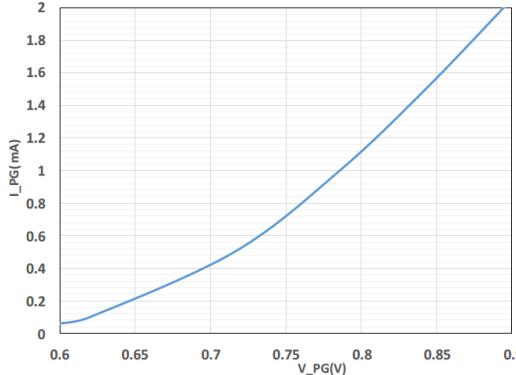


Figure 3: Power-Good Current vs. Power-Good Voltage

### Input Capacitor

The input current to a buck converter is discontinuous, and therefore, requires a capacitor to supply the AC current to the step-down module while maintaining the DC input voltage. Use ceramic capacitors for the best performance. During layout, place the input capacitors as close to the IN pin as possible.

The capacitance can vary significantly with temperature. Use capacitors with X5R and X7R ceramic dielectrics, because they are fairly stable over a wide temperature range.

The capacitors must also have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current using equation 4:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN}})}{V_{IN}}} \quad (4)$$

The worst-case condition occurs at  $V_{IN} = 2V_{OUT}$ , where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current.

The input capacitance value determines the converter input voltage ripple. Select a capacitor value that meets any input voltage ripple requirements.

Estimate the input voltage ripple using equation 6:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

The worst-case condition occurs at  $V_{IN} = 2V_{OUT}$ , where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (7)$$

### Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic capacitors or POSCAPs. Estimate the output voltage ripple using equation 8:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (8)$$

Where the module internal inductor is 0.36 $\mu$ H.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The capacitance also dominates the output voltage ripple. For simplification, estimate the output voltage ripple using equation 9:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

The ESR dominates the switching-frequency impedance for POSCAPs, so the output voltage ripple is determined by the ESR value.

For simplification, the output ripple can be approximated using equation 10:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (10)$$

### PCB Layout Guidelines

PCB layout plays an important role to achieve stable operation. For optimal performance, follow the guidelines below:

1. Place the input ceramic capacitors as close to the VIN and PGND pins as possible on the same layer of the MPM3695-25. Maximize the VIN and PGND copper plane to minimize the parasitic impedance.
2. Place VIN vias at least 1cm from the part to minimize noise coupling from input pulsating current.
3. Connect AGND to a solid ground plane through a single point.
4. Place sufficient output GND vias close to the GND pins to minimize both parasitic impedance and thermal resistance.
5. Keep the ISUM trace as short as possible. The ISUM trace should be away from the VIN copper in a multi-phase configuration. Vias should be avoided whenever possible.
6. The keep-out area must be kept clean.

Signal traces should avoid the area directly beneath the SW pad unless a PGND layer is used to provide shielding.

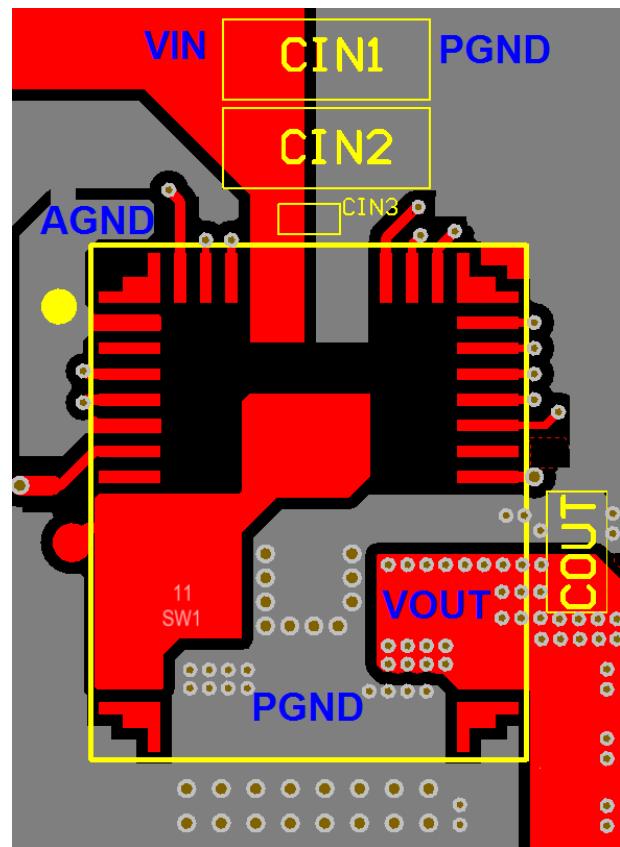


Figure 4. Example Layout - Top Layer

## TYPICAL APPLICATIONS

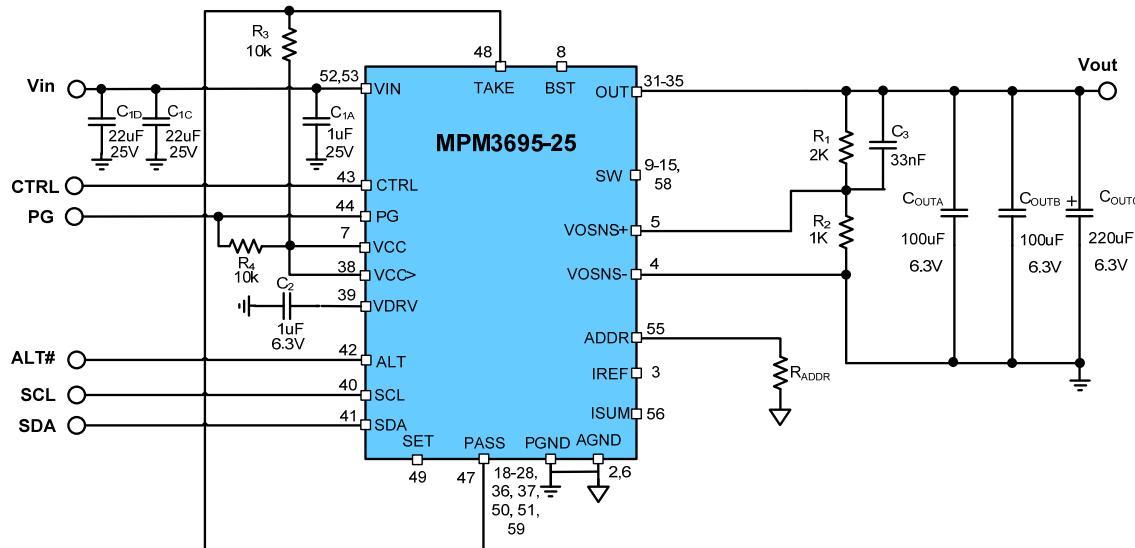


Figure 5: Typical Circuit  $V_{IN}=12V$ ,  $V_{OUT}=1.8V$  at 20A Output

| $V_o$      | $R_1(k\Omega)$ | $R_2(k\Omega)$ | $C_{FF}(nF)$ |
|------------|----------------|----------------|--------------|
| 0.9        | 0.5            | 1              | 33           |
| 1.2        | 1              | 1              | 33           |
| <b>1.8</b> | <b>2</b>       | <b>1</b>       | <b>33</b>    |
| 3.3        | 4.53           | 1              | 4.7          |
| 5          | 7.32           | 1              | 4.7          |

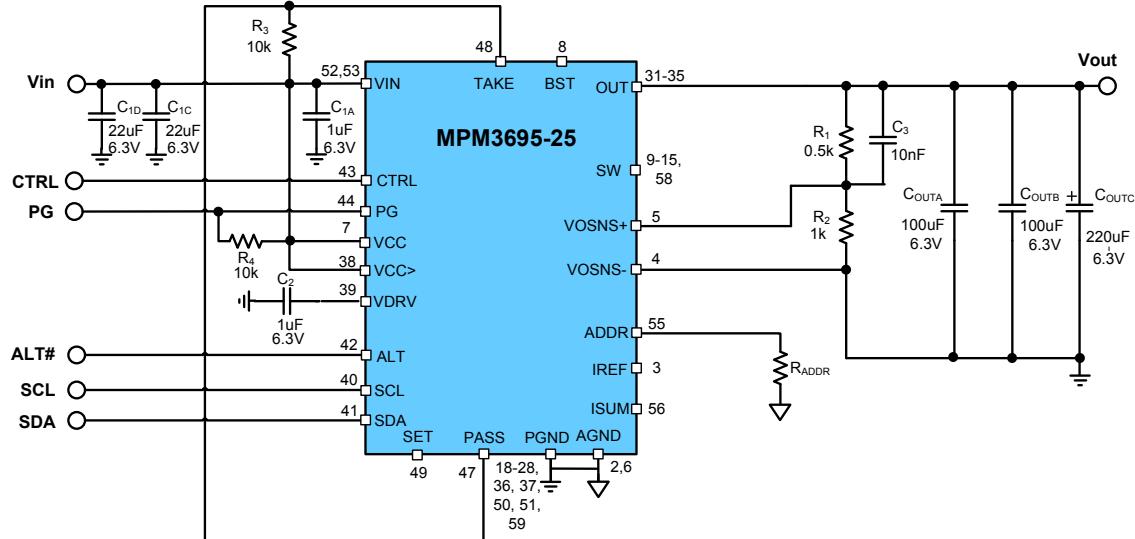


Figure 6: Typical Circuit  $V_{CC} = V_{IN} = 3.3V$ ,  $V_{OUT} = 0.9V$  at 20A Output

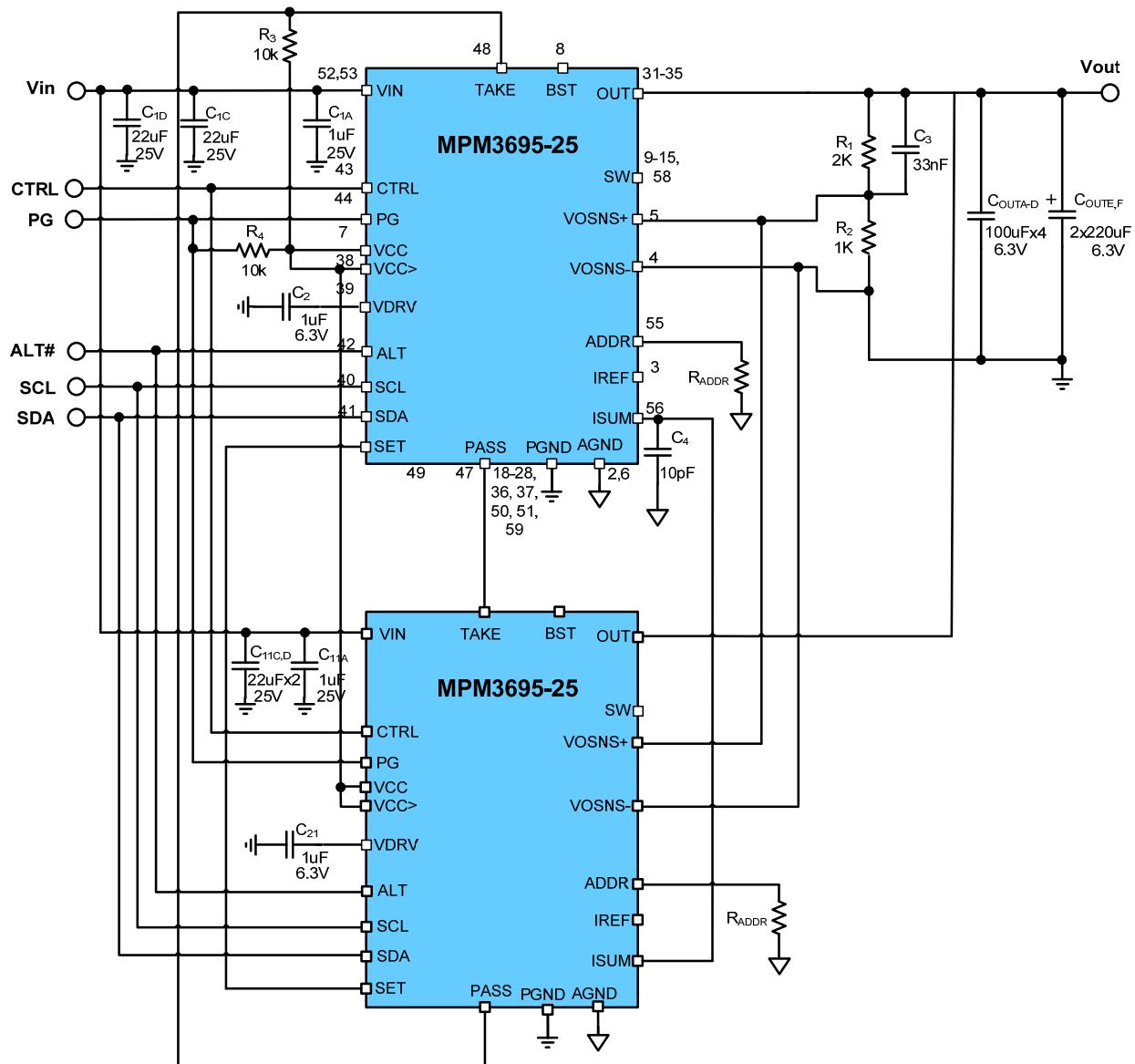


Figure 7: Multi Phase Typical Circuit  $V_{IN} = 12V$ ,  $V_{OUT} = 1.8V$  at 40A Output

**NOTE:**

8) When  $V_{IN} < 9V$ , additional input E-cap is required. Recommended value is  $220\mu F$ .

## PMBUS INTERFACE

### PMBus Serial Interface Description

The power management bus (PMBus) is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are “idle”. Connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. It is based on the principles of I<sup>2</sup>C operation. The MPM3695-25 interface is a PMBus slave, which will support both the standard mode (100kHz) and fast mode (400kHz and 1000KHz). The PMBus interface adds flexibility to the power supply solution.

### Device Address

To manage multiple MPM3695-25s through the same PMBus, use the ADDR pin to program the device address for the MPM3695-25s; there is a 10 $\mu$ A current flow out of the ADDR pin. Connect a resistor between the ADDR pin and AGND to set the ADDR voltage. The internal ADC converts the pin voltage to set the PMBus address. A maximum of 16 addresses can be set by the ADDR pin. The MFR\_ADDR\_PMBUS (F1h) register can be used to set the PMBus address digitally.

After the address is selected, each device must have a unique address during normal operation.

Table 2 shows ADDR resistor values versus the PMBus address.

Table 2: PMBus Address vs. ADDR Resistor

| R <sub>ADDR</sub> (k $\Omega$ ) | Device Address |
|---------------------------------|----------------|
| 4.99                            | 30h            |
| 15                              | 31h            |
| 24.9                            | 32h            |
| 34.8                            | 33h            |
| 45.3                            | 34h            |
| 54.9                            | 35h            |
| 64.9                            | 36h            |
| 75                              | 37h            |
| 84.5                            | 38h            |
| 95.3                            | 39h            |
| 105                             | 3Ah            |
| 115                             | 3Bh            |
| 124                             | 3Ch            |
| 133                             | 3Dh            |
| 147                             | 3Eh            |
| 154                             | 3Fh            |

### Start and Stop Conditions

The START/STOP are signaled by the master device, which signifies the beginning and the end of the PMBus data transfer. The START condition is defined as the SDA signal transitioning from HIGH to LOW while the SCL is HIGH. The STOP condition is defined as the SDA signal transitioning from LOW to HIGH while the SCL is HIGH (See Figure 8).

The master then generates the SCL clocks, and transmits the device address and the read/write direction bit R/W on the SDA line. Data is transferred in 8 bit bytes by the SDA line. Each byte of data is followed by an acknowledge bit.

### PMBus Update Sequence

The MPM3695-25 requires a start condition, a valid PMBus address, a register address byte, and a data byte for a single data packet update. After receipt of each byte, the MPM3695-25 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid PMBus address selects the MPM3695-25. The MPM3695-25 performs an update on the falling edge of the LSB byte.

### Protocol Usage

All PMBus transactions on the MPM3695-25 are done using defined bus protocols. The following protocols are implemented:

- Send byte with PEC
- Receive byte with PEC
- Write byte with PEC
- Read byte with PEC
- Write word with PEC
- Read word with PEC
- Block read with PEC

### PMBus Bus Message Format

In figures a-g below, unshaded cells indicate that the bus host is actively driving the bus; shaded cells indicate that the MPM3695-25 is driving the bus.

S = start condition

Sr = repeated start condition

P = stop condition

R = read bit

W = write bit

A = acknowledge bit (0)

$\bar{A}$  = acknowledge bit (1)

"A" represents the ACK (acknowledge) bit. The ACK bit is typically active low (Logic 0) if the transmitted byte is successfully received by a device. However, when the receiving device is the bus master, the acknowledge bit for the last byte read is a Logic 1, indicated by  $\bar{A}$ .

### Packet Error Checking (PEC)

The MPM3695-25 PMBus interface supports the use of the packet error checking (PEC) byte. The PEC byte is transmitted by the MPM3695-25 during a read transaction or sent by the bus host to the MPM3695-25 during a write transaction.

The PEC byte is used by the bus host or the MPM3695-25 to detect errors during a bus transaction, depending on whether the transaction is a read or a write. If the host determines that the PEC byte read during a read transaction is incorrect, it can decide to repeat the read. If the MPM3695-25 determines that the PEC byte sent during a write transaction is incorrect, it ignores the command (does not execute it), and it sets a status flag. Within a group command, the host can choose to send or not send a PEC byte as part of the message to the MPM3695-25.

### PMBus Alert Response Address (ARA)

The PMBus alert response address (ARA) is a special address that can be used by the bus host to locate any devices that need to talk to it. A host typically uses a hardware interrupt pin to monitor the PMBus ALERT pins of a number of devices. When the host interrupt occurs, the host issues a message on the bus using the PMBus receive byte or receive byte with PEC protocol.

The special address used by the host is 0x0C. Any devices that have a PMBus alert signal return their own 7-bit address as the seven MSBs of the data byte. The LSB value is not used and can be either 1 or 0. The host reads the device address from the received data byte and proceeds to handle the alert condition.

More than one device may have an active PMBus alert signal and attempt to communicate with the host. In this case, the device with the lowest address dominates the bus and succeeds in transmitting its address to the host. The device that succeeds disables its PMBus alert signal. If the host sees that the PMBus alert signal is still low, it continues to read addresses until all devices that need to talk to it have successfully transmitted their addresses.

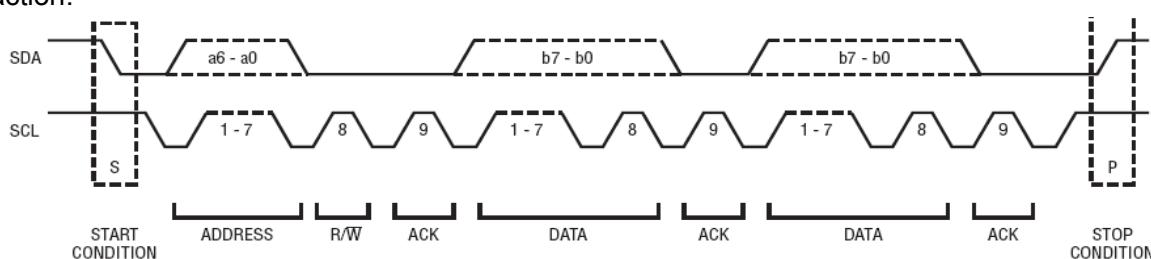


Figure 8: Data Transfer over PMBus

**a) Send Byte and Send Byte with PEC**

|   |               |    |   |           |   |     |
|---|---------------|----|---|-----------|---|-----|
| 1 | 7             | 1  | 1 | 8         | 1 | 1   |
| S | Slave Address | Wr | A | Data Byte | A | P   |
| 1 | 7             | 1  | 1 | 8         | 1 | 8   |
| S | Slave Address | Wr | A | Data Byte | A | PEC |

**b) Receive Byte and Receive Byte with PEC**

|   |               |    |   |           |   |     |
|---|---------------|----|---|-----------|---|-----|
| 1 | 7             | 1  | 1 | 8         | 1 | 1   |
| S | Slave Address | Rd | A | Data Byte | A | P   |
| 1 | 7             | 1  | 1 | 8         | 1 | 8   |
| S | Slave Address | Rd | A | Data Byte | A | PEC |

**c) Write Byte and Write Byte with PEC**

|   |               |    |   |              |   |           |   |     |
|---|---------------|----|---|--------------|---|-----------|---|-----|
| 1 | 7             | 1  | 1 | 8            | 1 | 8         | 1 | 1   |
| S | Slave Address | Wr | A | Command Code | A | Data Byte | A | P   |
| 1 | 7             | 1  | 1 | 8            | 1 | 8         | 1 | 8   |
| S | Slave Address | Wr | A | Command Code | A | Data Byte | A | PEC |

**d) Write Word and Write Word with PEC**

|   |               |    |   |              |   |               |   |                |   |     |
|---|---------------|----|---|--------------|---|---------------|---|----------------|---|-----|
| 1 | 7             | 1  | 1 | 8            | 1 | 8             | 1 | 8              | 1 | 1   |
| S | Slave Address | Wr | A | Command Code | A | Data Byte Low | A | Data Byte High | A | P   |
| 1 | 7             | 1  | 1 | 8            | 1 | 8             | 1 | 8              | 1 | 8   |
| S | Slave Address | Wr | A | Command Code | A | Data Byte Low | A | Data Byte High | A | PEC |

**e) Read Byte and Read Byte with PEC**

|   |               |    |   |              |   |   |               |    |   |           |   |     |
|---|---------------|----|---|--------------|---|---|---------------|----|---|-----------|---|-----|
| 1 | 7             | 1  | 1 | 8            | 1 | 1 | 7             | 1  | 1 | 8         | 1 | 1   |
| S | Slave Address | Wr | A | Command Code | A | S | Slave Address | Rd | A | Data Byte | A | P   |
| 1 | 7             | 1  | 1 | 8            | 1 | 1 | 7             | 1  | 1 | 8         | 1 | 8   |
| S | Slave Address | Wr | A | Command Code | A | S | Slave Address | Rd | A | Data Byte | A | PEC |

**f) Read Word and Read Word with PEC**

|   |               |    |   |              |   |   |                |    |   |               |   |
|---|---------------|----|---|--------------|---|---|----------------|----|---|---------------|---|
| 1 | 7             | 1  | 1 | 8            | 1 | 1 | 7              | 1  | 1 | 8             | 1 |
| S | Slave Address | Wr | A | Command Code | A | S | Slave Address  | Rd | A | Data Byte Low | A |
|   |               |    |   |              |   |   | 8              | 1  | 1 |               |   |
|   |               |    |   |              |   |   | Data Byte High | A  | P |               |   |
| 1 | 7             | 1  | 1 | 8            | 1 | 1 | 7              | 1  | 1 | 8             | 1 |
| S | Slave Address | Wr | A | Command Code | A | S | Slave Address  | Rd | A | Data Byte Low | A |
|   |               |    |   |              |   |   | 8              | 1  | 1 |               |   |
|   |               |    |   |              |   |   | Data Byte High | A  | P |               |   |

**g) Block Read with PEC**

|   |               |    |   |              |   |    |               |    |             |                |     |             |
|---|---------------|----|---|--------------|---|----|---------------|----|-------------|----------------|-----|-------------|
| 1 | 7             | 1  | 1 | 8            | 1 | 1  | 7             | 1  | 1           | 8              | 1   | ...         |
| S | Slave Address | Wr | A | Command Code | A | Sr | Slave Address | Rd | A           | Byte Count = N | A   | ...         |
|   |               |    |   |              |   |    | 8             | 1  | 1           |                |     |             |
|   |               |    |   |              |   |    | Data Byte 1   | A  | Data Byte 2 | A              | ... | Data Byte N |
|   |               |    |   |              |   |    |               |    |             |                |     | A           |
|   |               |    |   |              |   |    |               |    |             |                |     | P           |
| 1 | 7             | 1  | 1 | 8            | 1 | 1  | 7             | 1  | 1           | 8              | 1   | ...         |
| S | Slave Address | Wr | A | Command Code | A | Sr | Slave Address | Rd | A           | Byte Count = N | A   | ...         |
|   |               |    |   |              |   |    | 8             | 1  | 1           |                |     |             |
|   |               |    |   |              |   |    | Data Byte 1   | A  | Data Byte 2 | A              | ... | Data Byte N |
|   |               |    |   |              |   |    |               |    |             |                |     | A           |
|   |               |    |   |              |   |    |               |    |             |                |     | P           |

### Direct Format Conversion

The MPM3695-25 uses the direct format internally to represent real-world values such as voltage, current, power, and temperature. A direct format number takes the form of a 2-byte, twos complement, binary integer value.

The decimal equivalent of all warning and telemetry words are within the range of 0 to 1023.

Equation 11 converts from real-world values to a direct format, and Equation 12 converts direct format values to real-world values:

$$Y = (mX + b) \times 10^R \quad (11)$$

$$X = \frac{1}{m} (Y \times 10^{-R} - b) \quad (12)$$

where: Y is the value in a direct format.

X is the calculated real-world value (A, V, W, °C etc.).

m is the slope coefficient, a 2-byte, twos complement integer.

b is the offset, a 2-byte, twos complement integer.

R is a scaling exponent, a 1-byte, twos complement integer.

The same equations are used for voltage, current, power, and temperature conversions; the only difference being the values of the m, b, and R coefficients that are used. Table 2 lists all the coefficients required for the MPM3695-25.

**Table 2: Direct Format Conversion to Real-Word Coefficients**

| Commands  | m  | b  | R  | Units |
|---|----|----|----|-------|
| READ_IOUT<br>IOUT_OC_WARN_LIMIT<br>MFR_SPECIFIC_HYSTL<br>MFR_SPECIFIC_HYSTH | 16 | 0  | 0  | A     |
| READ_VIN<br>READ_VOUT<br>VIN_OV_FAULT_LIMIT<br>VIN_UV_FAULT_LIMIT           | 32 | 0  | 0  | V     |
| READ_PIN  | 1  | 0  | 0  | W     |
| OT_FAULT_LIMIT<br>OT_WARN_LIMIT<br>READ_TEMPERATURE                         | 2  | 0  | 0  | °C    |
| MFR_SPECIFIC_STARTUP_CURRENT_LIMIT  | 4  | 50 | -1 | A     |

### MTP Programming

The MPM3695-25 has built-in MTP (Multiple Time Program) cells to store the user configurations. The standard command of 15h (STORE\_USER\_ALL) is currently not supported by the MPM3695-25. Alternatively, the MTP cells must be programmed through the following commands sequence:

E7h(2000h) → E7h(1000h) → E7h(4000h)

The MPS GUI for the MPM3695-25 supports the STORE\_USER\_ALL command by integrating the above E7h command sequence and naming it 15h (STORE\_USER\_ALL).

When MTP is being programmed, the VCC voltage may go up as high as 5V. Be cautious if VCC is connected to circuits that can be damaged by such high voltage. The MTP programming usually takes about 300ms.

## REGISTER MAP

| Name                | Code | Type            | Bytes | Default Value (-0022 Part) | MTP |
|---------------------|------|-----------------|-------|----------------------------|-----|
| OPERATION           | 01h  | R/W w/PEC       | 1     | 80h                        | YES |
| ON_OFF_CONFIG       | 02h  | R/W w/PEC       | 1     | 1Eh                        | YES |
| CLEAR_FAULTS        | 03h  | Send byte w/PEC | 0     | -                          |     |
| WRITE_PROTECT       | 10h  | R/W w/PEC       | 1     | 00h                        | YES |
| STORE_USER_ALL      | 15h  | Send byte w/PEC | 0     | -                          |     |
| RESTORE_USER_ALL    | 16h  | Send byte w/PEC | 0     | -                          |     |
| CAPABILITY          | 19h  | R w/PEC         | 1     | B0h                        |     |
| VOUT_MODE           | 20h  | R w/PEC         | 1     | 40h                        |     |
| VOUT_COMMAND        | 21h  | R/W w/PEC       | 2     | 0384h (1.8V)               | YES |
| VOUT_MAX            | 24h  | R/W w/PEC       | 2     | 0BB8h (6V)                 | YES |
| VOUT_SCALE_LOOP     | 29h  | R/W w/PEC       | 2     | 01F4h (0.67V)              | YES |
| VOUT_MIN            | 2Bh  | R/W w/PEC       | 2     | 00FAh (0.5V)               | YES |
| VIN_ON              | 35h  | R/W w/PEC       | 2     | 0010h (4V)                 | YES |
| VIN_OFF             | 36h  | R/W w/PEC       | 2     | 000Fh (3.75V)              | YES |
| IOUT_OC_FAULT_LIMIT | 46h  | R/W w/PEC       | 2     | 00E3h (54A)                | YES |
| IOUT_OC_WARN_LIMIT  | 4Ah  | R/W w/PEC       | 2     | 00D7h (52A)                | YES |
| OT_FAULT_LIMIT      | 4Fh  | R/W w/PEC       | 2     | 00A0h (160°C)              | YES |
| OT_WARN_LIMIT       | 51h  | R/W w/PEC       | 2     | 008Ch (125°C)              | YES |
| VIN_OV_FAULT_LIMIT  | 55h  | R/W w/PEC       | 2     | 0024h (18V)                | YES |
| VIN_OV_WARN_LIMIT   | 57h  | R/W w/PEC       | 2     | 0022h (17V)                | YES |
| VIN_UV_WARN_LIMIT   | 58h  | R/W w/PEC       | 2     | 0001h (0.25V)              | YES |
| TON_DELAY           | 60h  | R/W w/PEC       | 2     | 0000h (0ms)                | YES |
| TON_RISE            | 61h  | R/W w/PEC       | 2     | 0000h (0ms)                | YES |
| TOFF_DELAY          | 64h  | R/W w/PEC       | 2     | 0000h (0ms)                | YES |
| STATUS_BYTE         | 78h  | R w/PEC         | 1     |                            |     |
| STATUS_WORD         | 79h  | R w/PEC         | 2     |                            |     |
| STATUS_VOUT         | 7Ah  | R w/PEC         | 1     |                            |     |
| STATUS_IOUT         | 7Bh  | R w/PEC         | 1     |                            |     |
| STATUS_INPUT        | 7Ch  | R w/PEC         | 1     |                            |     |
| STATUS_TEMPERATURE  | 7Dh  | R w/PEC         | 1     |                            |     |
| STATUS_CML          | 7Eh  | R w/PEC         | 1     |                            |     |
| READ_VIN            | 88h  | R w/PEC         | 2     |                            |     |
| READ_VOUT           | 8Bh  | R w/PEC         | 2     |                            |     |
| READ_IOUT           | 8Ch  | R w/PEC         | 2     |                            |     |
| READ_TEMPERATURE_1  | 8Dh  | R w/PEC         | 2     |                            |     |

**REGISTER MAP (continued)**

| Name                 | Code | Type             | Bytes               | Default Value (-0022 Part)                             | MTP   |
|----------------------|------|------------------|---------------------|--|-------|
| PMBUS_REVISION       | 98h  | R w/PEC          | 1                   | 33h, ASCII "13" (PMBus 1.3)                            |       |
| MFR_ID               | 99h  | Block read w/PEC | 1(byte)+<br>3(data) | 4Dh 50h 53h, ASCII "MPS"                               |       |
| MFR_MODEL            | 9Ah  | Block read w/PEC | 1(byte)+<br>8(data) | 4Dh 50h 51h 38h 36h 34h 35h<br>50h, ASCII "MPM3695-25" |       |
| MFR_REVISION         | 9Bh  | Block read w/PEC | 1(byte)+<br>1(data) | 32h, ASCII "MPM3695-25"                                | YES * |
| MFR_4_DIGIT          | 9Dh  | Block read w/PEC | 1(byte)+<br>6(data) | 31h 36h 30h 30h 30h 30h<br>(MPM3695-25 4-digit 0000)   | YES * |
| MFR_CTRL_COMP        | D0h  | R/W w/PEC        | 1                   | 0Ch  | YES   |
| MFR_CTRL_VOUT        | D1h  | R/W w/PEC        | 1                   | 00h  | YES   |
| MFR_CTRL_OPS         | D2h  | R/W w/PEC        | 1                   | 03h  | YES   |
| MFR_ADDR_PMBUS       | D3h  | R/W w/PEC        | 1                   | 30h  | YES   |
| MFR_VOUT_FAULT_LIMIT | D4h  | R/W w/PEC        | 1                   | 03h  | YES   |
| MFR_OVP_NOCP_SET     | D5h  | R/W w/PEC        | 1                   | 02h  | YES   |
| MFR_OT_OC_SET        | D6h  | R/W w/PEC        | 1                   | 08h  | YES   |
| MFR_OC_PHASE_LIMIT   | D7h  | R/W w/PEC        | 1                   | 12h (27A)  | YES   |
| MFR_HICCUP_ITV_SET   | D8h  | R/W w/PEC        | 1                   | 00h  | YES   |
| MFR_PGOOD_ON_OFF     | D9h  | R/W w/PEC        | 1                   | 00h  | YES   |
| MFR_VOUT_STEP        | DAh  | R/W w/PEC        | 1                   | 04h  | YES   |
| MFR_LOW_POWER        | E5h  | R/W w/PEC        | 1                   | 00h  | YES   |

\* For manufacturer WRITE only

## COMMANDS

### OPERATION (01h)

OPERATION is a paged register. The OPERATION command is used to turn the converter output on/off in conjunction with input from the CTRL pin. It is also used to set the output voltage to the upper or lower MARGIN voltages. The unit stays in the commanded operating mode until a subsequent OPERATION command or a change in the state of the CTRL pin instructs the converter to change to another mode. This OPERATION command is also used to re-enable the converter after a fault triggered shutdown. Writing an OFF command followed by an ON command will clear all faults. Writing only an ON command after a fault-triggered shutdown will not clear the fault registers.

| Command  | OPERATION       |     |     |     |     |     |   |   |
|----------|-----------------|-----|-----|-----|-----|-----|---|---|
| Format   | Unsigned binary |     |     |     |     |     |   |   |
| Bit      | 7               | 6   | 5   | 4   | 3   | 2   | 1 | 0 |
| Access   | r/w             | r/w | r/w | r/w | r/w | r/w | r | r |
| Function |                 |     |     |     |     |     | x | x |

| Bit[7:6] | Bit[5:4] | Bit[3:2] | Bit[1:0] | On/off        | Margin state               |
|----------|----------|----------|----------|---------------|----------------------------|
| 00       | xx       | xx       | Xx       | Immediate off | N/A                        |
| 01       | Xx       | xx       | Xx       | Soft off      | N/A                        |
| 10       | 00       | xx       | Xx       | on            | off                        |
| 10       | 01       | 01       | Xx       | on            | Margin low (ignore fault)  |
| 10       | 01       | 10       | Xx       | on            | Margin low (act on fault)  |
| 10       | 10       | 01       | Xx       | on            | Margin high (ignore fault) |
| 10       | 10       | 10       | Xx       | on            | Margin high (act on fault) |

### ON\_OFF\_CONFIG (02h)

The ON\_OFF\_CONFIG command configures the combination of the CTRL pin input and the PMBus commands needed to turn the converter on and off. This includes how the converter responds when input voltage is applied.

| Command  | OPERATION       |   |   |     |     |     |     |     |
|----------|-----------------|---|---|-----|-----|-----|-----|-----|
| Format   | Unsigned binary |   |   |     |     |     |     |     |
| Bit      | 7               | 6 | 5 | 4   | 3   | 2   | 1   | 0   |
| Access   | r               | r | r | r/w | r/w | r/w | r/w | r   |
| Function | X               | X | X | pon | op  | en  | pol | dly |

#### *pon*

The pon bit sets the default to either operate any time the input voltage is present or for the on/off to be controlled by the CTRL pin and PMBus commands.

| Bit[4] Value | Meaning  |
|--------------|--|
| 0            | Converter powers up any time the input voltage is present regardless of state of the CTRL pin                  |
| 1            | Converter does not power up until commanded by the CTRL pin and OPERATION command (as programmed in bits[3:0]) |

#### *op*

The op bit controls how the converter responds to the OPERATION commands.

| Bit[3] Value | Meaning   |
|--------------|---|
| 0            | Converter ignores the “on” bit in the OPERATION command from the PMBus  |
| 1            | Converter responds the “on” bit in the OPERATION command from the PMBus |

**en**

This en bit controls how the converter responds to the CTRL pin.

| Bit[2] Value | Meaning  |
|--------------|--|
| 0            | Converter ignores the CTRL pin (on/off controlled only by the OPERATION command).  |
| 1            | Converter requires the CTRL pin to be asserted to power up.<br>Depending on the bit[3] op bit, the OPERATION command may also be required to instruct the converter to power up. |

**pol**

The pol bit sets the polarity of the CTRL pin.

| Bit[1] Value | Meaning   |
|--------------|---|
| 0            | Active low (Pull CTRL pin low to start the converter)   |
| 1            | Active high (Pull CTRL pin high to start the converter) |

**dly**

The dly bit sets the turn off action when the converter is commanded off. This bit is read only and can't be modified by the end user.

| Bit[0] Value | Meaning               |
|--------------|-----------------------|
| 0            | TOFF_DELAY, TOFF_FALL |

**CLEAR\_FAULTS (03h)**

The CLEAR\_FAULTS command is used to reset all stored warning and fault flags. If a fault or warning condition still exists when the CLEAR\_FAULTS command is issued, the ALT# signal may not be cleared or will be re-asserted almost immediately. Issuing a CLEAR\_FAULTS command will not cause the converter to restart in the event of a fault turn-off. It must be done by issuing an OPERATION command after the fault condition is cleared. This command uses the PMBus to send byte protocol.

**WRITE PROTECT (10h)**

The WRITE\_PROTECT command is used to control writing to the converter. The intent of this command is to provide protection against accident changes. It's not intended to provide protection against deliberate or malicious changes to the converter's configuration or operation.

All the supported commands may have their parameters read, regardless of the WRITE\_PROTECT settings.

| Bit[7:0] Value |   |   |   |   |   |   |   | Meaning   |
|----------------|---|---|---|---|---|---|---|---|
| 0              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Enable writes to all commands.  |
| 0              | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG and VOUT_COMMAND commands. |
| 0              | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Disable all writes except to the WRITE_PROTECT, OPERATION and PAGE commands.                              |
| 1              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Disable all writes except to the WRITE_PROTECT command.   |

**STORE\_USER\_ALL (15h)**

Write all the data from the registers to the internal MTPs. This process will operate when the MPM3695-25 receives a STORE\_USER\_ALL command from the PMBus interface. Currently the MPM3695-25 doesn't support the standard 15h command. However, it can accept a 15h command from the MPS GUI for the MPM3695-25. See the "MTP Programming" section for additional details.

The following registers can be stored using STORE\_USER\_ALL:

|                           |                            |
|---------------------------|----------------------------|
| OPERATION (01h)           | TON_DELAY (60h)            |
| ON_OFF_CONFIG (02h)       | TON_RISE (61h)             |
| WRITE PROTECT (10h)       | TOFF_DELAY (64h)           |
| VOUT_COMMAND (21h)        | MFR_REVISION (9Bh)         |
| VOUT_MAX (24h)            | MFR_4_DIGIT (9Dh)          |
| VOUT_MARGIN_HIGH (25h)    | MFR_CTRL_COMP (D0h)        |
| VOUT_MARGIN_LOW (26h)     | MFR_CTRL_VOUT (D1h)        |
| VOUT_SCALE_LOOP (29h)     | MFR_CTRL_OPS (D2h)         |
| VOUT_MIN (2Bh)            | MFR_ADDR_PMBUS (D3h)       |
| VIN_ON (35h)              | MFR_VOUT_FAULT_LIMIT (D4h) |
| VIN_OFF (36h)             | MFR_OVP_NOCP_SET (D5h)     |
| IOUT_OC_FAULT_LIMIT (46h) | MFR_OT_OC_SET (D6h)        |
| IOUT_OC_WARN_LIMIT (4Ah)  | MFR_OC_PHASE_LIMIT (D7h)   |
| OT_FAULT_LIMIT (4Fh)      | MFR_HICCUP_ITV_SET (D8h)   |
| OT_WARN_LIMIT (51h)       | MFR_PGOOD_ON_OFF (D9h)     |
| VIN_OV_FAULT_LIMIT (55h)  | MFR_VOUT_STEP (DAh)        |
| VIN_OV_WARN_LIMIT (57h)   | MFR_LOW_POWER (E5h)        |
| VIN_UV_WARN_LIMIT (58h)   |                            |

### RESTORE\_USER\_ALL (16h)

The RESTORE\_USER\_ALL command instructs the MPM3695-25 to copy all content of the MTP values to the matching locations in the registers. The values in the registers are overwritten by the value retrieved from the MTP. Any items in the MTPs that do not have matching locations in the operating memory are ignored.

The RESTORE\_USER\_ALL command can be used while the MPM3695-25 is operating.

Please Note: While the RESTORE\_USER\_ALL command can be used, the MPM3695-25 may be unresponsive during the copy operation with unpredictable, undesirable, or even catastrophic results.

This command is write only.

### CAPABILITY (19h)

The CAPABILITY command returns information about the PMBus functions supported by the MPM3695-25. This command is read with the PMBus read byte protocol.

| Command  | CAPABILITY      |                |   |       |   |   |   |   |
|--|-----------------|----------------|---|-------|---|---|---|---|
| Format   | Unsigned binary |                |   |       |   |   |   |   |
| Bit  | 7               | 6              | 5 | 4     | 3 | 2 | 1 | 0 |
| Access   | r               | r              | r | r     | r | r | r | r |
| Function   | PEC             | Max. bus speed |   | Alert | x | x | x | x |
| Default value  | 1               | 0              | 1 | 1     | 0 | 0 | 0 | 0 |
| PEC supported, max speed 400kHz, supports PMBus Alert and ARA. |                 |                |   |       |   |   |   |   |

| Bit[6:5] | Value | Meaning                                |
|----------|-------|--|
| 0        | 0     | Maximum supported bus speed is 100kHz. |
| 0        | 1     | Maximum supported bus speed is 400kHz. |
| 1        | 0     | Maximum supported bus speed is 1MHz.   |
| 1        | 1     | Reserved.                              |

### VOUT\_MODE (20h)

The VOUT\_MODE command is used to command and read the output voltage. The 3 most significant bits are used to determine the data format (only a direct format is supported by the MPM3695-25), and the remaining 5 bits represent the exponent used in the output voltage read/write commands.

### VOUT\_COMMAND (21h)

The VOUT\_COMMAND sets the output voltage of the MPM3695-25. The VOUT\_COMMAND and the VOUT\_SCALE\_LOOP together determine the feedback reference voltage: VOUT\_COMMAND\*VOUT\_SCALE\_LOOP.

Please refer to the “Output Voltage Setting” section to program the output voltage.

| Command  | VOUT_COMMAND |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|--------------|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Direct       |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15           | 14 | 13 | 12 | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r            | r  | r  | r  | r/w |
| Function | x            |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |

The value is unsigned and 1LSB = 2mV.

The vout command accuracy is 2mV/K; K is the SCALE\_LOOP value. The default value is 1.8V.

### VOUT\_MAX (24h)

The VOUT\_MAX command sets an upper limit on the output voltage the converter can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output over-voltage protection.

| Command  | VOUT_MAX |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|----------|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Direct   |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15       | 14 | 13 | 12 | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r        | r  | r  | r  | r/w |
| Function | x        |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |

If an attempt is made to program the output voltage higher than the limit set by this command, the device shall respond as follows:

- The commanded output voltage shall be set to VOUT\_MAX,
- The NONE OF THE ABOVE bit shall be set in the STATUS\_BYTE
- The VOUT bit shall be set in the STATUS\_WORD
- The VOUT\_MAX\_MIN warning bit shall be set in the STATUS\_VOUT register
- The device shall notify the host

The value is unsigned and 1LSB=2mV. The maximum value of VOUT\_MAX is 6V, and the default value is 6V.

### VOUT\_MARGIN\_HIGH (25h)

| Command  | VOUT_MARGIN_HIGH |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|------------------|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Direct           |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15               | 14 | 13 | 12 | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r                | r  | r  | r  | r/w |
| Function | x                | x  | x  | x  |     |     |     |     |     |     |     |     |     |     |     |     |

The value is unsigned and 1LSB = 2mV.

### VOUT\_MARGIN\_LOW (26h)

| Command  | VOUT_MARGIN_LOW |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-----------------|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Direct          |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14 | 13 | 12 | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r               | r  | r  | r  | r/w |
| Function | x               | x  | x  | x  |     |     |     |     |     |     |     |     |     |     |     |     |

The value is unsigned and 1LSB = 2mV.

### VOUT\_SCALE\_LOOP (29h)

The VOUT\_SCALE\_LOOP sets the feedback resistor divider ratio. It equals VFB/VOUT. Regardless of the external or internal feedback resistor divider used, the VOUT\_SCALE\_LOOP should match the actual feedback resistor divider used.

| Command  | VOUT_SCALE_LOOP |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-----------------|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Direct          |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15              | 14 | 13 | 12 | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r               | r  | r  | r  | r/w |
| Function | x               |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |

The value is unsigned and 1LSB = 0.001. The default value is 0.335.

### VOUT\_MIN (2Bh)

The VOUT\_MIN command sets a lower limit on the output voltage the converter can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output under-voltage protection.

| Command  | VOUT_MIN |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|----------|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Direct   |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15       | 14 | 13 | 12 | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r        | r  | r  | r  | r/w |
| Function | x        |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |

If an attempt is made to program the output voltage lower than the limit set by this command, the device shall respond as follows:

- The commanded output voltage shall be set to VOUT\_MIN
- The NONE OF THE ABOVE bit shall be set in the STATUS\_BYTE
- The VOUT bit shall be set in the STATUS\_WORD
- The VOUT\_MAX\_MIN warning bit shall be set in the STATUS\_VOUT register
- The device shall notify the host

The minimum value of VOUT\_MIN is 0.5V. The value is unsigned and 1LSB=2mV. The default value is 0.5V.

**VIN\_ON (35h)**

The VIN\_ON command sets the value of the input voltage, in Volts, at which the converter should be turned on if all other required power-up conditions are met. The VIN\_ON value can be set between 4V and 15V with a 0.25V increment. The VIN\_ON value should always be set higher than the VIN\_OFF value, with enough margin, so that there will be no bouncing between VIN\_ON and VIN\_OFF during power conversion.

| Command  | VIN_ON |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|--------|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Direct |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15     | 14 | 13 | 12 | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r      | r  | r  | r  | r/w |
| Function | x      | x  | x  | x  |     |     |     |     |     |     |     |     |     |     |     |     |

The value is unsigned and 1LSB=250mV. The default value is 4V.

**VIN\_OFF (36h)**

The VIN\_OFF command sets the value of the input voltage, in Volts, at which the converter, once operation has started, should be turned off. The VIN\_OFF value can be set between 3.75V and 14.75V with a 0.25V increment. The VIN\_OFF value should be always set lower than VIN\_ON value, with enough margin, so that there will be no bouncing between VIN\_OFF and VIN\_ON during power conversion.

| Command  | VIN_OFF |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|---------|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Direct  |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15      | 14 | 13 | 12 | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r       | r  | r  | r  | r/w |
| Function | x       | x  | x  | x  |     |     |     |     |     |     |     |     |     |     |     |     |

The value is unsigned and 1 LSB=250mV. The default value is 2.75V.

The corresponding value is 54A.

**OT\_FAULT\_LIMIT (4Fh)**

The OT\_FAULT\_LIMIT is used to configure or read the threshold for the over-temperature fault detection. If the measured temperature exceeds this value, an over-temperature fault will be triggered. The way the MPM3695-25 operates after OTP depends on the AUTO bin in MFR\_CTRL (F0h) register; OT fault flags are set in the STATUS\_BYTE(78h), STATUS\_WORD(79h) respectively, and the ALT# signal is asserted. After the measured temperature falls below the value in this register, the converter will be turned back on with the OPERATION command when the part works in latch off mode. The minimum temperature fault detection time should be less than 20ms. The temperature range is 0 °C to 255°C.

If an OT fault occurs when the temperature rises above this register value, the part will auto-retry when the temperature drops below 20°C than this register value.

| Command  | OT_FAULT_LIMIT |    |    |    |    |    |   |   |   |          |     |     |     |     |     |     |  |  |  |  |  |  |  |  |  |
|----------|----------------|----|----|----|----|----|---|---|---|----------|-----|-----|-----|-----|-----|-----|--|--|--|--|--|--|--|--|--|
| Format   | Direct         |    |    |    |    |    |   |   |   |          |     |     |     |     |     |     |  |  |  |  |  |  |  |  |  |
| Bit      | 15             | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6        | 5   | 4   | 3   | 2   | 1   | 0   |  |  |  |  |  |  |  |  |  |
| Access   | r              | r  | r  | r  | r  | r  | r | r | r | r/w      | r/w | r/w | r/w | r/w | r/w | r/w |  |  |  |  |  |  |  |  |  |
| Function | x              |    |    |    |    |    |   |   |   | 1°C /LSB |     |     |     |     |     |     |  |  |  |  |  |  |  |  |  |

The value is unsigned and 1LSB=1°C. The default value is 0091h. The corresponding value is 145°C.

The OT\_FAULT\_LIMIT setting value should be lower than 160°C. If the OT\_FAULT\_LIMIT value is set higher than 160°C, the register value will be neglected, and the MPM3695-25 will enter thermal shutdown when the junction temperature reaches 160°C.

The table below shows the relationship between the direct value and the real word value.

| Direct Value | Real World Value / °C |
|--------------|-----------------------|
| 0000 0000    | 0                     |
| 0000 0001    | 1                     |
| 1111 1111    | +255                  |

#### OT\_WARN\_LIMIT (51h)

The OT\_WARN\_LIMIT is used to configure or read the threshold for the over-temperature warning detection. If the sense temperature exceeds this value, an over-temperature warning is triggered, the OT warn flags are set in the STATUS\_BYTE(78h), STATUS\_WORD(79h) respectively, and the ALT# signal is asserted. The minimum temperature warning detection time should be less than 20ms.

| Command  | OT_WARN_LIMIT |    |    |    |    |    |   |   |     |     |     |     |     |     |     |     |
|----------|---------------|----|----|----|----|----|---|---|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Direct        |    |    |    |    |    |   |   |     |     |     |     |     |     |     |     |
| Bit      | 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r             | r  | r  | r  | r  | r  | r | r | r/w |
| Function | 1 °C /LSB     |    |    |    |    |    |   |   |     |     |     |     |     |     |     |     |

The value is unsigned and 1LSB=1°C. The default value is 007Dh. The corresponding value is 125°C. The OT\_WARN\_LIMIT setting value should be lower than 160°C. The relationship between the direct value and the real word value is the same with OT\_FAULT\_LIMIT.

#### VIN\_OV\_FAULT\_LIMIT (55h)

The VIN\_OV\_FAULT\_LIMIT command is used to configure or read the threshold for the input over-voltage fault detection. If the measured value of VIN rises above the value in this register, the VIN OV fault flags are set in the respective registers. The power stage of the MPM3695-25 will be disabled. When VIN drops below the VIN\_OV\_FAULT\_LIMIT, the MPM3695-25 will be re-enabled.

| Command  | VIN_OV_FAULT_LIMIT |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|--------------------|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Direct             |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                 | 14 | 13 | 12 | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r                  | r  | r  | r  | r/w |
| Function | 500mV/LSB          |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |

The value is unsigned and 1LSB=500mV. The default value is 22h. The corresponding value is 17V.

The VIN\_OV\_FAULT\_LIMIT setting value should not be higher than 18V.

#### VIN\_OV\_WARN\_LIMIT (57h)

The VIN\_OV\_WARN\_LIMIT command is used to configure or read the threshold for the input over-voltage warning detection. If the measured value of VIN rises above the value in this register, VIN OV warning flags are set in the respective registers, and the ALT# signal is asserted.

| Command  | VIN_OV_WARN_LIMIT |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
|----------|-------------------|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Direct            |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                | 14 | 13 | 12 | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r                 | r  | r  | r  | r/w |
| Function | 500mV/LSB         |    |    |    |     |     |     |     |     |     |     |     |     |     |     |     |

The value is unsigned and 1LSB=500mV. The default value is 22h. The corresponding value is 17V.

The VIN\_OV\_WARN\_LIMIT setting value should not be higher than 18V.

### VIN\_UV\_WARN\_LIMIT (58h)

The VIN\_UV\_WARN\_LIMIT command is used to configure or read the threshold for the input undervoltage fault detection. If the measured value of VIN falls below the value in this register, VIN UV warning flags are set in the respective registers, and the ALT# signal is asserted.

| Command  | VIN_UV_WARN_LIMIT |    |    |    |     |     |     |     |     |     |     |     |     |     |     |           |
|----------|-------------------|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----------|
| Format   | Direct            |    |    |    |     |     |     |     |     |     |     |     |     |     |     |           |
| Bit      | 15                | 14 | 13 | 12 | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0         |
| Access   | r                 | r  | r  | r  | r/w       |
| Function | x                 |    |    |    |     |     |     |     |     |     |     |     |     |     |     | 250mV/LSB |

The value is unsigned and 1LSB=250mV. The default value is 01h.

The VIN\_UV\_WARN\_LIMIT setting value should be higher than 3.3V.

### TON\_DELAY (60h)

The TON\_DELAY command sets the time, in ms, from when a start condition is received (as programmed by the ON\_OFF\_CONFIG command) until the output voltage starts to rise.

| Command  | TON_DELAY |    |    |    |    |     |     |     |     |     |     |     |     |     |     |         |
|----------|-----------|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------|
| Format   | Direct    |    |    |    |    |     |     |     |     |     |     |     |     |     |     |         |
| Bit      | 15        | 14 | 13 | 12 | 11 | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0       |
| Access   | r         | r  | r  | r  | r  | r/w     |
| Function | x         | x  | x  | x  | x  |     |     |     |     |     |     |     |     |     |     | 4ms/LSB |

The value is unsigned and 1LSB=4ms. The maximum value is 60h=0100h (1024ms). The default value is 0ms.

### TON\_RISE (61h)

The TON\_RISE command sets the soft-start time, in ms, from when the output starts to rise until the voltage has reached the regulation point.

| Command  | TON_RISE |    |    |    |     |     |     |     |     |     |     |     |     |     |     |         |
|----------|----------|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------|
| Format   | Direct   |    |    |    |     |     |     |     |     |     |     |     |     |     |     |         |
| Bit      | 15       | 14 | 13 | 12 | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0       |
| Access   | r        | r  | r  | r  | r/w     |
| Function | x        | x  | x  | x  | x   |     |     |     |     |     |     |     |     |     |     | 1ms/LSB |

The supported values are as follows:

- 000b: 1ms
- 001b: 2ms
- 010b: 4ms
- 011b: 8ms
- 100b and up: 16ms.

The default value is 01h, i.e. 2ms for soft-start time.

### TOFF\_DELAY (64h)

The TOFF\_DELAY command sets the time, in ms, from when a stop condition is received (as programmed by the ON\_OFF\_CONFIG command) until the MPM3695-25 disables its power stage.

| command  | TON_DELAY |    |    |    |    |     |     |     |     |     |     |     |     |     |     |         |
|----------|-----------|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------|
| format   | Direct    |    |    |    |    |     |     |     |     |     |     |     |     |     |     |         |
| Bit      | 15        | 14 | 13 | 12 | 11 | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0       |
| Access   | r         | r  | r  | r  | r  | r/w     |
| Function | x         | x  | x  | x  | x  |     |     |     |     |     |     |     |     |     |     | 4ms/LSB |

The value is unsigned and 1LSB=4ms. The maximum value is 64h=0100h(1024ms) and the default value is 0ms.

**STATUS BYTE (78h)**

The STATUS\_BYTE command returns the value of a number of flags indicating the state of the MPM3695-25. Access to this command should use the read byte protocol. To clear bits in this register, the underlying fault should be removed and a CLEARFAULTS command issued.

| Bits | Name              | Behavior | Default Set | Description   |
|------|-------------------|----------|-------------|---|
| [7]  | Reserved          |          | 0           | Always read as 0  |
| [6]  | OFF               | Live     | 0           | 0 Part enabled<br>1 Part disabled, this can be triggered from: OC fault, OT fault, BAD FET fault, UV/OV fault, or the operation command to turn off |
| [5]  | VOUT_OV           |          | 0           | An output over-voltage fault has occurred.  |
| [4]  | IOUT_OC_FAULT     | Latched  | 0           | 0 Over-current fault detected<br>1 No over-current fault detected   |
| [3]  | VIN_UV            |          | 0           | Not supported, always read as 0   |
| [2]  | OT_FAULT_WARN     | Live     | 0           | 0 No over-temperature warning or fault detected<br>1 Over-temperature warning or fault detected   |
| [1]  | CUMM_ERROR        | Latched  | 0           | 0 No communication error detected<br>1 Communication error detected   |
| [0]  | NONE_OF_THE ABOVE | Live     | 0           | 0 No other fault or warning<br>1 Fault or warning not listed in bits [7:1] has occurred.  |

**STATUS WORD (79h)**

The STATUS\_WORD returns the value of a number of flags indicating the state of the MPM3695-25. To clear bits in this register, the underlying fault should be removed and a CLEARFAULTS command issued.

| Bits     | Name        | Behavior | Default Set | Description  |
|----------|-------------|----------|-------------|--|
| [15]     | VOUT_STATUS | Live     | 0           | 0 No output fault or warning<br>1 Output fault or warning  |
| [14]     | IOUT_STATUS | Live     | 0           | 0 No Iout fault<br>1 Iout fault  |
| [13]     | VIN_STATUS  | Live     | 0           | 0 No VIN fault<br>1 VIN fault, at the period when Vin starts up, the initial flag is 1 before the Vin passes the UVLO threshold. It is then cleared once the Vin passes UVLO |
| [12]     | MFR_STATUS  |          | 0           | Always read as 0   |
| [11]     | POWER_GOOD# | Live     | 0           | 0 Power good signal is asserted<br>1 Power good signal is not asserted   |
| [10]     | Reserved    |          | 0           | Always read as 0   |
| [9]      | Reserved    |          | 0           | Always read as 0   |
| [8]      | UNKNOWN     | Latched  | 0           | 0 No other fault has occurred<br>1 A fault type not specified in bits [15:1] of the STATUS_WORD has been detected.   |
| Low Byte | STATUS_BYTE |          |             | STATUS BYTE is the low byte of the STATUS WORD   |

### STATUS\_VOUT (7Ah)

The STATUS\_VOUT command returns one data byte with contents as follows:

| Bits | Name          | Behavior | Default Set | Description   |
|------|---------------|----------|-------------|---|
| [7]  | VOUT_OV_FAULT | Live     | 0           | 0 No output OV fault<br>1 Output OV fault   |
| [6]  | Reserved      | Latched  | 0           | Always read as 0  |
| [5]  | Reserved      | Latched  | 0           | Always read as 0  |
| [4]  | VOUT_UV_FAULT | Live     | 0           | 0 No output UV fault<br>1 output UV fault   |
| [3]  | VOUT_MAX_MIN  | Live     | 0           | 0 No VOUT_MAX, VOUT_MIN warning<br>1 An attempt has been made to set the output voltage to a value higher than allowed by the VOUT_MAX command or lower than the limit allowed by the VOUT_MIN command. |
| [2]  | Reserved      |          | 0           | Always read as 0  |
| [1]  | Reserved      |          | 0           | Always read as 0  |
| [0]  | UNKNOWN       | Latched  | 0           | 0 No other fault has occurred<br>1 A fault type not specified in bits [15:1] of the STATUS_WORD has been detected.  |

### STATUS\_IOUT (7Bh)

| Command       | STATUS_IOUT     |                   |                 |   |   |   |   |   |
|---------------|-----------------|-------------------|-----------------|---|---|---|---|---|
| Format        | Unsigned binary |                   |                 |   |   |   |   |   |
| Bit           | 7               | 6                 | 5               | 4 | 3 | 2 | 1 | 0 |
| Access        | r               | r                 | r               | r | r | r | r | r |
| Function      | IOUT_OC         | IOUT_OC & VOUT_UV | IOUT_OC_WARNING | x | x | x | x | x |
| Default value | 0               | 0                 | 0               | 0 | 0 | 0 | 0 | 0 |

### STATUS\_INPUT (7Ch)

The STATUS\_INPUT returns the value of flags indicating the input voltage status of the MPM3695-25. To clear bits in this register, the underlying fault or warning should be removed and a CLEAR\_FAULTS command issued.

| Bits  | Name         | Behavior  | Default Set | Description  |
|-------|--------------|-----------|-------------|--|
| [7]   | VIN_OV_FAULT | R Latched | 0           | 0 means no over-voltage detected on the OV pin<br>1 means over-voltage detected on the OV pin                  |
| [6]   | VIN_OV_WARN  | R Latched | 0           | 0 means over-voltage condition on VIN has not occurred<br>1 means over-voltage condition on VIN has occurred   |
| [5]   | VIN_UV_WARN  | R Latched | 0           | 0 means under-voltage condition on VIN has not occurred<br>1 means under-voltage condition on VIN has occurred |
| [4:0] | Reserved     | r         | 0           | Always read as 0000  |

### STATUS\_TEMPERATURE (7Dh)

The STATUS\_TEMPERATURE returns the value of flags indicating the VIN over-voltage or under-voltage of the MPM3695-25. To clear bits in this register, the underlying fault should be removed and a CLEAR\_FAULTS command issued.

| Bits  | Name       | Behavior  | Default Set | Description                                   |
|-------|------------|-----------|-------------|---|
| [7]   | OT_FAULT   | R Latched | 0           | 1 means over-temperature fault has occurred   |
| [6]   | OT_WARNING | R Latched | 0           | 1 means over-temperature warning has occurred |
| [5:0] | Reserved   | R         | 0           | Always read as 0                              |

### STATUS\_CML (7Eh)

| Command  | STATUS_CML                  |                            |   |                       |   |   |             |             |
|----------|-----------------------------|----------------------------|---|-----------------------|---|---|-------------|-------------|
| Format   | Unsigned binary             |                            |   |                       |   |   |             |             |
| Bit      | 7                           | 6                          | 5 | 4                     | 3 | 2 | 1           | 0           |
| Access   | r                           | r                          | r | r                     | r | r | r           | r           |
| Function | Invalid unsupported command | Invalid / unsupported data | x | Memory fault detected | x | x | Other fault | Memory busy |

### READ\_VIN (88h)

The READ\_VIN command returns the 10-bit measured value of the output voltage.

| Command  | READ_VOUT |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|----------|-----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format   | Direct    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Bit      | 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r         | r  | r  | r  | r  | r  | r | r | r | r | r | r | r | r | r | r |
| Function | x         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### READ\_VOUT (8Bh)

The READ\_VOUT command returns the 10-bit measured value of the output voltage.

| Command  | READ_VOUT |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|----------|-----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format   | Direct    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Bit      | 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r         | r  | r  | r  | r  | r  | r | r | r | r | r | r | r | r | r | r |
| Function | x         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### READ\_IOUT (8Ch)

The READ\_VOUT command returns the 10-bit measured value of the output current. This value is also used for the IOUT\_OC\_WARNING and then affects the STATUS\_IOUT.

| Command  | READ_IOUT |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|----------|-----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format   | Direct    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Bit      | 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access   | r         | r  | r  | r  | r  | r  | r | r | r | r | r | r | r | r | r | r |
| Function | x         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

### READ\_TEMPERATURE\_1 (8Dh)

The READ\_TEMPERATURE\_1 command returns the internal sensed temperature. This value is also used internally for the over-temperature fault and warning detection. This data has a range of -255°C to +255°C.

| Command  | READ_TEMPERATURE_1 |    |    |    |    |    |     |     |     |     |     |     |     |     |     |     |
|----------|--------------------|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format   | Direct             |    |    |    |    |    |     |     |     |     |     |     |     |     |     |     |
| Bit      | 15                 | 14 | 13 | 12 | 11 | 10 | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| Access   | r                  | r  | r  | r  | r  | r  | r/w |
| Function | x                  |    |    |    |    |    |     |     |     |     |     |     |     |     |     |     |

READ\_TEMPERATURE is a 2-byte, twos complement integer. The bit9 is the sign bit. The default value is 0032h. The corresponding value is 25°C.

The table below shows the relationship between the direct value and the real word value.

| Sign | Direct Value | Real World Value / °C |
|------|--------------|-----------------------|
| 0    | 0 0000 0000  | 0                     |
| 0    | 0 0000 0001  | 1                     |
| 0    | 1 1111 1111  | +511                  |
| 1    | 0 0000 0001  | -511                  |
| 1    | 1 1111 1111  | -1                    |

**PMBUS\_REVISION (98h)**

The PMBUS\_REVISION command returns the protocol revision we used. Access to this command should use the read byte protocol. Bits [7:4] indicate the PMBus revision of specification Part I to which the device is compliant. Bits [3:0] indicate the revision of specification Part II to which the device is compliant.

| Command       | PMBUS_REVISION  |   |   |   |   |   |   |   |
|---------------|-----------------|---|---|---|---|---|---|---|
| Format        | Unsigned binary |   |   |   |   |   |   |   |
| Bit           | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access        | r               | r | r | r | r | r | r | r |
| Default value | 0               | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

Bits [7:4] always read as 0010, specification PMBus Part I Revision 1.3.

Bits [3:0] always read as 0011, specification PMBus Part II Revision 1.3.

**MFR\_ID (99h)**

The MFR\_ID command returns the company identification.

| Byte | Byte Name   | Value       | Description   |
|------|-------------|-------------|---|
| 0    | Byte Count  | 0x03        | Always reads as 0x03, the number of data bytes that the block read command expects to read. |
| 1    | Character 1 | 0x4D or "M" | Always reads as 0x4D.   |
| 2    | Character 2 | 0x50 or "P" | Always reads as 0x50.   |
| 3    | Character 3 | 0x53 or "S" | Always reads as 0x53.   |

**MFR\_DATE (9Dh)**

The MFR\_4\_DIGIT sets the unique 4-digit number to identify different MTP default configurations. The MFR\_4\_DIGIT has a total of 6 bytes.

| Byte | Byte Name   | Value    |
|------|-------------|----------|
| 0    | Character 0 | 31h      |
| 1    | Character 1 | 36h~39h  |
| 2    | Character 2 | 30h, 31h |
| 3    | Character 3 | 30h~30F  |
| 4    | Character 4 | 30h~33h  |
| 5    | Character 5 | 30h~3Fh  |

The default 4-digit number for the MPM3695-25 is -0000, which corresponds 31h 36h 30h 30h 30h 30h (Byte 0~5).

### MFR\_CTRL\_COMP (D0h)

The MFR\_CTRL\_COMP command is used to adjust the loop compensation of the MPM3695-25.

| Bits  | Name                  | Access | Behavior | Default Set | Description  |                        |
|-------|-----------------------|--------|----------|-------------|--|------------------------|
| [7:5] | Reserved              | R/W    | Live     | 0000        |  |                        |
| [4]   | Cff                   | R/W    | Live     | 0           | 0: 20pF.<br>1: 50pF.   |                        |
| [3:1] | RAMP                  | R/W    | Live     | 110         | EAh[3]=0 (single phase)  | EAh[3]=1 (Multi-phase) |
|       |                       |        |          |             | 000: 5.6mV RAMP  | 000: 8.6mV RAMP        |
|       |                       |        |          |             | 001: 9.8mV RAMP  | 001: 15mV RAMP         |
|       |                       |        |          |             | 010: 18mV RAMP   | 010: 27mV RAMP         |
|       |                       |        |          |             | 011: 30mV RAMP   | 011: 45mV RAMP         |
|       |                       |        |          |             | 100: 8.5mV RAMP  | 100: 13mV RAMP         |
|       |                       |        |          |             | 101: 15.1mV RAMP   | 101: 23mV RAMP         |
|       |                       |        |          |             | 110: 27mV RAMP   | 110: 41mV RAMP         |
|       |                       |        |          |             | 111: 44mV RAMP   | 111: 68mV RAMP         |
| [0]   | Slave Fault Detection | R/W    | Live     | 1           | 0: Slave-phase fault detection is enabled; 1: Slave-phase fault detection is disabled. |                        |

Bit[4] (Cff): Set the feed-forward capacitance when the internal feedback resistor divider is selected.

Bit[3:1]: Set the internal RAMP compensation to stabilize the loop.

Bit[0]: Enable or disable the slave fault detection function through the PG pin.

### MFR\_CTRL\_VOUT (D1h)

The MFR\_CTRL\_VOUT command is used to adjust the output voltage of the MPM3695-25.

| Bits  | Name         | Access | Behavior | Default Set | Description  |
|-------|--------------|--------|----------|-------------|--|
| [7]   | Reserved     | R/W    | Live     | 0           |  |
| [6]   | Vo discharge | R/W    | Live     | 1           | 1: Output voltage discharge at CTRL low.<br>0: No active output voltage discharge. |
| [5:2] | PG delay     | R/W    | Live     | 0000        | 0000:2ms<br>0001: 3ms<br>.....<br>1110: 15ms<br>1111: 1ms                          |
| [1:0] | VO_RANGE     | R/W    | Live     | 10          | 0: Vo/Vref=1, Vref=0.5~0.672V, LSB=2mV   |

### MFR\_CTRL\_OPS (D2h)

The MFR\_CTRL\_OPS command is used to set the switching frequency and light-load operation mode of the MPM3695-25.

| Bits  | Name                | Access | Behavior | Default Set | Description   |
|-------|---------------------|--------|----------|-------------|---|
| [7:3] | Reserved            |        |          | 00000       |   |
| [2:1] | SWITCHING_FREQUENCY | R/W    | Live     | 01          | 00: Set the fs to 400KHz.<br>01: Set the fs to 600KHz.<br>10: Set the fs to 800KHz.<br>11: Set the fs to 1000Khz. |
| [0]   | SKIP_CCM (SYNC)     | R/W    | Live     | 1           | 0: Pulse-skip mode at light load.<br>1: Forced CCM at light load.   |

**MFR\_ADDR\_PMBUS (D3h)**

| Command  | MFR_ADDR_PMBUS |      |     |     |     |     |     |     |  |
|----------|----------------|------|-----|-----|-----|-----|-----|-----|--|
| Format   | Direct         |      |     |     |     |     |     |     |  |
| Bit      | 7              | 6    | 5   | 4   | 3   | 2   | 1   | 0   |  |
| Access   | r/w            | r/w  | r/w | r/w | r/w | r/w | r/w | r/w |  |
| Function | enable         | ADDR |     |     |     |     |     |     |  |

**Enable Bit**

1- The address is decided by MFR\_ADDR\_PMBUS [6:0]

0- The address is decided by ADDR pin.

**MFR\_VOUT\_UV\_OV\_FAULT\_LIMIT (D4h)**

This MFR\_VOUT\_UV\_OV\_FAULT\_LIMIT command sets the thresholds for UVP and OVP.

| Bits  | Name     | Access | Behavior | Default Set | Description  |
|-------|----------|--------|----------|-------------|--|
| [7:4] | Reserved |        |          | 0000        |  |
| [3:2] | UV_TH    | R/W    | Live     | 01          | 00:10%*V <sub>REF</sub><br>01:50%*V <sub>REF</sub><br>10:80%*V <sub>REF</sub><br>11:102.5%*V <sub>REF</sub>  |
| [1:0] | OV_TH    | R/W    | Live     | 01          | 00:115%*V <sub>REF</sub><br>01:120%*V <sub>REF</sub><br>10:125%*V <sub>REF</sub><br>11:130%*V <sub>REF</sub> |

The thresholds of UVP and OVP are relative values of the reference voltage.

**MFR\_OVP\_NOCP\_SET (D5h)**

The MFR\_OVP\_SET command sets the responses of the output voltage OVP and the input voltage OVP.

| Bits  | Name              | Access | Behavior | Default Set | Description  |
|-------|-------------------|--------|----------|-------------|--|
| [7:4] | Reserved          |        |          | 0000        |  |
| [3]   | DELAY_NOCP (D400) | R/W    | Live     | 0           | 0: 100ns delay after NOCP<br>1: 200ns delay after NOCP   |
| [2]   | NOCP              | R/W    | Live     | 0           | 0: Set NOCP to -10A.<br>1: Set NOCP to -15A.   |
| [1:0] | VOUT_OV_Response  | R/W    | Live     | 10          | 00: Latch-off with output voltage discharge<br>01: Latch-off without output voltage discharge<br>10: HICCUP with output voltage discharge<br>11: HICCUP without output voltage discharge |

The bit[1:0] of MFR\_VOUT\_OVP\_NOCP\_SET command tells the converter what action to take in response to an output over-voltage fault. The device also does the following:

- Sets the VOUT\_OV bit in the STATUS\_BYTE
- Sets the VOUT bit in the STATUS\_WORD
- Sets the VOUT over-voltage fault bit in the STATUS\_VOUT command
- Notifies the host by asserting ALERT pin

There are four OVP response modes. The mode can be chosen through bit[1:0] of MFR\_VOUT\_OVP\_NOCP\_SET:

- Latch-off with output discharge: Once it hits the OV entry threshold, the LSFET is ON until it hits NOCP, then it is OFF for a fixed time, and then it is ON again. It operates in this manner until FB drops below the OVP exit threshold set by register D4[3:2], then the LSFET is off. If FB rises above the OV entry threshold again, the LSFET is turned on again to discharge the output voltage. However, the converter won't attempt to restart until there is power recycle either in Vin, VCC, or CTRL.
- Latch-off without output discharge (only effective in DCM): Once it hits the OV entry threshold, the LSFET is ON. When the inductor current crosses zero, the converter enters high-z mode (output disabled). The converter stops discharging the output voltage. The converter won't attempt to restart until there is power recycle either in Vin, VCC, or CTRL.
- HICCUP with output discharge: Once it hits the OV entry threshold, the LSFET is ON until it hits NOCP, then it is OFF for a fixed time, and then it is ON again. It operates in this manner until FB drops below the OVP exit threshold set by register D4[3:2], and then the LSFET is OFF. A new SS will be initiated.
- HICCUP without output discharge: Once it hits OV, the LSFET is ON until it hits NOCP, then it initiates a new SS.

#### MFR\_OT\_OC\_SET (D6h)

This MFR\_OT\_OC\_SET command sets the responses of the OCP and the responses and hysteresis of the OTP. It's a 1 byte command.

| Bits  | Name        | Access | Behavior | Default Set | Description   |
|-------|-------------|--------|----------|-------------|---|
| [7:4] | Reserved    |        |          | 0000        |   |
| [3]   | OC_response | R/W    | Live     | 00          | 0:Latch-off, never retry<br>1:Retry   |
| [2:1] | OT_hyst     | R/W    | Live     | 00          | 00: 20°C<br>01: 25°C<br>10: 30°C<br>11: 35°C  |
| [0]   | OT_Response | R/W    | Live     | 0           | 0:Latch-off, never retry<br>1:Retry after the temp drops by the value set by bits [2:1] |

The MFR\_OT\_OC\_SET command tells the converter what kind of action to take in response to an over-temperature fault and a total output over-current fault.

#### MFR\_OC\_PHASE\_LIMIT (D7h)

The MFR\_OC\_PHASE\_LIMIT command sets the inductor valley current limit of each individual phase. This is a cycle-by-cycle current limit. After 31 consecutive cycles of OC, it triggers OCP. It's a 1 byte command.

| Bits  | Name     | Access | Behavior | Default Set | Description                         |
|-------|----------|--------|----------|-------------|-------------------------------------|
| [7:5] | Reserved |        |          | 000         |                                     |
| [4:0] | OC_limit | R/W    | Live     | 12h         | Current limit. 1.5A/LSB;[00000]=0A. |

The value is unsigned and 1LSB=1.5A. The default value is 27A.

#### MFR\_HICCUP\_ITV\_SET (D8h)

The MFR\_HICCUP\_ITV\_SET command sets the interval of HICCUP during OCP. It's a 1 byte command.

| Bits  | Name       | Access | Behavior | Default Set | Description                                 |
|-------|------------|--------|----------|-------------|---|
| [7:6] | Reserved   |        |          | 00          |   |
| [5:0] | Hiccup_itv | R/W    | Live     | 0           | OC fault hiccup interval time.<br>1 LSB=4ms |

### MFR\_PGOOD\_ON\_OFF\_LIMIT (D9h)

The MFR\_PGOOD\_ON\_OFF\_LIMIT command sets the thresholds for PGOOD on and off.

| Bits  | Name     | Access | Behavior | Default Set | Description  |
|-------|----------|--------|----------|-------------|--|
| [7:4] | Reserved |        |          | 0000        |  |
| [3:2] | PG_OFF   | R/W    | Live     | 01          | 00:69%*V <sub>REF</sub><br>01:74%*V <sub>REF</sub><br>10:79%*V <sub>REF</sub><br>11:84%*V <sub>REF</sub>     |
| [1:0] | PG_ON    | R/W    | Live     | 01          | 00:90%*V <sub>REF</sub><br>01:92.5%*V <sub>REF</sub><br>10:95%*V <sub>REF</sub><br>11:97.5%*V <sub>REF</sub> |

Any fault condition will pull PG low.

### MFR\_VOUT\_STEP (DAh)

The MFR\_VOUT\_STEP command sets the slew rate of the output voltage transition.

| Bits  | Name      | Access | Behavior | Default Set | Description   |
|-------|-----------|--------|----------|-------------|---|
| [7:4] | Reserved  |        |          | 0000        |   |
| [3:0] | Vout_step | R/W    | Live     | 0000        | 0000=20us/2mV<br>0001=22.5us/2mV<br>0010=25us/2mV<br>0011=27.5us/2mV<br>0100=30.2us/2mV<br>0101=32.5us/2mV<br>0110=35us/2mV<br>0111=37.5us/2mV<br>1000=40us/2mV |

### MFR\_LOW\_POWER (E5h)

The MFR\_LOW\_POWER is used to enable/disable the slave phase(s) in a multi-phase configuration.

| Bits  | Name     | Access | Behavior | Default Set | Description  |
|-------|----------|--------|----------|-------------|--|
| [7:2] | Reserved |        |          | 000000      |  |
| [1]   | LP_PS#   | R/W    | Live     | 0           | 0: Low power mode is disabled regardless of PS#.<br>1: Low power mode is enabled when PS# is low, and is disabled when PS# is high |
| [0]   | LP_PMBus | R/W    | Live     | 0           | 0: Low power mode is disabled<br>1: Low power mode is enabled  |

The slave phase(s) can be enabled/disabled directly through bit[0] of the MFR\_LOW\_POWER command. And when bit[1] of MFR\_LOW\_POWER is set to “1,” the slave phase(s) can be enabled/disabled by the PS# pin.

The master phase can't be disabled through the MFR\_LOW\_POWER command.

### MFR\_CTRL (EAh)

The bits of the MFR\_CTRL are used to enable/disable the functions below:

| Bits    | Name                     | Access | Behavior | Default Set | Description   |
|---------|--------------------------|--------|----------|-------------|---|
| [15:11] | Reserved                 | R      | Live     |             | For manufacturer use only                                     |
| [10]    | total_oc_hiccup_interval | R/W    | Live     | 0           | 0: Fixed OCP HICCUP interval<br>1: Adjustable OCP HICCUP      |
| [9]     | osm                      | R/W    | Live     | 0           | 0: Enable OSM (Output Sink Mode).<br>1: Disable OSM           |
| [8:4]   | reserved                 | R      | Live     |             | For manufacturer use only                                     |
| [3]     | phase_operation          | R/W    | Live     |             | 0: For single-phase operation<br>1: For multi-phase operation |
| [2:0]   | reserved                 | R      | Live     |             | For manufacturer use only                                     |

bit[10], bit[9] and bit[3] are user accessible for the MFR\_CTRL (EAh). The other bits are reserved for manufacturer use only.

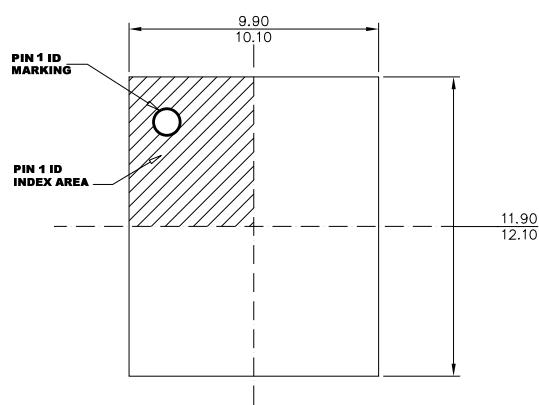
Bit[10] total\_oc\_hiccup\_interval: Chooses whether the interval during OCP HICCUP can be changed through register D8h.

Bit[9] osm enables or disables the Output Sink Mode (OSM) function.

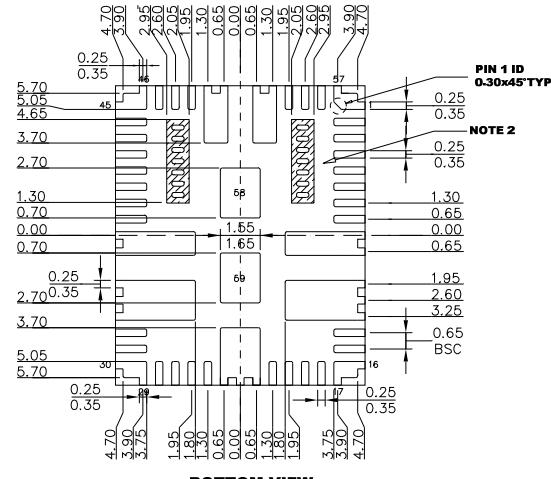
Bit[3] phase operation is used to choose single or multi-phase operation. The selection of this bit will affect the actual RAMP amplitude chosen through register D0h[3:1]. See register description of MFR\_CTRL\_COMP (D0h).

## PACKAGE INFORMATION

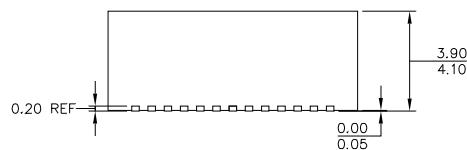
## QFN-59 (10mmx12mmx4mm)



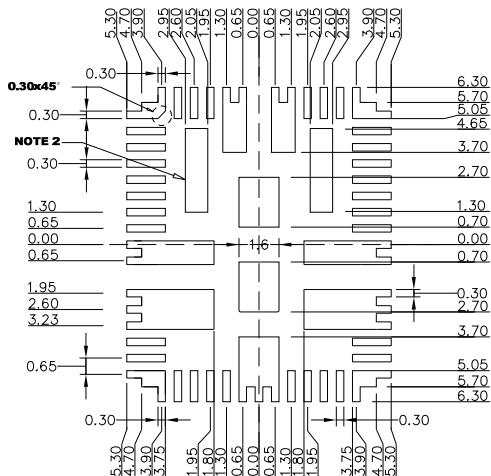
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

## NOTE

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

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