XR77103

Universal PMIC

Universal PMIC 3 Output Buck Regulator

April 2016 Rev. 1A

GENERAL DESCRIPTION

The XR77103 features three synchronous wide input range high efficiency buck converters. Each converter is digitally programmable requiring minimal external components thus providing the smallest size solution possible.

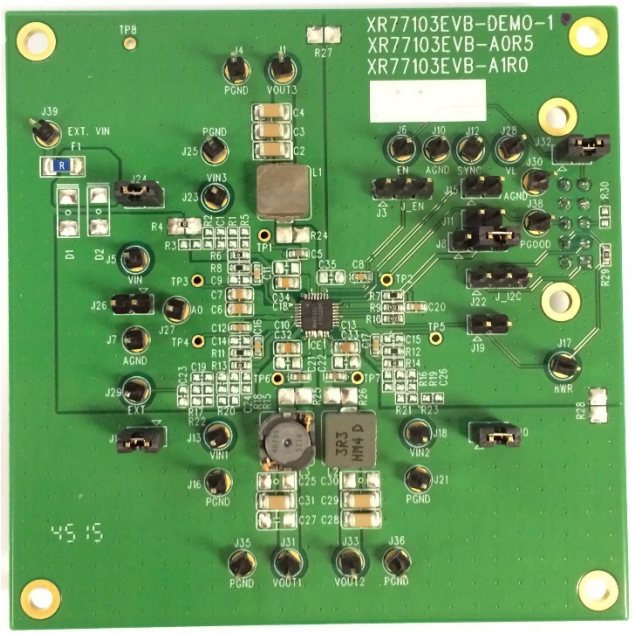
The converters can operate in 5V, 9V, and 12V systems and have integrated power switches. The output voltage of each converter can be adjusted by programming the values in the VOUT setting registers through I^2C interface. The adjustable range is 0.8~6V with 50mV resolution. The output voltage also can be set externally using an external resistor divider. Output sequence among the outputs, soft-start time and the peak inductor current limit are also set through I^2C.

The switching frequency of the converters can either be set with I^2C or can be synchronized to an external clock connected to SYNC pin if needed. The switching regulators are designed to operate from 300kHz to 2.2MHz. Each converter operates in phase or out of phase according to the value in the phase setting register. This can minimize the input filter requirements.

XR77103 features a supervisor circuit that monitors each converter output. PGOOD pin is asserted once sequencing is done, all outputs are reported in regulation, and the reset timer expires. The polarity of the signal is active high.

XR77103 also features a light load pulse skipping mode (PSM). It is set through I^2C. The PSM mode allows for a reduction on the input power supplied to the system when the host processor is in stand-by mode (low activity) mode.

EVALUATION BOARD MANUAL



FEATURES

- 4.5V to 14V wide input supply voltage range
- Built-In MOSFET & Synchronous rectifier
- I^2C programmable supplies
  - Output voltage (0.8~6V)
  - Power on sequence
  - Soft start timing
  - Switching frequency (300kHz~2.2MHz)
  - Individual current limit
  - Optional power saving mode at light loads
- Non Volatile Memory (NVM) with up to 10,000 times write operation.
- 0.8V, high accuracy reference (1%)
- Current-mode control with simple compensation circuit
- External synchronization
- Power Good
- Protection
  - Thermal shutdown
  - Overvoltage transient protection
  - Over current protection

  32pin TQFN package, 4mm x 4mm

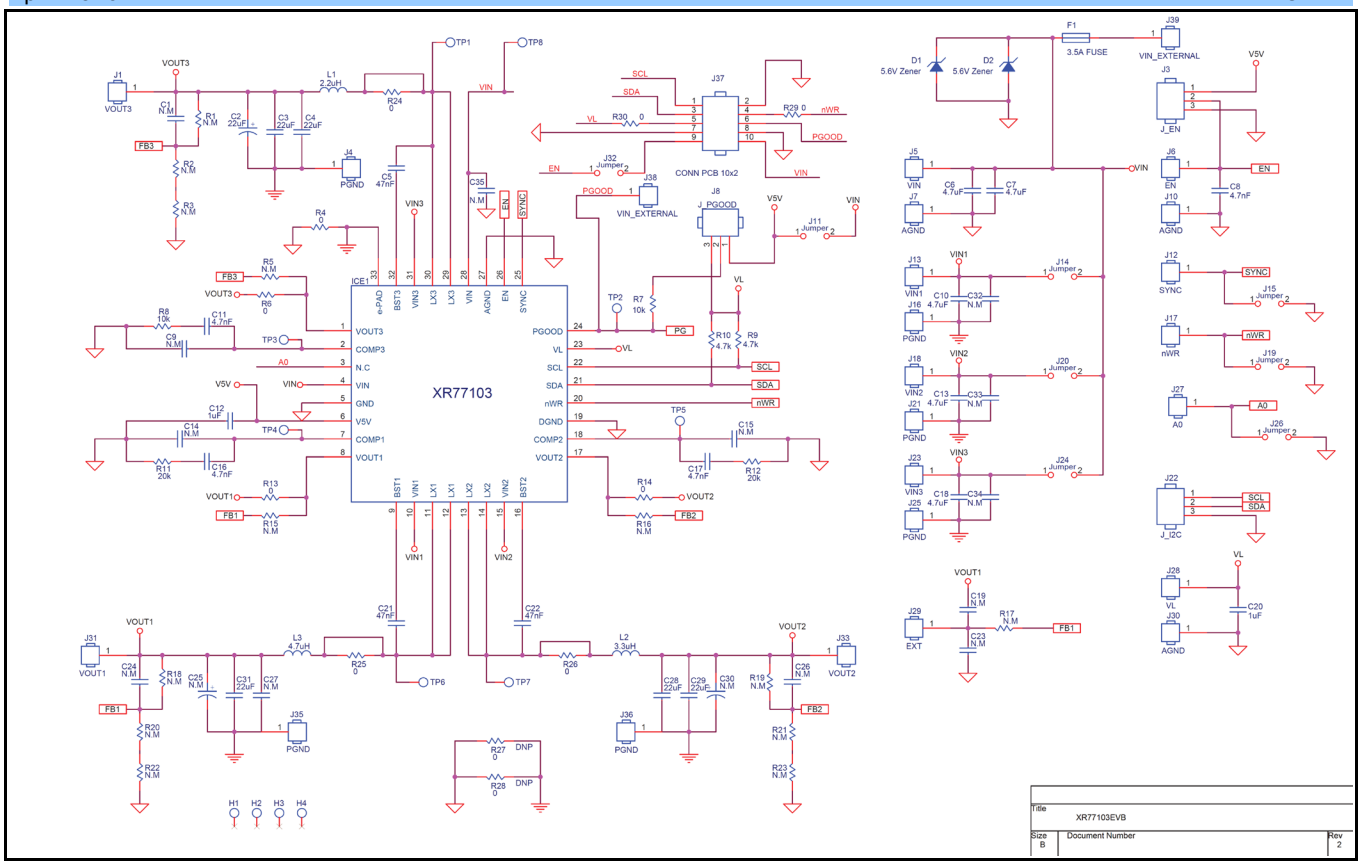


Figure 1: XR77103 Evaluation Board Schematics

PIN ASSIGNMENT

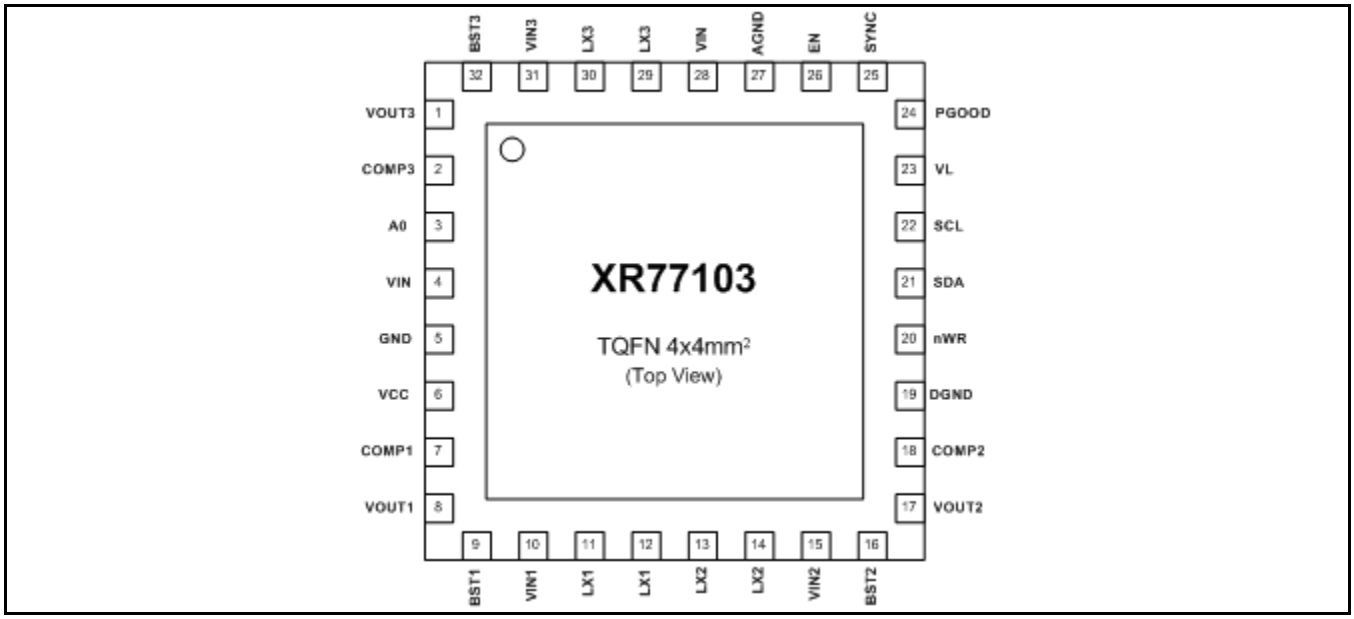


Figure 2: XR77103 Pin Assignment

PIN DESCRIPTION

Name	Pin Number	Description
VOUT3	1	Buck 3 output sense pin
COMP3	2	Compensation pin for Buck 3. Connect a series RC circuit to this pin for compensation.
A0	3	I^2C Address Select Pin. A0 is internally pulled HIGH through a 100kΩ pull up resistor.
VIN	4	IC supply pin. Connect a capacitor as close as possible to this pin.
GND	5	Ground
VCC	6	Internal supply. Connect a ceramic capacitor from this pin to ground.
COMP1	7	Compensation pin for Buck 1. Connect a series RC circuit to this pin for compensation.
VOUT1	8	Buck 1 output sense pin
BST1	9	Bootstrap capacitor for Buck 1. Connect a bootstrap capacitor from this pin to LX1.
VIN1	10	Input supply for Buck 1. Connect a capacitor as close as possible to this pin.
LX1	11	Switching node for Buck 1
LX1	12	Switching node for Buck 1
LX2	13	Switching node for Buck 2
LX2	14	Switching node for Buck 2
VIN2	15	Input supply for Buck 2. Connect a capacitor as close as possible to this pin.
BST2	16	Bootstrap capacitor for Buck 2. Connect a bootstrap capacitor from this pin to LX2.
VOUT2	17	Buck 2 output sense pin
COMP2	18	Compensation pin for Buck 2. Connect a series RC circuit to this pin for compensation.
DGND	19	Digital Ground
nWR	20	Write Protection Input for NVM. The Data can be written to NVM when this pin is low. This pin is internally pulled high through 100kΩ pull up resistance.
SDA	21	Data I/O Pin for I^2C Serial Interface.
SCL	22	Clock Input Pin for I^2C Serial Interface.
VL	23	Supply Pin for I^2C interface. Supply 3.3V typically for I^2C communication.
PGOOD	24	Power Good output. Open drain output asserted after all converters are sequenced and within regulation.
SYNC	25	External clock input pin. Connect to signal ground when unused.
EN	26	Enable Control Input. Set EN high to enable converters.
AGND	27	Analog ground
VIN	28	IC supply pin. Connect a capacitor as close as possible to this pin.
LX3	29	Switching node for Buck 3
LX3	30	Switching node for Buck 3
VIN3	31	Input supply for Buck 3. Connect a capacitor as close as possible to this pin.
BST3	32	Bootstrap capacitor for Buck 3. Connect a bootstrap capacitor from this pin to LX3.
E-PAD	-	Connect to Power ground

ORDERING INFORMATION

Refer to XR77103 datasheet and/or www.exar.com for exact and up to date ordering information.

USING THE EVALUATION BOARD

INPUT VOLTAGE RANGE

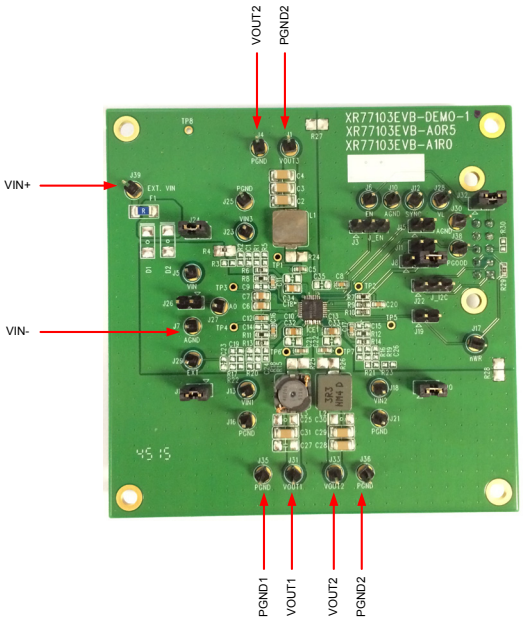
The input voltage range is 5.5V to 14V. The power components have been optimized for a 12V input rail.

I²C INTERFACE

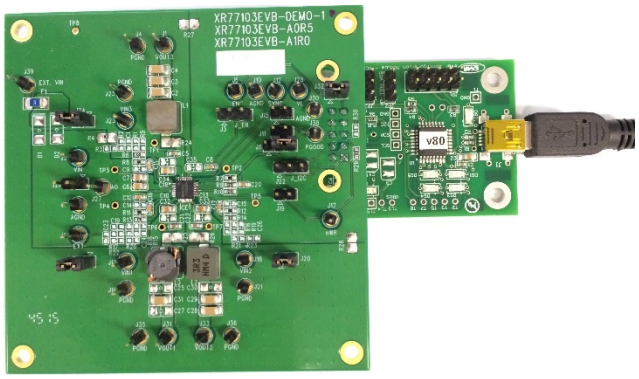
The XR77103 programmable power controller employs a standard I2C interface. The interface lines (SCL and SDA) are pulled up on board to the V_L rail which needs to be supplied externally between test points J28 (V_L) and J30 (AGND). If the pull-up resistor are used on the master side (on XCM configuration module for example), the pull-up resistors on the evaluation board, R9, R10 and the pull-up rail bypassing capacitor C20 need to be removed.

POWERING UP

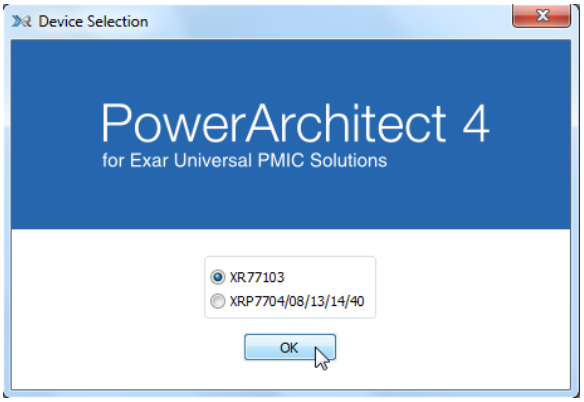
Connect the VIN+/VIN- with short leads to power supply. Use test pins EXT. VIN (J39) and AGND (J7) to connect VIN+ and VIN- to the EVB respectively. Connect VOUTx/PGNDx test points (J31 VOUT1, J35 PGND1, J33 VOUT2, J36 PGND2, J1 VOUT3, J4 PGND3) with short leads to an electronic load. Use test pins VOUTx and PGNDx to monitor VOUTx+ and VOUTx- respectively.



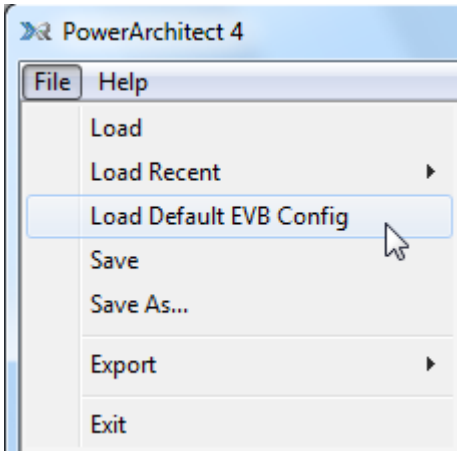
Connect the XR77103EVB-DEMO-1 evaluation board to the XCM controller board as shown below.



Load Power Architect 4.24 or later and run it.



After selecting the proper family (device), go to File menu and load the default EVB configuration.



XR77103EVB-DEMO-1 will already be programmed with the same configuration. This default configurations sets the switching frequency at 500kHz, UVLO setting at 7V, enables the low power mode of operation, sets channels 2 and 3 180°out of phase so they could be paralleled (hardware modifications needed in addition for this configuration), sets output voltages at 3.3V, 1.8V and 1.2V on channels 1, 2, 3 respectively, sets peak inductor current limit at 3.5A, start-up delay at 10ms and ramp up time at 6ms for all channels.

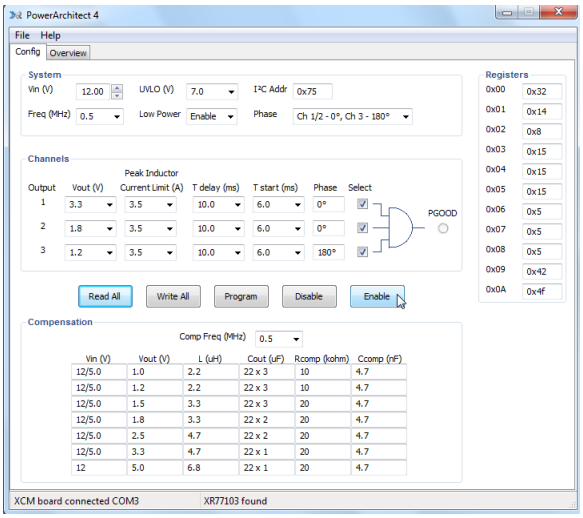
Apply 12V using the power supply. Make sure J14, J20 and J24 have jumpers installed to provide VIN to individual regulators.

Apply 3.3V to V_L between test points J28 (V_L) and J30 (AGND).

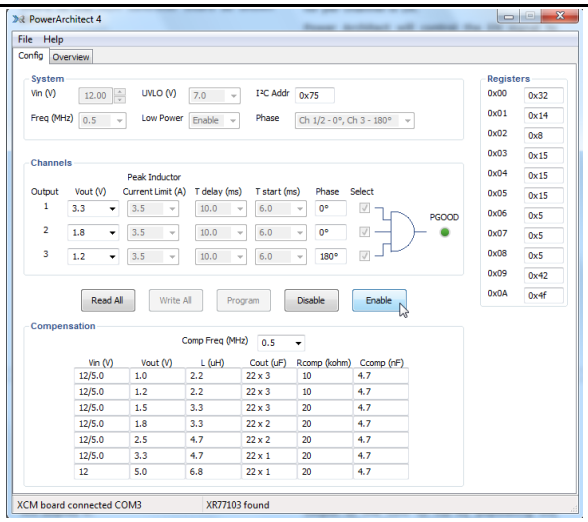
Use USB cable to connect the computer (type A) and the XCM controller board (type mini B).

The XR77103EVB-DEMO-1 is configured to regulate the output at 3.3V, 1.8V and 1.2V at channels 1, 2, and 3. Maximum rated current for per channel is 2A.

Power Architect will control the EN signal to the evaluation board. To enable channels click the Enable button.



Power Architect will poll PGOOD regularly and will display it.



JUMPER J3

This jumper controls the EN pin. Its default position is open and controlled by Power Architect. It is not recommended strapping the EN pin to 5V VCC or GND while connected to XCM. J32 connects/disconnects EN from XCM.

JUMPER J8

This jumper controls the pull up of the PGOOD signal. The default position is between pins 2 and 3 in which case PGOOD is pulled up to 3.3V V_L supply (supplied between J28 – V_L and J30 – AGND). It is not recommended pulling PGOOD to 5V VCC while connected to XCM due to signaling level limitation of the micro controller.

OPERATION FROM A 5V RAIL (V_{IN}=4.5V-5.5V) J11

For operation from a 5V rail it is required tie output of the LDO to V_{IN} by populating the jumper J11. This enhances the operation of the drivers at V_{IN}<5V.

Please remember to remove R11 for operation at higher V_{IN}. The board also has place holders for Zener diodes which can be installed to protect the IC if higher Vin is accidentally applied.

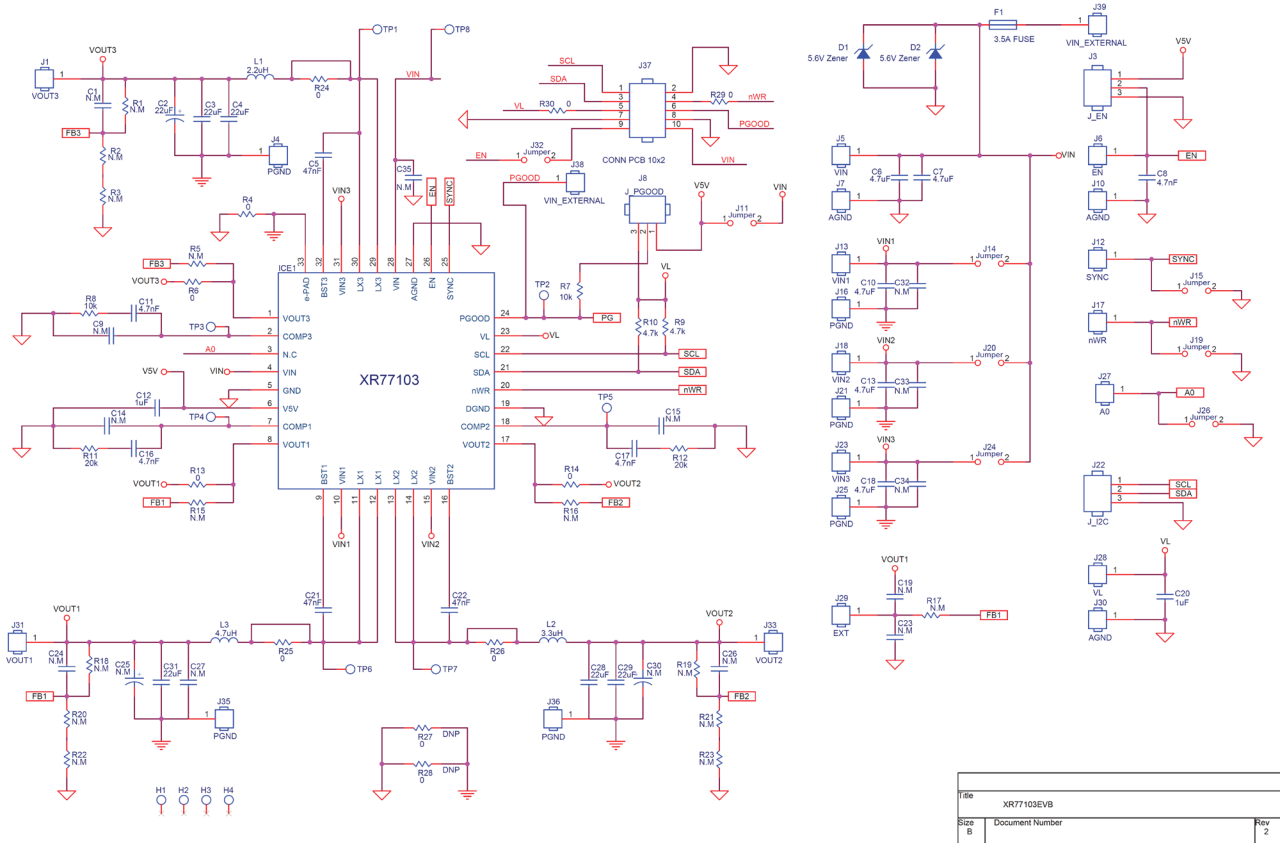
PROGRAMMING THE OUTPUT VOLTAGE

Vout is programmed from Power Architect through the I^2C interface.

Alternatively, V_{OUT} can be programmed by changing resistor divider at the output according to:

$$Rtop = Rbottom \times \left(\frac{V_{OUT}}{0.8} - 1\right)$$

EVALUATION BOARD SCHEMATICS



XR77103EVB-DEMO-1 BILL OF MATERIALS

Reference Designator	Qty.	Manufacturer	Manufacturer Part Number	Size	Component
PCB	1	Exar	XR77103		XR77103 EVB PCB
U1	1	Exar	XR77103		
L1	1	VISHAY	IHLP2525CZER2R2M01	6.86 x 6.47mm	Inductor 2.2uH 6A 30mOHM SMD
L2	1	EATON	HCM0703-3R3-R	6.86 x 6.47mm	Inductor 3.3uH 6A 30mOHM SMD
L3	1	TDK	CLF7045NIT-4R7N	7.40x7.40mm	Inductor 4.7uH 4.1A 18mOHM SMD
C2, C3, C4, C28, C29, C31	6	MURATA	GRM31CR61C226KE15K	1206	CAP CER 22UF 16V X5R 1206 10%
C5,C21,C22	3	MURATA	GRM188R71H473KA61D	0603	CAP CER 47nF 50V X7R 10%
C6,C7,C10,C13,C18	5	MURATA	GRM21BR71E475KA73L	0805	CAP CER 4.7uF 25V X7R 10%
C8, C11,C16,C17	4	MURATA	GRM188R71H472KA01D	0603	CAP CER 4.7nF 50V X7R 10%
C12, C20	2	MURATA	GRM188R71A105KA61D	0603	CERAMIC CAP., 1uF, 10V, X7R, 10%
R4, R6, R13, R14, R29	5	PANASONIC	ERJ-3GEY0R00V	0603	Resistor 0.00 Ohm, Jumper, 1/10W, SMD
R7, R8	2	PANASONIC	ERJ-3EKF1002V	0603	Resistor 10.0K Ohm, 1/10W,1%,SMD
R9, R10	2	PANASONIC	ERJ-3EKF4701V	0603	Resistor 4.7K Ohm, 1/10W,5%,SMD
R11,R12	2	PANASONIC	ERJ-3EKF2002V	0603	Resistor 20.0K Ohm, 1/10W,1%,SMD
F1	1	Vishay	MFU1206FF03500P100	1206	Fuse Board Mount 3.5A,63VDC
J1, J4, J5, J6, J7, J10, J12, J13, J16, J17, J18, J21, J23, J25, J27, J28, J29, J30, J31, J32, J33, J35, J36, J38, J39	25	Wurth Elektronik	61300111121	2.54mm	Header 1 pin
J3, J8, J22	3	Wurth Elektronik	61300311121	2.54mm	Header 3 pin
J11, J14, J15, J19, J20, J24, J26	7	Wurth Elektronik	61300211121	2.54mm	Jumper 2 pin
J37	1	Wurth Elektronik	61301021821	2.54mm	2.54mm Dual Socket Header

EVALUATION BOARD LAYOUT

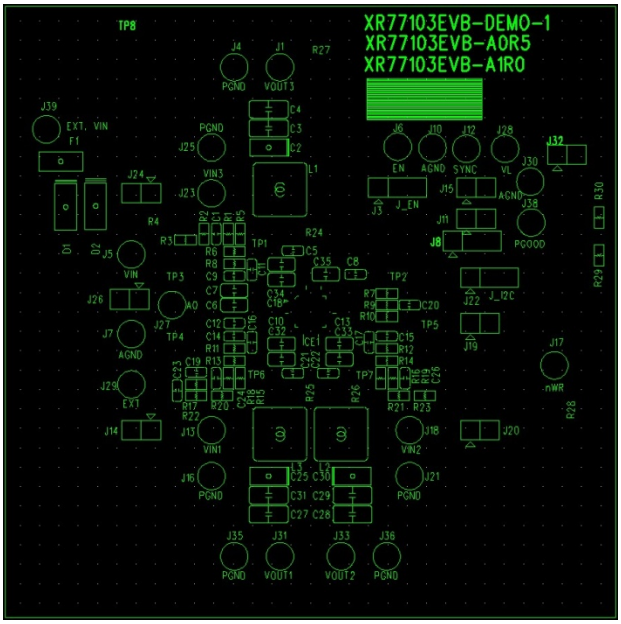


Figure 3: Assembly Top

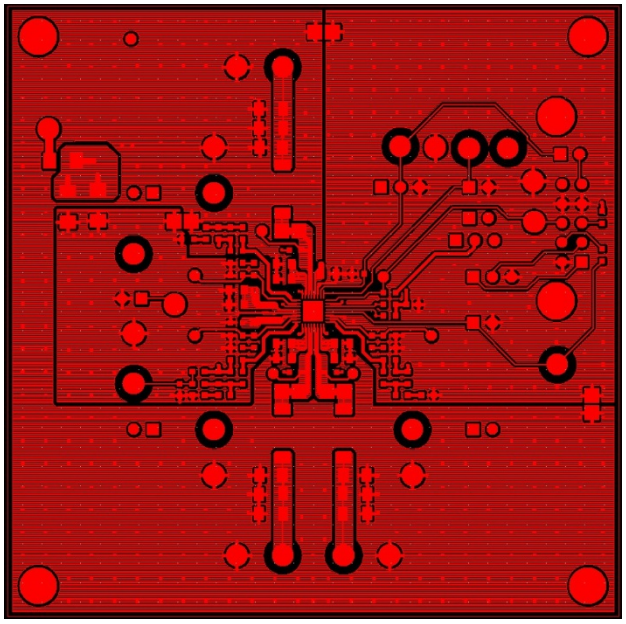


Figure 4: Top

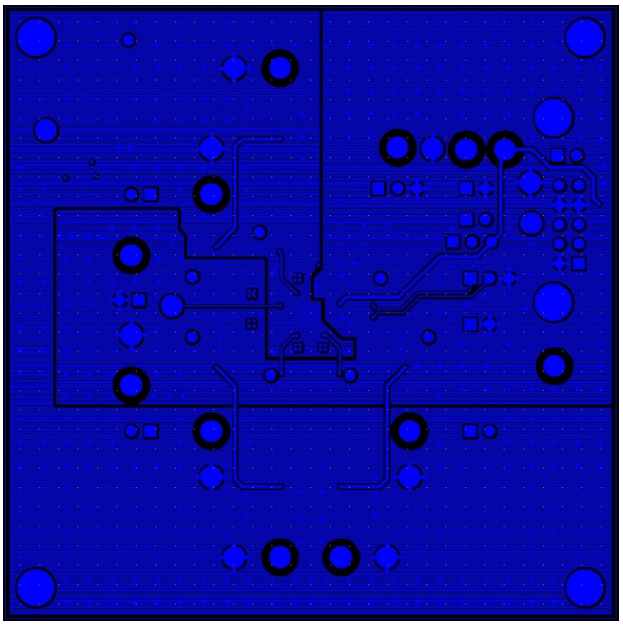


Figure 5: Bottom

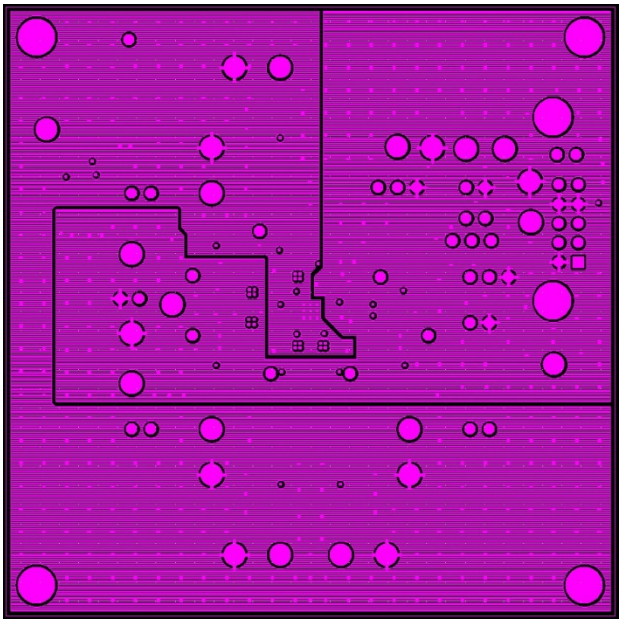


Figure 6: Layer 2

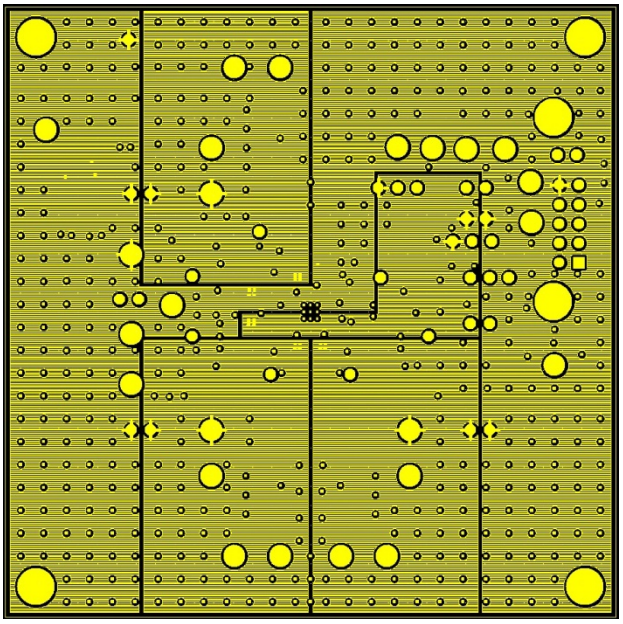


Figure 7: Layer 3

DOCUMENT REVISION HISTORY

Revision	Date	Description
1A	04/21/16	Initial release of document

BOARD REVISION HISTORY

Board Revision	Date	Description
REV. 2.0	09/21/15	Initial release of evaluation board

FOR FURTHER ASSISTANCE

Email: customersupport@exar.com

powertechsupport@exar.com

Exar Technical Documentation: www.exar.com/technical-documentation

EXAR CORPORATION

HEADQUARTERS AND SALES OFFICES

48720 Kato Road

Fremont, CA 94538 – USA

Tel.: +1 (510) 668-7000

Fax: +1 (510) 668-7030

www.exar.com

NOTICE