Creating a Negative Output Voltage Using a Buck Converter

By Owain Bryant

Vishay constant on-time (COT) converters combine high-efficiency regulation with extremely small transient response time and simple designs. The COT converters can also be configured in a buck-boost topology, allowing for a negative output voltage. This application note looks at the SiP12116 configured as a negative output buck converter.

INTRODUCTION

The buck topology is conventionally used to convert a larger bus or system voltage into a smaller voltage. The advantage of using a buck converter is that efficiency is very high when compared to a linear regulator performing the same conversion.

In order to generate a negative output voltage from a positive input voltage, the designer would usually opt for the buck-boost topology or possibly a SEPIC converter, both of which offer reasonable efficiency that is much higher than a linear regulator. However, the same outcome can be reached with a buck converter. With a slight alteration to the nodal references of a synchronous buck converter, we can create a negative boost converter, as shown in Fig. 1.

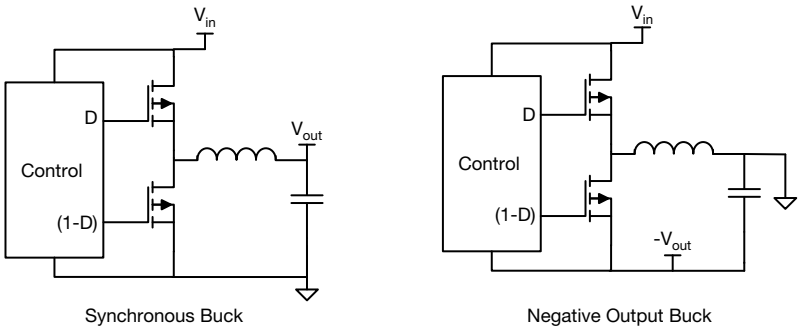

Fig. 1

This will suit applications that need to generate complimentary output voltages, such as audio, or industrial applications requiring negative voltage levels, such as IGBT gate drive turn-off. Other uses have been observed in LCD displays and embedded applications, where some application-specific ICs require a negative supply. This circuit offers the advantages of the positive output buck converter in the sparsely supported negative output switching regulator application.

CIRCUITRY

The circuitry is built around the SiP12116 synchronous buck converter, which has a fixed frequency of 600 kHz and offers a simple design with outstanding efficiency. The SiP12116 comes in a DFN 3 x 3 package, which offers the designer a compact footprint. The use of COT topology allows the user to develop a very straightforward power supply with no compensation requirements. The SiP12116 develops the current ramp feedback from the internal low-side MOSFET so the external components required are the power LC filter, input capacitive decoupling, and bootstrap capacitor.

The circuit uses the same design equations that can be found in the SiP12116 user guide. In fact, the circuitry uses the same parts; the input capacitors are rated to 25 V, so these are suitable. Care must be taken to ensure the voltage rating of the part is followed. For example, if the input voltage of the circuit is 12 V and the output voltage is 5 V, the differential voltage across the part is 17 V, which does not exceed the recommended 18 V. A Zener diode will also be used to clamp the enable pin to 4.7 V, which should safeguard the part at switch on and off while allowing for easy enable.

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OPERATION OF CIRCUIT

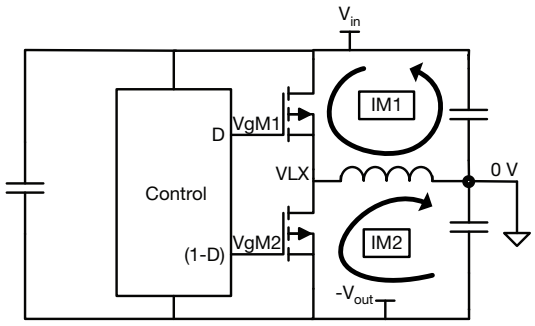

Fig. 2 - Negative Output Buck Topology

The control of the circuit will be identical to that of the standard buck converter; however, there is a key difference in that the change in nodal connection of the Inductor from V_{out} to 0 V will cause a change in circuit current flow. This in turn allows the negative output voltage to be generated; the IC's 0 V now becomes the negative output voltage.

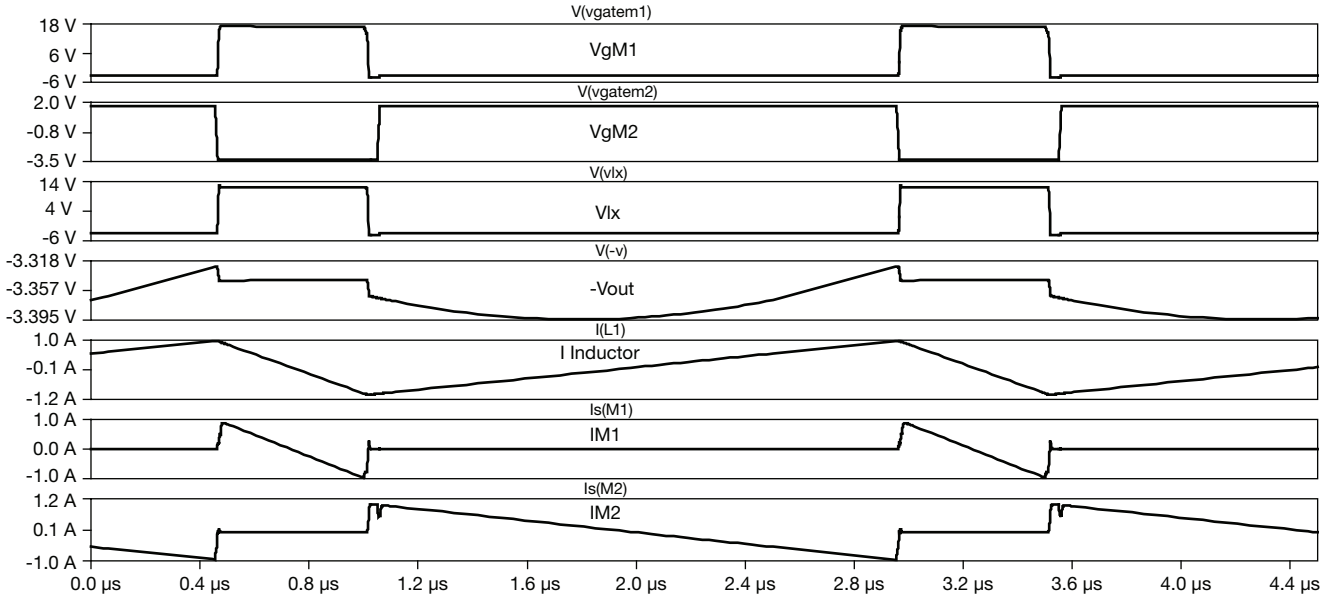

Fig. 3 - Simulation of Nodal Waveforms from Fig. 2

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The MOSFET drive waveforms can be seen in Fig. 3, which are similar to a standard buck converter. The LX voltage is also shown. LX waveforms range from -3.3 V to +12 V, and the majority of the magnitude is from -3.3 V to 0 V when the low-side MOSFET is on. The next trace represents the output voltage -3.3 V.

The inductor current can be seen next, which is centered around 0 A; there is no load in the simulation. The key waveforms appear next - IM1 and IM2 - which indicate the current flow in the circuit. Note that these waveforms are referenced to 0 V.

Current flows from +V to 0 V through the high-side MOSFET; however, the current is flowing from positive to negative, so it is decreasing, as can be seen in the IM1 trace. When M1 is switched off and M2 switched on, the current flows from -V to 0 V. This is seen in the increasing current, while MOSFET M2 shows a decreasing current due to the reference point of 0 V.

In order to determine the duty cycle, the similarity with the buck converter is maintained. However, the voltage across the inductor will now be $V_{in} + |V_{out}|$,

$$D = \frac{V_{out}}{V_{in} + |V_{out}|}$$

The remaining calculations are similar to a standard buck converter.

DESIGN CALCULATIONS

The overall design specifications for the circuit are as follows:
V_{in} = 12 V, V_{out} = -3.3 V, f_{sw} = 600 kHz, I_{out} = 3 A, V_{ripple} = 150 mV, and V_{in_ripple} = 100 mV.

The SiP12116 senses the current across the low-side MOSFET, so this signal needs to be reasonably large in order to stand out from any system noise that may be present. The method for this is to use a large ripple current, set to 40 % of the load current. This will also allow the user to downscale the size of the inductor. It is worth noting at this point that the calculations for the controller are relatively straightforward as the system runs with a COT topology, while also controlling current internally, derived through the low-side MOSFET, leaving few external parts that need design calculations.

TABLE 1 - DESIGN CALCULATIONS

Duty cycle	$D = \frac{V_{out}}{V_{in} + \lvert V_{out}\rvert}$	0.22
Inductance	$L = \frac{V_{in} \times D}{(f_{sw} \times \Delta I_L)}$	3.3 µH
Output capacitance	$C_{out} = \frac{(I_{LOAD} \times D)}{f_{sw} \times \Delta \lvert V_{out}\rvert}$	10 µF
Input capacitance	$I_{RMS} = I_{LOAD} \times \sqrt{D \times (1 - D)}$	1.24 A
	$C_{IN} = I_{RMS} \times \frac{D}{(\Delta V_{in} \times f_{sw})}$	10 µF

The calculations can be made and carried through as seen in Table 1. Note that some of the values have been translated to the available manufacturing values.

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CIRCUIT SCHEMATIC

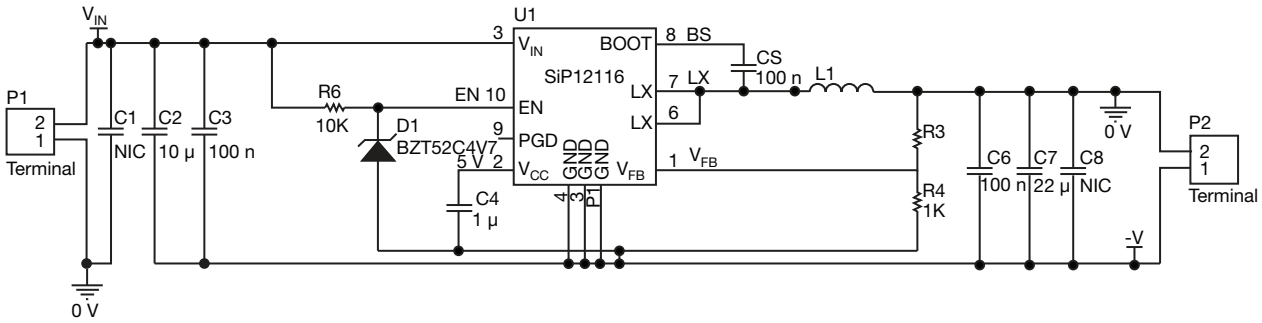

Fig. 4 - Schematic

The schematic represents the changes to the nodal reference with V_{out} becoming 0 V and 0 V becoming V_{out}. One must ensure there is decoupling across the input to 0 V, and some decoupling across the input to -V_{out}. The PCB design and BOM can be found in the appendix.

TYPICAL WAVEFORMS

Transient Response

Fig. 5 - Green = Load Current,
Purple = V_{out} Ripple Voltage, +240 mV, -80 mV

The transient response has a recovery spike of 300 mV; this is reasonable considering the 22 µF of holdup capacitance at the output. The current step is well controlled.

Voltage Ripple

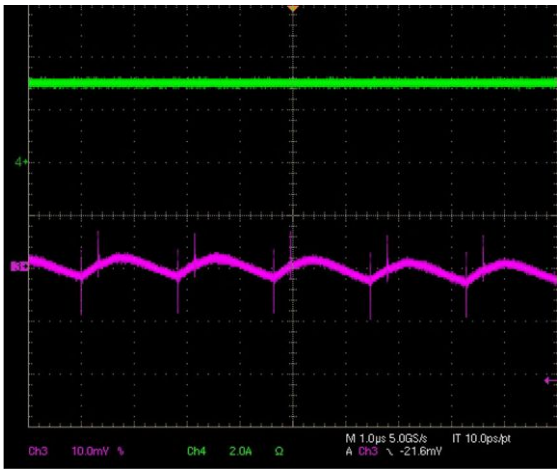

Fig. 6 - Green = I_{Load} 2 A / div,
Purple = V_{out} Ripple 10 mV / div

The voltage ripple is very well contained; no more than 80 mV can be observed for an output capacitance of 22 µF. This is helped by the high switching frequency.

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Voltage Rise on Start-Up

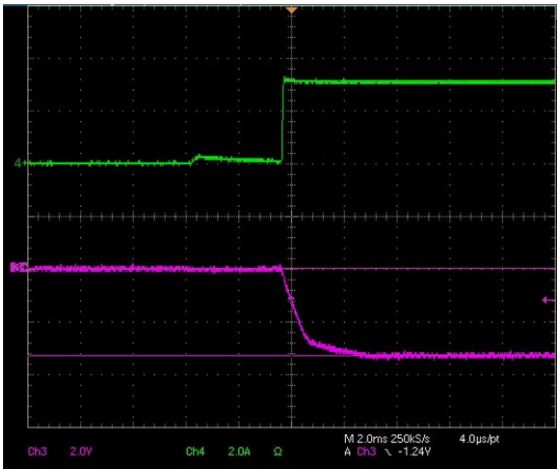

Fig. 7 - Green = I_{Load} 2 A / div,
Purple = V_{out} 2 V / div

It can be seen in Fig. 7 that the voltage rise time is monotonic into a 3 A load. This is well controlled.

Temperature Performance

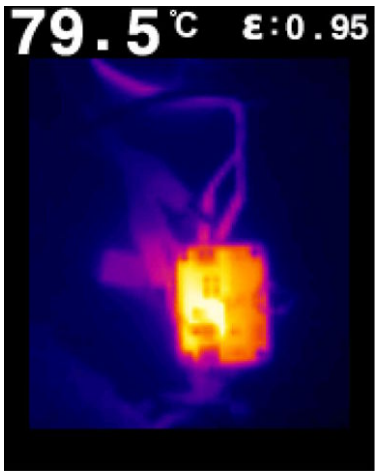

Fig. 8 - Temperature Measurement

Note: the part is running at 3.3 V, 3 A continuously. The ambient temperature is 24 °C.

This gives the user a temperature rise of 55.5 °C, which works out as 5.6 °C/ or 18.5 °C/A.

Efficiency and Power Loss

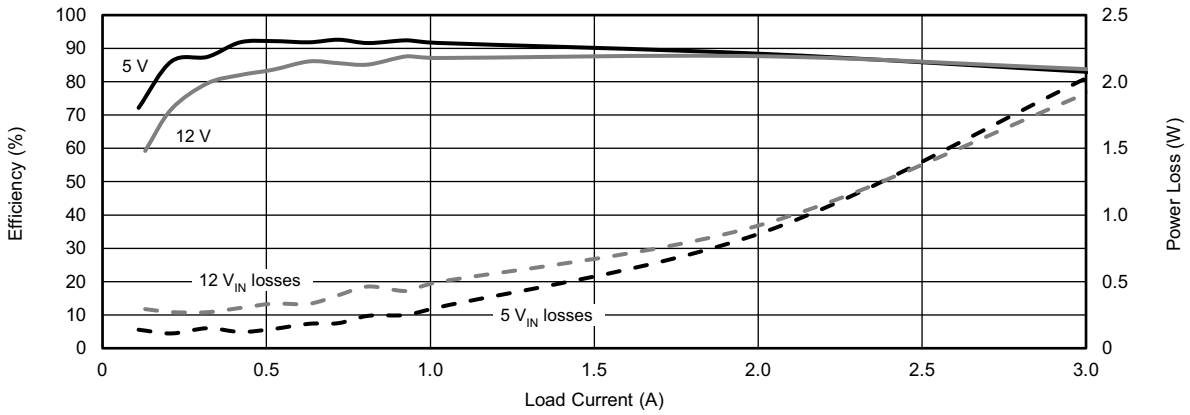

Fig. 9 - Efficiency Measurements
Test Conditions: V_{IN} = 12 V, 5 V, V_{OUT} = -3.3 V, f_{sw} = 600 kHz, L = 3.3 µH

CONCLUSION

The SiP12116 offers an ideal way of creating a high-performance negative voltage output from a positive supply. If the designer follows the rules, a maximum input voltage of 12 V can supply a 5 V output, or in this application a 3.3 V output. Peak efficiency is just over 90 % and the temperature rise for the evaluation PCB at ambient is 55 °C.

A reference design including schematics, layout, and complete BOM for a negative buck regulator using the SiP12116 is available by request by submitting a product support request here: www.vishay.com/ppg?62969.

References:

1. SiP12116 datasheet: www.vishay.com/doc?62969

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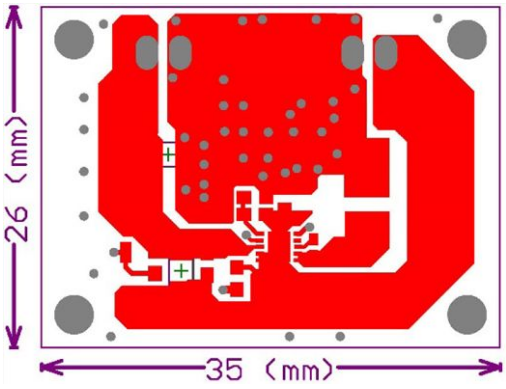
APPENDIX A

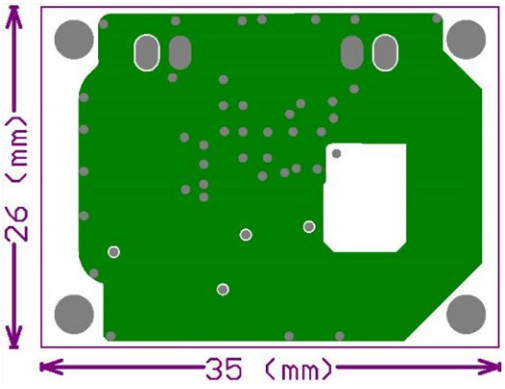
TABLE 2 - BILL OF MATERIALS FOR SiP12116 NEGATIVE OUTPUT VOLTAGE
(V_{in} = 12 V, V_{out} = 3.3 V, f_{sw} = 600 kHz)

ITEM	QUANTITY	REFERENCE	PCB FOOTPRINT	VALUE	VOLTAGE	PART NUMBER	MANUFACTURER
1	2	C1, C2	1210	10µ	35 V	C1210C106M6PACTU	KEMET
2	2	C3, C6	0402	10n	50 V	GRM155R71H103KA88D	MURATA
3	1	C4	0603	1µ	10 V	C0402C105M8PACTU	KEMET
4	1	C5	0402	100n	50 V	CGA2B3X7R1V104K050BB	VISHAY
5	1	C7	0805	22µ	10 V	CL21A226MPQNNNE	SAMSUNG
6	1	R3	0402	4K53	-	CRCW04024K53FKED	VISHAY
7	1	R4	0402	1K	-	CRCW04021K00FKED	VISHAY
8	1	L1	IHLP2525	3µ3	-	IHLP2020BZER3R3M01	VISHAY
9	1	U1	DFN10-3x3	-	-	SiP12116	VISHAY
10	1	D1	SOD-123	4V7	-	BZT52C4V7	-
11	2	P1, P2	TERM2	-	-	282834-2	TE CONNECTIVITY

PCB LAYOUT



Top Layer



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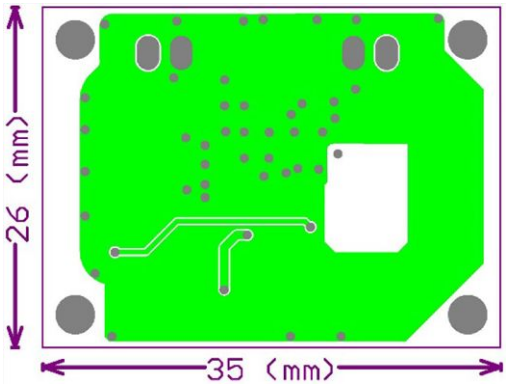

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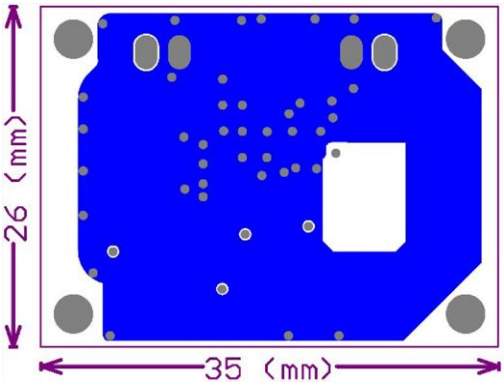

Bottom Layer

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