Measurement and comparison of thermal properties of case forms D^{2}PAK and PowerPAK 8x8L

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Introduction

As a result of the continuing miniaturisation of electronic power circuits, heat dissipation has come to play an increasingly important role. The following text relates the thermal properties of various MOSFET case forms to circuit board space requirements. This is intended to allow users to better assess the suitability of MOSFETs with regard to applications requiring circuit footprints which are subject to size restrictions. Tests are performed on two MOSFETs joined to create a half-bridge in order to facilitate the transfer of the results obtained to real-life application scenarios, e.g. inverter output stages.

Theoretical Overview

The conventional approach to thermal characterisation of FETs is to quote the thermal resistance R_{th} between the active semi-conductor junction and the case R_{thJC} or the ambient medium to which heat is dissipated R_{thJA}. The thermal resistance expresses the temperature difference ΔT required to dissipate a power output P from the component. These figures define the thermal performance of the component in question but do not provide any definitive indication as to which component is most effective in dissipating heat in respect of the circuit board surface area used.
In order to perform a quantitative assessment of this aspect, the heat transfer coefficient h_{JA} is considered with the unit $\left[\frac{W}{m^2K}\right]$. This expresses the heat transfer at a given temperature spread in relation to the footprint of the component under review. The higher the value, the greater the heat dissipation given the same temperature spread and footprint. This renders this parameter a basis for decision making, in particular in selecting components for electronic circuits with limited available space and pre-defined heat sinks.

Experimental Setup

By way of an example, the following R_{thJA} and h_{JA} determines values on the basis of experiments on a half-bridge and compares these with the results for case forms D^{2}PAK (SQM60030) and PowerPAK 8x8L (SQJQ480E). For this purpose, two N-channel MOS-

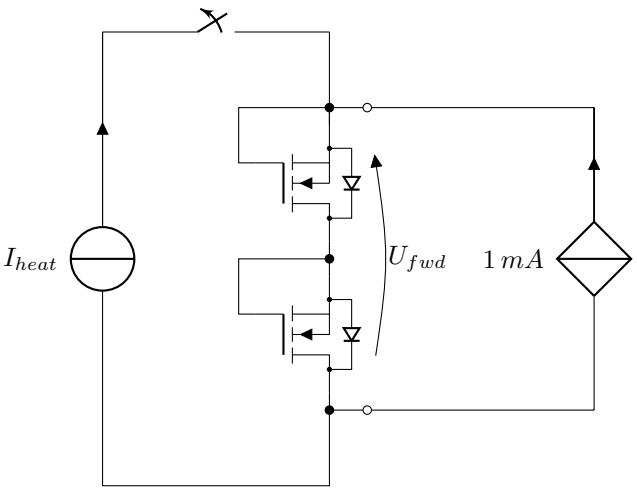
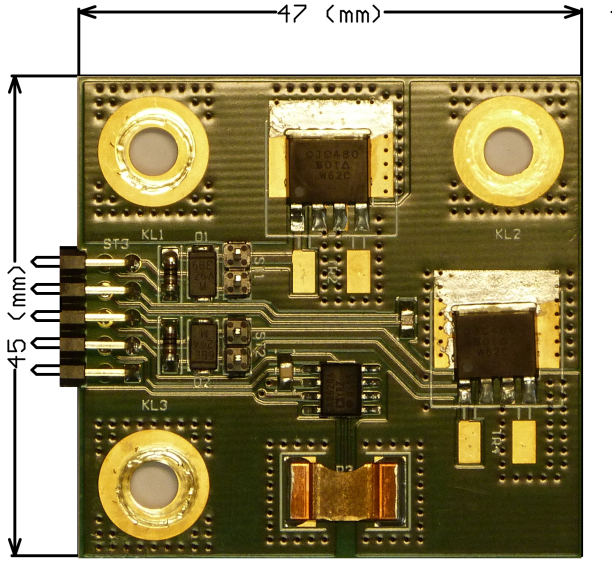


Figure 1: Basic circuit to measure junction temperature of a half-bridge.

FETs each were joined to create a half-bridge in the manner illustrated in Fig. 1. The two copper surfaces on either side as shown in Fig. 3 with a surface of approx. 3180 mm^2 were coated in solder resist and attached to FR4. This equates to a cooling surface area of approx. 1590 mm^2 or approx. 2.46 in^2 per MOSFET. However, as the circuit boards were tested lying flat against a smooth surface with poor heat-conducting properties, the active cooling surface areas must be presumed to be 795 mm^2 or 1.23 in^2 per MOSFET. The solder surfaces of the circuit boards are designed in such a way as to allow both case forms to be tested on identical circuit boards. This guarantees a precise comparison of cooling surfaces. During the tests, the circuit boards were laid flat on a level surface. As there is no active ventilation, it must be presumed that all heat is dissipated through natural convection.

The determination of the junction temperature utilises the fact that the forward voltage of the body diode has a characteristic temperature correlation. With the aid



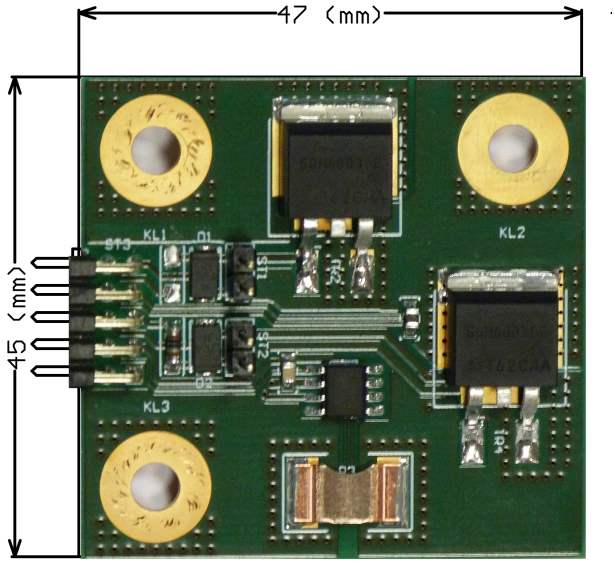
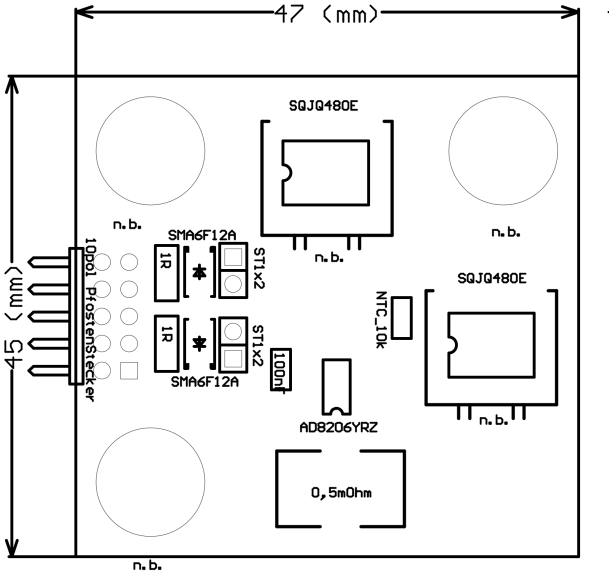
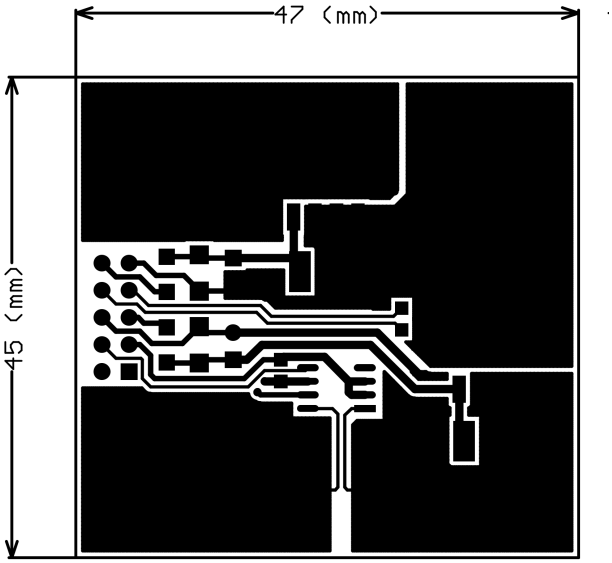


Figure 2: Circuit board used for thermal characterisation. The circuit boards can be optionally populated with either D^{2}PAK or PowerPAK 8x8L cases.





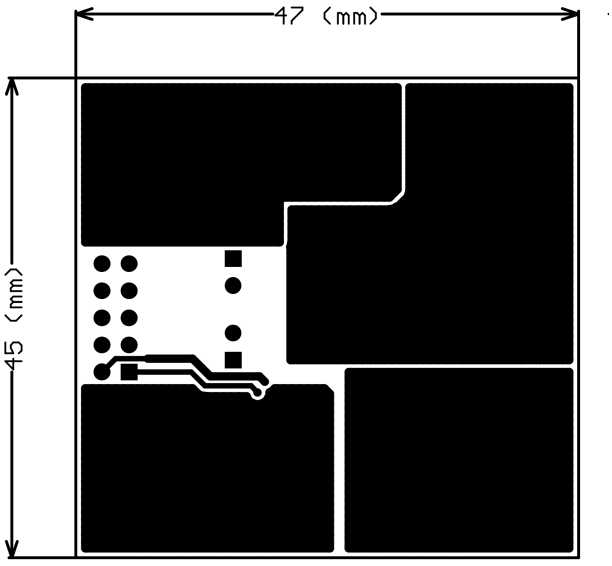


Figure 3: Copper surfaces of circuit board. The cooling surface area available for each MOSFET is approx. 1590 mm^2 or approx. 2.46 in^2

	20.2 °C	75 °C	123 °C
D^2PAK	0.987 V	0.736 V	0.48 V
PPAK 8x8L	0.992 V	0.741 V	0.484 V
T_C of bridge		$-4.6\,\frac{mV}{K}$	$-4.9\,\frac{mV}{K}$

Table 1: Temperature correlation of forward voltage at a current of 1 mA

of a current constant I_{meas} it is possible to derive a value which corresponds to the junction temperature. In order to determine the appropriate conversion factors, the forward voltage of the body diodes $U_{fwd}(T_J)$ is recorded at pre-defined steady-state temperatures $T_A = T_J$. During the determination of the temperature correlation of the diode voltage and during measurements, the ambient temperature T_A is recorded using a Type K thermocouple. This results in the values listed in the table 1.

The thermal power loss is achieved by applying a constant current I_{heat} to the half-bridge in the direction of flow of the body diodes. The heat dissipated in the half-bridge P_{diss} is calculated using the parameters of the system at equilibrium, i.e. $P_{diss} = U_{fwd} \cdot I_{heat}$. If the heating current is suddenly switched off and the voltage drop U_{fwd} at the body diodes caused by measuring current $I_{meas} = 1\,mA$ is instantaneously recorded, a value is obtained which can be converted into a junction temperature T_J through linear extrapolation of data from Table 1. The same values apply to both MOSFET cases.

Measurement Results

When measuring the interrelationship between the junction temperature T_J and the thermal dissipation loss P_{diss}, the tables 4a and 4b provide composite values. In the case of the circuit board under review (cf. Fig. 2 and 3), a mean value for the thermal transition resistance for a half-bridge consisting of two N-channel MOSFETS was calculated to be $R_{th} = 16.6\,\frac{K}{W}$ for the SQM60030 in case type D^2PAK and $R_{th} = 20.6\,\frac{K}{W}$ for the SQJQ480E in case type PowerPAK 8x8L. The values obtained correlate well with the values quoted in the relevant datasheets. A comparisons of the two is shown in Table 2.

In order to enable a comparison of thermal properties, the heat transfer coefficient is calculated as described above. The results are summarised in Table 3.

Conclusion

A comparison of the thermal behaviour of the case forms D^2PAK and PowerPAK 8x8L reveals that under equal peripheral conditions (junction temperature, ambient temperature, heat sink design) the thermal transition resistance R_{thJA} of the PowerPAK 8x8L case is slightly higher than that of the D^2PAK case type. On closer scrutiny, it however becomes apparent that this is chiefly a result of the size. A comparison with the circuit board surface used clearly highlights the advantages of the PowerPAK 8x8L. Compared with the D^2PAK, the PowerPAK 8x8L enables heat dissipation loss densities higher by an order of 2. Therefore it is ideally suited to miniaturised circuits.

	Datenblatt		Messung	
	R_{th} Limit	A	R_{th}	A
D^2PAK	$40\,\frac{W}{K}$	$1\,in^2$	$33\,\frac{W}{K}$	$1.23\,in^2$
PPAK 8x8L	$50\,\frac{W}{K}$	$1\,in^2$	$41\,\frac{W}{K}$	$1.23\,in^2$

Table 2: Comparison of datasheet entries with recorded values for a single FET in consideration of the active cooling surface area A

	R_{thJA}	A	h_{JA}
D^2PAK	$16.6\,\frac{W}{K}$	$344\,mm^2$	$0.18\,\frac{mW}{K\,mm^2}$
PPAK 8x8L	$20.6\,\frac{W}{K}$	$130\,mm^2$	$0.38\,\frac{mW}{K\,mm^2}$

Table 3: Comparison of heat transfer coefficient h_{JA} using the surface area of the components used A[2]

I_{heat}	P_{diss}	T_A	U_{fwd}	T_J	R_{th}
1 A	1.26 W	21.0 °C	0.98 V	43.5 °C	$17.8\,\frac{K}{W}$
2 A	2.48 W	21.0 °C	0.78 V	65.2 °C	$17.8\,\frac{K}{W}$
3 A	3.63 W	20.7 °C	0.70 V	95.1 °C	$16.0\,\frac{K}{W}$
4 A	4.68 W	20.5 °C	0.62 V	78.8 °C	$15.9\,\frac{K}{W}$
5 A	5.70 W	20.7 °C	0.54 V	111.4 °C	$15.9\,\frac{K}{W}$
6 A	6.66 W	20.5 °C	0.46 V	127.8 °C	$16.1\,\frac{K}{W}$

(a) Measurements on half-bridge consisting of two SQM60030

I_{heat}	P_{diss}	T_A	U_{fwd}	T_J	R_{th}
1 A	1.24 W	20.2 °C	0.85 V	51.1 °C	$24.9\,\frac{K}{W}$
2 A	2.42 W	20.0 °C	0.76 V	70.6 °C	$20.9\,\frac{K}{W}$
3 A	3.51 W	18.8 °C	0.64 V	92.0 °C	$20.9\,\frac{K}{W}$
4 A	4.52 W	20.5 °C	0.57 V	106.3 °C	$19.0\,\frac{K}{W}$
5 A	5.45 W	20.5 °C	0.48 V	124.7 °C	$19.1\,\frac{K}{W}$
6 A	6.36 W	20.5 °C	0.41 V	139.0 °C	$18.6\,\frac{K}{W}$

(b) Measurements on half-bridge consisting of two SQJQ480E

Table 4: Calculation of junction temperature at a measuring current of $I_{meas} = 1\,mA$ for a half-bridge

References

[1] Vishay, AN819: MOSFET Thermal Characterization in the Application, 14-May-2001

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[3] Vishay, SQM60030E Automotive N-Channel 80 V (D-S) 175 °C MOSFET, 14-Dec-2015

[4] Vishay, SQJQ480E N-Channel 80 V (D-S) 175 °C MOSFET, 26-Feb-2015

[5] Vishay, AN834: Estimating Junction Temperature by Top Surface Temperature in Power MOSFETs, 01-Oct-2015