Power MOSFET Basics - Understanding Voltage Ratings

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DESCRIPTION

Two kinds of voltage ratings are provided for MOSFETs in their datasheets - V_{DS} and V_{GS}. For each, both absolute maximum and rated voltages are specified. Usually, the numbers are the same, but manufacturers use them in different contexts and for different purposes. By definition, absolute maximum ratings specify the limits for long term reliability and / or survival. Rated values are used for characterizing the device and act as reference values at which other measurements are taken. Most qualification tests are done at the rated voltages or at a specified percentage thereof. For example, leakage currents from drain to source or gate to source are measured and specified at rated voltages, both at normal ambient as well as at elevated temperatures. Qualification tests such as High Temperature Reverse Bias (HTRB) or High Temperature Gate Bias (HTBG) are performed at 80 % of the rated voltage.

In this context, it may be useful to compare rated vs. absolute maximum voltages for integrated circuits and discrete devices. For ICs there is a recommended range of applied voltages within which performance is guaranteed. These limits are set by internal circuitry and bias conditions. In addition, absolute maximum limits are also provided, and these are invariably higher than the recommended or operating maximum voltage values. In the case of ICs, these are defined by the process, and exceeding them may permanently damage the device. By contrast, there is no “operating range” of voltages for MOSFETs; they can be operated at any voltage from zero up to and including rated voltage. However, since the absolute values are the same as rated values, it is important not to exceed either of the limits under all operating conditions.

OVERVOLTAGE INDUCED FAILURES

Intentionally or otherwise, a MOSFET might be subjected to higher voltages during operation which could lead to its destruction. There are different ways an overvoltage can occur and different mechanisms by which a device can fail. Figures 1a and 1b show the cross section of a typical trench MOSFET and its equivalent electrical circuit. Of particular interest are the junctions where the body diode and the parasitic bipolar junction transistor (BJT) are formed. The reverse diode is a result of P+ body diffusion into the N epi, and the BJT is formed when the N+ source contact is diffused on top. It should be remembered that the schematic is only a lumped representation. Circuit elements such as resistors, capacitors, or the body diode are distributed over the entire map. Also, a typical MOSFET may consist of millions of cells, all operating in parallel but not equal in all respects. The survival of the device as a whole under extreme conditions is determined by the weakest of those millions of cells.

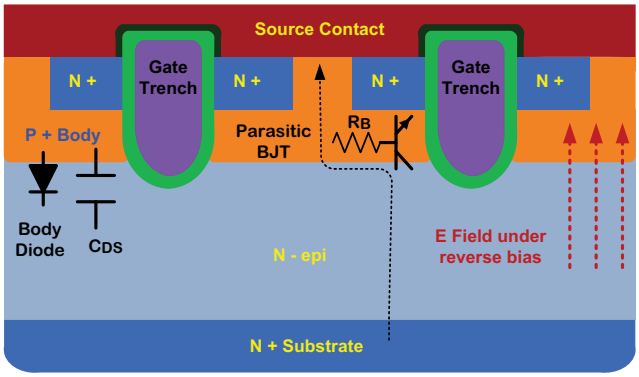

Fig. 1a - Cross Section of a Trench MOSFET

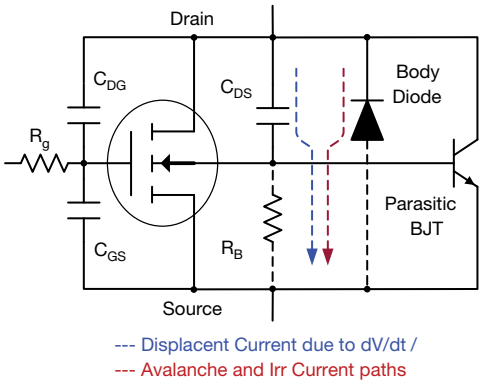

Fig. 1b - Equivalent Circuit

APPLICATION NOTE

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When a reverse bias is applied between drain and source, an electric field is set up across the P-N junction. When the applied voltage increases beyond the rating, a critical field is reached where the junction can no longer support the applied voltage. Impact ionization intensifies rapidly, leading to avalanche multiplication of carriers. The resulting reverse current tends to flow laterally in the P body, as shown in Figure 1a, since the electric field is the strongest at the point where the junction bends along the gate trench contour. The current is represented by the dashed red line in the schematic of Figure 1b. The subsequent failure may happen due to excessive heat in the die, or due to parasitic bipolar latch-up. When the voltage drop across R_B is sufficient to forward bias the parasitic BJT, it will turn on, leading to catastrophic failure. There have been many advances in MOSFET design technology targeted at minimizing the base resistance R_B to prevent the bipolar turn-on. However, no MOSFET is totally immune to latch-up.

Junction temperature plays an important role in triggering the failure. Silicon resistivity increases with temperature, and the forward bias threshold of the base emitter junction reduces at the same time. The combination of higher R_B and a lower threshold results in bipolar turn-on at much lower currents. Paradoxically, the critical field value at which avalanche breakdown is initiated also increases with temperature. At higher values of junction temperature T_J, the device can support greater values of V_{DS} across the P-N junction before the temperature-specific critical field is reached. Typically, this is reflected in the rated voltage specifications of high voltage MOSFETs (HVMs). A 600 V MOSFET at T_J = 25 °C has a 650 V or higher rating at T_J = 150 °C. However, the improved rating is not of much benefit to the user as it is relevant only in steady state where V_{DS} is gradually increased. In all practical applications, the high V_{DS} is accompanied by large drain currents, which lead to bipolar latch-up.

One common application condition where the MOSFET will see voltages well above the rated V_{DS} is under unclamped inductive switching (UIS). The standard UIS circuit and simplified waveforms are shown in Figures 2a and 2b. Though overvoltage and avalanche breakdown are evident, it should be noted that the UIS is a current-driven, transient event. The avalanche current in this case is the same as the peak inductor current indicated by the red dashed line in Figure 1b. The P-N junction breaks down and creates a voltage necessary and sufficient to sink the forced current. Generally, the UIS ratings relate only to power and current handling capabilities of the device during turn-off. They should not be related to or interpreted as voltage ratings. The peak V_{DS} under UIS-driven avalanche is a property of the device structure and magnitude of the current. Users have no control over it; no upper or safe limit can be specified by the device manufacturer. Failure can happen due to thermal stress or bipolar latch-up.

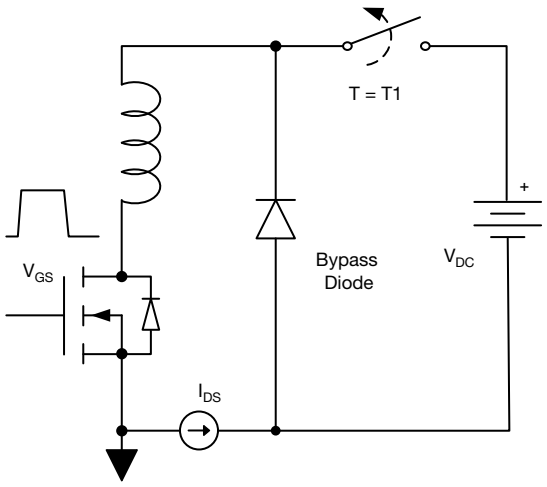

Fig. 2a - UIS Test Set Up

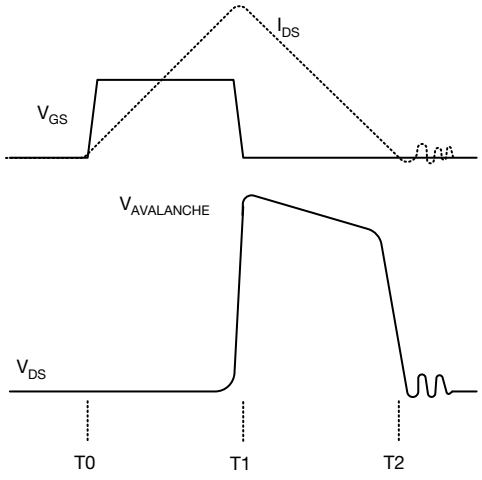

Fig. 2b - UIS Waveforms

A related failure mode is due to high rate of dV/dt, especially for HVMs. The dV/dt may be caused by fast turn-off at the gate or hard turn-off of the body diode. Standard HVMs have large Q_{rr} values, running into tens of µC with abrupt recovery characteristics. The reverse recovery current will be flowing into the bipolar base resistance, potentially causing the latch-up. In bridge circuits, it is recommended to use MOSFETs with low Q_{rr} and soft recovery specifically created for such applications. With or without being accompanied by diode recovery, high dV/dt must also charge the output capacitance C_{oss}, which causes a displacement current shown by the blue dashed line in Figure 1b.

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Manufacturers provide maximum values of dV/dt that can be applied to HVMs without triggering the bipolar latch-up. The information is omitted for low voltage devices since their R_B values are also low and the dV/dt stress required to cause failure is much higher than what is encountered in practical applications. Device datasheets also provide maximum ratings for the gate to source voltage rating $V_{GSMAX.}$ in addition to $V_{DSMAX.}$. However, there are no avalanche or latch-up mechanisms here. Exceeding the rated gate voltage may cause rupturing of the thin gate oxide material that insulates the trench, causing permanent damage. Again, the strength of the gate oxide is not uniform around the trench but is at its weakest around the edges. Typically, it takes more than 50 % above the rated gate voltage for the rupture to happen. While this should not be a major concern in normal operation, poorly designed gate drive loops with high parasitic inductances can cause unexpected voltage spikes around the gate, especially under transient conditions, or when MOSFETs are operating in parallel. Another potential source of gate voltage is during input surge tests. Immunity standards such as EN 61000-4 specify line transients up to 2 kV between line and neutral. Unless properly attenuated at the source and isolated from the control circuit, the surges manifest themselves as voltage spikes on the MOSFET gate.

DERATING THE DEVICES

While a continuous violation of rated voltages must be avoided, designers often want to know if it is acceptable to exceed the rating for a short period. For example, is it OK if the peak ringing exceeds the rated voltage for a few nanoseconds during turn-off, and only during start up or a load transient? Also, is there a recommended derating factor for voltage stress under nominal operating conditions?

Unfortunately, neither question falls within the MOSFET manufacturers' scope; they can only recommend that neither absolute maximum nor rated voltage be exceeded under any condition. “Any” refers to a worst case combination of possibilities - high line, load transient, sudden short circuit, input surges, etc. Peak voltages under every combination are not always predictable. Besides the wide variety of products and design practices, the end product containing the MOSFET can be used in any electrical environment of which the manufacturers have no knowledge.

Industry standards such as IPC9592 and several other guidelines in the literature recommend 80 % derating on operating voltage. This is based on the qualification process mentioned in the beginning, where MOSFETs are subject to reverse bias under high temperature. The HTRB requirements are based on JEDEC® and military standards for power MOSFETs, and they typically specify V_{DS} of 80 % of the rated value at $T_A = T_J = 100$ °C. However, the 80 % rule is not easy to interpret for switching circuits. Figure 3 shows the turn-off waveform in a practical flyback circuit. There is an initial overshoot as the energy stored in the leakage inductance is discharged by the snubber, followed by a lower V_{DSOFF} during the flyback operation. If the operating mode is DCM, the voltage would settle at supply voltage V_{IN}, before turning on again. It is not clear whether the 80 % derating rule should be applied w.r.t. peak V_{DS} or V_{DSOFF}. While the intent of an 80 % voltage derating rule is quite clear for, say, an electrolytic capacitor, it is far from obvious in the case of switching waveforms.

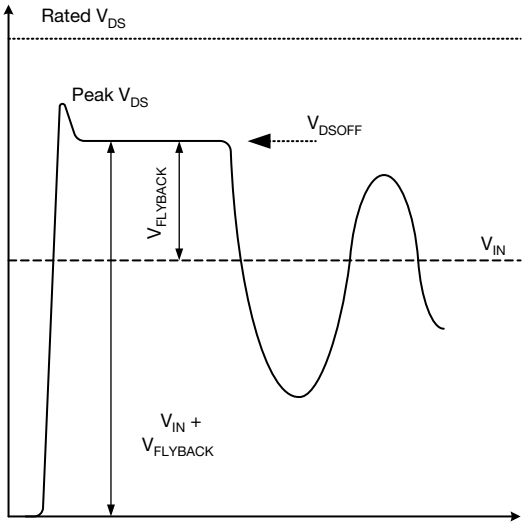

Fig. 3 - V_{DS} Waveforms During Turn-Off

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There is a cost associated with an excessive derating factor and a risk associated with inadequate derating. It is for the system designers to balance the two and optimize the tradeoff. The risk, it must be emphasized, refers to the possibility of overvoltages beyond the rated V_{DS} that may happen in the field, and not to any of the intrinsic properties or life expectancy of the device. While the MOSFET capacitances vary a great deal from zero to 50 % of the rated voltage, they are fairly stable under the top 20 % of voltage excursion. There are no studies that link voltage derating to long term failure rates for MOSFETs. There is no voltage equivalent of the Arrhenius equation, or a lifetime vs. operating voltage formula as is offered for electrolytic capacitors. Another factor to keep in mind is that MOSFET characteristics change significantly with rated voltages. For a given die size, a 10 % increase in rated voltage may mean more than a 25 % increase in $R_{DS(on)}$. The combination of $R_{DS(on)}$, gate, and output capacitances available in a 500 V MOSFET may not be possible in a derated 600 V device.

Bottom line is that voltage derating factors are based on individual perceptions and depend entirely on what is agreed between system designers, their managements, and their customers. Each company can define its own margins. End customers may demand conformance to an industry standard such as IPC9592 or impose their own limits. In the absence of any other guideline, the 80 % rule may be applied as the rule of thumb to peak V_{DS} of Figure 3, after taking into account the full range of operating conditions. Again, this is not a recommendation from reliability considerations; the manufacturer's recommendation will always be not to exceed the rated voltage under any operating conditions. The key to achieving a robust and reliable design is to minimize the voltage spikes and overshoots during normal operation as much as possible; this will require careful attention to circuit parasitics, tailoring the MOSFET switching speed and use of snubbers as necessary. The derating margins should then be added to account for unexpected transients in the field.

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