UG326: Class 2 Non-Isolated Evaluation Board for the Si3406

The Si3406 non-isolated Flyback topology based evaluation board is a reference design for a power supply in a Power over Ethernet (PoE) Powered Device (PD) application.

This Si3406-non-ISO-FB EVB maximum output level is Class 2 power (η x 6.5W).

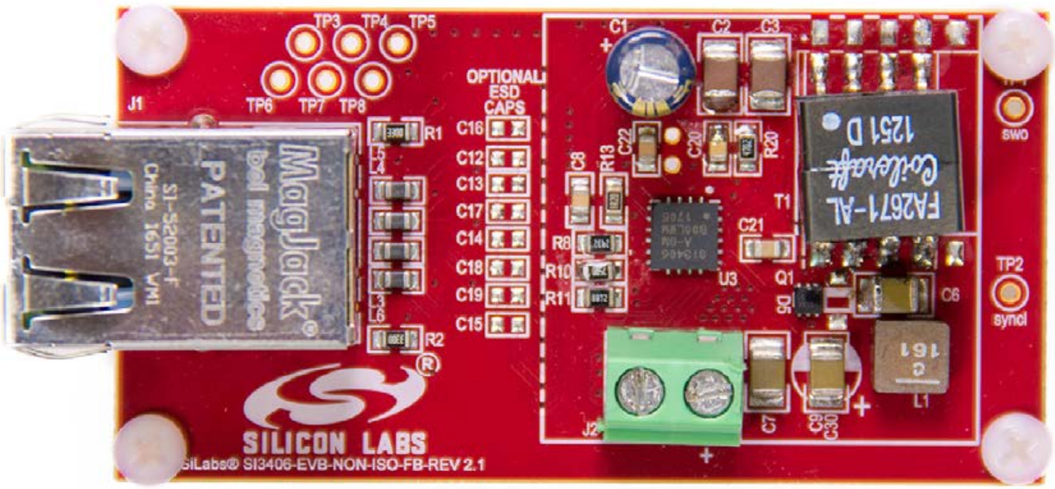
The Si3406-non-ISO-FB EVB board is shown below. The Si3406 IC integrates an IEEE 802.03at compatible PoE interface as well as a current control based dc/dc converter.

The Si3406 PD integrates two diode bridges, which can be used up to 200 mA input current, detection circuit, classification circuit, DC/DC switch, hot-swap switch, TVS overvoltage protection, dynamic soft-start circuit, cycle-by-cycle current limit, syncrhonous gate driver, maintain power signature (MPS), thermal shutdown, and inrush current protection.

The switching frequency of the converter is tunable by an external resistor.

KEY FEATURES

- IEEE 802.03at Compatible
- Very Small Application PCB Surface
- High Efficiency
- High Integration
- Optional MPS Function
- Synchronous Gate Driver
- Low BOM Cost
- Transient Overvoltage Protection
- Thermal Shutdown Protection
- 5x5 mm 20-pin QFN



1. Kit Description

The Si3406-non-isolated Flyback topology based evaluation board is a reference design for power supplies in Power over Ethernet (PoE) Powered Device (PD) applications. The Si3406 device is described more completely in the data sheet and application notes. This document describes the evaluation board.

The Si3406-non-ISO-FB EVB board is shown on the cover page. The schematic is shown in Figure 2.3 Si3406 Non-Isolated Flyback EVB Schematic: 5 V, Class 2 PD on page 4, and the layout can be found in 17. Board Layout. The dc output is at connector J2.

Boards are shipped configured to produce 5 V output voltage but can be configured for different output voltages, such as 3.3 or 12 V for example, by changing resistor R14 and a few other components. Refer to “AN1130: Using the Si3406/Si34061/Si34062 PoE+ and Si3404 PoE PD Controller in Isolated and Non-Isolated Designs” for more information. The preconfigured Class 2 signature can also be modified, which is described as well in AN1130.

The Si3406 includes integrated diode bridges for both CT and SP connection. The integrated diode bridges can be used up to 200 mA input current. Above 200 mA input current the external diode bridge is required.

The external diode bridge can be a Schottky or silicon type.

The Si3406 device can operate with CT/SP pins open, but in this configuration the external bridge should be Schottky type diode bridge.

To compensate for the reverse leakage of the Schottky type diode bridges at high temperatures, the recommended detection resistor should be adjusted to the values listed in the following table:

Table 1.1. Recommended Detection Resistor Values

External Diode Bridge	R_{DET}
Silicon Type	24.3 kΩ
Schottky Type	24.9 kΩ

2. Getting Started: Powering Up the Si3406 Non-ISO-FB Board

Ethernet data and power are applied to the board through the RJ45 connector (J1). The board itself has no Ethernet data transmission functionality, but, as a convenience, the Ethernet transformer secondary-side data is brought out to test points.

The design can be used in Gigabit (10/100/1000) systems as well by using PoE RJ45 Magjack, such as type L8BE-1G1T-BFH from Bel Fuse.

Power may be applied in the following ways:

- Using an IEEE 802.3-2015-compliant, PoE-capable PSE, such as Trendnet TPE-1020WS
- Using a laboratory power supply unit (PSU):
  - Connecting a dc source between blue/white-blue and brown/white-brown of the Ethernet cable (either polarity), (End-span) as shown below:

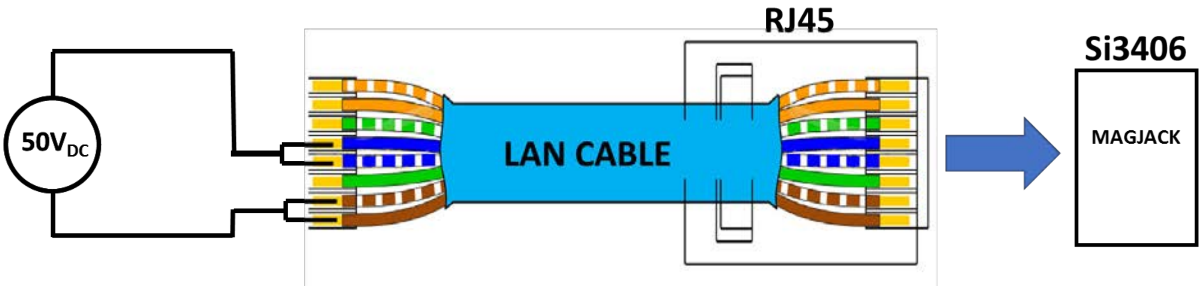


Figure 2.1. Endspan Connection using Laboratory Power Supply

  - Connecting a dc source between green/white-green and orange/white-orange of the Ethernet cable (either polarity), (Mid-span) as shown below:

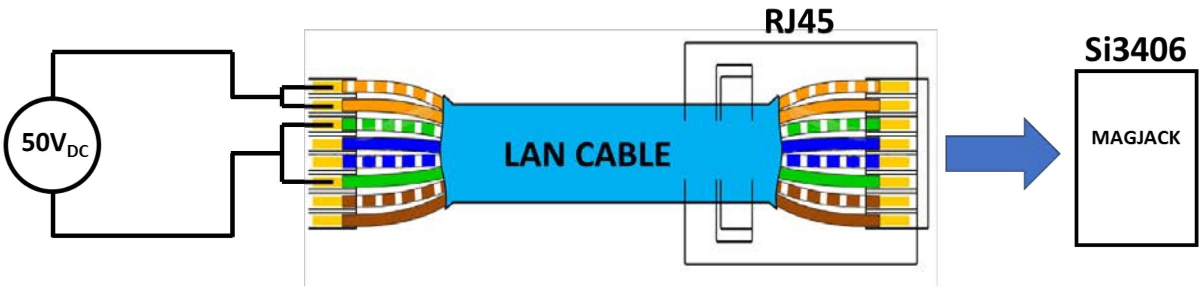


Figure 2.2. Midspan Connection using Laboratory Power Supply

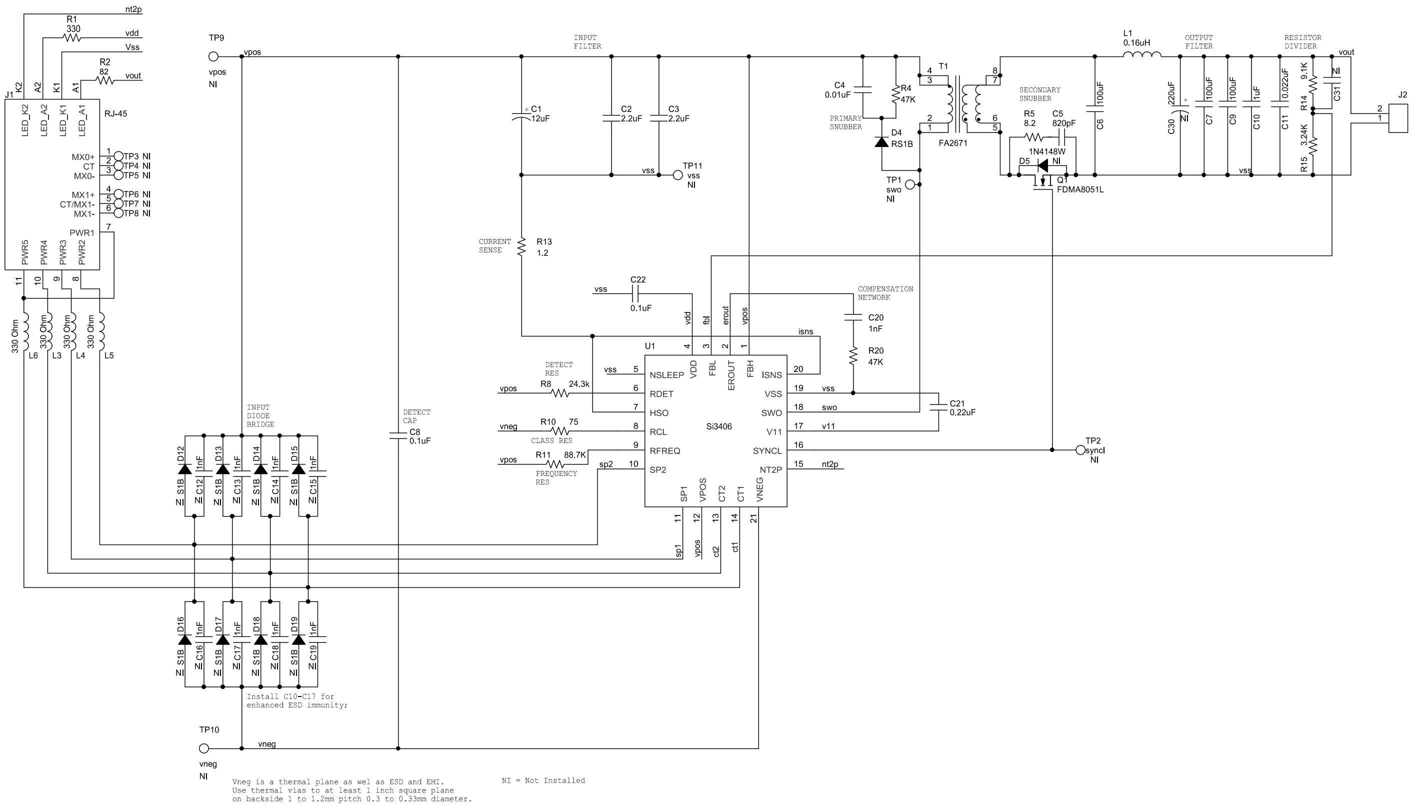


Figure 2.3. Si3406 Non-Isolated Flyback EVB Schematic: 5 V, Class 2 PD

3. Overall EVB Efficiency

The overall efficiency measurement data of the Si3406-non-ISO-FB EVB board is shown below. The input voltage is 50 V, and the output voltage is 5 V.

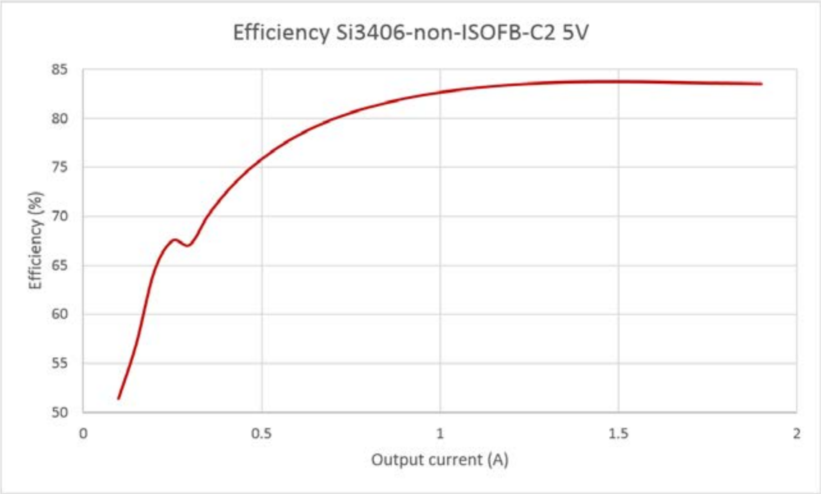


Figure 3.1. Si3406 Non-Isolated Flyback EVB Overall Efficiency (50 V Input, 5 V Output, Class 2 PD)

Note: The chart shows overall EVB efficiency. The voltage drop on the standard silicon diode bridge is included.

4. SIFOS PoE Compatibility Test Results

The Si3406-non-ISO-FB EVB board has been successfully tested with PDA-300 Powered Device Analyzer from SIFOS Technologies. The PDA-300 Powered Device Analyzer is a single-box comprehensive solution for testing IEEE 802.3at PoE Powered Devices (PD's).

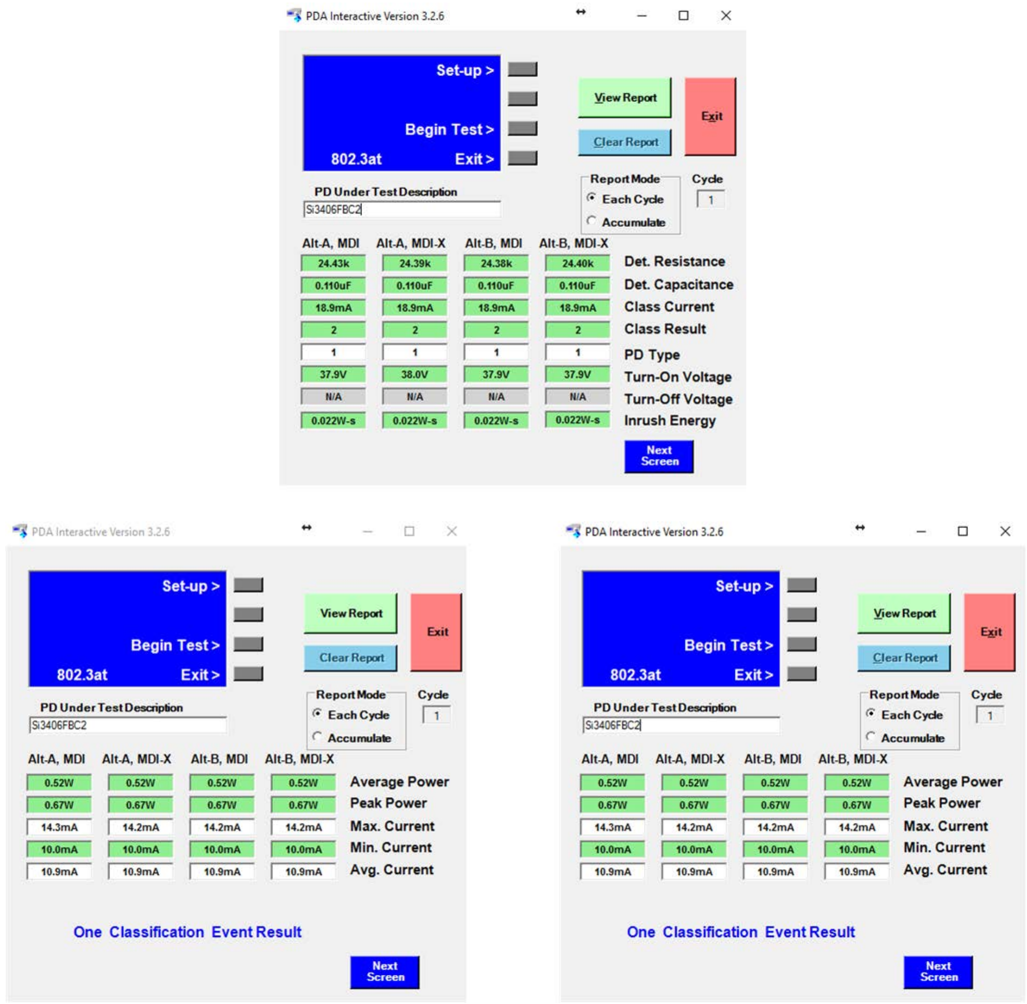


Figure 4.1. Si3406 Non-Isolated Flyback PD SIFOS PoE Compatibility Test Results

5. Control Loop Phase Shift and Gain Measurement Results (Bode Plots)

The Si3406 device integrates a current mode controlled switching mode power supply controller circuit. Therefore, the application is a closed-loop system. To guarantee a stable output voltage of a power supply and to reduce the influence of input supply voltage variations and load changes on the output voltage, the control loop should be stable.

To verify the stability of the loop, the loop gain and loop phase shift has been measured.

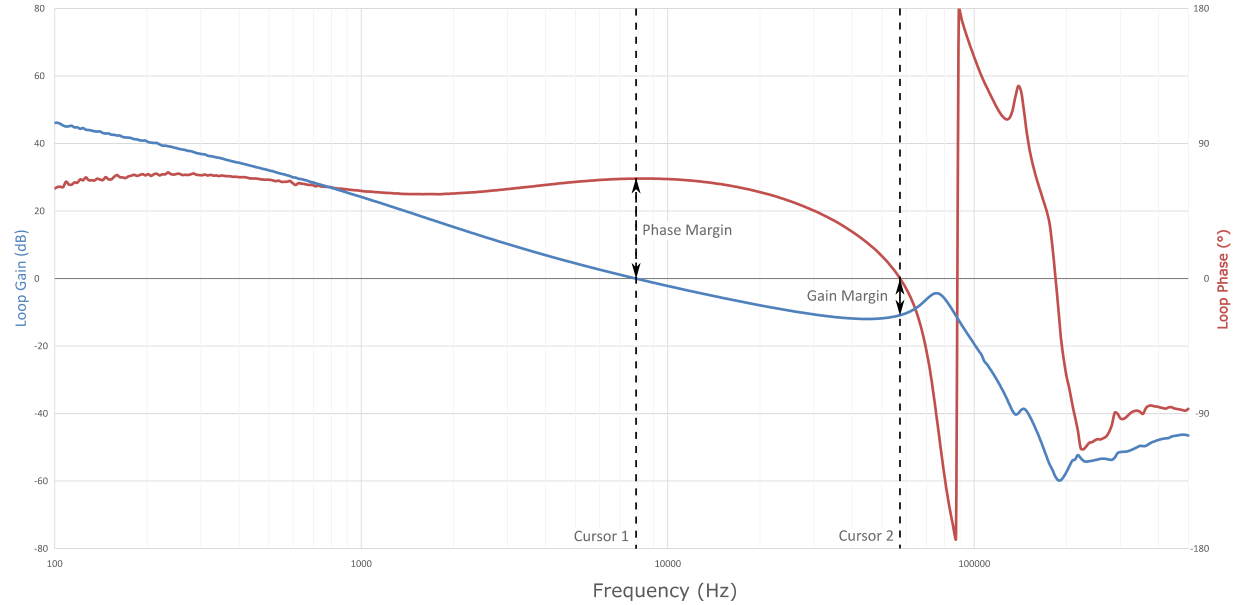


Figure 5.1. Si3406 Non-ISOFB-EVB-C2 Measured Loop-Gain and Phase Shift

Table 5.1. Measured Loop Gain and Phase Shift

	Frequency	Gain	Phase
Cursor 1 (Phase Margin)	7.8 kHz	0 dB	66 °
Cursor 2 (Gain Margin)	56.7 kHz	–11 dB	0 °

6. Step Load Transient Measurement Results

The Si3406-non-ISO-FB EVB board's output has been tested with a step load function to verify the converters output dynamic response.

Step load: from 0.3A to 1.3A output current;	Step load: from 1.3A to 0.3A output current;

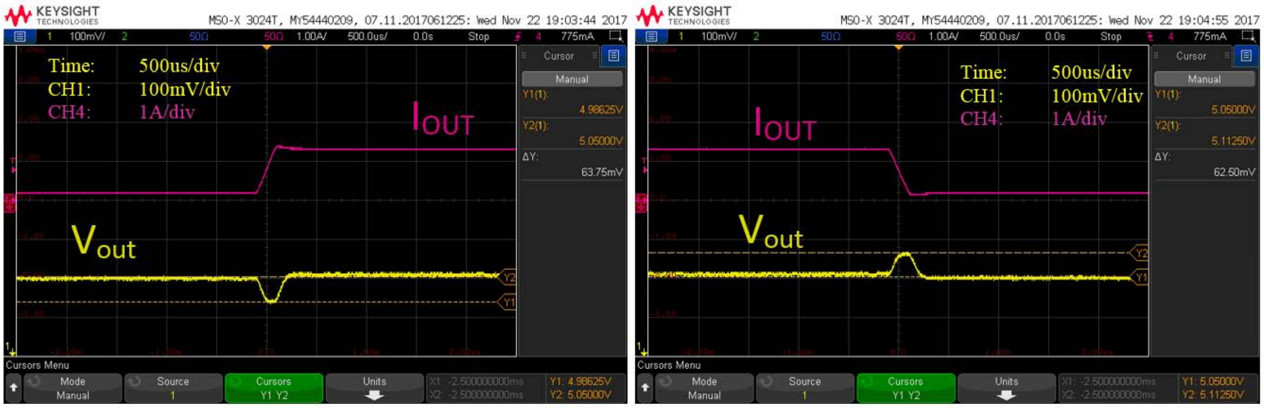


Figure 6.1. Si3406 Non-Isolated Flyback EVB PD Output Step Load Transient Test

7. Output Voltage Ripple

The Si3406-non-ISO-FB output voltage ripple has been measured in both no load and heavy load conditions.

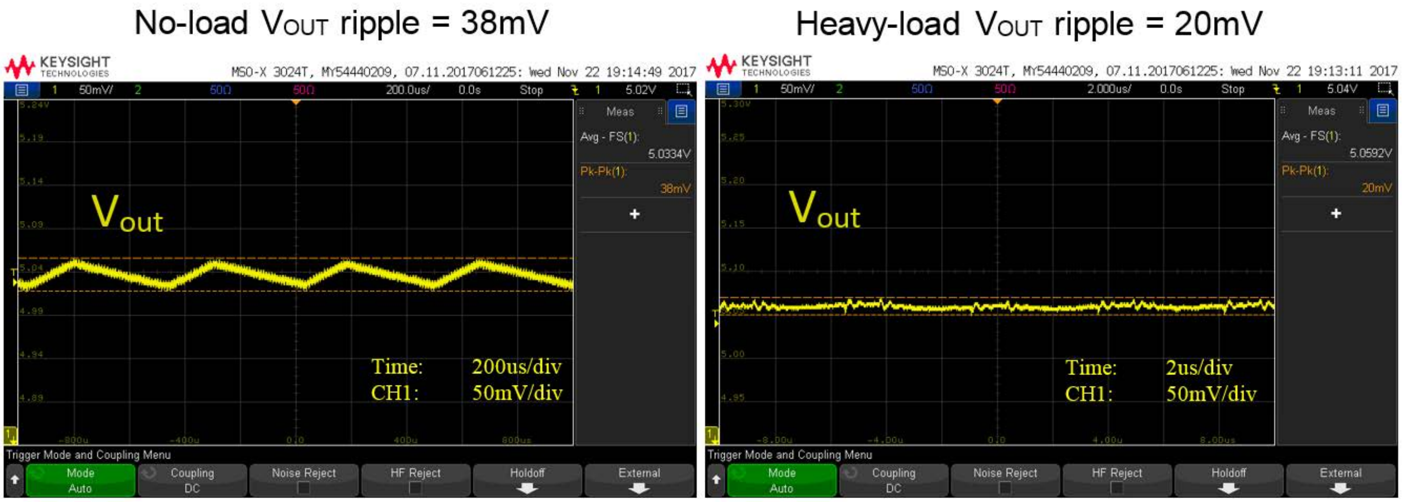


Figure 7.1. Si3406 Non-Isolated Flyback EVB Output Voltage Ripple No Load (Left) and Heavy Load (Right) Conditions

8. Soft-Start Protection

The Si3406 device has an integrated dynamic soft-start protection mechanism to avoid stressing the components by the sudden current or voltage changes associated with the initial charging of the output capacitors.

The intelligent dynamic soft-start adjusts the rise time of the output voltage based on the connected output load.

Figure 8.1. Si3406 Non-Isolated Flyback EVB Input Current and Output Voltage Soft-Start at Low Load (Left) and Heavy Load (Right) Conditions

9. Output Short Protection

The Si3406 device has an integrated output short protection mechanism, which protects the IC itself and the surrounding external components from overheating in the case of electrical short on the output.

Figure 9.1. Si3406 Non-Isolated Flyback EVB Output Voltage and Input Current when the Output is Shorted

10. Pulse Skipping at No-Load Condition

The Si3406 device has an integrated pulse skipping mechanism to ensure ultra-low power consumption at no load condition.

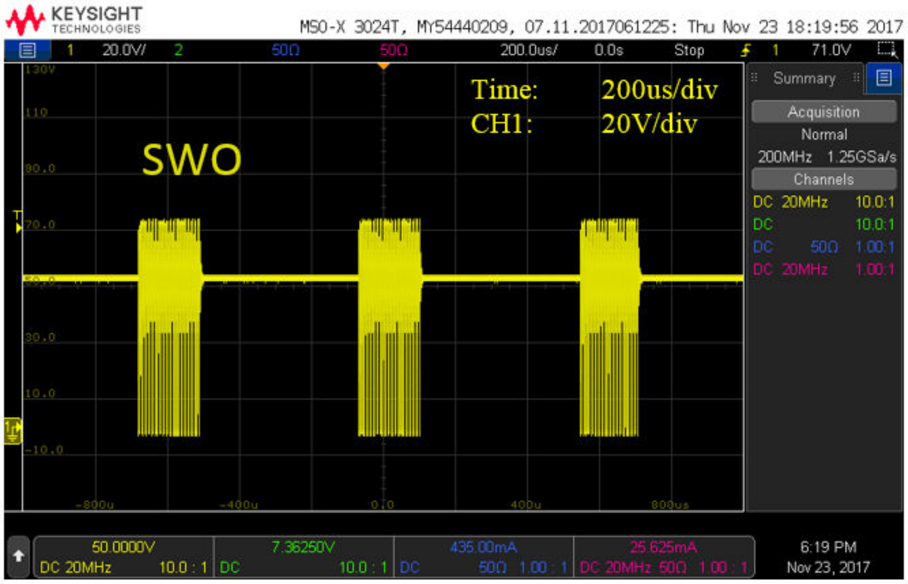


Figure 10.1. Si3406 Pulse Skipping at No-Load Condition (SWO Waveform)

11. Adjustable EVB Current Limit

For additional safety, the Si3406 has an adjustable EVB current limit feature. The EVB current limit through the ISNS pin measures the voltage on R_{SENSE}. When V_{RSENSE} = –270 mV (referenced to V_{SS}), the current limit circuit restarts the circuit to protect the application.

The EVB current limit for Class 2 application can be calculated with the following formula:

$$R_{SENSE} = 1.2\Omega$$

$$I_{LIMIT} = \frac{270mV}{1.2\Omega} = 225mA$$

Equation 1. EVB Current Limit

12. Tunable Switching Frequency

The switching frequency of the oscillator is selected by choosing an external resistor (RFREQ) connected between RFREQ and VPOS pins. The following figure will aid in choosing the RFREQ value to achieve the desired switching frequency.

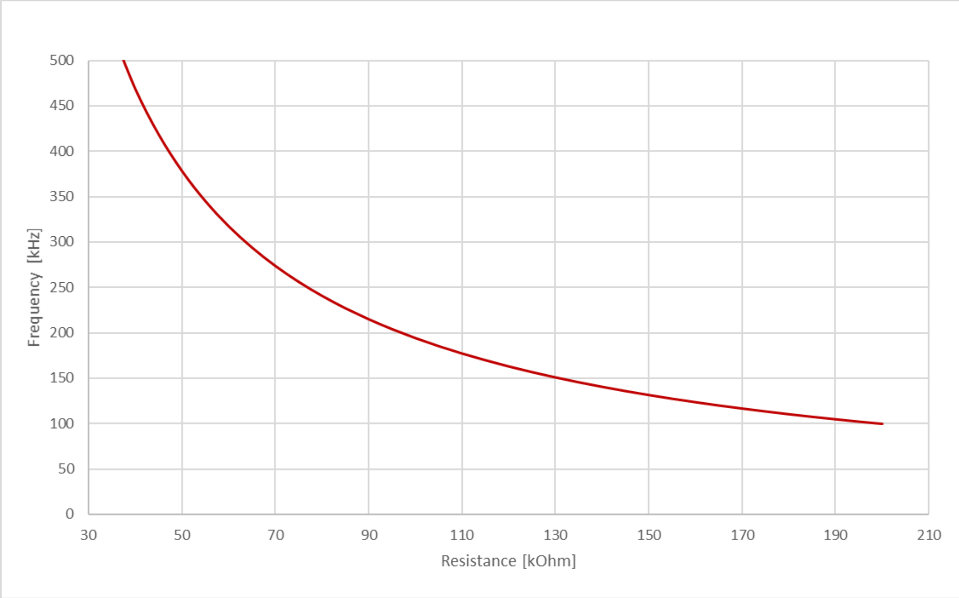


Figure 12.1. Switching Frequency vs. RFREQ

The selected switching frequency for this application is 220 kHz, which is achieved by setting the RFREQ resistor to 88.7 kΩ.

13. Synchronous Rectification

The Si3406 device has synchronous gate driver (SYNCL) to drive the rectifier MOSFET. At low-load the converter works in discontinuous current mode (DCM); at heavy load, the converter runs in continuous current mode (CCM). At low-load the SWO voltage waveform has a ringing waveform, which is typical for a DCM operation.

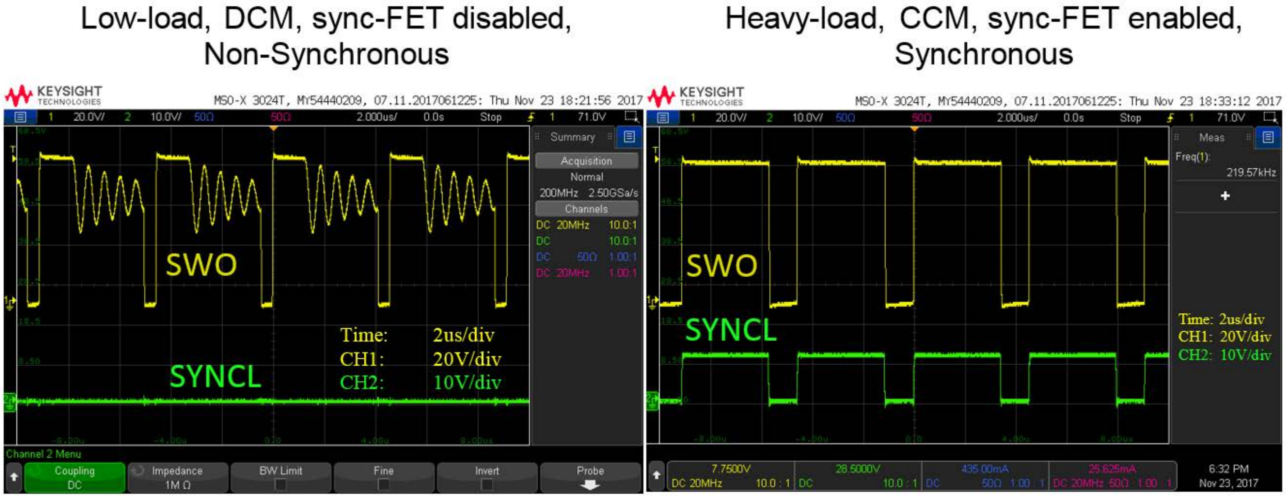


Figure 13.1. SWO and SYNCL Voltage Waveforms at Discontinuous Current Mode (DCM) (Left) and in Continuous Current Mode (CCM) (Right)

The device operates in non-synchronous mode at light load (I_{IN} < 25 mA). As the input current increases, Si3406 automatically changes its switching operation from "Non-Synchronous" to "Synchronous". The dynamic operation adjustment maximizes overall power efficiency.

14. Maintain Power Signature (MPS)

The Si3406 device integrates an MPS circuit which ensures connection with the PSE if the PD application current drops below PSE threshold level.

There are two modes of MPS operation:

- Automatic mode MPS (consumption-based)
- User mode MPS

Automatic Mode MPS (Consumptions Based):

If *nSLEEP* is low at startup, MPS generation depends on chip current consumption:

- MPS pulses are enabled below a certain level of total PD current consumption to ensure connection with the PSE
- MPS pulses are disabled above a certain level of total PD current consumption not to degrade overall board efficiency

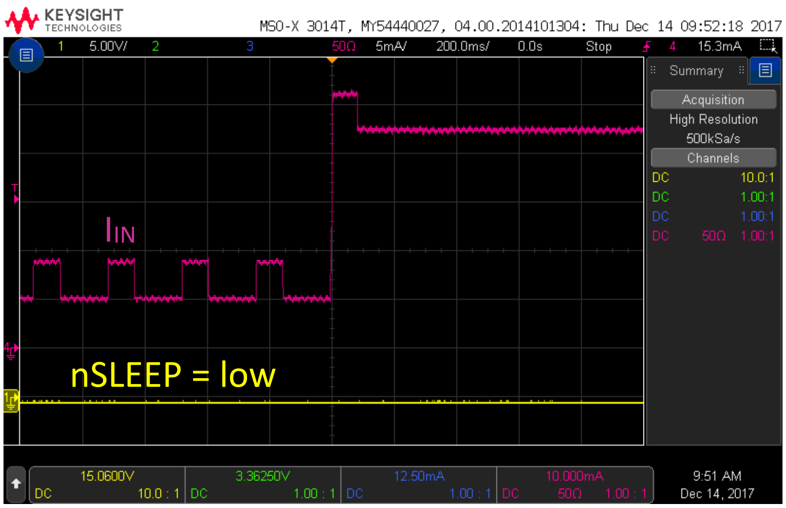


Figure 14.1. Automatic MPS Mode, nSLEEP is Low; MPS is Enabled when PD Consumption is Low; MPS is Disabled when PD Consumption is Higher

User Mode MPS:

If *nSLEEP* is high at startup, MPS generation depends on *nSLEEP.*

- if *nSLEEP* is high, MPS disabled (independently of the current consumption)
- if *nSLEEP* is low, MPS enabled (independently of the current consumption)

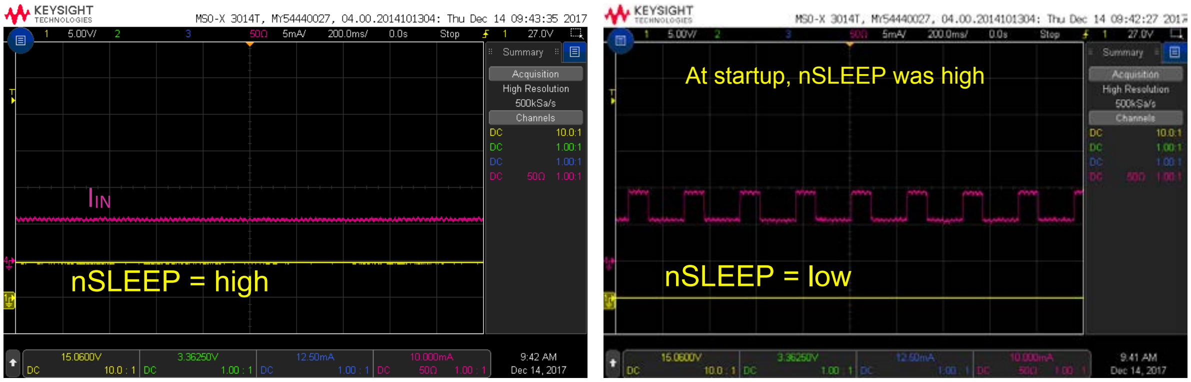


Figure 14.2. With nSLEEP High, MPS is Disabled (Left); with *nSLEEP* Low, MPS is Enabled (Right); MPS Generation is Fully Controlled by the User

15. Radiated Emissions Measurement Results

Radiated emissions have been measured of the Si3406-non-ISO-FB EVB board with 50 V input voltage and full load connected to the output – 6.5 W.

As shown below, the Si3406-non-ISO-FB EVB is fully compliant with the international EN 55022 class B emissions standard.

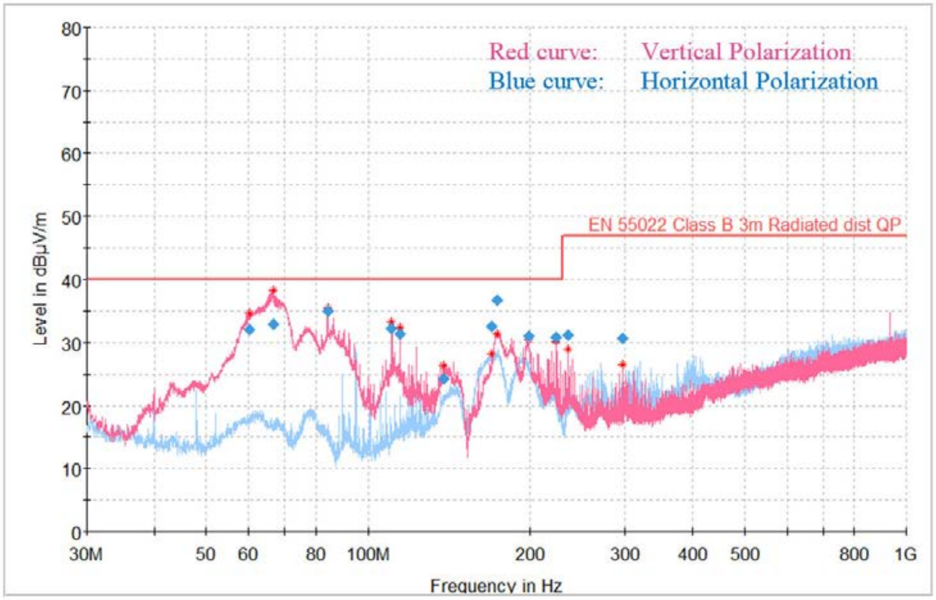


Figure 15.1. Si3406 Non-Isolated Flyback EVB Radiated Emissions Measurements Results (50 V Input, 5 V Output, 6.5 W Output Load)

15.1 Radiated EMI Measurement Process

The EVB is measured at full load with peak detection in both vertical and horizontal polarizations. This is a relatively fast process that produces a red curve (vertical polarization) and a blue curve (horizontal polarization). Next, specific frequencies are selected (red stars) for quasi-peak measurements. The board is measured again at those specific frequencies with a quasi-peak detector, which is a very slow but accurate measurement. The results of this quasi-peak detector measurement are the blue rhombuses.

The blue rhombuses represent the final result of the measurement process. To have passing results, the blue rhombuses should be below the highlighted EN 55022 Class B limit.

16. Conducted Emissions Measurement Results

The Si3406-non-ISO-FB EVB board's conducted emissions have been measured, the result is shown below.

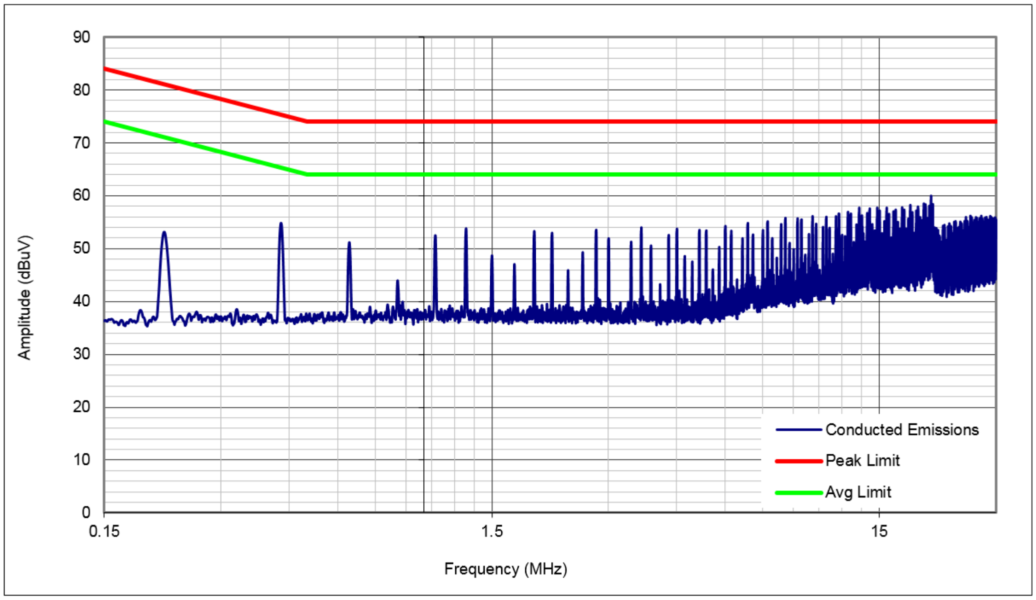


Figure 16.1. Si3406 Non-Isolated Flyback EVB Conducted Emissions Measurements Results (50 V Input, 5 V Output, 6.5 W Output Load)

17. Board Layout

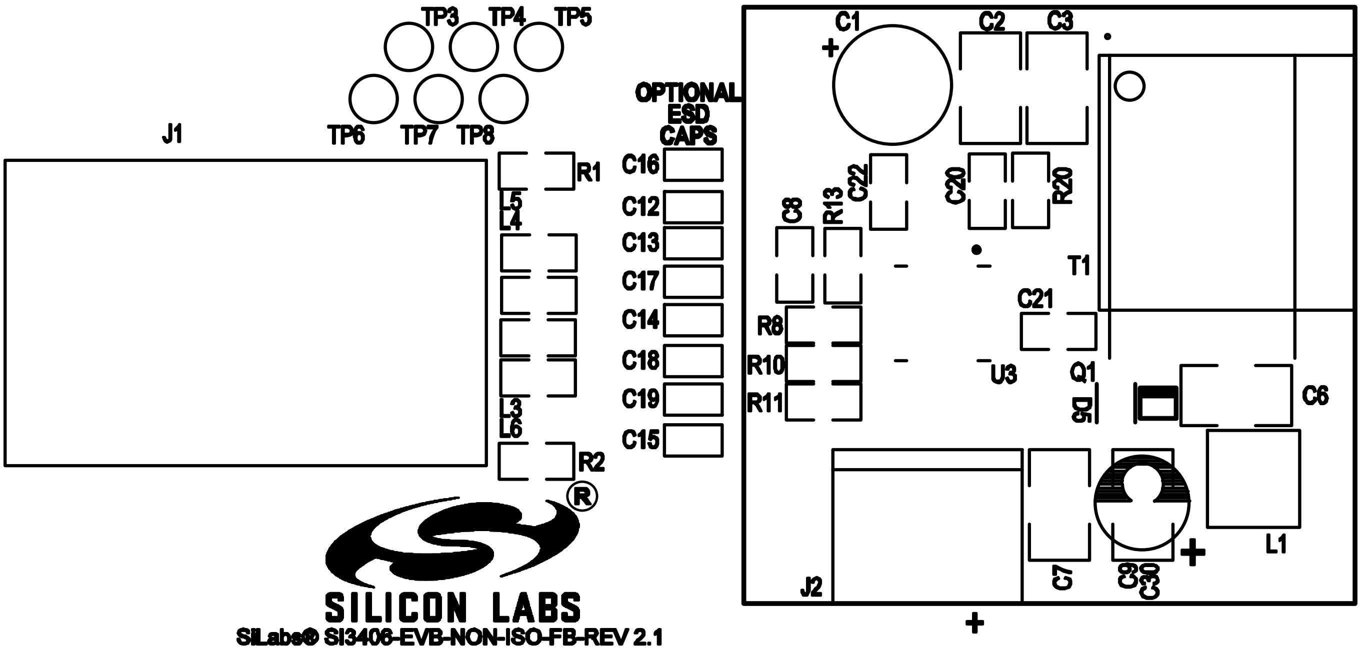


Figure 17.1. Top Silkscreen

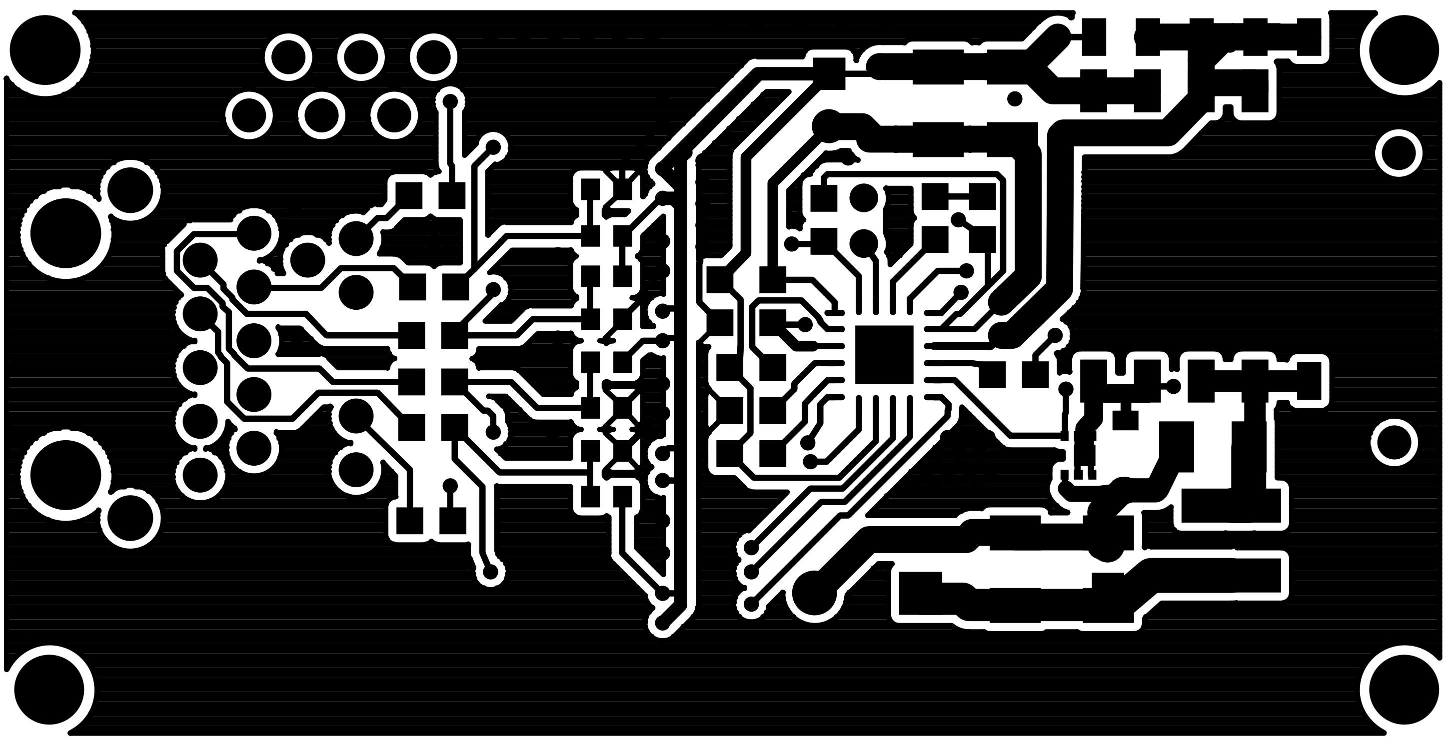


Figure 17.2. Top Layer

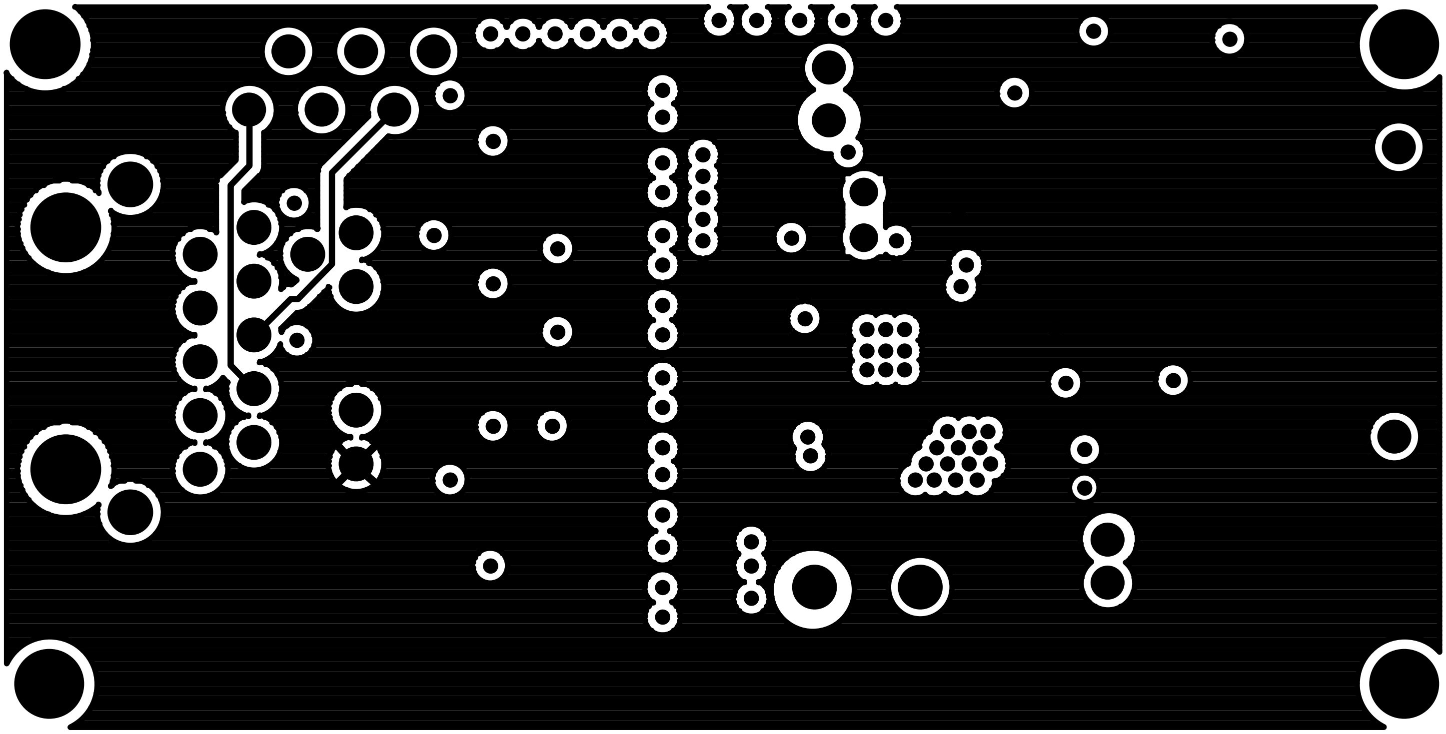


Figure 17.3. Internal 1 (Layer 2)

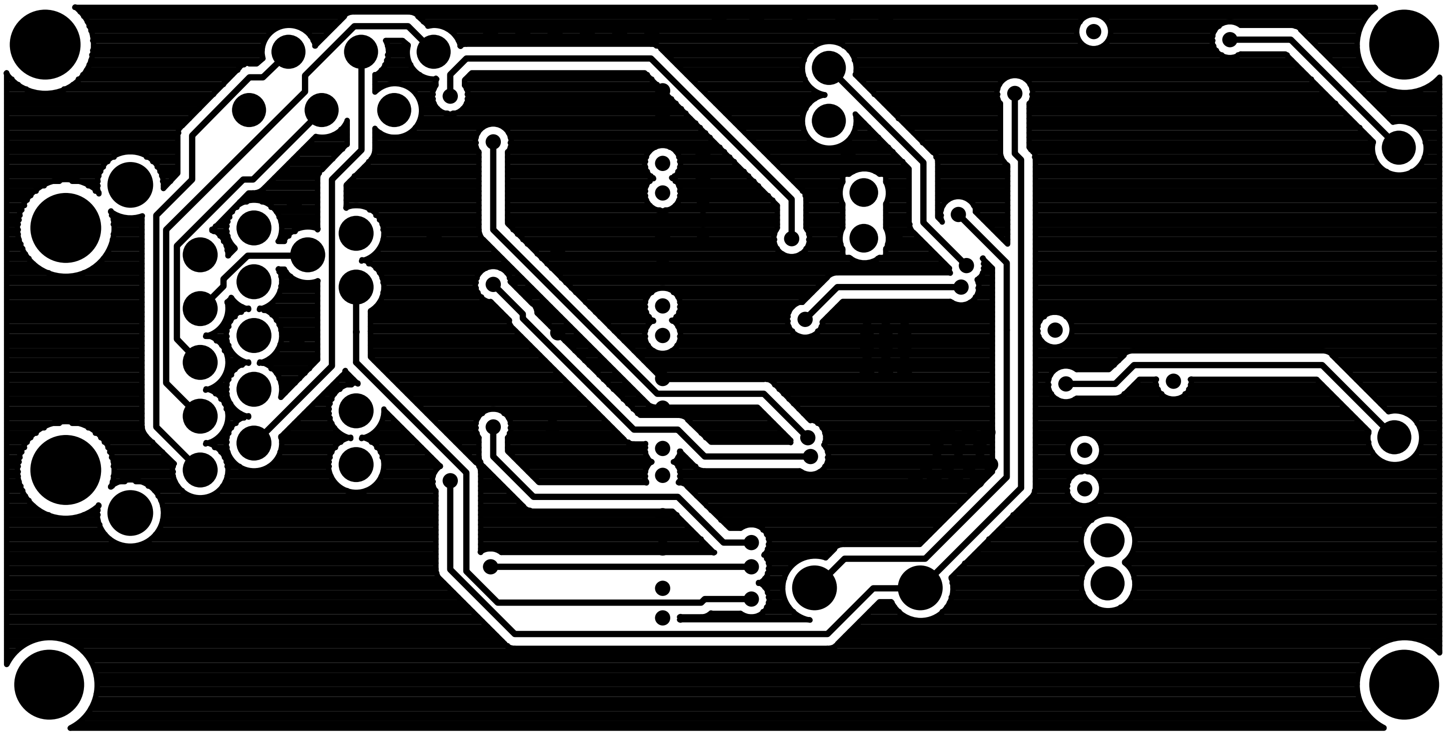


Figure 17.4. Internal 2 (Layer 3)

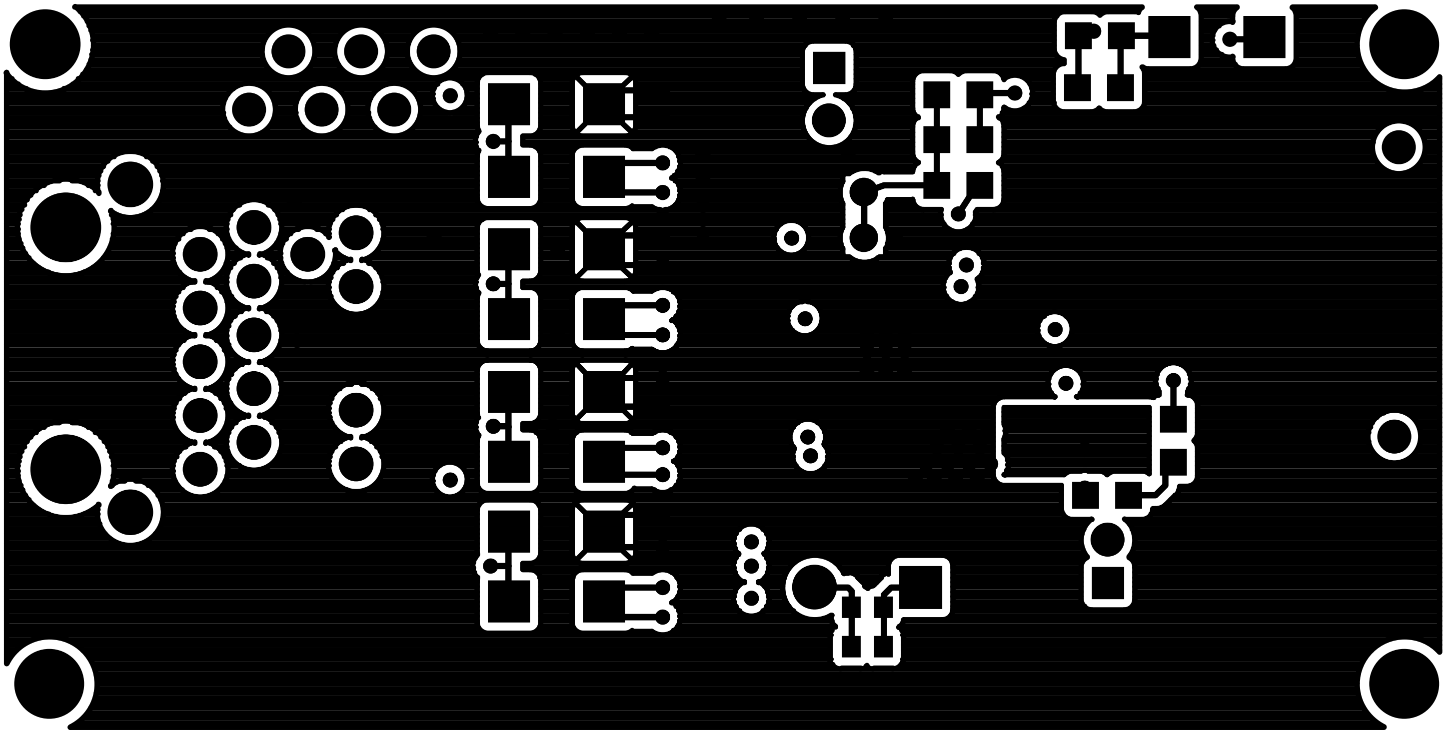


Figure 17.5. Bottom Layer

18. Bill of Materials

The following table is the BOM listing for the standard 5 V output evaluation board with option PoE Class 2.

Table 18.1. Si3406FBC2 Evaluation Board Bill of Materials

Qty	Value	Refer-ence	Rating	Voltage	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
1	12 µF	C1		100V	±20%	Alum_Elec	C2.5X6.3MM-RAD	EEUFC2A120	Panasonic
2	2.2 µF	C2		100V	±10%	X7R	C1210	CL32B225KCJSNNE	Samsung
		C3		100V	±10%	X7R	C1210	CL32B225KCJSNNE	Samsung
1	0.01 µF	C4		100V	±10%	X7R	C0805	C0805X7R101-103K	Venkel
1	820 pF	C5		50V	±10%	C0G	C0805	CC0805KRX7R9BB821	Yageo
3	100 µF	C6		6.3V	±10%	X5R	C1210	C1210X5R6R3-107K	Venkel
		C7		6.3V	±10%	X5R	C1210	C1210X5R6R3-107K	Venkel
		C9		6.3V	±10%	X5R	C1210	C1210X5R6R3-107K	Venkel
2	0.1 µF	C8		100V	±10%	X7R	C0805	C0805X7R101-104K	Venkel
		C22		100V	±10%	X7R	C0805	C0805X7R101-104K	Venkel
1	1 µF	C10		6.3V	±10%	X5R	C0603	C0603X5R6R3-105K	Venkel
1	0.022 µF	C11		50V	±20%	X7R	C0603	C1608X7R1H223M	TDK Corporation
8	1 nF	C12		100V	±10%	X7R	C0603	C0603X7R101-102K	Venkel
		C13		100V	±10%	X7R	C0603	C0603X7R101-102K	Venkel
		C14		100V	±10%	X7R	C0603	C0603X7R101-102K	Venkel
		C15		100V	±10%	X7R	C0603	C0603X7R101-102K	Venkel
		C16		100V	±10%	X7R	C0603	C0603X7R101-102K	Venkel
		C17		100V	±10%	X7R	C0603	C0603X7R101-102K	Venkel
		C18		100V	±10%	X7R	C0603	C0603X7R101-102K	Venkel
		C19		100V	±10%	X7R	C0603	C0603X7R101-102K	Venkel
1	1 nF	C20		50V	±1%	C0G	C0805	C0805C0G500-102F	Venkel
1	0.22 µF	C21		10V	±10%	X7R	C0805	C0805X7R100-224K	Venkel
1	220 µF	C30		6.3V	±20%	Alum_Elec	C2X5MM-RAD	ECA0JM221	Panasonic
1	330 pF	C31		100V	±20%	X7R	C0805	C0805X7R101-331M	Venkel
1	RS1B	D4	1.0A	100V		Standard	DO-214AC	RS1B	Fairchild
1	1N4148W	D5	300mA	100V		Single	SOD-123	1N4148W-7-F	Diodes Inc.
8	S1B	D12	1.0A	100V		Single	DO-214AC	S1B	Fairchild
		D13	1.0A	100V		Single	DO-214AC	S1B	Fairchild
		D14	1.0A	100V		Single	DO-214AC	S1B	Fairchild
		D15	1.0A	100V		Single	DO-214AC	S1B	Fairchild

Qty	Value	Reference	Rating	Voltage	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
		D16	1.0A	100V		Single	DO-214AC	S1B	Fairchild
		D17	1.0A	100V		Single	DO-214AC	S1B	Fairchild
		D18	1.0A	100V		Single	DO-214AC	S1B	Fairchild
		D19	1.0A	100V		Single	DO-214AC	S1B	Fairchild
1	RJ-45	J1				Receptacle	RJ45-SI-52004	SI-52003-F	Bel
1	CONN TRBLK 2	J2				TERM BLK	CONN-1X2-TB	1729018	PHOENIX CONTACT
1	0.16 µH	L1	16A		±20%	Shielded	IND-XAL50xx	XAL5030-161ME	Coilcraft
4	330 Ohm	L3	1500mA			SMT	L0805	BLM21PG331SN1	MuRata
		L4	1500mA			SMT	L0805	BLM21PG331SN1	MuRata
		L5	1500mA			SMT	L0805	BLM21PG331SN1	MuRata
		L6	1500mA			SMT	L0805	BLM21PG331SN1	MuRata
1	FDMA8051L	Q1	10A	40V		N-CHNL	DFN6N2X2P0.65E1.0X1.05	FDMA8051L	Fairchild
1	330 Ω	R1	1/10W		±1%	Thick-Film	R0805	CR0805-10W-3300F	Venkel
1	82 Ω	R2	1/8W		±5%	Thick-Film	R0805	RC0805JR-0782RL	Yageo
2	47 kΩ	R4	1/10W		±5%	Thick-Film	R0805	CR0805-10W-473J	Venkel
		R20	1/10W		±5%	Thick-Film	R0805	CR0805-10W-473J	Venkel
1	8.2 Ω	R5	1/8W		±1%	Thick-Film	R0805	RC0805FR-078R2L	Yageo
1	24.3 kΩ	R8	1/8W		±1%	Thick-Film	R0805	CRCW080524K3FKEA	vishay
1	75 Ω	R10	1/10W		±1%	Thick-Film	R0805	CR0805-10W-75R0F	Venkel
1	88.7 kΩ	R11	1/8W		±1%	Thick-Film	R0805	CRCW080588K7FKEA	Vishay
1	1.2 Ω	R13	1/10W		±5%	Thick-Film	R0805	CR0805-10W-1R2J	Venkel
1	9.1 kΩ	R14	1/8W		±1%	Thick-Film	R0805	RC0805FR-079K1L	Yageo
1	3.24 kΩ	R15	1/8W		±1%	Thick-Film	R0805	CRCW08053K24FKEA	Vishay
4	Standoff	SO1				HDW		2397	SPC Technology

Qty	Value	Reference	Rating	Voltage	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
		SO2				HDW		2397	SPC Technology
		SO3				HDW		2397	SPC Technology
		SO4				HDW		2397	SPC Technology
1	FA2671	T1	10W				XFMR-FA2671	FA2671	Coilcraft
1	Si3406	U1		120V		PD	QFN20N5X5P0.8	Si3406	SiLabs

19. Appendix—Si3406 Non-ISO-FB Design and Layout Checklist

Although the EVB design is pre-configured as a Class 2 PD with 5 V output, the schematics and layouts can easily be adapted to meet a wide variety of common output voltages and power levels.

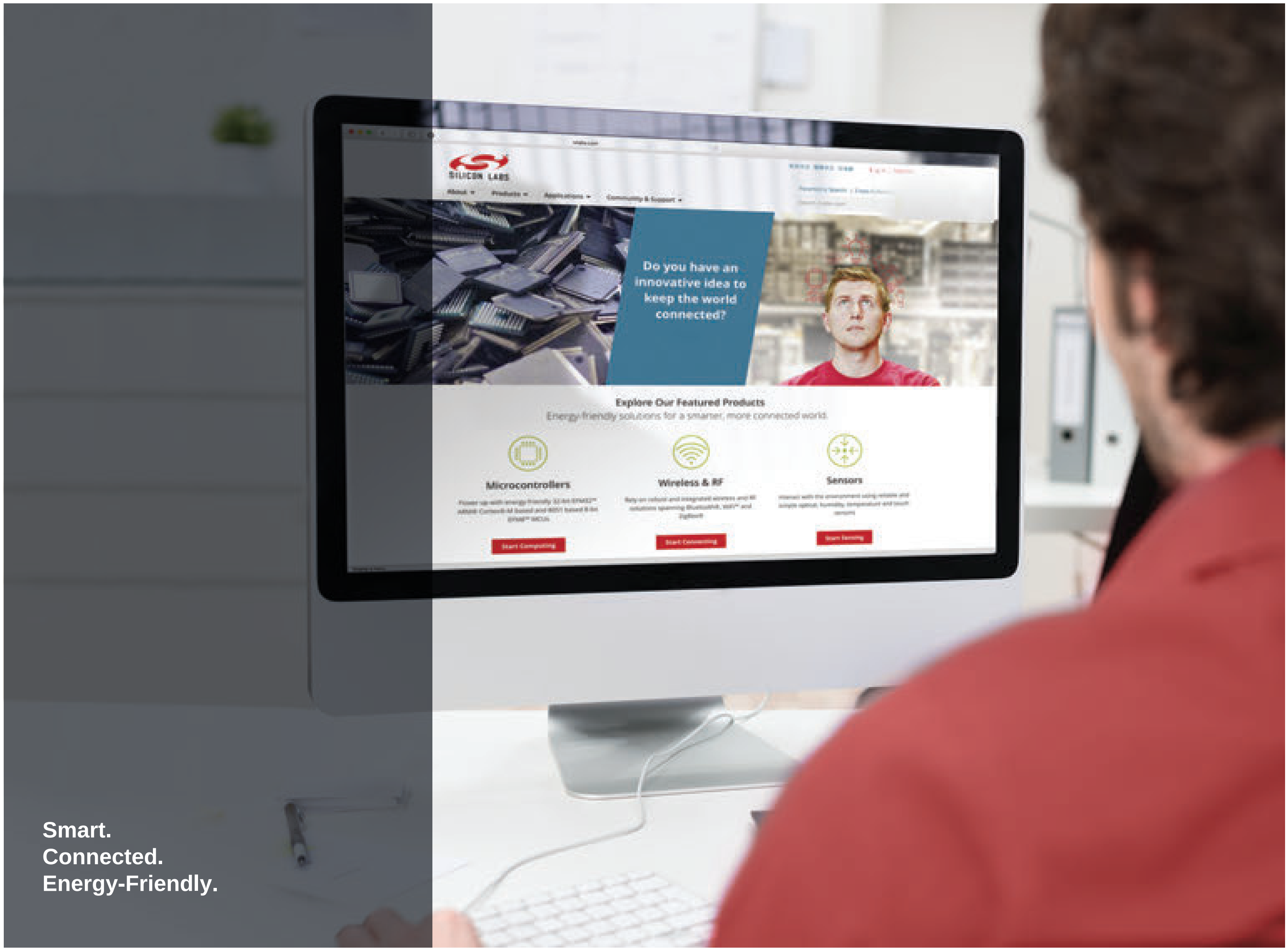
The complete EVB design databases for the standard 5 V/Class 2 configuration are located at www.silabs.com/PoE link. Silicon Labs strongly recommends using these EVB schematics and layout files as a starting point to ensure robust performance and avoid common mistakes in the schematic capture and PCB layout processes.

Below is a recommended design checklist that can assist in trouble-free development of robust PD designs.

Refer also to the Si3406-non-ISO-FB data sheet and AN1130 when using the following checklist.

1. Design Planning checklist:
   a. Determine if your design requires an isolated or non-isolated topology. For more information, see AN1130.
   b. Silicon Labs strongly recommends using the EVB schematics and layout files as a starting point as you begin integrating the Si3406-non-ISO-FB into your system design process.
   c. Determine your load's power requirements (i.e., VOUT and IOUT consumed by the PD, including the typical expected transient surge conditions). In general, to achieve the highest overall efficiency performance of the Si3406-non-isolated Flyback, choose the highest output voltage option used in your PD and then post regulate to the lower supply rails, if necessary.
   d. Based on your required PD power level, select the appropriate class resistor RCLASS value by referring to AN1130.
2. General Design checklist:
   a. ESD caps (C12–C19 in Figure 2.3 Si3406 Non-Isolated Flyback EVB Schematic: 5 V, Class 2 PD on page 4) are strongly recommended for designs where system-level ESD (IEC6100-4-2) must provide >15 kV tolerance.
   b. If your design uses an AUX supply, be sure to include a 3 Ω surge limiting resistor in series with the AUX supply for hot insertion. Refer to AN1130 when AUX supply is 48 V.
3. Layout Guidelines:
   a. Make sure VNEG pin of the Si3406 is connected to the backside of the QFN package with an adequate thermal plane, as noted in the data sheet and AN1130.
   b. Keep the trace length from SWO and to VSS as short as possible. Make all of the power (high current) traces as short, direct, and thick as possible. It is a good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per ampere.
   c. Usually, one standard via handles 200 mA of current. If the trace needs to conduct a significant amount of current from one plane to the other, use multiple vias.
   d. Keep the circular area of the loop from the Switcher FET output to the inductor or transformer and returning from the input filter capacitors (C1–C3) to VSS as small a diameter as possible. Also, minimize the circular area of the loop from the output of the inductor or transformer to the Schottky diode and returning through the first stage output filter capacitor back to the inductor or transformer as small as possible. If possible, keep the direction of current flow in these two loops the same.
   e. Keep the high power traces as short as possible.
   f. Keep the feedback and loop stability components as far from the transformer/inductor and noisy power traces as possible.
   g. If the outputs have a ground plane or positive output plane, do not connect the high current carrying components and the filter capacitors through the plane. Connect them together, and then connect to the plane at a single point.

To help ensure first-pass success, contact our customer support by submitting a help ticket and uploading your schematics and layout files for review.



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