SprIoT 6UL

Schematics DevBoard

Table of Content

Revision History

Rev. Code	Date	By	Description
A	2016-09-08		

1. Unless Otherwise Specified:

   All resistors are in ohms, 10%, 1/8 Watt,0603
   All capacitors are in uF, 20%, 50V,0603
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

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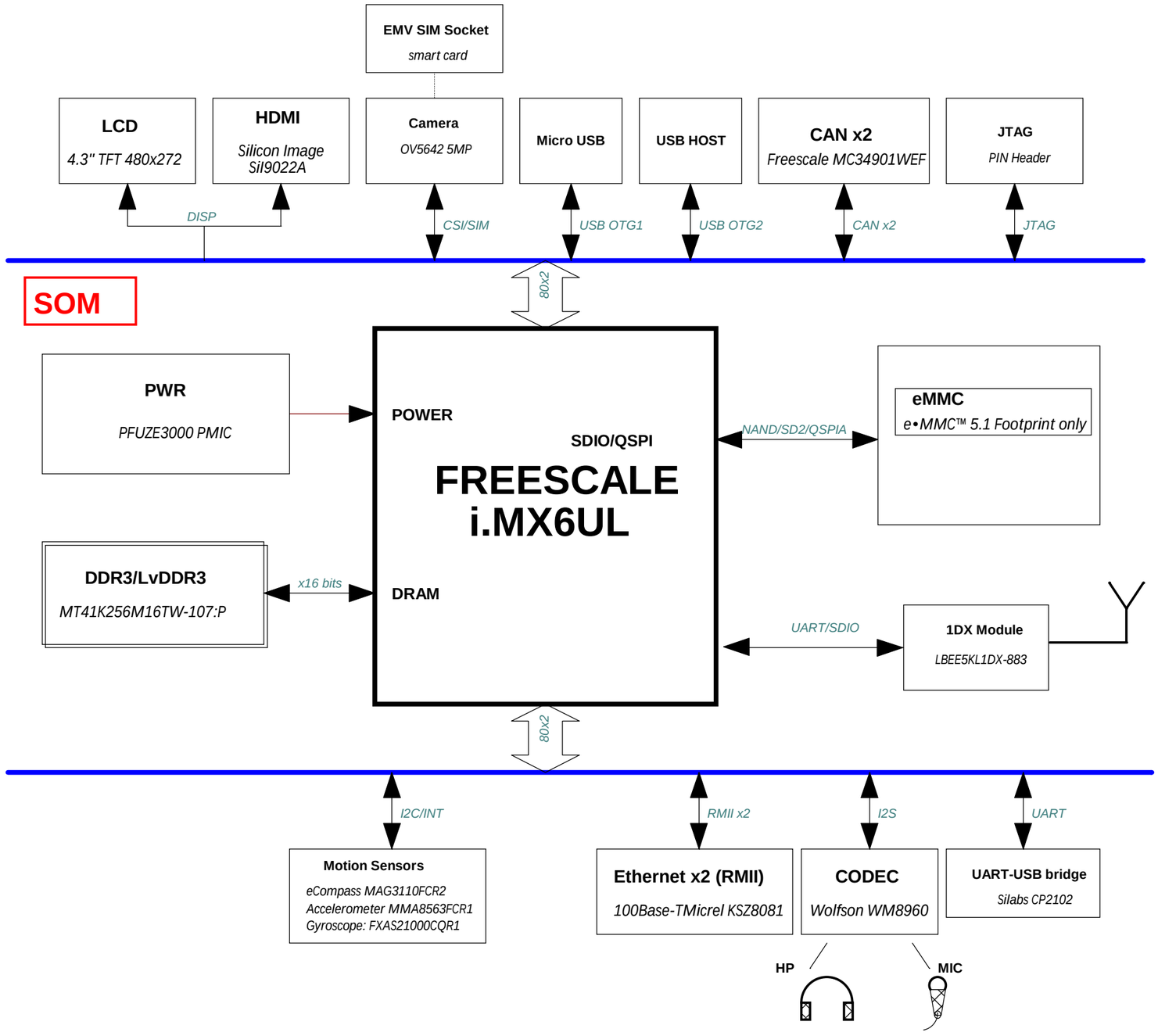
Title: Title and Rev History			
Size: C	Document Number: 801108	Engineer: VH	Rev: PR2
Date: Tuesday, August 01, 2017	Sheet 1 of 11		

i.MX6UL-SOM EVK Block Diagram



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Block Diagram			
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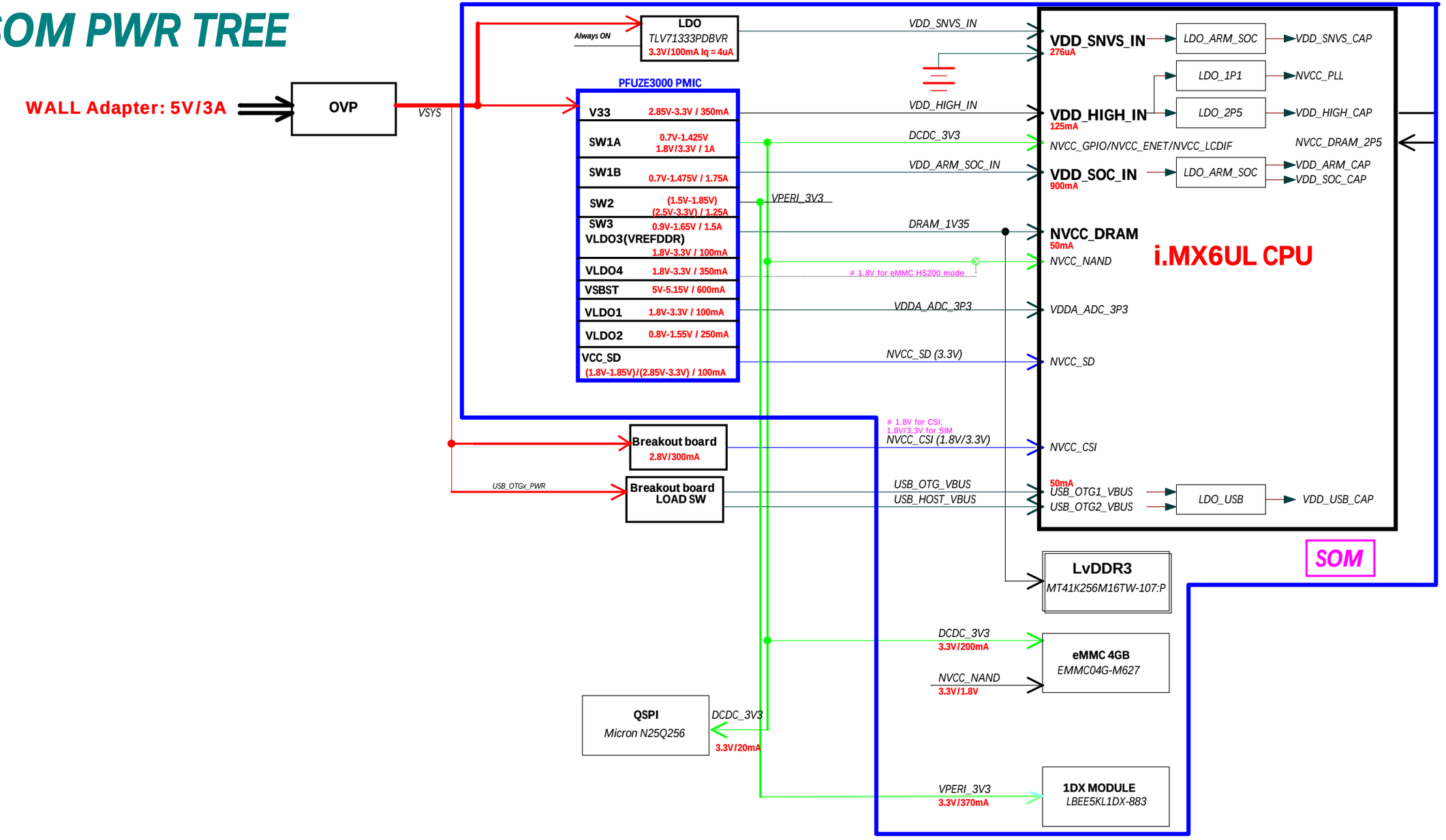
SOM PWR TREE



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SDIO interface maping.

i.MX6UL	Type 1DX
SD1_CMD	SDIO_CMD
SD1_CLK	SDIO_CLK
SD1_DATA3	SDIO_D3
SD1_DATA2	SDIO_D2
SD1_DATA1	SDIO_D1
SD1_DATA0	SDIO_D0

WIFI interface maping.

i.MX6UL	Type 1DX
SNVS_TAMPER1	WL_REG_ON
SNVS_TAMPER3	WL_GPIO_HOST_WAKE

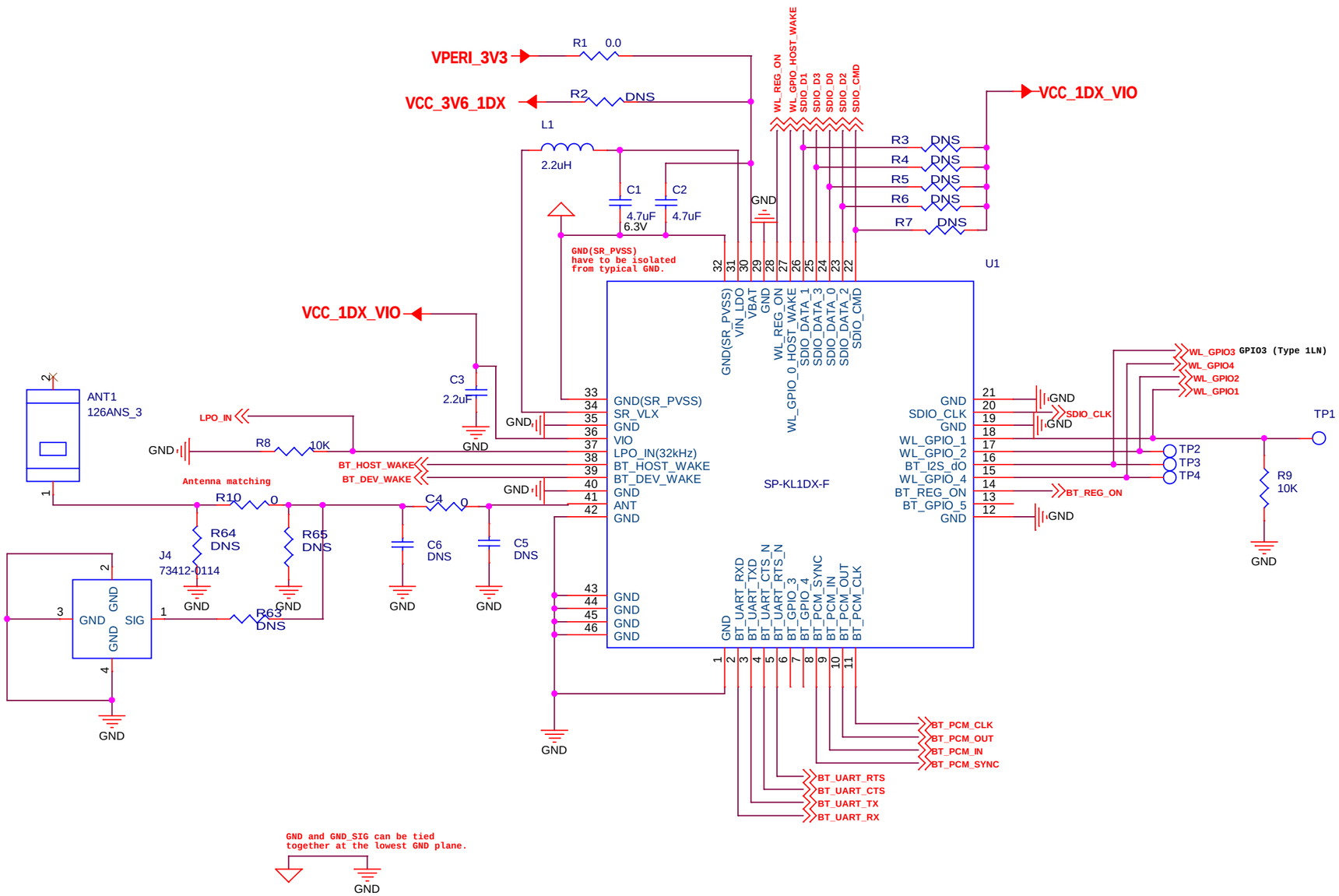
UART interface maping.

i.MX6UL	Type 1DX
HCI_UART2_TXD	BT_UART_RX
HCI_UART2_RXD	BT_UART_TX
HCI_UART2_CTS	BT_UART_CTS
HCI_UART2_RTS	BT_UART_RTS

Bluetooth control interface maping.

i.MX6UL	Type 1DX
UART3_RTS_B	BT_REG_ON
SNVS_TAMPER6	BT_HOST_WAKE
UART3_CTS_B	BT_DEV_WAKE

LPO_IN ⟵ WB_LO_IN



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Title: 1DX Module			
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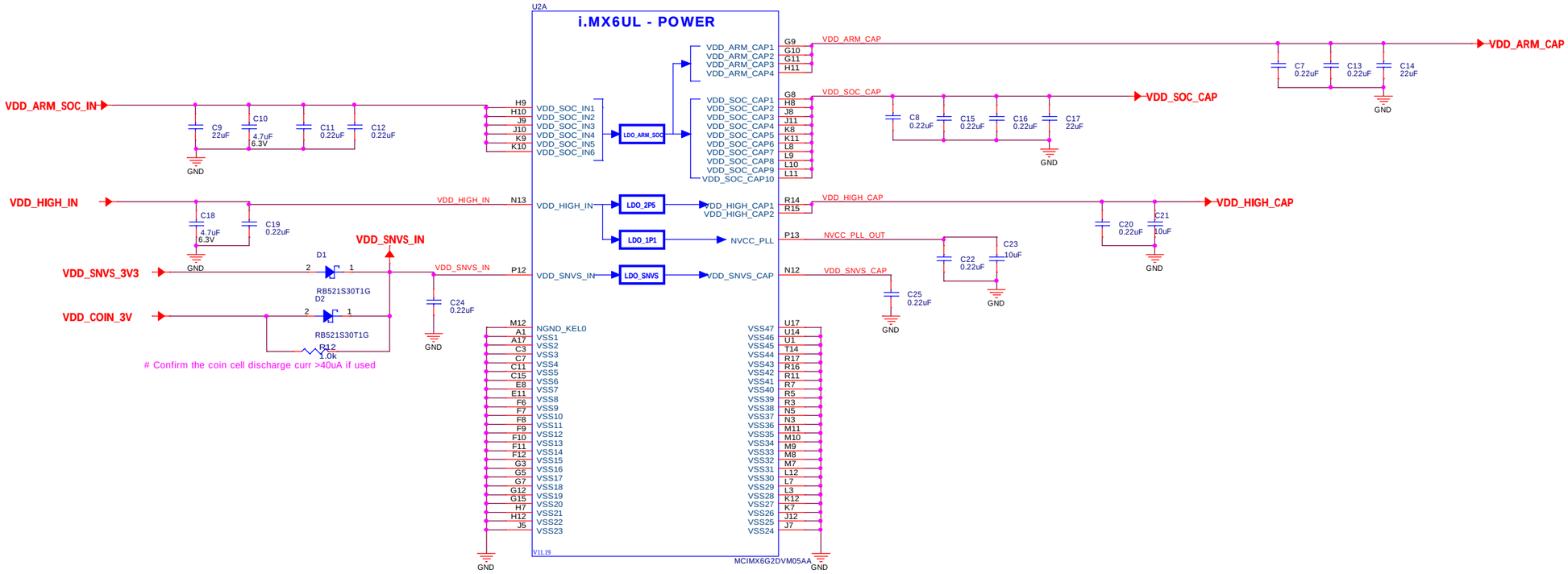
i.MX6UL PWR



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Title	CPU PWR		
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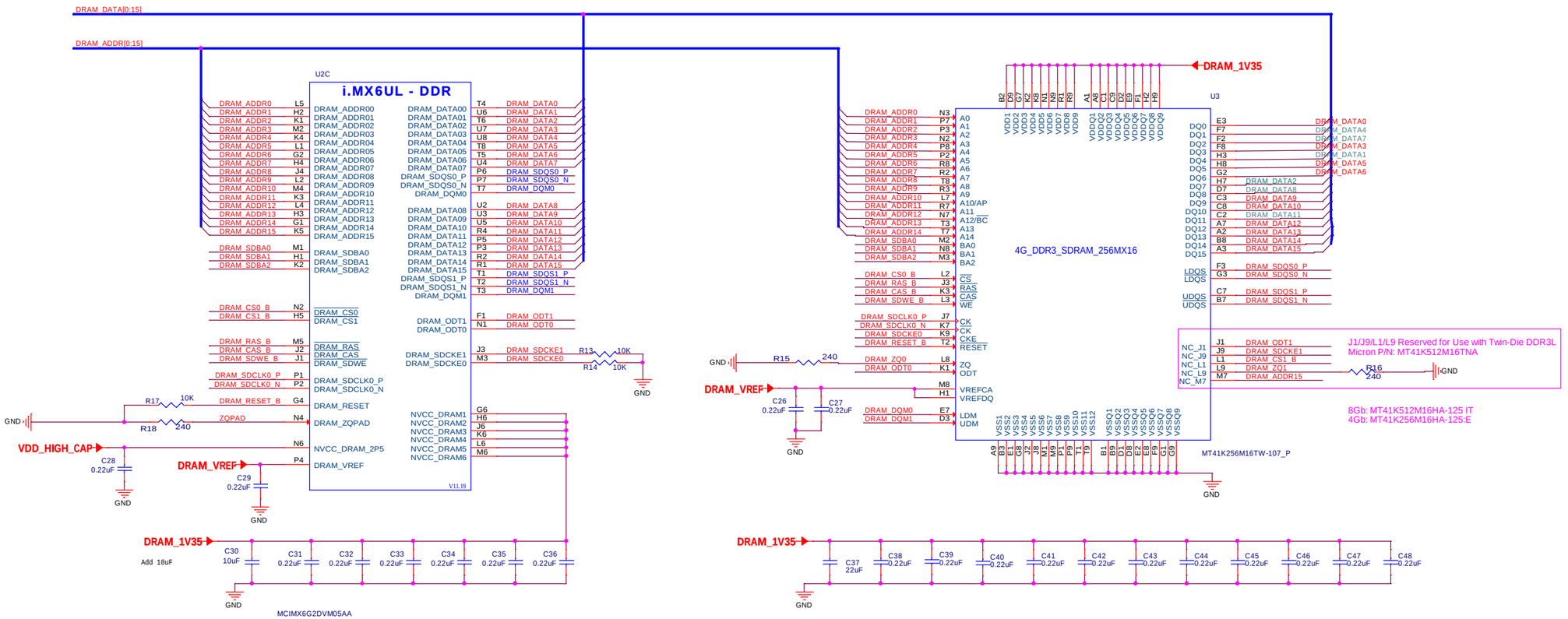
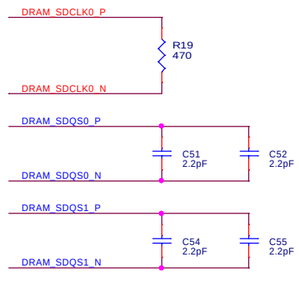
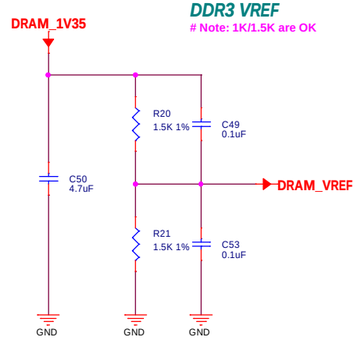
DDR3/LvDDR3



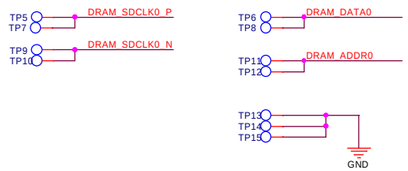
Note:
CLK termination: Place R54 close to U2.



DDR3 VREF
 # Note: 1K/1.5K are OK



DRAM Test Points



 # Note:
Test points for signal integrity measurement

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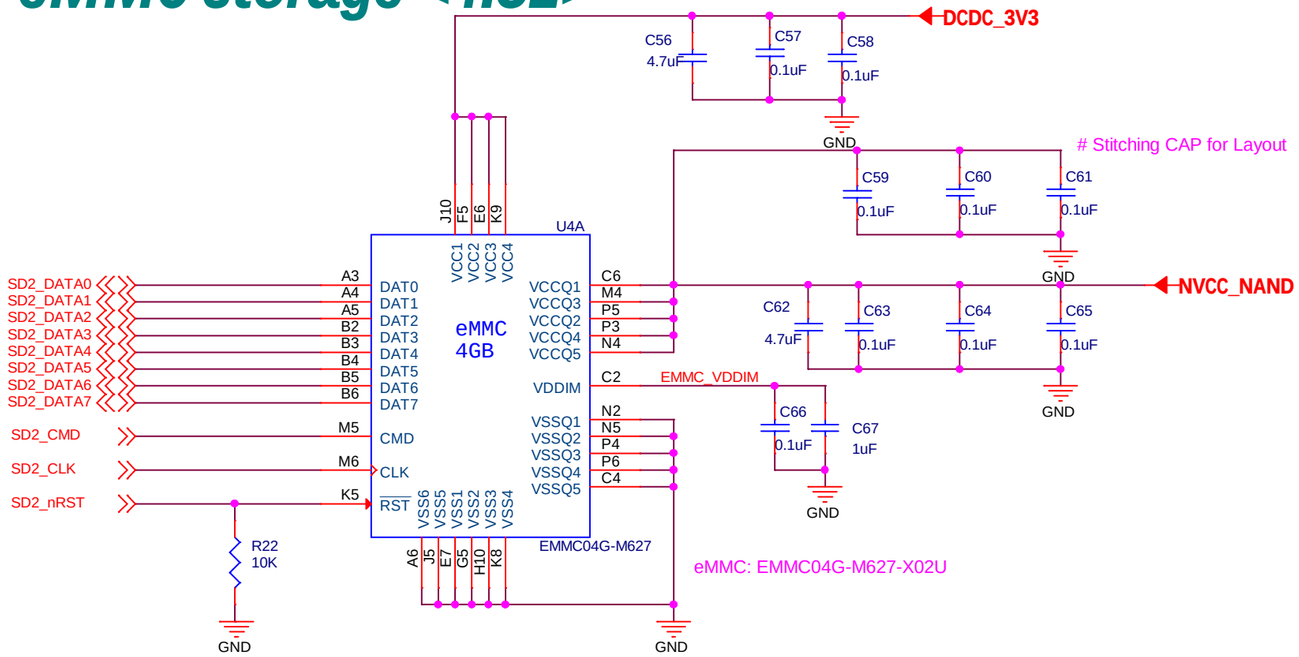
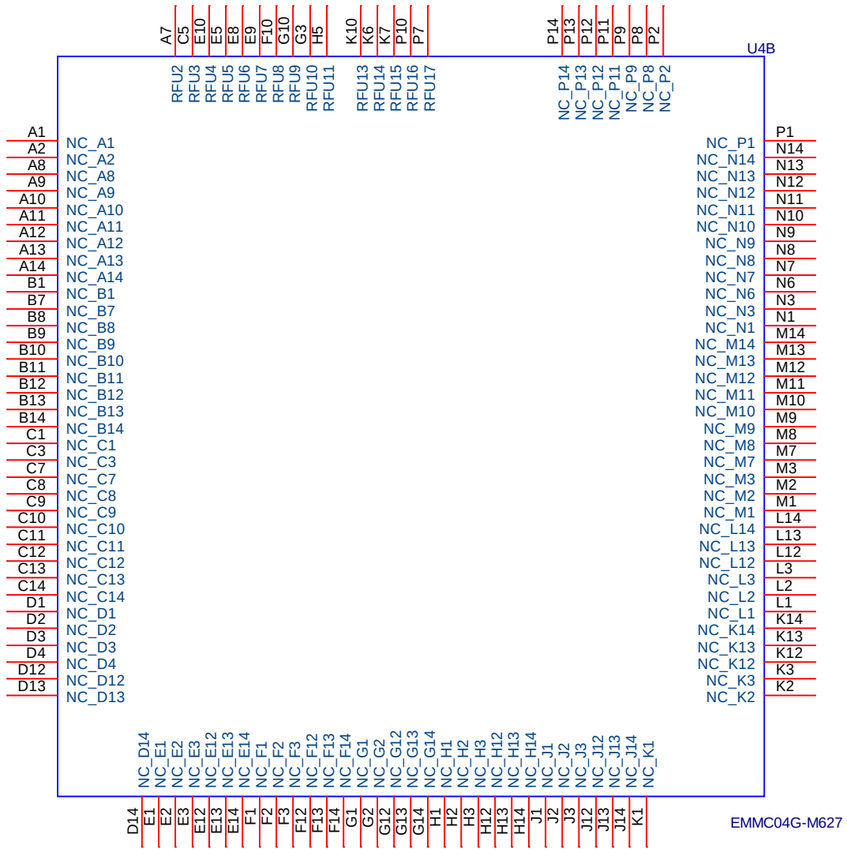
eMMC Storage <4.51>





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MX6UL PERI

U2J i.MX6UL - NAND

NVCC_NAND → E7 NVCC_NAND; C72 0.22uF → GND

C5	NAND_CE0	NAND_CE0
B5	NAND_CE1	NAND_CE1
B4	R24 0	NAND_ALE
A4	NAND_CLE	NAND_CLE
D8	R25 10	NAND_nRE
C8	R26 10	NAND_nWE
D5	NAND_nWP	
A3	NAND_nREADY	
E6	R27 10	NAND_DQS
D7	NAND_DATA0	NAND_DATA00
B7	NAND_DATA1	NAND_DATA01
A7	NAND_DATA2	NAND_DATA02
D6	NAND_DATA3	NAND_DATA03
C6	NAND_DATA4	NAND_DATA04
B6	NAND_DATA5	NAND_DATA05
A6	NAND_DATA6	NAND_DATA06
A5	NAND_DATA7	NAND_DATA07

C70 DNS; C71 18pF; GND

MCIMX6G2DVM05AA

 # QSPI_DQS only for loop back mode test

NAND/eMMC/MicroSD/QSPI

NAND_nCE0	QSPIA_DATA1
NAND_nCE1	QSPIA_DATA2
NAND_ALE	SD2_nRST
NAND_CLE	QSPIA_DATA3
NAND_nRE	SD2_CLK
NAND_nWE	SD2_CMD
NAND_nWP	QSPIA_SCLK
NAND_nREADY	QSPIA_DATA0
NAND_DQS	QSPIA_nSS0
NAND_DATA0	SD2_DATA0
NAND_DATA1	SD2_DATA1
NAND_DATA2	SD2_DATA2
NAND_DATA3	SD2_DATA3
NAND_DATA4	SD2_DATA4
NAND_DATA5	SD2_DATA5
NAND_DATA6	SD2_DATA6
NAND_DATA7	SD2_DATA7

Camera/EVMSIM

U2E i.MX6UL - CSI

NVCC_CSI → F4 NVCC_CSI; C74 0.22uF → GND

F5	CSI_MCLK	CSI_MCLK
E5	CSI_PIXCLK	CSI_PIXCLK
F2	CSI_VSYNC	CSI_VSYNC
F3	CSI_HSYNC	CSI_HSYNC
E4	CSI_DATA0	CSI_DATA00
E3	CSI_DATA1	CSI_DATA01
E2	CSI_DATA2	CSI_DATA02
E1	CSI_DATA3	CSI_DATA03
D4	CSI_DATA4	CSI_DATA04
D3	CSI_DATA5	CSI_DATA05
D2	CSI_DATA6	CSI_DATA06
D1	CSI_DATA7	CSI_DATA07

CSI_DATA[7:0]

U2K i.MX6UL - GPIO

NVCC_GPIO → J13 NVCC_GPIO; C79 0.22uF → GND

K13	GPIO_0	GPIO1_IO00
L15	GPIO_1	GPIO1_IO01
L14	GPIO_2	GPIO1_IO02
L17	GPIO_3	GPIO1_IO03
M16	GPIO_4	GPIO1_IO04
M17	GPIO_5	GPIO1_IO05
K17	GPIO_6	GPIO1_IO06
L16	GPIO_7	GPIO1_IO07
N17	GPIO_8	GPIO1_IO08
M15	GPIO_9	GPIO1_IO09

GPIO_0	USB_OTG1_ID
GPIO_1	USB_OTG1_OC
GPIO_2	USB_HST_PWR
GPIO_3	USB_HST_OC
GPIO_4	USB_OTG1_PWR
GPIO_5	ADCx_INS
GPIO_6	ENET_MDIO
GPIO_7	ENET_MDC
GPIO_8	BLT_PWM

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C83 DNS; C84 18pF; GND

U2H i.MX6UL - ENET

NVCC_ENET → F13 NVCC_ENET; C85 0.22uF; C86 0.22uF → GND

 # 100M MII/RMII

 # Ethernet / SPI

E15	ENET1_TXD0	ENET1_TXD0
E14	ENET1_TXD1	ENET1_TXD1
F15	ENET1_TXEN	ENET1_TXEN
F14	R31 10	ENET1_TX_CLK
F16	ENET1_RXD0	ENET1_RXD0
E17	ENET1_RXD1	ENET1_RXD1
D15	ENET1_RXER	ENET1_RXER
E16	ENET1_CRS_DV	ENET1_CRS_DV
A15	ENET2_TXD0	ENET2_TXD0
A16	ENET2_TXD1	ENET2_TXD1
B15	ENET2_TXEN	ENET2_TXEN
D17	R32 10	ENET2_TX_CLK
C17	ENET2_RXD0	ENET2_RXD0
C16	ENET2_RXD1	ENET2_RXD1
D16	ENET2_RXER	ENET2_RXER
B17	ENET2_CRS_DV	ENET2_CRS_DV

ENET1_RXD0 → TP16

ENET2_TXD1	SPI4_SCLK
ENET2_TXEN	SPI4_MOSI
ENET2_TX_CLK	SPI4_MISO
ENET2_RXD0	TP17
ENET2_RXER	SPI4_SS0

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C89 18pF; C90 18pF; GND

U2D i.MX6UL - LCD

 # LCD RGB

NVCC_LCDIF → E13 NVCC_LCD; C73 0.22uF → GND

C68 DNS; C69 DNS; GND

A8	R23 10	LCD_PCLK
B8	LCD_DE	LCD_ENABLE
D9	LCD_HSYNC	LCD_HSYNC
C9	LCD_VSYNC	LCD_VSYNC
E9	LCD_RESET	LCD_RESET

B9	LCD_DATA0	LCD_DATA00
A9	LCD_DATA1	LCD_DATA01
E10	LCD_DATA2	LCD_DATA02
D10	LCD_DATA3	LCD_DATA03
C10	LCD_DATA4	LCD_DATA04
B10	LCD_DATA5	LCD_DATA05
A10	LCD_DATA6	LCD_DATA06
D11	LCD_DATA7	LCD_DATA07
B11	LCD_DATA8	LCD_DATA08
A11	LCD_DATA9	LCD_DATA09
E12	LCD_DATA10	LCD_DATA10
D12	LCD_DATA11	LCD_DATA11
C12	LCD_DATA12	LCD_DATA12
B12	LCD_DATA13	LCD_DATA13
A12	LCD_DATA14	LCD_DATA14
D13	LCD_DATA15	LCD_DATA15
C13	LCD_DATA16	LCD_DATA16
B13	LCD_DATA17	LCD_DATA17
A13	LCD_DATA18	LCD_DATA18
D14	LCD_DATA19	LCD_DATA19
C14	LCD_DATA20	LCD_DATA20
B14	LCD_DATA21	LCD_DATA21
A14	LCD_DATA22	LCD_DATA22
B16	LCD_DATA23	LCD_DATA23

LCD_DATA[23:0]

MCIMX6G2DVM05AA

U2F i.MX6UL - USB

USB_OTG1_VBUS → T12; C75 1uF → GND

USB_OTG2_VBUS → U12; C78 1uF → GND

LDO_USB → VDD_USB_CAP → R12 → C76 10uF; C77 0.1uF; GND → VDDUSB

T15	USB_OTG1_DN	USB_OTG1_DN
U15	USB_OTG1_DP	USB_OTG1_DP
U16	nUSB_OTG_CHD	nUSB_OTG_CHD
T13	USB_OTG2_DN	USB_OTG2_DN
U13	USB_OTG2_DP	USB_OTG2_DP

 # Layout: Route 90ohm DIFF

MCIMX6G2DVM05AA

NVCC_SD

U2I i.MX6UL - SD

NVCC_SD → C4 NVCC_SD1; C82 0.22uF → GND

C80 DNS; C81 DNS; R28 DNS; R29 DNS; GND

C1	SD1_CLK	SD1_CLK
C2	SD1_CMD	R30 10 SD1_CLK
B3	SD1_DATA0	SD1_DATA0
B2	SD1_DATA1	SD1_DATA1
B1	SD1_DATA2	SD1_DATA2
A2	SD1_DATA3	SD1_DATA3

SD1_CLK; SD1_CMD; SD1_DATA0

MCIMX6G2DVM05AA

 # Murata type 1DX

U2G i.MX6UL - ADC

VDDA_ADC_3P3 → C87 0.1uF; C88 1uF; GND

R33 DNS

L13	VDDA_ADC_3P3
M13	ADC_VREFH

ADC_VREFH

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JTAG Debug

TP18 JTAG_nTRST
TP19 JTAG_TDI
TP20 JTAG_TMS
TP21 JTAG_TCK
TP22 JTAG_TDO
TP23 POR_B

i.MX6UL RESET

VDD_SNVS_IN
R34 DNS
POR_B — R35 1.0k
500ms delay on POR_B 32KHz
C91 0.1uF
GND

U2B
i.MX6UL - CONTROL

ONOFF — ONOFF PU (100K) R8; POR_B_CPU PU (100K) P8 → ONOFF, POR
BOOT_MODE0 — BOOT_MODE0 PD (100K) T10 → BOOT_MODE0
BOOT_MODE1 — BOOT_MODE1 PD (100K) U10 → BOOT_MODE1
TEST_MODE PD (100K) N7 → TEST_MODE
GND

SNVS_TAMPER0 R10 → SNVS_TAMPER0
SNVS_TAMPER1 R9 → SNVS_TAMPER1
SNVS_TAMPER2 P11 → SNVS_TAMPER2
SNVS_TAMPER3 P10 → SNVS_TAMPER3
SNVS_TAMPER4 P9 → SNVS_TAMPER4
SNVS_TAMPER5 N8 → SNVS_TAMPER5
SNVS_TAMPER6 N11 → SNVS_TAMPER6
SNVS_TAMPER7 N10 → SNVS_TAMPER7
SNVS_TAMPER8 N9 → SNVS_TAMPER8
SNVS_TAMPER9 R6 → SNVS_TAMPER9

PMIC_STBY_REQ — PMIC_STBY_REQ PD (100K) U9 → CCM_PMIC_STBY_REQ
PMIC_ON_REQ — PU (100K) T9 → SNVS_PMIC_ON_REQ

VDD_SNVS_IN PWR domain, IO CFG is need to prevent leakage. When TMAPER PIN used as GPIO, need to PULL DOWN 1M to GND to give a fixed state to the PIN to reduce the power consumption, Just for TO1.0

DNS R62 — GND
XTALI T16 → XTALI
XTALO T17 → XTALO
NVCC_PLL

Y1 24MHZ
C92 12pF — GND
C93 12pF — GND

RTC_XTALI T11 → RTC_XTALI
RTC_XTALO U11 → RTC_XTALO
VDD_SNVS_CAP

Y2 32.768 KHz
C94 12pF — GND
C95 12pF — GND

R13 → GPANAIO
NT_HIGH_VDD

V11.19

JTAG_TCK M14 PU (47K) JTAG_TCK → JTAG_TCK
JTAG_TMS P14 PU (47K) JTAG_TMS → JTAG_TMS
JTAG_TDI N16 PU (47K) JTAG_TDI → JTAG_TDI
JTAG_TDO N15 PU (100K) JTAG_TDO → JTAG_TDO
JTAG_TRST N14 PU (47K) JTAG_nTRST → JTAG_nTRST
JTAG_MOD P15 PU (100K) JTAG_MOD → JTAG_MOD
JTAG_MOD → SPDIF_TX

CCM_CLK1_N P16
CCM_CLK1_P P17

NVCC_GPIO

 # NVCC_GPIO (J13) and NVCC_UART (H13) should share one 0.22uF de-coupling cap. There is no PCB space to fit two caps.

NVCC_UART H13 → NVCC_UART

UART1_TX_DATA K14 UART1_TXD → UART1_TXD
UART1_RX_DATA K16 UART1_RXD → UART1_RXD
UART1_RTS J14 UART1_RTS → UART1_RTS
UART1_CTS K15 UART1_CTS → UART1_CTS

UART2_TX_DATA J17 UART2_TXD → HCI_UART2_TXD
UART2_RX_DATA J16 UART2_RXD → HCI_UART2_RXD
UART2_RTS H14 UART2_RTS → UART2_RTS
UART2_CTS J15 UART2_CTS → UART2_CTS
UART2_RTS → CAN2_RX
UART2_CTS → CAN2_TX

UART3_TX_DATA H17 UART3_TXD → HCI_UART2_CTS
UART3_RX_DATA H16 UART3_RXD → HCI_UART2_RTS
UART3_RTS G14 UART3_RTS → UART3_RTS_B
UART3_CTS H15 UART3_CTS → UART3_CTS_B

UART4_TX_DATA G17 UART4_TXD → UART4_TXD
UART4_RX_DATA G16 UART4_RXD → UART4_RXD
UART4_TXD → I2C1_SCL
UART4_RXD → I2C1_SDA

UART5_TX_DATA F17 UART5_TXD → UART5_TXD
UART5_RX_DATA G13 UART5_RXD → UART5_RXD

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PFUZE3000 PMIC

i.MX6UL PWR

Power Rail	MIN	TYP	MAX	CURR
VDD_SNVS_IN	2.4	3	3.6	276uA
VDD_HIGH_IN	2.8	3	3.6	125mA
VDD_ARM_IN	0.9	1.275	1.5	400mA
VDD_SOC_IN	0.9	1.275	1.5	500mA
NVCC_DRAM	1.425	1.5	1.575	50mA
	1.283	1.35	1.45	
	1.14	1.2	1.3	
NVCC_xxx	1.65	1.8/2.5/3.3	3.6	
VDDA_ADC_3P3	3	3.3	3.6	
USB_OTG1_VBUS	4.4	5	5.25	50mA
USB_OTG2_VBUS				

VSYS → VSYS_4V4

C96 47uF, C97 47uF, C98 4.7uF, C99 0.1uF, C100 47uF, C101 47uF, C102 4.7uF, C103 0.1uF — GND

Q1 FDMA908PZ

C104 470pF

C105 0.1uF, C106 0.22uF, C107 0.1uF, C108 0.1uF

DCDC_3V3

R36 0

VSYS_4V4

DCDC

VFWR, LDOG_VIN, VCOREDIG, VCOREREF, VCORE, VDDIO, VDDOTP

SW1AFB, SW1ALX — L2 1.5uH — DCDC_3V3

C111 22uF, C109 22uF, C112 10uF

SW1BFB, SW1BLX — L3 1.5uH — VDD_ARM_SOC_IN

1.8V for iMX6.

C114 22uF, C115 22uF, C116 10uF

SW2FB, SW2LX — L4 1.5uH — VPERI_3V3

C118 22uF, C119 22uF, C120 10uF

SW3FB, SW3LX — L5 1.5uH — DRAM_1V35

C122 22uF, C123 22uF, C124 10uF

SW1AIN C113 4.7uF

SW1BIN C110 4.7uF

SW2IN C117 4.7uF

SW3IN C121 4.7uF

SWBSTLX, SWBSTFB

LDO

VLDO1 — C125 4.7uF — VDDA_ADC_3P3

VLDO2 — C127 4.7uF — TP42

VLDO3 — C129 4.7uF — TP43

VLDO4 — C131 4.7uF — VLDO_1V8

VCC_SD — C133 4.7uF — NVCC_SD

V33 — C135 4.7uF — R44 0 — VDD_OSC_3V3 / VDD_HIGH_IN

VSNVS — R46 DNS — VDD_SNVS_3V3

C137 0.22uF, C138 0.22uF — GND

VINREFDDR — TP44

C139 0.1uF, C140 0.1uF — GND

VHALF

VREFDDR — C141 1uF — GND

VLDO1IN C126 1uF — GND

VPERI_3V3

VLDO2IN C128 1uF — GND

VLDO34IN C130 1uF — GND

VIN2 C132 0.22uF, C134 4.7uF — GND

LICELL — VDD_COIN_3V — R45 1.0k — C136 0.1uF — GND

SDA — I2C1_SDA — R47 0

SCL — I2C1_SCL — R48 0

PWRON — PMIC_ON_REQ — R49 1.0k

SD_VSEL — R50 10K — GND — Open Drain

INTB — PMIC_nINT — Open Drain

RESETBMCU — POR_B — Open Drain

STANDBY — PMIC_PWRON

GNDREF, GNDREF1, GNDREF2, EPAD, ICTEST

U5 MC32PF3000A7EP — GND

DCDC_3V3 — R41 1.5K 1% — R42 1.5K 1% — R43 100K — VDD_SNVS_3V3

1% 1%

Additional current may be drawn in the coin cell mode when RESETBMCU is pulled up to VSNVS due an internal path from RESETBMCU to VIN. The additional current is <30 uA with a pull up resistor of 100 k?. The i.MX 6 processors have an internal pull-up from the POR_B pin to the VDD_SNVS_IN pin. If additional current in the coin cell mode is not desired for i.MX6 applications, use an external switch to disconnect the RESETBMCU path when VIN is removed. Pull-up RESETBMCU to a rail that is off in the coin cell mode, for non-i.MX 6 applications.

VDD_SNVS_3V3 — R57 100K — R58 100K — R60 100K — Q2-1 UM6K34NTCN — R59 DNS — GND

PMIC_STBY_REQ

When PMIC_STBY_REQ pad is driving high state in SUSPEN mode, the output voltage level is about 2.0V. This voltage is lower than the 3.0V VDD_SNVS_IN supply voltage.

DNP

XC6220B361ER-G U6 — Vin, Vout, Vss, Pad, CE

VSYS — C142 10uF DNS — GND

C143 10uF DNS — GND

TP24 — # 3.6V/1A — VCC_3V6_1DX

SNVS

VSYS — C144 10uF — C145 0.1uF — GND

U7 TLV71333PDBVR — IN, OUT, GND, EN, NC

C146 4.7uF, C147 0.1uF — GND

TP25 — # 3.3V/100mA Iq = 4uA — VDD_SNVS_3V3

DCDC_3V3 — NVCC_3V3 — NVCC_LCDIF, NVCC_GPIO, NVCC_ENET, NVCC_UART

DCDC_3V3 / VLDO_1V8 — R51 0, R52 DNS — NVCC_NAND

1.8V for eMMC HS200 mode

DCDC_3V3 / VLDO_1V8 — R53 DNS, R54 DNS — NVCC_CSI

CSI default 2.8V from the base board

NVCC_SD / DCDC_3V3 — R55 0, R56 DNS — VCC_1DX_VIO

muRata
Murata, Inc.
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Carrollton, TX 75007

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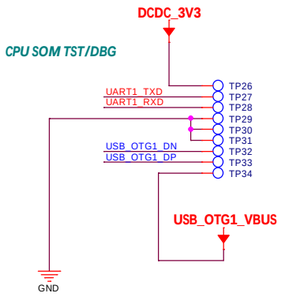
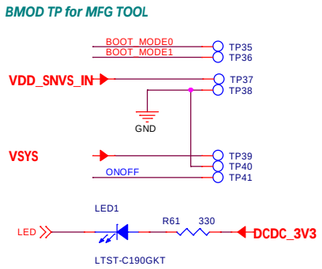
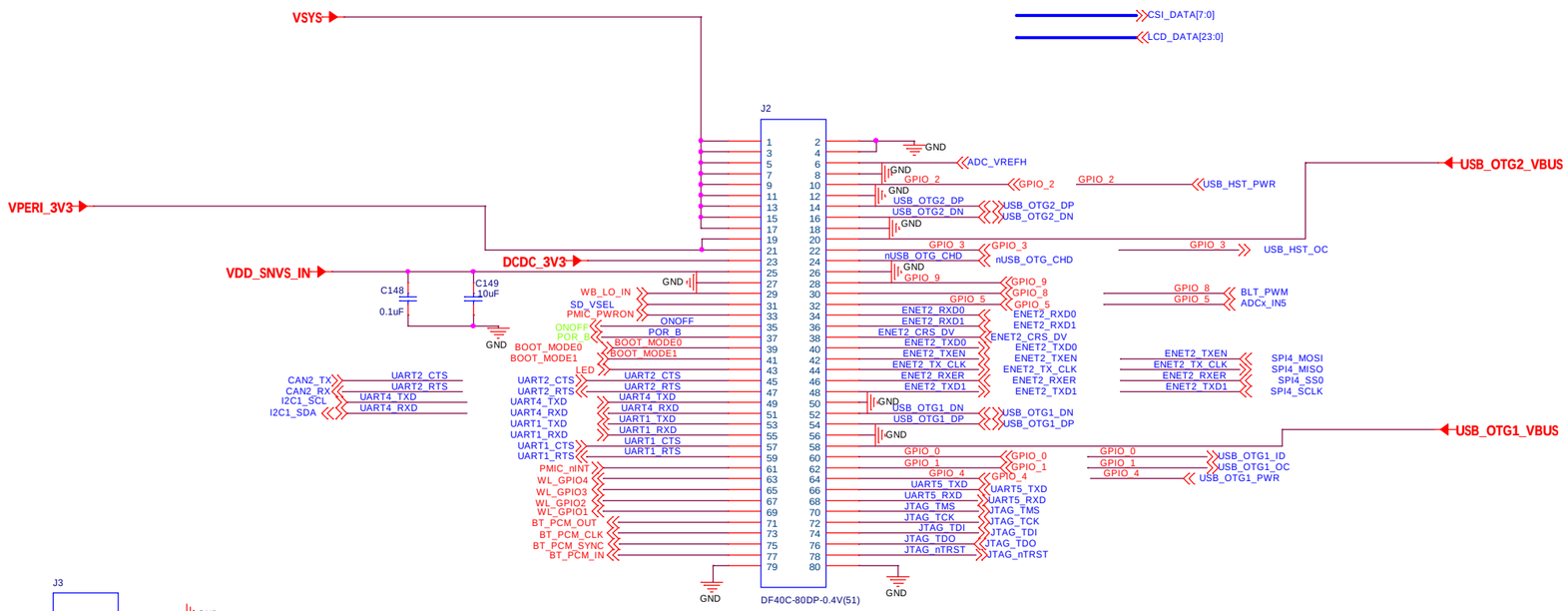
Date: Thursday, March 23, 2017 | Sheet 10 of 11

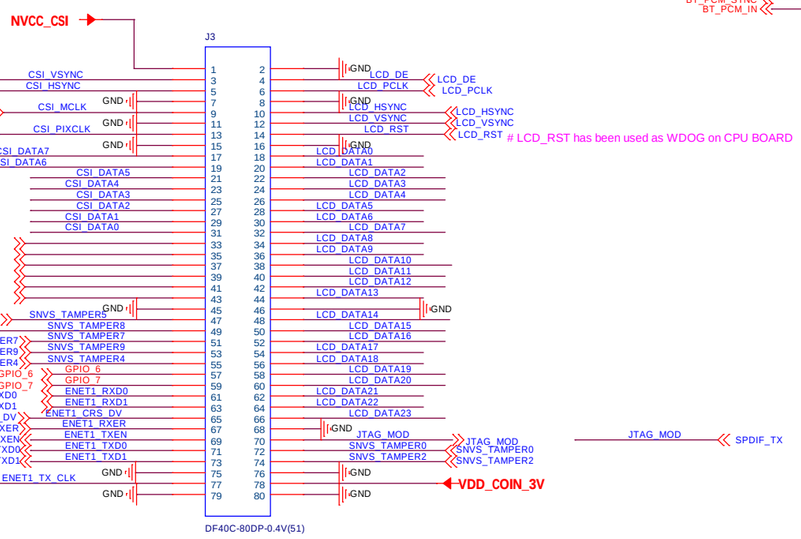
TP for SOM MFG





SOM 80x2





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Title: CPU-SODIMM200			
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