*Click **here** for production status of specific part numbers.*

SC1905

698MHz to 3800MHz RF Power Amplifier Linearizer (RFPAL)

General Description

The SC1905 is a pin-compatible upgrade of the popular SC1894 RF PA linearizer (RFPAL) supporting signal bandwidths up to 100MHz. The SC1905 is a fully adaptive, RFin/RFout predistortion linearization solution optimized for a wide range of amplifiers, power levels, and communication protocols. The SC1905 uses the PA output and input signals to adaptively generate an optimized correction function in order to minimize the PA's self-generated distortion and impairments. Using RF-domain analog signal processing enables the SC1905 to operate over wide-signal bandwidths and consume very low power.

Design support features are accessed through the SC1905's serial peripheral interface (SPI) bus.

Applications

- 4G and 5G Cellular Infrastructure
  - Single/Multicarrier, Multistandard: WCDMA, LTE, and TD-LTE
  - BTS Amplifiers, RRH, Booster Amplifiers, Repeaters, Small Cells, Microcells, Picocells, DAS, AAS, and MIMO Systems
- Wide Range of PAs and Output Power
  - Amplifier: Class A/AB and Doherty
  - PA Process: LDMOS, GaN, GaAs, and InGaP
- Any Application Requiring PA Linearization

Benefits and Features

- RFin/RFout PA Linearizer SoC in Standard CMOS
  - Fully Adaptive Correction
- External Reference Clock Support:
  - 10MHz, 13MHz, 15.36MHz, 19.2MHz, 20MHz, 26MHz, and 30.72MHz
- Low Power Consumption: 1280mW
- Frequency Range: 698MHz to 3800MHz
- Input Signal Bandwidth: 5MHz to 100MHz
- Packaged in 9mm x 9mm QFN Package
- Operating Case Temperature: -40°C to +105°C
- Fully RoHS Compliant, Green Materials
- Ease of Use
  - Integrated RFin/RFout Solution
  - Reduced SW Development
- Reduces System Power Consumption and OPEX
- Reduces BOM Costs, Area, and Total Volume
  - Smaller Power Supply, Heat Sink, and Enclosure
  - Small Implementation Size (< 6.5cm^2)

***Ordering Information** appears at end of data sheet.*

19-100404; Rev 1; 10/18

maxim integrated™

Absolute Maximum Ratings

Supply Voltage (A/VDD33 to GND)..... -0.3V to +3.8V
Supply Voltage (A/VDD18 to GND)..... -0.2V to +2.2V
Input Voltage (1.8V pins)..... -0.2V to A/VDD18 + 0.2V
Input Voltage (3.3V pins)..... -0.3V to A/VDD33 + 0.3V
Input into the BALUN (RMS) ..... +7dBm

Storage Temperature Range .....-65°C to +150°C
Operating Case Temperature .....-40°C to 105°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

64 QFN

Package Code	K6499MK+1B
Outline Number	21-0765
Land Pattern Number	90-0605

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(Operation at +25°C, A/DVDD18 = 1.85V, A/DVDD33 = 3.3V, A/DVDD18 = 1.85V, and 20MHz external clock, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Rating						
Operating Case Temperature			-40		105	ºC
DC Electrical Characteristics						
Supply Voltage (A/VDD33 to GND)			3.1	3.3	3.5	V
Supply Voltage (A/VDD18 to GND)			1.75	1.85	1.95	V
Average Power Dissipation		(Note 1) (Note 2) (Note 5)		1280	1700	mW
Supply Peak Current (A/VDD33 to GND)		(Note 1) (Note 2) (Note 5)		95	120	mA
Supply Peak Current (A/VDD18 to GND)		(Note 1) (Note 2) (Note 5)		942	1100	mA
Radio Frequency Signals						
Operating Frequency				698 - 3800		MHz
Input Signal Bandwidth		(Note 3) (Note 4)		5 - 100		MHz
Noise Power		Referred to 0dBm at PA input		-140		dBm/Hz
RF Input Range for Maximum Correction—700MHz to 2700MHz						
Minimum Peak RFIN_BLN Level		When PA operates at maximum output power. (Note 6) (Note 7)		-2		dBm
Peak RFIN_BLN Level		When PA operates at maximum output power. (Note 6) (Note 7)		+4		dBm
Maximum Peak RFIN_BLN Level		When PA operates at maximum output power. (Note 6) (Note 7)		+6		dBm
Minimum Peak RFFB_BLN Level		When PA operates at maximum output power. (Note 6) (Note 7)		-12		dBm
Peak RFFB_BLN Level		When PA operates at maximum output power. (Note 6) (Note 7)		-4		dBm
Maximum Peak RFFB_BLN Level		When PA operates at maximum output power. (Note 6) (Note 7)		-2		dBm
RFIN_BLN Operating Range		Average power, over PA output power range		-49 to -4		dBm
RFFB_BLN Operating Range		Average power, over PA output power range		-52 to -12		dBm
RF Input Range for Maximum Correction—2700MHz to 3300MHz						
Peak RFIN_BLN Level		When PA operates at maximum output power. (Note 6) (Note 7)		+6		dBm
Peak RFFB_BLN Level		When PA operates at maximum output power. (Note 6) (Note 7)		-4		dBm

Electrical Characteristics (continued)

(Operation at +25°C, A/DVDD18 = 1.85V, A/DVDD33 = 3.3V, A/DVDD18 = 1.85V, and 20MHz external clock, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RFIN_BLN Operating Range		Average power, over PA output power range		-44 to -4		dBm
RFFB_BLN Operating Range		Average power, over PA output power range		-54 to -14		dBm
RF Input Range for Maximum Correction—3300MHz to 3800MHz						
Minimum Peak RFIN_BLN Level		When PA operates at maximum output power. (Note 6) (Note 7)		+3		dBm
Peak RFIN_BLN Level		When PA operates at maximum output power. (Note 6) (Note 7)		+9		dBm
Maximum Peak RFIN_BLN Level		When PA operates at maximum output power. (Note 6) (Note 7)		+11		dBm
Minimum Peak RFFB_BLN Level		When PA operates at maximum output power. (Note 6) (Note 7)		-12		dBm
Peak RFFB_BLN Level		When PA operates at maximum output power. (Note 6) (Note 7)		-4		dBm
Maximum Peak RFFB_BLN Level		When PA operates at maximum output power. (Note 6) (Note 7)		-2		dBm
RFIN_BLN Operating Range		Average power, over PA output power range		-41 to +1		dBm
RFFB_BLN Operating Range		Average power, over PA output power range		-52 to -12		dBm
Digital I/O - DC Characteristics						
Minimum CMOS Input Logic-Low	V_{IL}			-0.3		V
Maximum CMOS Input Logic-Low	V_{IL}			+0.8		V
Minimum CMOS Input Logic-High	V_{IH}	V_{DD} = 3.3V		2.0		V
Maximum CMOS Output Logic-Low	V_{OL}			0.4		V
Minimum CMOS Output Logic-High	V_{OH}	V_{DD} = 3.3V		2.4		V
EEPROM Endurance						
Minimum EEPROM write/erase cycles		Page mode, +25°C		1M		E/W Cycles

Note 1: Continuous adaptation, tracking.

Note 2: Power dissipation may be FW dependent. Refer to the FW release notes for any changes to values listed above.

Note 3: In the case where the carrier configuration is NON-fully occupied, then the average power delta between the two outermost carriers must be ≤ 20dB, the carrier configuration must be static (no hopping), the outermost carriers must be ≥ 5MHz and the center frequency must be stored in EEPROM.

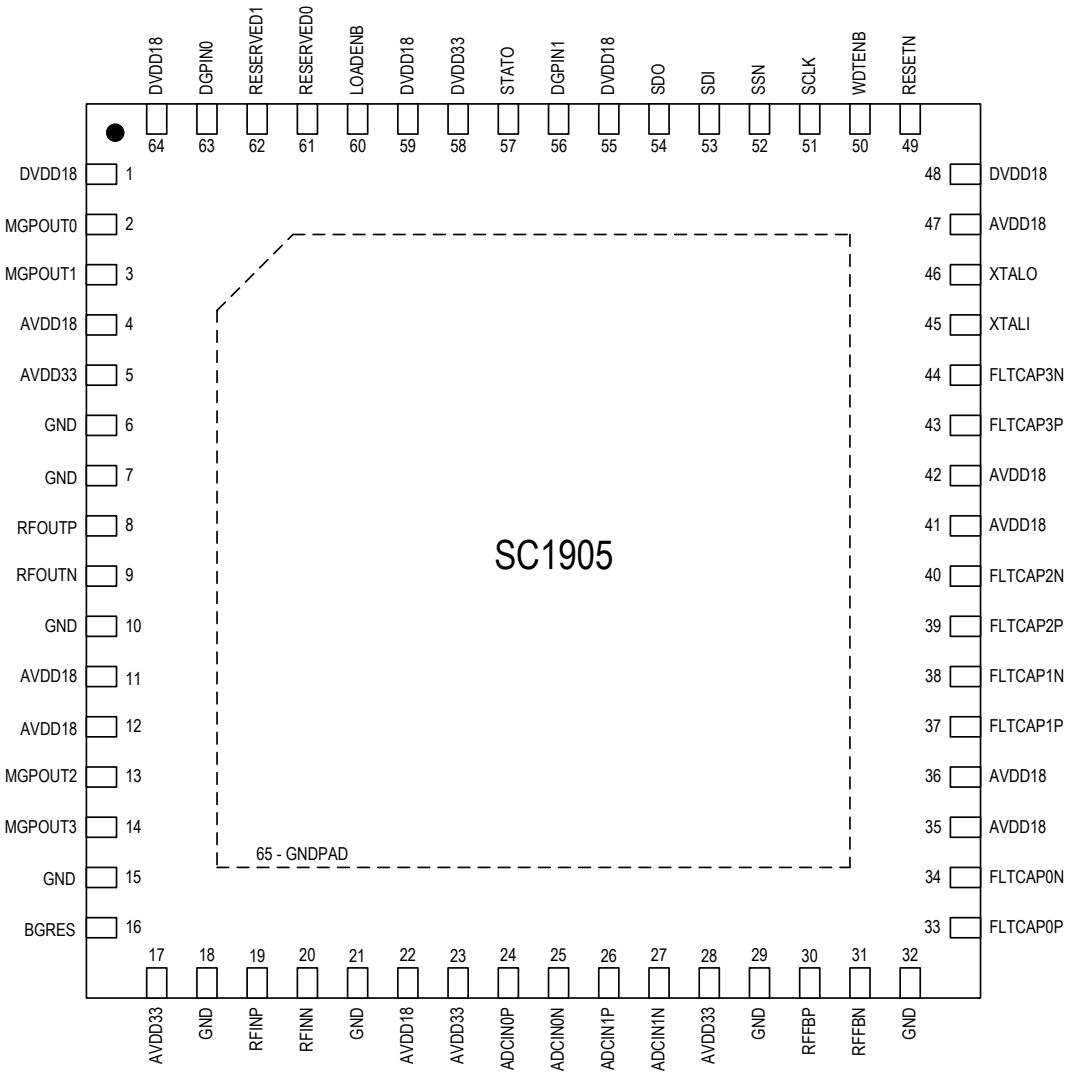
Note 4: Correction performance across range of input signal BWs also depends on PA output power and carrier configuration.

Note 5: Characterized at typical voltages, +25°C operating case temperature, and 100MHz input signal bandwidth.

Note 6: Peak power is defined as the 10^{-4} point on the CCDF (complementary cumulative distribution function) of the signal.

Note 7: Referred to 50Ω impedance into a 1:2 balun.

Pin Configuration



Pin Description

PIN	NAME	FUNCTION	TYPE
1	DVDD18	+1.8V DC Supply Voltage for Digital Circuits.	Supply
2	MGPOUT 0	Do Not Connect. Reserved for internal use.	Analog Out
3	MGPOUT 1	Do Not Connect. Reserved for internal use.	Analog Out
4	AVDD18	+1.8V DC Supply Voltage for Analog Circuits	Supply
5	AVDD33	+3.3V DC Supply Voltage for Analog Circuits	Supply
6	GND	Ground	Supply
7		Ground for Shield of RF Signal	RF Shield
8	RFOUTP	RF Output Signal, Differential Positive Output.	Analog Out
9	RFOUTN	RF Output Signal, Differential Negative Output	Analog Out
10	GND	Ground for Shield of RF Signal.	RF Shield
11, 12	AVDD18	+1.8V DC Supply Voltage for Analog Circuits.	Supply
			Supply
13	MGPOUT 2	Do Not Connect. Reserved for internal use.	Analog Out
14	MGPOUT 3	Do Not Connect. Reserved for internal use.	Analog Out
15	GND	Ground	Supply
16	BGRES	Bandgap Resistor.	Analog In
17	AVDD33	+3.3V DC Supply Voltage for Analog Circuits.	Supply
18	GND	Ground for Shield of RF Signal.	RF Shield
19	RFINP	RF Input Signal, Differential Positive Input.	Analog In
20	RFINN	RF Input Signal, Differential Negative Input.	Analog In
21	GND	Ground for Shield of RF Signal.	RF Shield
22	AVDD18	+1.8V DC Supply Voltage for Analog Circuits.	Supply
23	AVDD33	+3.3V DC Supply Voltage for Analog Circuits.	Supply
24	ADCIN0P	Do Not Connect. Reserved for internal use.	Analog In
25	ADCIN0N	Do Not Connect. Reserved for internal use.	Analog In
26	ADCIN1P	Do Not Connect. Reserved for internal use.	Analog In
27	ADCIN1N	Do Not Connect. Reserved for internal use.	Analog In
28	AVDD33	+3.3V DC Supply Voltage for Analog Circuits.	Supply
29	GND	Ground for Shield of RF Signal.	RF Shield
30	RFFBP	RF Feedback Signal, Differential Positive Input.	Analog In
31	RFFBN	RF Feedback Signal, Differential Negative Input.	Analog In
32	GND	Ground for Shield of RF Signal.	RF Shield
33	FLTCAP0 P	Dedicated External Filter Capacitor #0.	Analog Out

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
34	FLTCAP0N	Dedicated External Filter Capacitor #0.	Analog Out
35, 36	AVDD18	+1.8V DC Supply Voltage for Analog Circuits.	Supply
			Supply
37	FLTCAP1P	Dedicated External Filter Capacitor #1.	Analog Out
38	FLTCAP1N	Dedicated External Filter Capacitor #1.	Analog Out
39	FLTCAP2P	Dedicated External Filter Capacitor #2.	Analog Out
40	FLTCAP2N	Dedicated External Filter Capacitor #2.	Analog Out
41, 42	AVDD18	+1.8V DC Supply Voltage for Analog Circuits.	Supply
			Supply
43	FLTCAP3P	Dedicated External Filter Capacitor #3.	Analog Out
44	FLTCAP3N	Dedicated External Filter Capacitor #3.	Analog Out
45	XTALI	Crystal Input. For standard internal clock, connect crystal or ceramic resonator from XTALI to XTALO. May alternatively be driven by an external clock.	Analog In
46	XTALO	Crystal Output. Excitation driver for crystal or ceramic resonator.	Analog Out
47	AVDD18	+1.8V DC Supply Voltage for Analog Circuits.	Supply
48	DVDD18	+1.8V DC Supply Voltage for Digital Circuits.	Supply
49	RESETN	Active-Low Reset Input. Has internal pullup to DVDD33.	Digital In
50	WDTENB	Watch Dog Timer Enable. WDTENB enabled when high. Has internal pullup to DVDD33. See applications schematic for further details.	Digital In
51	SCLK	SPI Clock. Has internal pulldown to GND.	Digital In
52	SSN	SPI Slave Select Enabled "Low". Has internal pullup to DVDD33.	Digital In
53	SDI	SPI Slave Data Input to RFPAL. Has internal pulldown to GND.	Digital In
54	SDO	SPI Slave Data Output from RFPAL. Tri-state. DVDD33 logic.	Digital Out
55	DVDD18	+1.8V DC Supply Voltage for Digital Circuits.	Supply
56	DGPIN1	Digital General Purpose Input 1. Has internal pullup to DVDD33. See Firmware Release Notes for further details.	Digital In
57	STATO	General Purpose Status Output, as Defined in Firmware Release Notes. Open-drain output with internal pullup to DVDD33.	Digital Out
58	DVDD33	+3.3V DC Supply Voltage for Digital Circuits.	Supply
59	DVDD18	+1.8V DC Supply Voltage for Digital Circuits.	Supply
60	LOADENB	Load Enable. Required for FW upgrades. Has internal pulldown to GND. See applications schematic for further details.	Digital In
61	TESTSEL1	Do Not Connect. Reserved for internal use. Has internal pulldown to GND.	Reserved

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
62	TESTSEL 2	Do Not Connect. Reserved for internal use. Has internal pulldown to GND.	Reserved
63	DGPIN0	Digital General Purpose Input 0. Do not connect. Reserved for future use. Has internal pulldown to GND. See applications schematic for further details.	Digital In
64	DVDD18	+1.8V DC Supply Voltage for Digital Circuits.	Supply
65	GNDPAD	Common Ground for Entire Integrated Circuit. Also provides path for thermal dissipation.	Supply

Detailed Description

The SC1905 is the latest generation of RFPAL linearizer IC. The maximum signal bandwidth has been increased to 100MHz from the previous generation SC1894 device in order to support 5G signals.

Introduction to Predistortion Using the SC1905

Wideband signals in today's telecommunications systems have high peak-to-average ratios and stringent spectral regrowth specifications. These specifications place high linearity demands on power amplifiers. Linearity may be achieved by backing off output power at the price of reducing efficiency. However, this increases the component and operating costs of the power amplifier. Better linearity may be achieved through the use of digital predistortion and other linearization techniques, but many of these are time consuming and costly to implement. Wireless service providers are deploying networks with wider coverage, greater subscriber density, and higher data rates. These networks require more efficient power amplifiers. Additionally, the emergence of distributed architectures and active antenna systems is driving the need for smaller and more efficient power amplifier implementations. Further, there continues to be a strong push toward reducing the total capital and operating costs of base stations.

With the SC1905, the complex signal processing is done in the RF domain. This results in a simple system-on-chip that offers wide signal bandwidth, broad frequency of operation, and very low power consumption. It is an elegant solution that reduces development costs and speeds time to market. Applicable across a broad range of signals—including 2G, 3G, 4G, 5G wireless, and other modulation types—the powerful analog signal-processing engine is capable of linearizing the most efficient power amplifier topologies. The SC1905 is a true RFin and RFout solution, supporting modular power amplifier designs that are independent of the baseband and transceiver subsystems. The SC1905 delivers the required efficiency and performance demanded by today's wireless systems.

Serial Peripheral Interface (SPI)

The SC1905 contains a microprocessor that is executing firmware. The system software referred to henceforth as the "host", communicates with the firmware through a handshaking protocol called the message protocol. The host configures the SC1905 by writing to various parameters stored in an EEPROM contained within the SC1905, or by issuing commands to the firmware through the message protocol. All this communication is done through a 4-wire Serial Peripheral Interface (SPI).

Detailed information on the message protocol, accessing EEPROM, etc. is contained in the SC1905 SPI Programming Guide. Figure 1 shows the timing relationships between the SPI signals. Refer to Table 1.

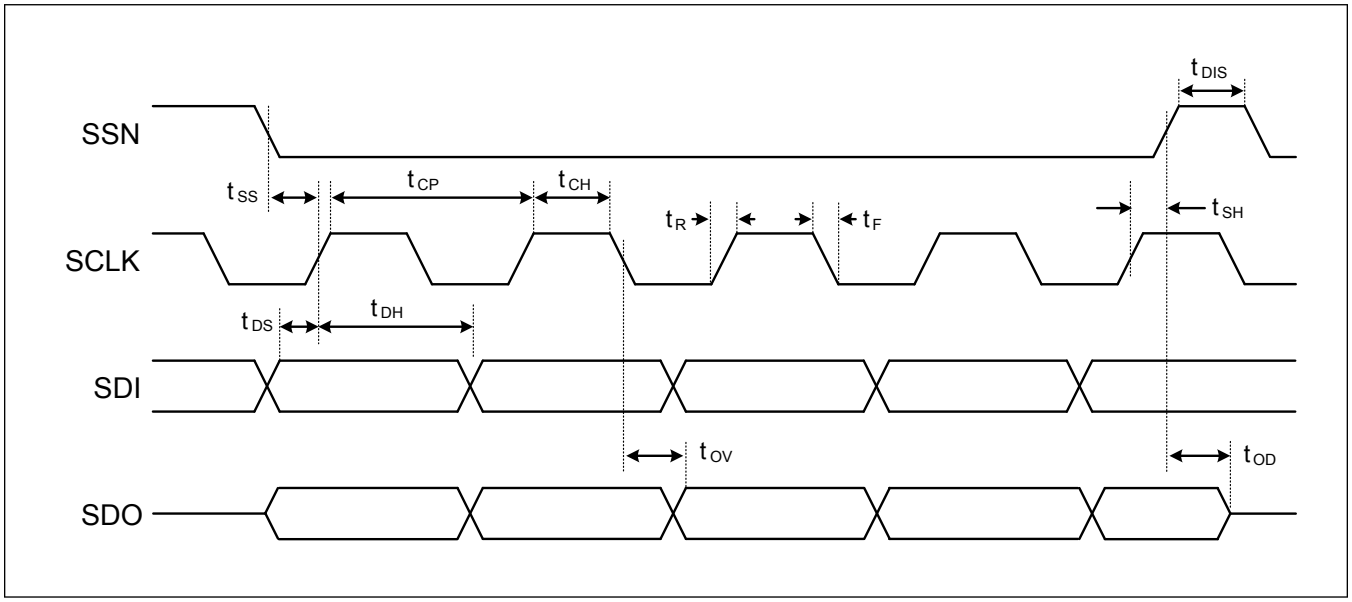


Figure 1. Serial Interface Timing Diagram

Table 1. Serial Interface Timing Requirements

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Minimum Select Setup Time	t_{SS}		100		ns
Minimum Select Hold Time	t_{SH}		250		ns
Minimum Select Disable Time	t_{DIS}		100		ns
Minimum Data Setup Time	t_{DS}		25		ns
Minimum Data Hold Time	t_{DH}		45		ns
Maximum Rise Time	t_{R}		25		ns
Maximum Fall Time	t_{F}		25		ns
Minimum Clock Period	t_{CP}		250		ns
Minimum Clock High Time	t_{CH}		100		ns
Maximum Time to Output Valid	t_{OV}		100		ns
Maximum Output Data Disable	t_{OD}		50		ns

Applications Information

External Clock (XTALI) Requirements

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
External Clock Frequency*		10	20	30.72	MHz
External Clock Frequency Accuracy				1	%
External Clock Frequency Drift	Including aging and temperature			100	ppm
Duty Cycle	Square wave	45		55	%
External Clock Amplitude	Sine or square wave	500		1500	mV_{p-p}
External Clock Phase	At 100kHz			-130	dBc/Hz

**Selecting an external reference clock frequency other than 20MHz requires programming the SC1905 through the SPI bus. See SPI Programming Guide and Hardware Design Guide for more information. User may program the SC1905 to accept the following clock frequencies: 10MHz, 13MHz, 15.36MHz, 19.2MHz, 20MHz, 26MHz, and 30.72MHz.*

Crystal Requirements

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ESR				50	Ω
Capacitive Load to Ground			10	12	pF
Frequency Accuracy				250	ppm
Frequency Drift	Including aging and temerature			100	ppm

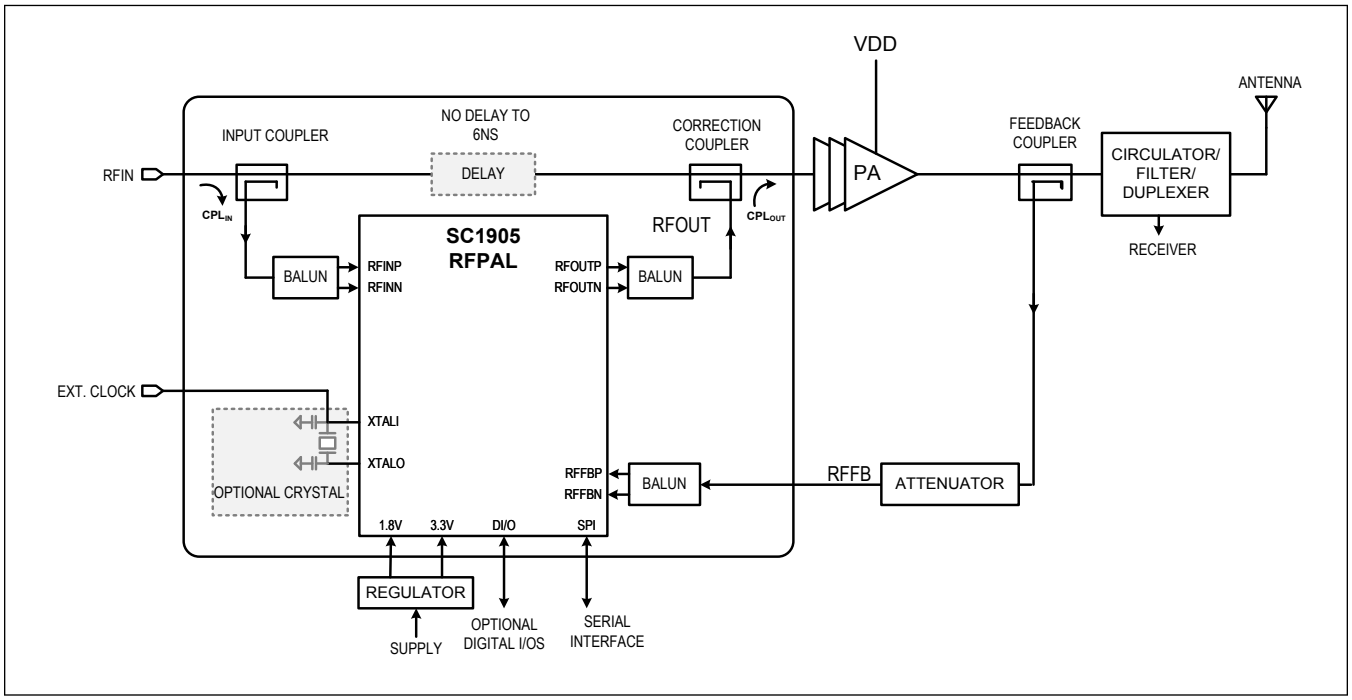
Auxiliary Documentation

From a programming perspective, the SC1905, like previous RFPAL products, is quite complex. An entire document, the SC1905 SPI Programming Guide, is dedicated to describing how the host communicates with the SC1905. It describes the communication protocol in addition to the addresses of all the variables and and parameters for monitoring the status and configuration of the SC1905.

For guidance on how to design the SC1905 into a system; for example, recommendations on PCB layout, regulator and delay line selection etc. please refer to the SC1905 Hardware Design Guide. The Firmware 6.0.01.00 Release Notes provide data on linearization performance of the firmware. These auxiliary documents are available on the SC1905 product web page on Maxim's website.

Typical Application Circuits

Circuit 1



Ordering Information

PART NUMBER	DESCRIPTION	FIRMWARE VERSION
SC1905A-00A00	Bulk	6.0.01.00
SC1905A-00A00E	Tape-and-Reel	6.0.01.00

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/18	Initial release	—
1	10/18	Updated *Ordering Information*	12

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