The Right Choice for HMI Designs

RZ/A1 Embedded ARM® Microprocessors

Expanded product family – now with Linux support

Renesas Electronics America
www.renesas.com

RZ/A1 Embedded ARM® Microprocessors

Innovative Architecture & Advanced Integration

Renesas RZ/A1 series microprocessors (MPUs) offer an innovative architecture based on the ARM Cortex®-A9 processor and up to an industry-leading 10 MB of on-chip memory. RZ/A1 MPUs can execute code at 1000 DMIPS from the abundant on-chip memory or in-place from inexpensive QSPI memory, while using on-chip memory for graphics buffering up to WXGA (1280x800) resolution. The 128-bit wide internal memory bus with x4 parallel access enables higher-throughput memory access as compared to systems with external DDR memory. The RZ/A1 series offers enormous advantages in terms of BOM cost, performance, power consumption, and system design time, making it the right choice for Human Machine Interface (HMI) and other system-on-chip applications.

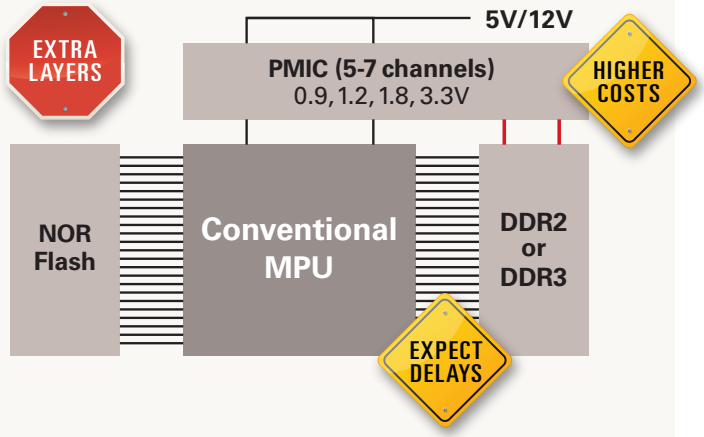
- ARM Cortex®-A9 processor that can execute code at 1000 DMIPS
- Remove need for external RAM with up to 10 MBs of on-chip RAM
- Execute-In-Place (XIP) from QSPI memory enabled with three layers of cache
- Up to two Camera inputs available for video and graphics blending usages
- Scalable line-up with three sizes of on-chip RAM to choose from: 3 MB (RZ/A1L or RZ/A1LU), 5 MB (RZ/A1M), and 10 MB (RZ/A1H)
- Implement up to two independent LCD displays with WXGA (1280x800) resolution for impressive graphical user interfaces

Renesas RZ/A1 solution streamlines board design and reduces BOM cost

Conventional Solution

– Complicated power-management and PCB layout

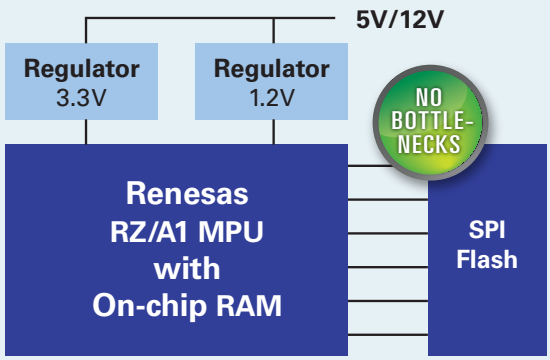
– Memory bandwidth split between code and graphics



BOM Component	Conventional Solution
Flash	$$$ (NOR Flash)
RAM	$$$ (DDR2)
Regulators	$$$ (5-7 PMIC channels)
PCB layers	$$$ (DDR2 supplies, routing)
Total BOM cost	$$$

Renesas RZ/A1 HMI Solution

– Easy system design and testing

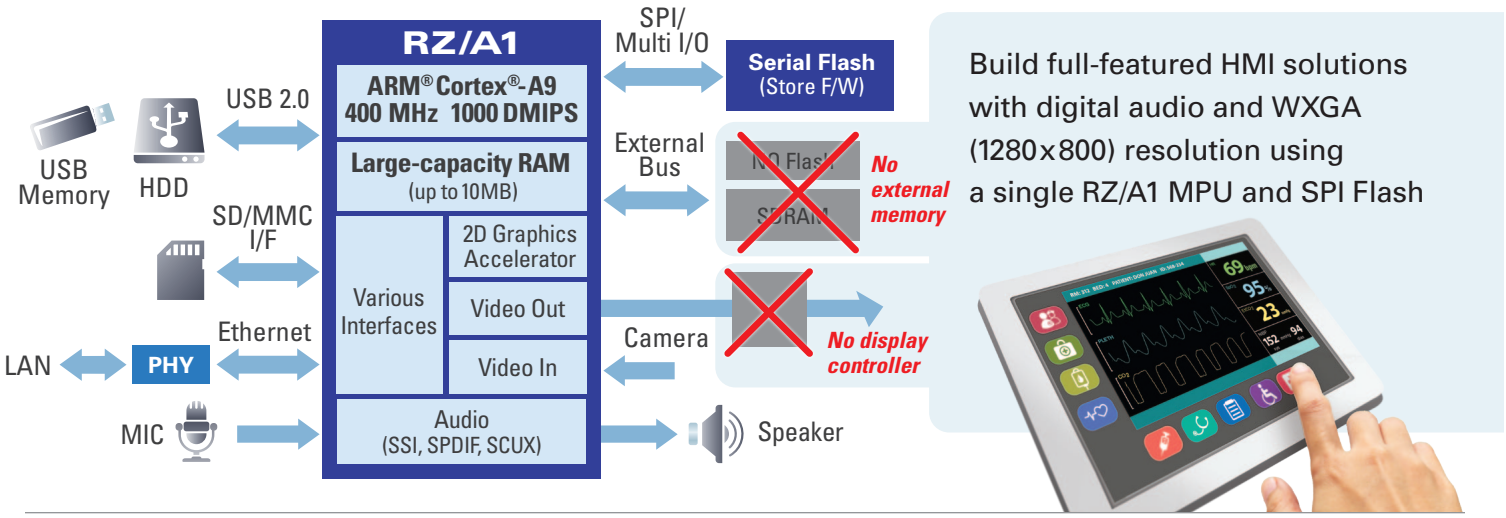


BOM Component	RZ/A1 Solution
Flash	$ (SPI Flash)
RAM	n/a (internal)
Regulators	$ (3.3V, 1.2V regulator)
PCB layers	$ (as few as two)
Total BOM cost	$

Create superior HMI designs with fewer components

On-chip functions provided by RZ/A1 MPUs reduce BOM cost, save board space and minimize integration tasks. Typical applications like the one shown below take advantage of a rich portfolio of intellectual property from Renesas and can utilize a range of built-in peripherals, including: CMOS camera interface, JPEG Codec Unit, 12-bit ADC, and OpenVG 2D graphics engine, among others.

RZ/A1 Series System Diagram



Features

Up to 10 MB on-chip RAM
- For code execution/data buffering

128-bit memory bus
- With parallel (x4) access to deliver superior memory throughput

Execute-In-Place (XIP) from inexpensive QSPI memory
- With three layers of cache

LCD controller to drive up to two independent WXGA displays
- For vivid displays

Benefits

Lower BOM Cost
- No external SDRAM or LCD controller
- Simpler voltage regulators
- Reduced PCB layers

Increased Performance
- 1000 DMIPS at 400 MHz
- 6x throughput of 333 MHz 16-bit DDR2

Decreased Power Consumption
- Fewer board components
- No copying of code from flash to RAM

Accelerate Time to Market
- Simpler PCB design
- Decreased EMI via reduced switching
- No DDR procurement issues

One RZ/A1 MPU can accommodate an entire software stack (libraries, operating system and application code), plus a graphics frame buffer.

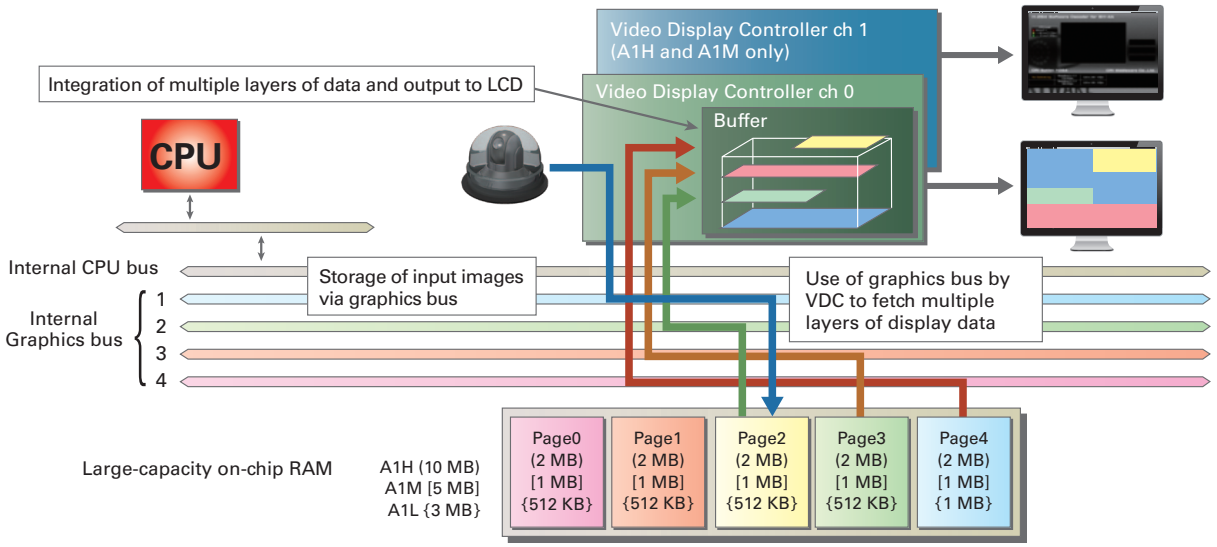
Graphics Capabilities

Number of Images in Frame Buffer	RZ/A1L QVGA 320x240 16bpp	RZ/A1L WQVGA 480x272 16bpp	RZ/A1M VGA 640x480 32bpp	RZ/A1M WVGA 800x480 32bpp	RZ/A1H SVGA 800x600 32bpp	RZ/A1H WSVGA 1024x600 32bpp	RZ/A1H XGA 1024x768 32bpp	RZ/A1H WXGA 1280x800 32bpp
4	0.6 MB	1.0 MB	4.7 MB	5.9 MB	7.3 MB	9.4 MB		
3	0.4 MB	0.7 MB	3.5 MB	4.4 MB	5.5 MB	7.0 MB	9.0 MB	
2	0.3 MB	0.5 MB	2.3 MB	2.9 MB	3.7 MB	4.7 MB	6.0 MB	7.8 MB
1	0.1 MB	0.2 MB	1.2 MB	1.5 MB	1.8 MB	2.3 MB	3.0 MB	3.9 MB

Display Resolutions Supported by RZ/A1 MPUs

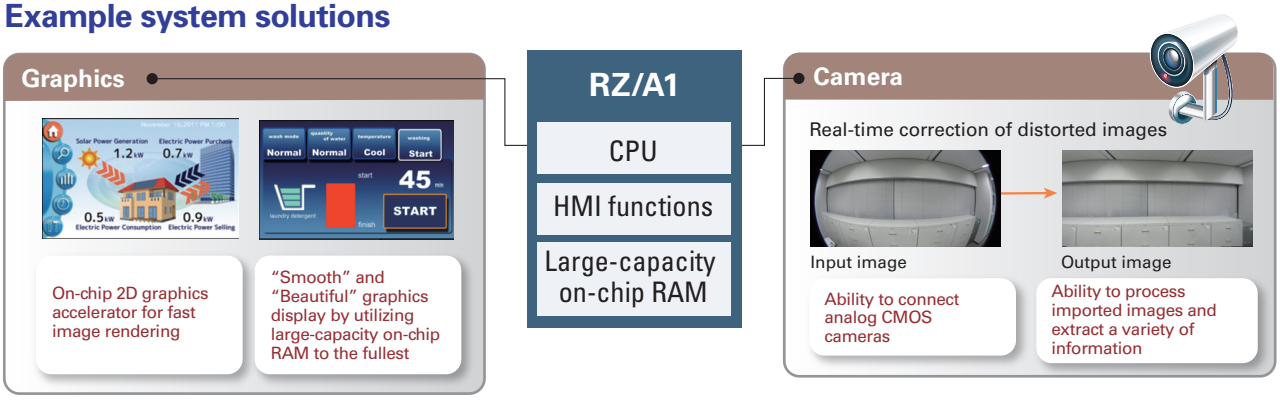
Graphics display and camera input capabilities on a single chip

RZ/A1 MPUs have a unique combination of graphics display and camera functions that, coupled with their parallel-access, 128-bit memory bus, enables systems with rich graphical and video capabilities.



The bus configuration, with independent buses for images and hardware-based superimposition processing, makes it easy to create graphical applications.

Example system solutions

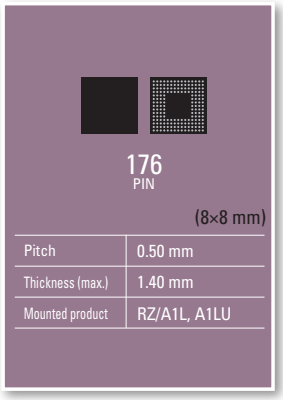


Target applications

The performance of the ARM Cortex-A9 MPU and the simplicity of a MCU-style platform design makes the RZ/A1 MPU the ideal choice for a range of applications, such as those shown below.

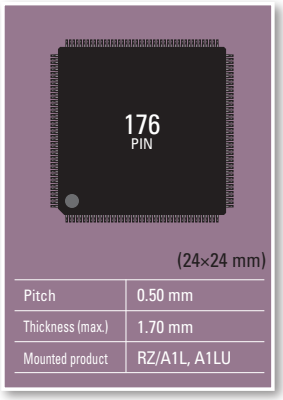
Renesas RZ/A1 packaging options

176-LFBGA



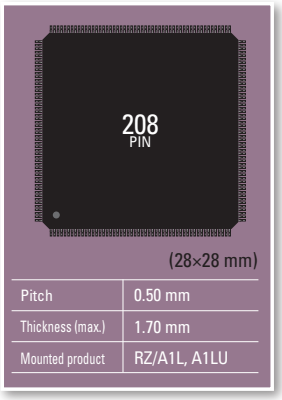
Pitch	0.50 mm
Thickness (max.)	1.40 mm
Mounted product	RZ/A1L, A1LU

176-LFQFP



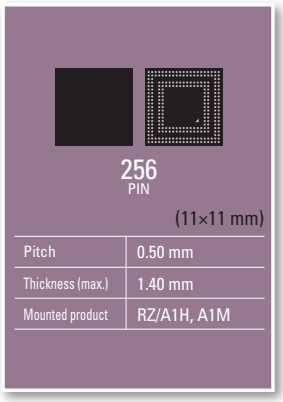
Pitch	0.50 mm
Thickness (max.)	1.70 mm
Mounted product	RZ/A1L, A1LU

208-LFQFP



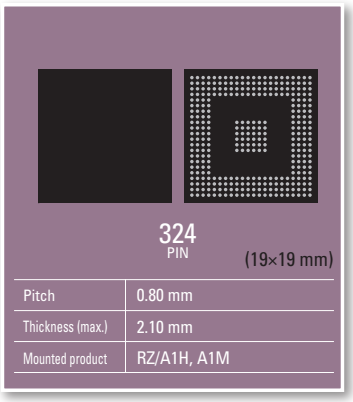
Pitch	0.50 mm
Thickness (max.)	1.70 mm
Mounted product	RZ/A1L, A1LU

256-LFBGA



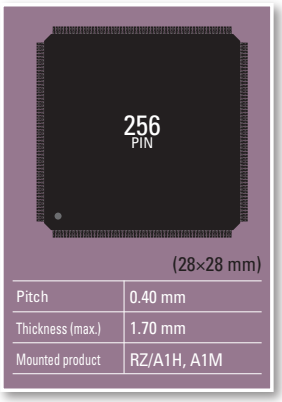
Pitch	0.50 mm
Thickness (max.)	1.40 mm
Mounted product	RZ/A1H, A1M

324-FBGA



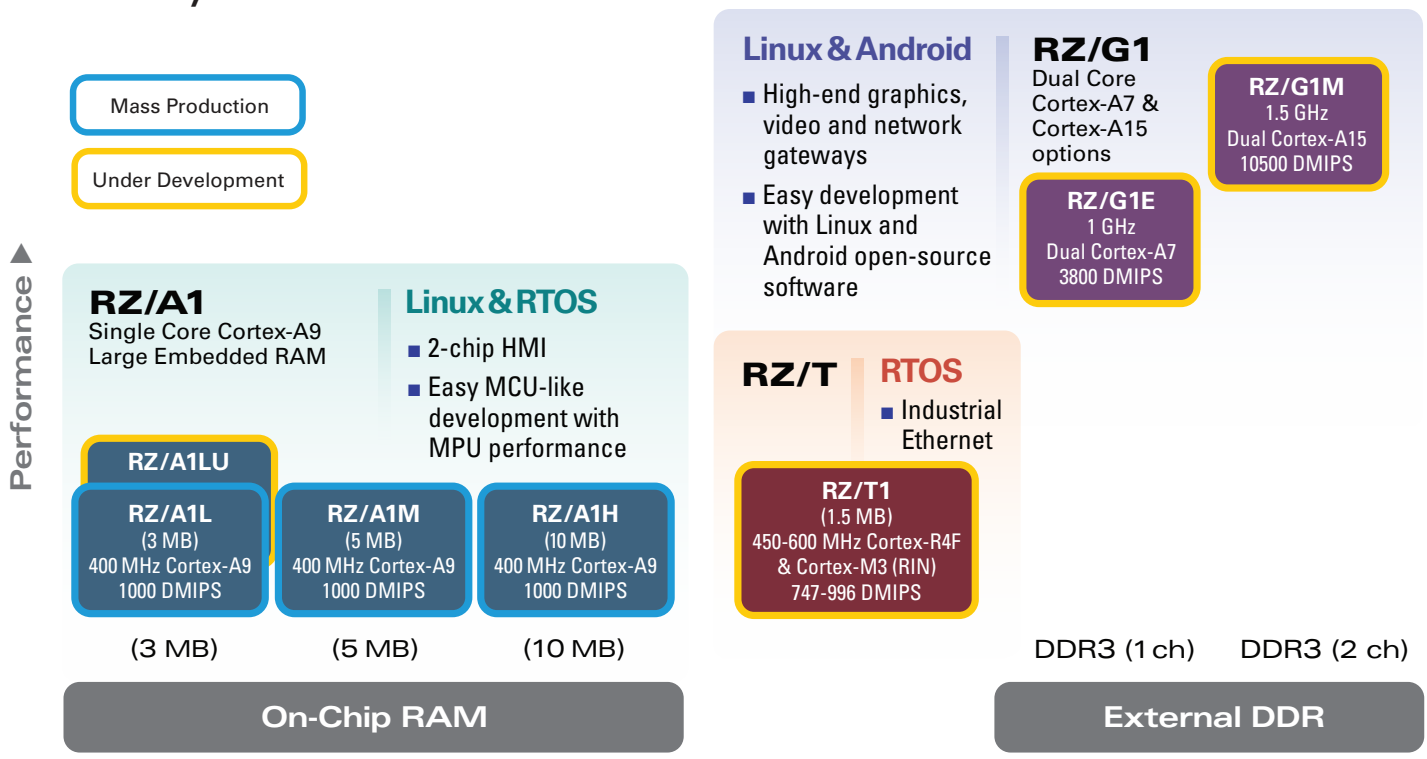
Pitch	0.80 mm
Thickness (max.)	2.10 mm
Mounted product	RZ/A1H, A1M

256-LFQFP



Pitch	0.40 mm
Thickness (max.)	1.70 mm
Mounted product	RZ/A1H, A1M

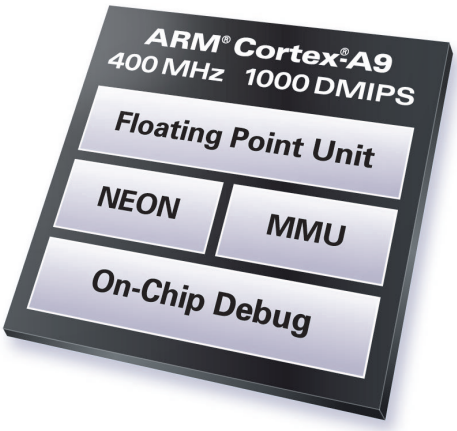
RZ Family of ARM-based MPUs



RZ/A1H and RZ/A1M MPUs

Best choices for higher-end HMI designs (up to WXGA resolution)

- Buffer up to two independent WXGA (1280x800) images with a single RZ/A1H MPU chip
- Buffer up to two WSVGA (1024x600) images or a single WXGA (1280x800) image with one RZ/A1M MPU chip
- Utilize the on-chip OpenVG graphics engine for impressive 2D graphics acceleration
- Connect to one or two independent LCD displays
- Exploit additional peripherals, including: NAND Flash interface, JPEG Codec Unit, IMR engine, sound generator, NTSC/PAL decoder for video, and PWM timer



Highly Efficient 32-bit CPU Core (ARM Cortex-A9)

- 1000 DMIPS performance at 400MHz
- ARM NEON multimedia engine
- Boots from parallel or serial flash

10 MB (RZ/A1H) and 5 MB (RZ/A1M) Internal RAM

- Use as large data buffer or to run system from internal memory
- Employs parallel bus structure dedicated to SRAM to speed processing

Execute-In-Place Operation from QSPI Flash

- Take full advantage of cost-effective external serial flash
- Simplifies program execution

Single- and Double-Precision Floating Point Unit, IEEE754 Compliant

- Accelerates trigonometric operations such as scaling and rotation

2D-Graphics Engine with OpenVG 1.1 Capability

- Fully supports the Khronos™ OpenVG 1.1 API
- Offloads CPU for rendering, animation and video acceleration operations

LCD Controller with 24-bit RGB and 16-bit LVDS Interfaces

- Handles 4-layer overlays
- Provides 2-ch video input, 2-ch display output with 1 ch of LVDS
- Implements alpha blending
- Supports chroma keying

Bus Interface Controller

- Directly connects to SRAM, SDRAM, and flash (NOR, NAND, eMMC), as well as 128 KB L2 cache

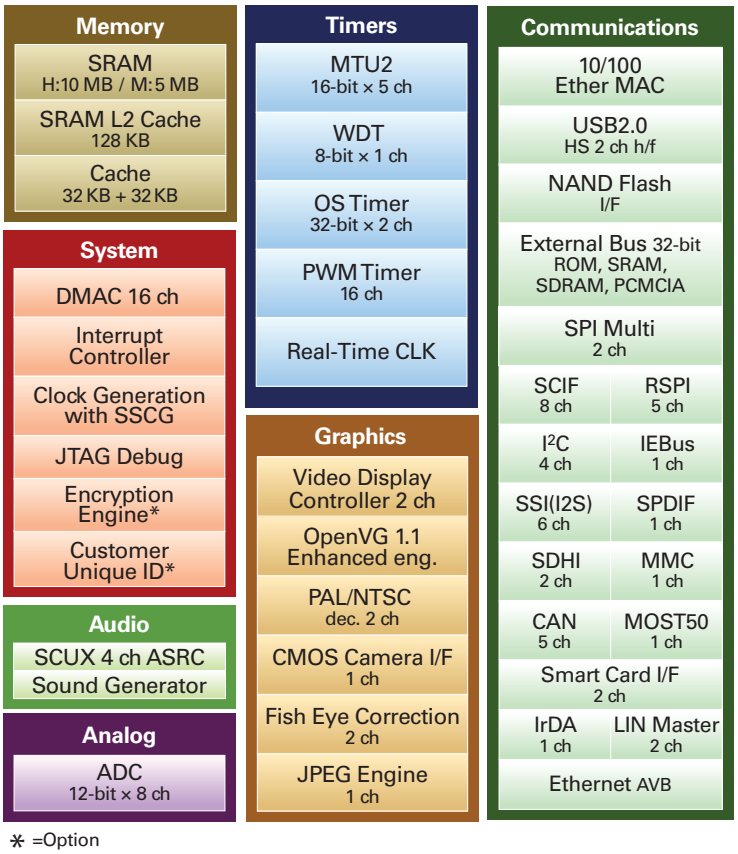
Multiple Network Connectivity Interfaces

- Integrates 10/100 EtherMAC controller (1 ch)
- Includes USB 2.0 host and function controller with integrated USB transceiver (2 ch)
- Offers up to 5 CAN channels

Three Package Options

- 324-pin BGA (0.8 mm)
- 256-pin QFP (0.4 mm)
- 256-pin BGA (0.5 mm)

RZ/A1H and RZ/A1M Block Diagram



* =Option

RZ/A1L MPUs

Ideal solutions for cost-sensitive designs (up to WSVGA resolution)

- Buffer up to WSVGA (1024×600) images in internal memory
- Accelerate multimedia processing with ARM NEON™ SIMD (Single Instruction, Multiple Data) engine
- Connect to single LCD display

NEW

RZ/A1LU MPUs

More features to expand system capabilities

- Secure Boot and Secure Communications with optional security unit
- Simplify designs with JPEG Codec Unit
- Transport audio and video over Ethernet with Ethernet AVB support
- Use Dual-Data-Rate QSI support to get higher bandwidth access to the SPI Flash

Highly Efficient 32-bit CPU Core (ARM Cortex-A9)

- 1000 DMIPS performance at 400 MHz
- ARM NEON multimedia engine
- Boots from parallel or serial flash

3 MB Internal RAM

- Use as large data buffer or to run system from internal memory
- Employs parallel bus structure dedicated to SRAM to speed processing

Execute-In-Place Operation from QSPI Flash

- Take full advantage of cost-effective external serial flash
- Simplifies program execution

Single- and Double-Precision Floating Point Unit, IEEE754 Compliant

- Accelerates trigonometric operations such as scaling and rotation

LCD Controller with 24-bit RGB Interface

- Handles 3-layer overlays
- Provides 1-ch video input, 1-ch display output
- Implements alpha blending
- Supports chroma keying

Bus Interface Controller

- Directly connects to SRAM, SDRAM, and flash (NOR, NAND, eMMC), as well as 128 KB L2 cache

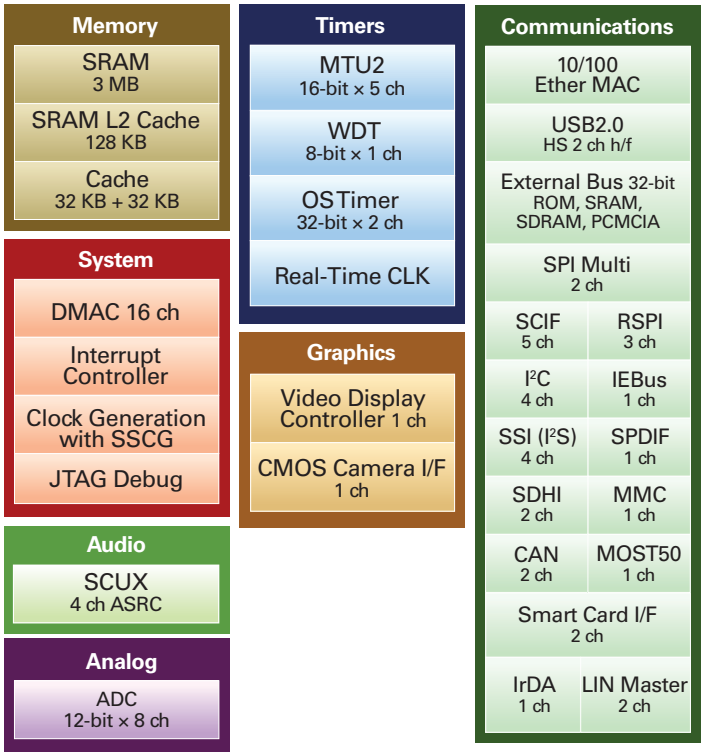
Multiple Network Connectivity Interfaces

- Integrates 10/100 EtherMAC controller (1 ch)
- Includes USB 2.0 host and function controller with integrated USB transceiver (2 ch)
- Offers up to 2 CAN channels

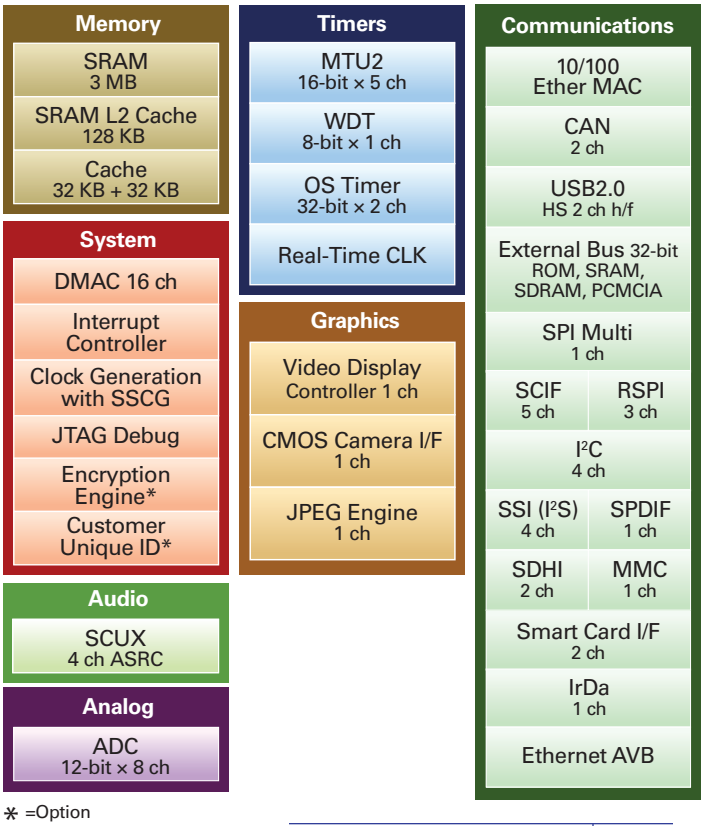
Three Package Options

- 208-pin QFP (0.5 mm)
- 176-pin QFP (0.5 mm)
- 176-pin BGA (0.5 mm)

RZ/A1L Block Diagram



RZ/A1LU Block Diagram



* =Option

Renesas RZ/A1 Device Selector

	RZ/A1H					RZ/A1M					RZ/A1L					RZ/A1LU				
Pin count	256-pin			324-pin		256-pin			324-pin		176-pin			208-pin		176-pin			208-pin	
Product name	R7S7210 00VCBG	R7S7210 00VCFP	R7S7210 00VLFP	R7S7210 01VCBG	R7S7210 01VLBG	R7S7210 10VCBG	R7S7210 10VCFP	R7S7210 10VLFP	R7S7210 11VCBG	R7S7210 11VLBG	R7S7210 20VCBG	R7S7210 20VCFP	R7S7210 20VLFP	R7S7210 21VCFP	R7S7210 21VLFP	R7S7210 30VCBG	R7S7210 30VCFP	R7S7210 30VLFP	R7S7210 31VCFP	R7S7210 31VLFP
CPU core	ARM® Cortex®-A9																			
RAM	10 MB					5 MB					3 MB					3 MB				
Cache memory	Primary cache: 64 KB (instruction 32 KB/data32 KB), TLB128 Secondary cache: 128 KB (Corelink™ Level 2 Cache Controller L2C-310)																			
Max. operating frequency (MHz)	400																			
Subclock (external: 32.768kHz)	Yes																			
PLL	Yes																			
Real-time clock	Yes																			
Power-on reset	Yes																			
Floating-point unit	Yes																			
DMA	DMAC × 16 ch																			
External memory interfaces	Serial flash (eXecute-In-Place (XIP) support), SRAM, SDRAM, burst ROM, NAND flash					Serial flash (eXecute-In-Place (XIP) support), SRAM, SDRAM, burst ROM, NAND flash					Serial flash (eXecute-In-Place (XIP) support), SRAM, SDRAM, burst ROM					Serial flash (eXecute-In-Place (XIP) support), SRAM, SDRAM, burst ROM				
External interrupt pins	148			180		148			180		109			131		109			131	
I/O ports	139			171		139			171		100			122		100			122	
16-/32-bit timer (ch)	5/2																			
Watchdog timer (ch)	1					1					–					1				
Other timers	Motor Controll PWM Timer × 8					Motor Controll PWM Timer × 8					–					–				
PWM output	16					16					–					–				
3-phase PWM output function	Yes					Yes					–					–				
12-bit A/D converter (channels)	8																			
CAN (channels)	5					5					2					2				
Ethernet	Yes																			
Ethernet AVB	Yes					Yes					–					Yes				
USB host function	Yes																			
USB peripheral function	Yes																			
USB (channels)	2																			
USB High Speed support	Yes																			
USB endpoints	16																			
USB isochronous transfer support	Yes																			
USB additional information	Low-speed Support (host only)																			
SD host interface (channels)	2																			
MMC host interface (channels)	1																			
Clock-synchronous serial interface (ch)	17					17					12					12				
SPI (channels)	5					5					5					3				
UART (channels)	8					8					8					5				
I²C (channels)	4																			
LIN (channels)	2					2					2					–				
IEBus (channels)	1					1					1					–				
Serial additional information	SCIF (CSI: 8 ch/UART: 8 ch), SCI (CSI: 2 ch), RSPI (SPI: 5 ch), SPI multi (SPI: 2 ch), SSI (CSI: 6 ch), SPDIF (CSI: 1 ch)					SCIF (CSI: 8 ch/UART: 8 ch), SCI (CSI: 2 ch), RSPI (SPI: 5 ch), SPI multi (SPI: 2 ch), SSI (CSI: 6 ch), SPDIF (CSI: 1 ch)					SCIF (CSI: 5 ch/UART: 5 ch), SCI (CSI: 2 ch), RSPI (SPI: 2 ch), SPI multi (SPI: 1 ch), SSI (CSI: 4 ch), SPDIF (CSI: 1 ch)					SCIF (CSI: 5 ch/UART: 5 ch), SCI (CSI: 2 ch), RSPI (SPI: 2 ch), SPI multi (SPI: 1 ch), SSI (CSI: 4 ch), SPDIF (CSI: 1 ch)				
Other display functions	VDC5: WXGA (1280 × 768), JPEG Engine, OpenVG Accelerator (2D)					VDC5: WXG(1280 × 768), JPEG Engine, OpenVG Accelerator (2D)					VDC5: XGA (1024 × 768)					VDC5: XGA (1024 × 768), JPEG Engine				
Power supply voltage (V)	3.3V/1.18V																			
Power supplies	VCC = PLLVCC = LVDSPLLVCC = USBAVCC = USBUVCC = USBDVCC = 1.10 to 1.26 V, PVCC = AVCC = USBAPVCC = VDAVCC = LVDSAPVCC = USBDPVCC = 3.0 to 3.6 V, VSS = AVSS = 0 V																			
Operating temp (°C)	TA = -40 to +85°C																			
Package (size [mm])	256-LFBGA (11 × 11 mm)	256-LQFP (28 × 28 mm)		324-FBGA (19 × 19 mm)		256-LFBGA (11 × 11 mm)	256-LQFP (28 × 28 mm)		324-FBGA (19 × 19 mm)		176-LFBGA (8×8 mm)	176-LQFP (24×24 mm)		208-LQFP (28×28 mm)		176-LFBGA (8×8 mm)	176-LQFP (24×24 mm)		208-LQFP (28×28 mm)	

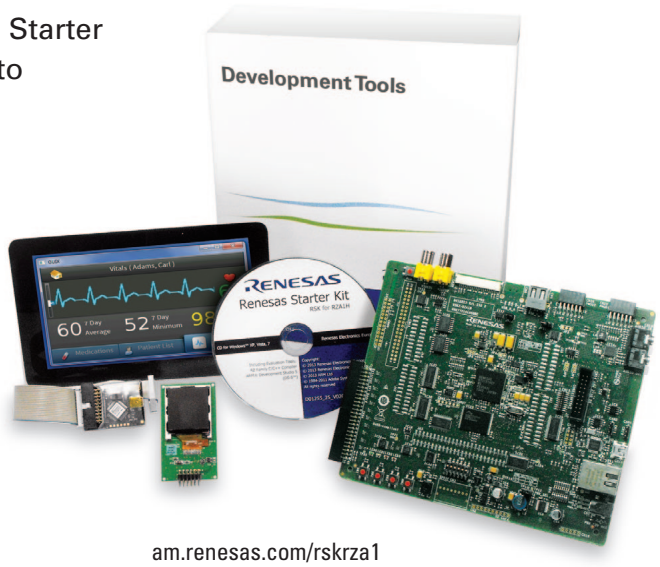
Renesas RZ/A1 Series Starter Kit

Shorten product development cycles with the Renesas Starter Kit (RSK). The RZ/A1 kit includes everything you need to jump-start your system development and ease the design and debug process.

The kit includes:

- 800 x 480 touch panel for HMI development (optional)
- Segger JTAG-lite debugger
- Embedded IDE and compiler with evaluation license
- Sample code and peripheral drivers

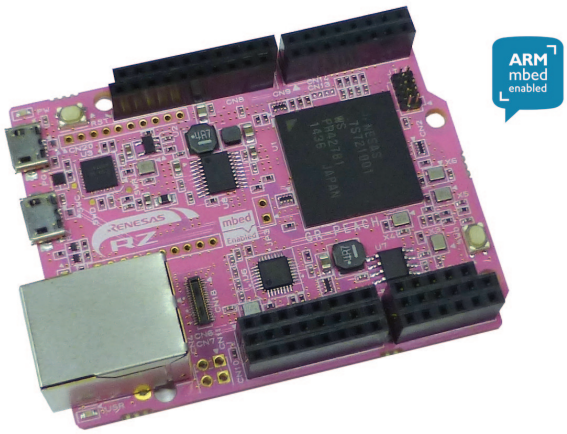
Part Number	TFT Display	Debugger
YR0K77210S001BE	No	Yes
YR0K77210S003BE	Yes	Yes



am.renesas.com/rskrza1

Renesas (GR-PEACH) ARM® mbed™ Platform

GR-PEACH from Renesas is an mbed enabled platform that combines the advantages of the mbed ecosystem and Arduino form factor. It is the first and only ARM mbed platform powered by a Cortex®-A class MPU.



Features

- 8 MB Flash
- 2xUSB Host/Device Interface, 1x Ethernet
- 3xSPI, 3xI²C, 8xUART, 7x12-bits ADC, 2xCAN
- 2xCamera Input

Arduino form-factor

- Compatible with a wide range of commercially available shields
- Built-in USB 'drag & drop' Flash programmer

mbed.org Developer Website

- Online Compiler
- High-level C/C++ SDK
- Active developer community

https://developer.mbed.org/platforms/Renesas-GR-Peach/

Part Number	Description
YGRPEACHFULL	GR-PEACH
YGRPEACHAUDIOCAMERASHIELD	GR-PEACH Audio Camera Shield
YGRPEACHLCDSHIELD	GR-PEACH LCD Shield

Linux support now available on RZ/A1 MPUs

Implementation Options

1. **XIP Linux (Execute-in-Place) with Advanced XIP File System (AXFS)**
   - Run from QSPI NOR Flash or on-chip SRAM
   - Buildroot and Yocto build options available
2. **Execute from SDRAM (up to 128 MB SDRAM)**

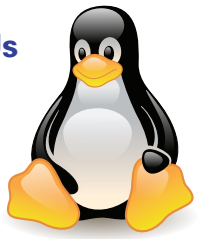
Commercial support

Embedded Linux from a Trusted Source
timesys®
www.timesys.com

Community support

RenesasRulz.com

Benefits of XIP Linux on RZ/A1 MPUs



- Direct execution from low-cost Quad-SPI Flash
- Memory size expansion without changing board layout
- Dual QSPI interface provides data access up to 528 Mb/s
- No external memory required
- Kernel memory usage as low as 1.5 MB of RAM
- Advanced XIP File System (AXFS) allows for lowest possible memory usage
- Faster system boot and application startup times
- Faster zero-copy page faults
- Separate buses allow simultaneous instruction fetches, data accesses and LCD frame buffer displaying without contention

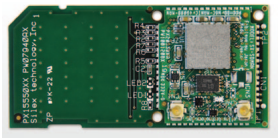
Renesas RZ/A1 XIP Linux Solution

Device drivers provided for:

- Ethernet
- USB Host/ USB Gadget
- RTC (real-time clock)
- NOR Flash
- LCD Display
- Touch Panel
- Audio
- SDHC
- MMC
- QSPI
- SPI
- GPIO
- UART
- I²C

Wi-Fi Support – SX-SDCAN for RZ/A1 XIP Linux

802.11 a/b/g/n plus Bluetooth® SDIO Radio Card

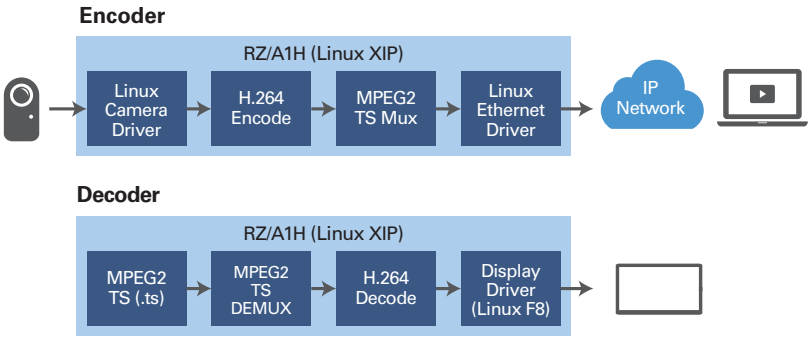


This proven connectivity solution has an SD-card form factor that implements a vendor-independent form factor

silex technology

- Offers IEEE 802.11a/b/g/n conformity (2.4 & 5 GHz)
- Applies single-stream 1x1 SISO technology and 40 MHz bandwidth mode for 5 GHz connectivity
- Supports IEEE 802.11e, IEEE 802.11h and IEEE 802.11i
- Supports SDIO 2.0 as host IF of wireless LAN
- Supports Bluetooth 4.0 + LE dual mode

H.264 Solution Enabled for XIP Linux



Consilient Technologies

www.consilient-tech.com

Graphics Support Packages for XIP Linux

Accelerates embedded UI development

Crank software inc.

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- The ARM DS-5™ Development Studio, Renesas RZ Edition, is a complete software development environment for systems that use RZ/A1 MPUs.
- This IDE provides the DS-5's code editor, compiler, debugger and performance analyzer. These tools seamlessly generate, debug and optimize code for the powerful ARM Cortex-A9 CPU built into RZ/A1 series chips.

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- Complete IDE supports IAR and free GNU compilers
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- Green Hills Software supports Renesas RZ/A1 MPUs with its MULTI® IDE, C/C++ optimizing compilers, Probe debugger, and many other development tools. These products let system engineers generate fast, compact code, quickly find and fix bugs, and make sense of complex systems.

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