RICOH

RP510L Series

4 A Forced PWM Step-down DC/DC Converter with Synchronous Rectifier

NO.EA-366-161118

OVERVIEW

The RP510L is a step-down DC/DC converter that operates the low input voltage of 2.5 V to 5.5 V. The RP510L being suitable for power supply of SoC (System-on-chip) can be output to 4 A (Max.). And, the foldback type protection, which be released automatically from the overcurrent protection, is user-selectable.

KEY BENEFITS

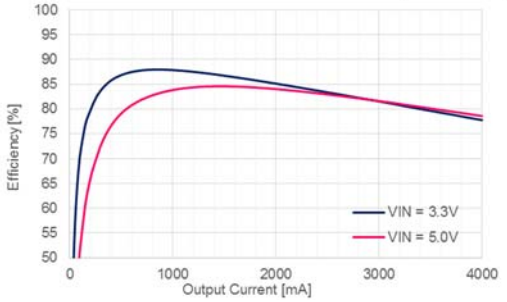
- The realization of the high-density mounting by the adoption of a small package DFN3030-12.
- A simplification of the power sequencing by power-good and adjustable soft-start functions.
- Selectable overcurrent protection: Latch type or Foldback type.

KEY SPECIFICATIONS

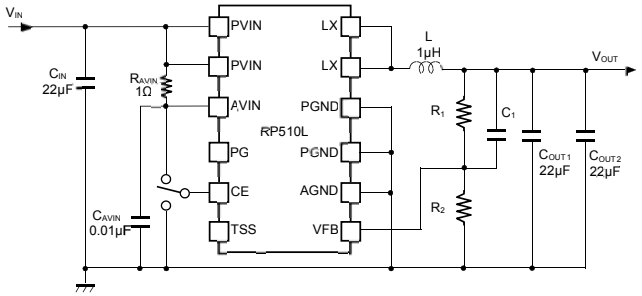
- Operating Temperature Range: −40°C to 85°C
- Output Voltage Range [1]: 0.8 V to 3.3 V
- Output Voltage Accuracy[2] : ±1% (V_{SET} ≥ 1.2V),
  ±12mV (V_{SET} < 1.2V)
- Feedback Voltage Accuracy[3] : ±6mV (V_{FB} = 0.6 V)
- Output/Feedback Voltage Temperature Coefficient: ±100ppm/°C
- Standby Current: Typ.0.35 µA (RP510LxxN)
  Typ.0.01 µA or less(RP510LxxG/H/J)
- Oscillator Frequency: Typ. 2.3MHz
- Built-in Driver On-resistance (Pch./Nch.): Typ.0.04Ω(V_{IN}=3.6V)
- Maximum Duty Cycle: Min. 100%
- Minimum On Time: Typ. 55ns
- Protection Features: UVLO, LX Peak Current Limit, Overcurrent protection (Latch/Foldback type), and Thermal shutdown.

TYPICAL CHARACTERISTICS

RP510L Series
V_{OUT} = 1.2V, V_{IN} = 3.3V / 5.0V
(Ta = 25°C)



TYPICAL APPLICATION CIRCUIT



RP510L001G/1H/4G/4H (Adjustable Output Voltage Type)

PACKAGE

DFN3030-12

Size: 3.0mm x 3.0mm, t = 0.8mm (Max.)

APPLICATIONS

- POL (Point of Load) Converter, and Micro-processor Power Supply with using Battery
- Server, Networking Equipment, FPGA, and DSP

[1] Refer to the section *SELECTION GUIDE* for details of V_{SET}.
[2] Fixed Output Voltage Type
[3] Adjustable Output Voltage Type

SELECTION GUIDE

The set output voltage, the output voltage type, the auto-discharge function(1), and the protection type are user-selectable options.

Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
RP510Lxx$$-TR	DFN3030−12	3,000 pcs	Yes	Yes

xx: Specify the set output voltage (V_{SET}).

00: Adjustable Output Voltage (0.8V to 3.3V)

xx: Selectable Fixed Output Voltage (0.8V, 1.0V, 1.1V, 1.2V, 1.3V, 1.5V, 1.8V, 3.0V, 3.3V)

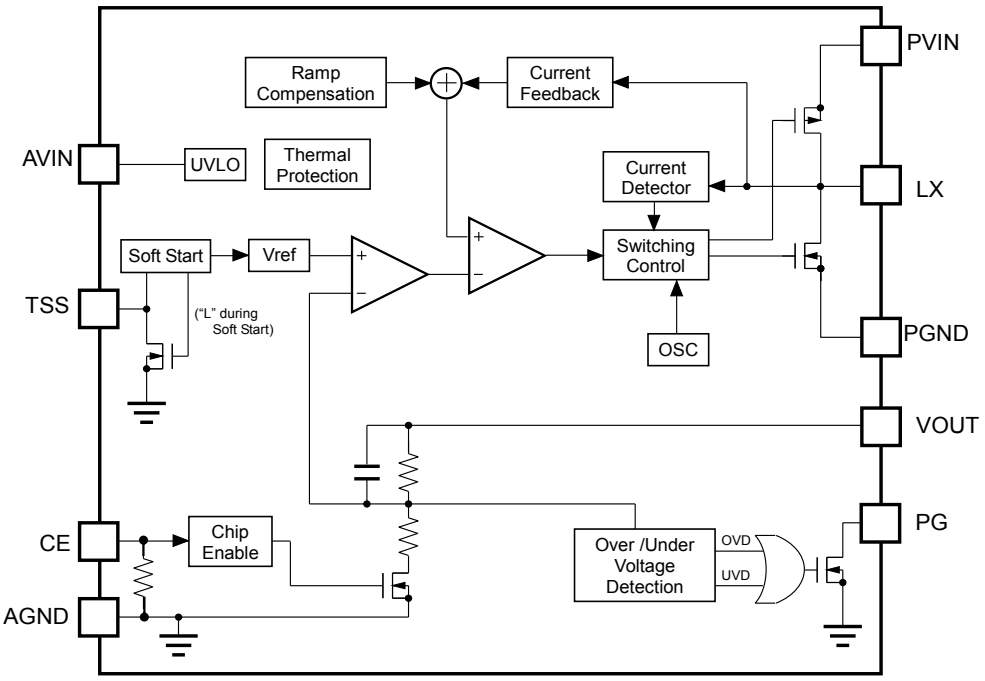
$$: Specify the combination of the output voltage type, the auto-discharge function, and the protection type.

Version	Output Voltage Type (V_{SET})	Auto-discharge Function	Oscillator Frequency	Protection Type	Product Name
1G	Fixed	No	2.3 MHz	Latch	**RP510Lxx1G**
1H		Yes			**RP510Lxx1H**
1J	Adjustable	No			**RP510L001J**
1N		Yes			**RP510L001N**
4G	Fixed	No		Foldback	**RP510Lxx4G**
4H		Yes			**RP510Lxx4H**
4J	Adjustable	No			**RP510L004J**
4N		Yes			**RP510L004N**

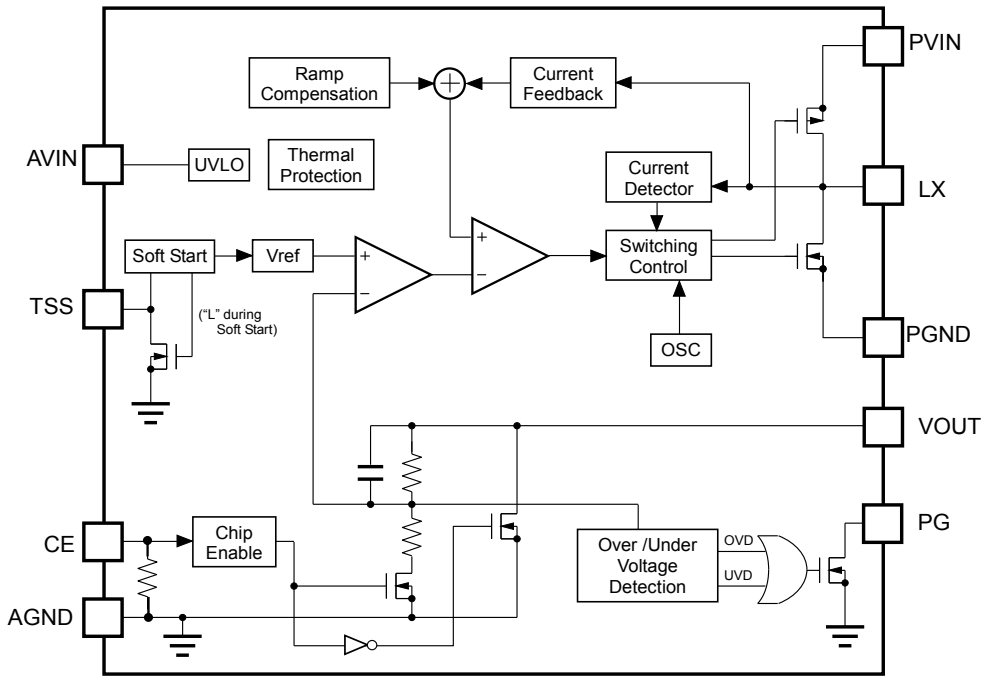
(1) Auto-discharge function quickly lowers the output voltage to 0 V, when the chip enable signal is switched from the active mode to the standby mode, by releasing the electrical charge accumulated in the external capacitor.

BLOCK DIAGRAM

RP510Lxx1G/4G/1H/4H (Fixed Output Voltage Type)

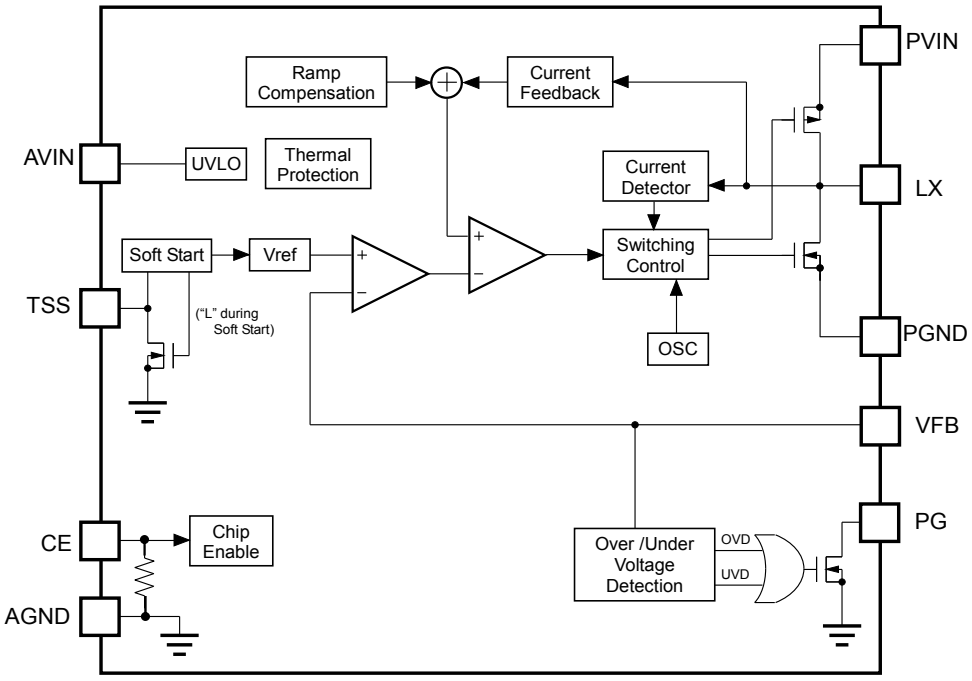


RP510Lxx1G/ 4G Block Diagram

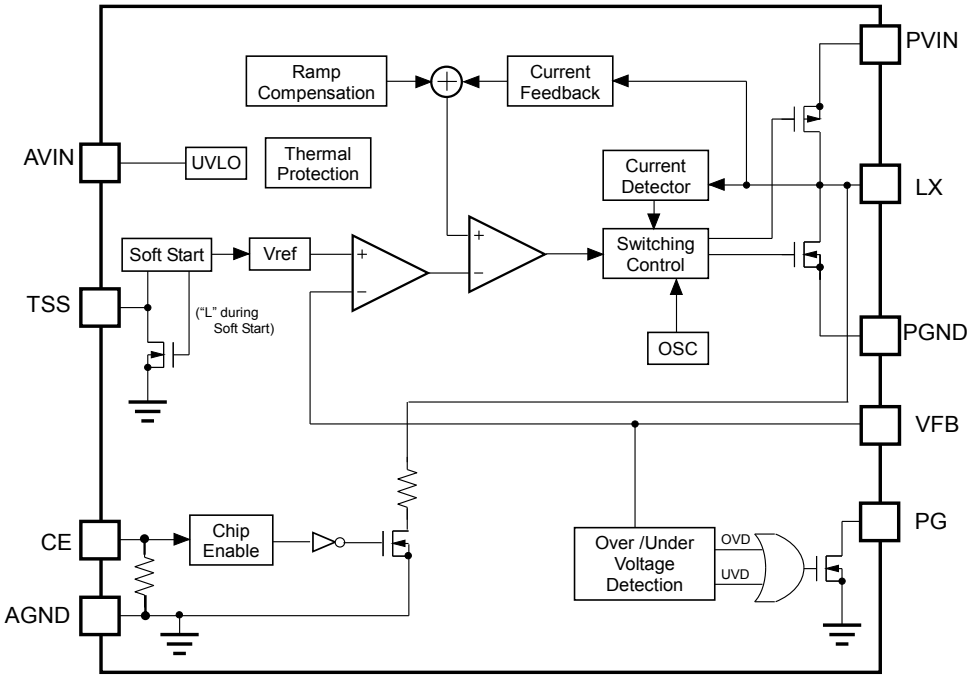


RP510Lxx1H/ 4H Block Diagram

RP510L001J/4J/1N/4N (Adjustable Output Voltage Type)

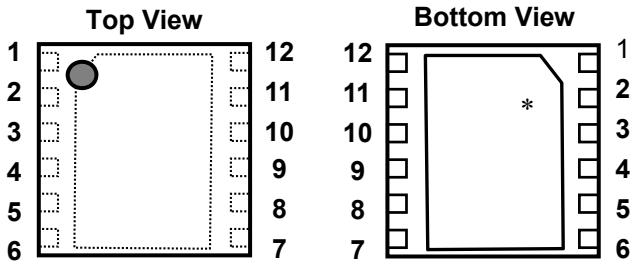


RP510L001J/ 4J Block Diagram



RP510L001N/ 4N Block Diagram

PIN DESCRIPTION



DFN3030-12 Pin Configurations

DFN3030-12 Pin Description

Pin No.	Pin Name	Description
1	PVIN (1)	Input Voltage Pin
2	PVIN (1)	Input Voltage Pin
3	AVIN (2)	Input Voltage Pin
4	PG	Power Good Pin (NMOS Open-drain)
5	CE	Chip Enable Pin (Active “H”)
6	TSS	Soft-start Pin
7	VOUT/ VFB	Output Voltage Pin / Feedback Voltage Pin
8	AGND (3)	Analog Ground Pin
9	PGND (3)	Power Ground Pin
10	PGND (3)	Power Ground Pin
11	LX	Switching Pin
12	LX	Switching Pin

∗ The tab on the bottom of the package must be connected to the ground plane on the board to enhance thermal performance.

(1) No.1 pin and No.2 pin must be wired to the V_{IN} plane when mounting on boards.
(2) No.3 pin must be wired to No.1 and No.2 pins via a low-pass filter (LPF: 1Ω, 10nF) when mounting on boards.
(3) No.8 pin, No.9 pin and No.10 pin must be wired to the GND plane when mounting on boards.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings (AGND = PGND = 0 V)

Symbol	Item		Rating	Unit
V_{IN}	A/PVIN Pin Voltage		−0.3 to 6.5	V
V_{LX}	LX Pin Voltage		−0.3 to V_{IN} + 0.3	V
V_{CE}	CE Pin Voltage		−0.3 to 6.5	V
V_{OUT}/ V_{FB}	Output Voltage / Feedback Voltage		−0.3 to 6.5	V
V_{PG}	PG Pin Voltage		−0.3 to 6.5	V
V_{TSS}	TSS Pin Voltage		−0.3 to V_{IN} + 0.3	V
P_D	Power Dissipation (1)	Standard Land Pattern	1000	mW
		JEDEC STD. 51-7 Test Land Pattern	1950	
Tj	Junction Temperature Range		−40 to 125	°C
Tstg	Storage Temperature Range		−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field.
The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	2.5 to 5.5	V
Ta	Operating Temperature Range	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

(1) Refer to *POWER DISSIPATION* for detailed information.

ELECTRICAL CHARACTERISTICS

The specification in ☐ is checked and guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

RP510Lxx1/4 Electrical Caharacteristics (Ta = 25°C)

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
$I_{STANDBY}$	Standby Current	V_{IN} = 5.5 V, V_{CE} = 0 V	RP510LxxxN		0.35	15.5	µA
			RP510LxxxG/H/J		0.01	7.5	
R_{CE}	CE Pin Pull-down Resistance				1		MΩ
I_{CEL}	CE Pin Input Current, Low	V_{IN} = 5.5 V, V_{CE} = 0 V		−1	0	1	µA
$I_{LXLEAKH}$	LX Pin Leakage Current, High	V_{IN} = V_{LX} = 5.5 V, V_{CE} = 0 V		−1	0	3	µA
$I_{LXLEAKL}$	LX Pin Leakage Current, Low	V_{IN} = 5.5 V, V_{CE} = V_{LX} = 0 V		-10	0	1	µA
V_{CEH}	CE Pin Input Voltage, High	V_{IN} = 5.5 V		1.0			V
V_{CEL}	CE Pin Input Voltage, Low	V_{IN} = 2.5 V				0.4	V
t_{START1}	Soft-start Time1	V_{IN} = V_{CE} = 3.6 V or V_{SET} + 1 V, TSS = OPEN		75	150	300	µs
t_{START2}	Soft-start Time2	V_{IN} = V_{CE} = 3.6 V or V_{SET} + 1 V, C_{SS} = 0.1 µF		15	30	45	ms
I_{LXLIM}	LX Current Limit	V_{IN} = V_{CE} = 3.6 V or V_{SET} + 1 V		5000	6500		mA
t_{PROT}	Protection Delay Time	V_{IN} = V_{CE} = 3.6 V or V_{SET} + 1 V		0.5	1.5	5	ms
V_{UVLO1}	UVLO Threshold Voltage	V_{IN} = V_{CE}, Falling		2.1	2.2	2.3	V
V_{UVLO2}		V_{IN} = V_{CE}, Rising		2.2	2.3	2.4	V
T_{TSD}	Thermal Shutdown Threshold Temperature, Detection	Tj, Rising			165		°C
T_{TSR}	Thermal Shutdown Threshold Temperature, Release	Tj, Falling			115		°C
R_{PGDIS}	PG Pin Low Output ON Resistance	V_{IN} = 3.6 V, V_{OUT} = 0 V or V_{FB} = 0 V			45		Ω
f_{OSC}	Oscillation Frequency	V_{IN} = V_{CE} = 3.6 V or V_{SET} + 1 V		2.00	2.3	2.50	MHz

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

The specification in ☐ is checked and guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

RP510Lxx1G/1H/4G/4H [Fixed Output Voltage Type] (Ta = 25°C)

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	V_{IN} = V_{CE} = 3.6 V or V_{SET} + 1 V	V_{SET} ≥ 1.2 V	x0.99		x1.01	V
				☐x0.98		☐x1.02	
			V_{SET} < 1.2 V	−0.012		0.012	
				☐−0.024		☐0.024	
I_{SS}	Supply Current	V_{IN} = V_{CE} = 5.5 V			800		μA
I_{VOUTL}	VOUT Pin Current, Low	V_{IN} = 5.5 V, V_{CE} = V_{OUT} = 0 V		☐−1	0	☐1	μA
V_{OVD}	OVD Voltage	V_{IN} = 3.6 V			V_{SET} × 1.2		V
V_{UVD}	UVD Voltage	V_{IN} = 3.6 V			V_{SET} × 0.8		V
RP510Lxx1G/4G [Fixed Output Voltage Type, without Auto-discharge function]							
I_{VOUTH}	VOUT Pin Current, High	V_{IN} = V_{OUT} = 5.5 V, V_{CE} = 0 V		☐−1	0	☐1	μA
RP510Lxx1H/4H [Fixed Output Voltage Type, with Auto-discharge function]							
$R_{VOUTDIS}$	VOUT Pin Discharge NMOS ON-resistance	V_{IN} = 2.5 V, V_{CE} = 0 V, V_{OUT} = 0.5 V			45		Ω

RP510L001J/1N/4J/4N [Adjustable Output Voltage Type]

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{FB}	Feedback Voltage	V_{IN} = V_{CE} = 3.6 V	0.594	0.600	0.606	V
			☐0.588	0.600	☐0.612	
I_{SS}	Supply Current	V_{IN} = V_{CE} = 5.5 V		800		μA
I_{VFBH}	VFB Pin Current, High	V_{IN} = V_{FB} = 5.5 V, V_{CE} = 0 V	☐−1	0	☐1	μA
I_{VFBL}	VFB Pin Current, Low	V_{IN} = 5.5 V, V_{CE} = V_{FB} = 0 V	☐−1	0	☐1	μA
V_{OVD}	OVD Voltage	V_{IN} = 3.6 V		0.72		V
V_{UVD}	UVD Voltage	V_{IN} = 3.6 V		0.48		V
RP510L001N/4N [Adjustable Output Voltage Type, with Auto-discharge function]						
R_{LXDIS}	LX Pin Discharge NMOS ON-resistance	V_{IN} = 2.5 V, V_{CE} = 0 V, L_X = 0.5 V		65		Ω

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

The specification in ☐ is checked and guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

RP510Lxx1G/1H/4G/4H [Fixed Output Voltage Type] Product-specific Electrical Characteristics

Product Name	V_{OUT} [V]					
	Ta = 25°C			−40°C ≤ Ta ≤ 85°C		
	Min.	Typ.	Max.	Min.	Typ.	Max.
RP510x08xx	0.788	0.800	0.812	0.776	0.800	0.824
RP510x10xx	0.988	1.000	1.012	0.976	1.000	1.024
RP510x11xx	1.088	1.100	1.112	1.076	1.100	1.124
RP510x12xx	1.188	1.200	1.212	1.176	1.200	1.224
RP510x13xx	1.287	1.300	1.313	1.274	1.300	1.326
RP510x15xx	1.485	1.500	1.515	1.470	1.500	1.530
RP510x18xx	1.782	1.800	1.818	1.764	1.800	1.836
RP510x30xx	2.970	3.000	3.030	2.940	3.000	3.060
RP510x33xx	3.267	3.300	3.333	3.234	3.300	3.366

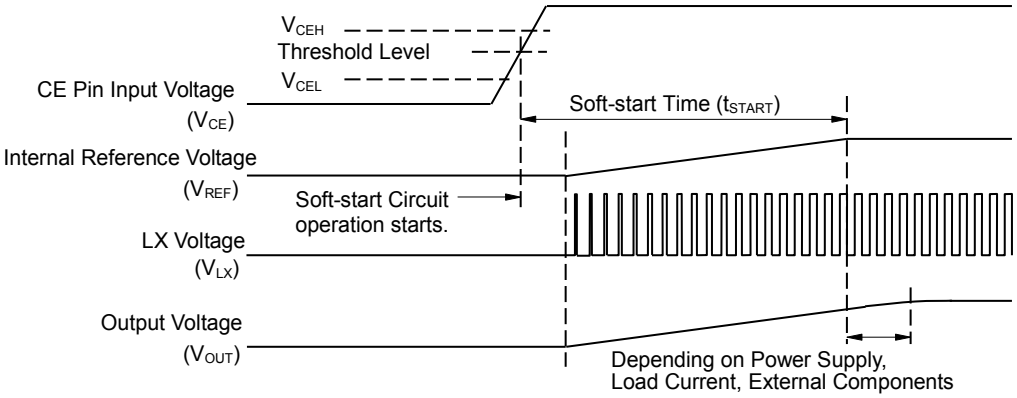
THEORY OF OPERATION

Soft-start

Starting-up with CE Pin

The device starts to operate when the CE pin voltage (V_{CE}) exceeds the threshold voltage. The threshold voltage is preset between CE "High" input voltage (V_{CEH}) and CE "Low" input voltage (V_{CEL}). The soft-start circuit also starts to operate after the device start-up. Then, after a certain period of time, the reference voltage (V_{REF}) in the device gradually increases up to the specified value.

Notes: Soft-start time (t_{START})[1] might not be always equal to an actual turn-on speed of the output voltage. Please note that the turn-on speed could be affected by the power supply capacity, the output current, the inductance value, and the C_{OUT} value.



Timing Chart when Starting-up with CE Pin

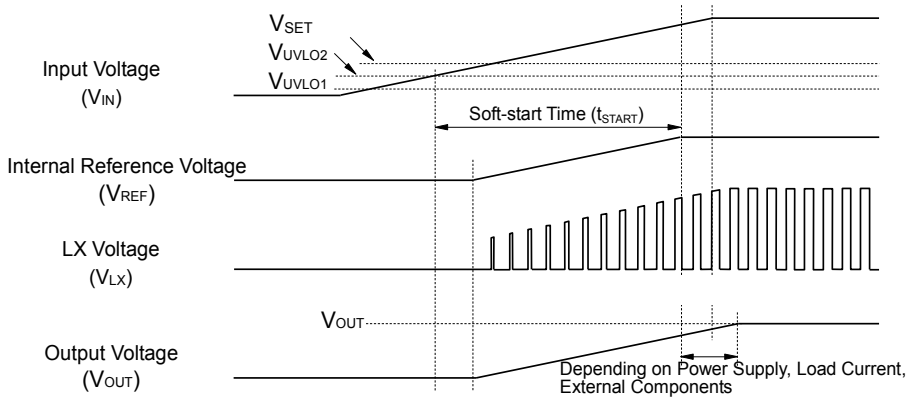
Starting-up with Power Supply

After the power-on, the device starts to operate when V_{IN} exceeds the UVLO released voltage (V_{UVLO2}). The soft-start circuit also starts to operate. Then after a certain period of time, V_{REF} gradually increases up to the specified value.

Notes: Please note that the turn-on speed of V_{OUT} could be affected by the following conditions.

1. Power supply capacity and Turn-on speed of V_{IN} determined by C_{IN}
2. Values of Inductor, Capacitor and Output current

[1] Soft-start time (t_{START}) indicates the duration until the reference voltage (V_{REF}) reaches the specified voltage after soft-start circuit's activation.

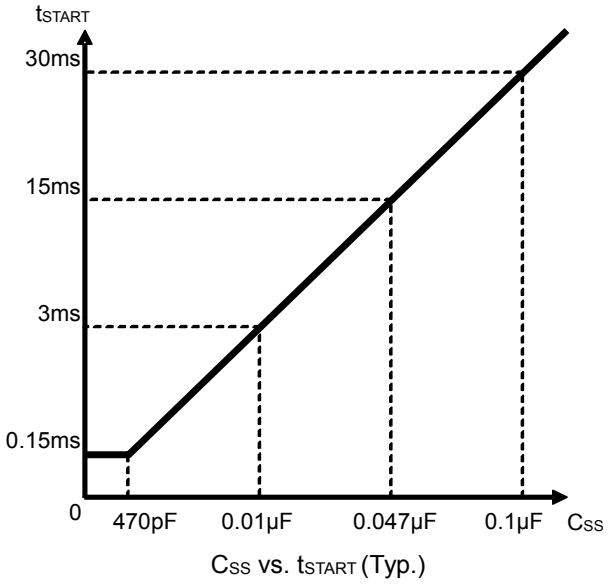


Timing Chart when Starting-up with Power Supply

Soft-start Time Adjustment

Soft-start time (t_{START}) of the RP510L is adjustable by connecting a soft-start time adjustment capacitor (C_{SS}) between the TSS pin and GND. t_{START} can be set from Typ. 0.15 ms as a lower limit. As the figure below shows, t_{START} is Typ. 30 ms when C_{SS} is 0.1 µF. If not requiring to adjust t_{START}, t_{START} is set to 0.15 ms (Typ.) by making the TSS pin open. The capacitance value for required soft-start time (t_{START}) can be calculated by the following equation.

$$C_{SS}\ [nF] = 3.5 \times t_{START}\ [ms]$$



Soft-start Time (t_{START}) vs. Soft-start Time Adjustment Capacitor (C_{SS})

Power Good Function

If any condition as follows is detected, power good function with using Nch. open drain turns Nch. transistor ON and switches the PG pin to “Low”. After the condition is removed, the power good function turns Nch. transistor OFF and switches the PG pin back to “High”. The time until the Nch. transistor is turned OFF includes the release delay time of 0.05 ms (Typ.).

- CE = ”L” (Shut down)
- UVLO
- Thermal Shutdown
- Over Voltage Detection (Typ.):

  V_{OUT} > V_{SET} x 1.2 V (RP510Lxx1G/1H/4G/4H) or V_{FB} > 0.72 V (RP510L001J/1N/4J/4N)
- Under Voltage Detection (Typ.):

  V_{OUT} < V_{SET} x 0.8 V (RP510Lxx1G/1H/4G/4H) or V_{FB} < 0.48 V (RP510L001J/1N/4J/4N)
- During the Latch Type Protecting operation

Notes: When using the power good function, the resistance of PG pin (R_{PG}) should be between 10 kΩ to 100 kΩ. The PG pin must be open or connected to GND if the power good function is not used.

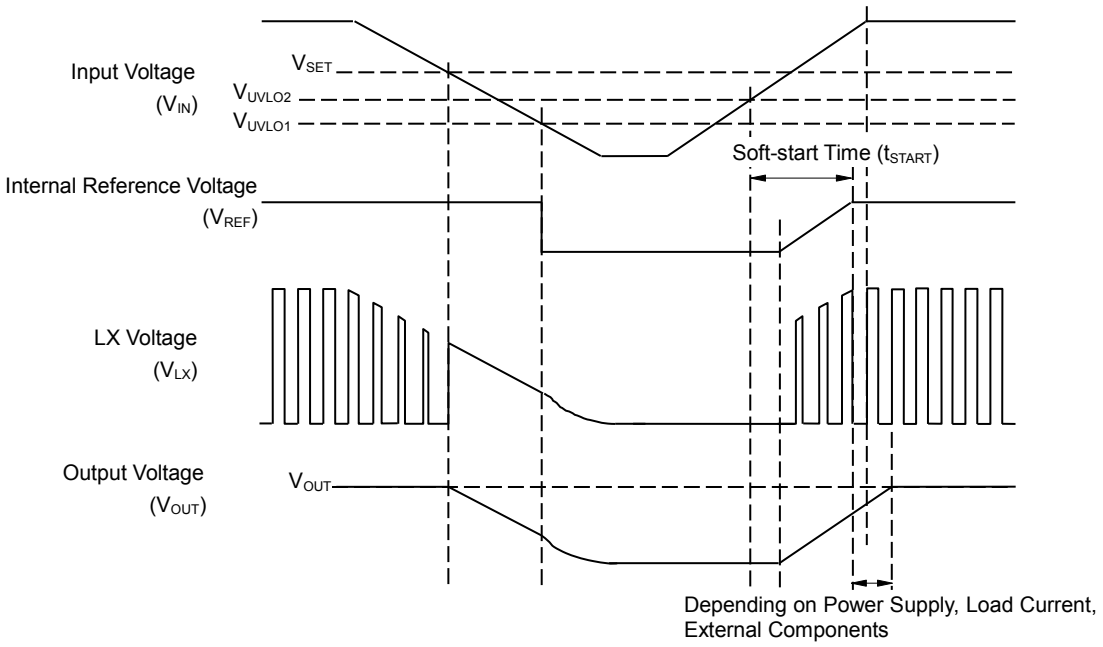
Under Voltage Lockout (UVLO)

If V_{IN} becomes lower than V_{SET}, the step-down DC/DC converter stops the switching operation and ON duty becomes 100%, and then V_{OUT} gradually drops according to V_{IN}.

If the V_{IN} drops more and becomes lower than the UVLO detector threshold (V_{UVLO1}), the UVLO circuit starts to operate, V_{REF} stops, and Pch. and Nch. built-in transistors become the OFF state. As a result, V_{OUT} drops according to the C_{OUT} capacitance value and the load.

To restart the operation, V_{IN} is required to be higher than V_{UVLO2}. The timing chart below shows the voltage shifts of V_{REF}, V_{LX} and V_{OUT} in response to variation of the V_{IN} value.

Notes: Falling edge (operating) and rising edge (releasing) waveforms of V_{OUT} might be affected by the initial voltage of C_{OUT} and the output current of V_{OUT}.



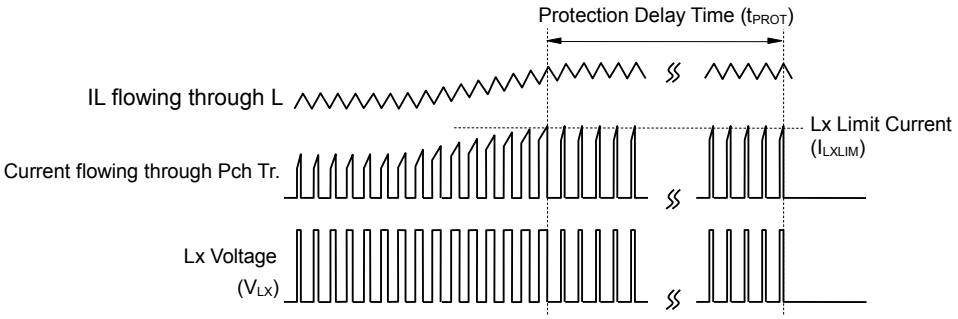
Timing Chart with Variations in Input Voltage (V_{IN})

Current limit Function

Current limit circuit supervises the inductor current flowing through the Pch. transistor in each switching cycle. If the current exceeds the LX current limit (I_{LXLIM}, Typ.6.5A), a Pch. transistor is turned off and the upper limit of the inductor peak current is imposed.

Latch Type Protection (RP510Lxx1G/1H, RP510L001J/1N)

Latch type protection circuit latches Pch. and Nch. transistors in the OFF state and stops the operation of the step-down DC/DC converter when the over current status or the output voltage (V_{OUT}) / the feedback voltage (V_{FB}) being dropped to the half of the setting voltage due to shorting continues for the protection delay time (t_{PROT}). To release the latch type protection circuit, restart the device by inputting "Low" signal to the CE pin or making the supply voltage lower than V_{UVLO1}.



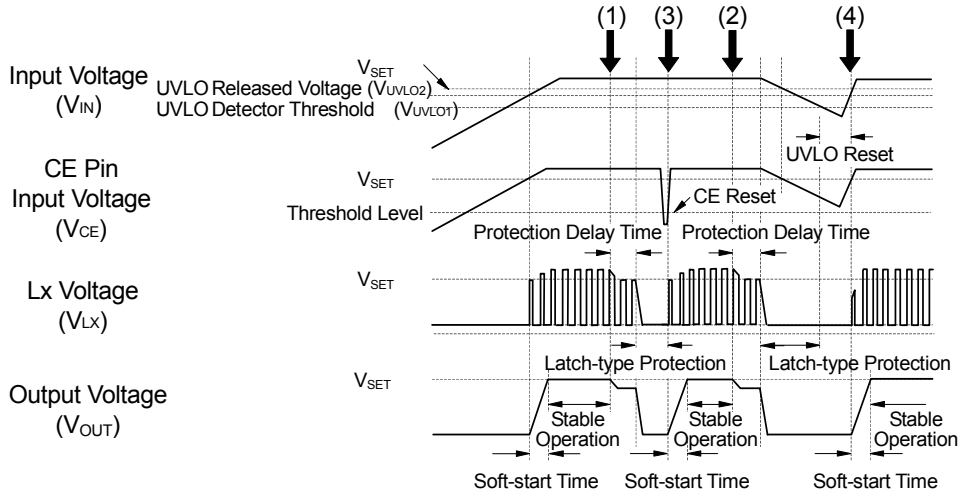
Protection Delay Time

The timing chart below shows the voltage shift of V_{CE}, V_{LX} and V_{OUT} when the device status is changed by the following orders: V_{IN} rising → stable operation → high load → CE reset → stable operation → V_{IN} falling → V_{IN} recovering (UVLO reset) → stable operation.

(1)(2) If the overcurrent flows through the circuit or the device goes into low V_{OUT} condition due to short-circuit or other reasons, the latch type protection circuit latches Pch. and Nch. transistors in the OFF state after t_{PROT}. Then, V_{LX} becomes "Low" and V_{OUT} turns OFF.

(3) The latch type protection circuit is released by CE reset, which puts the device into "Low" once with the CE pin and back into "High".

(4) The latch type protection circuit is released by UVLO reset, which makes V_{IN} lower than V_{UVLO1}.



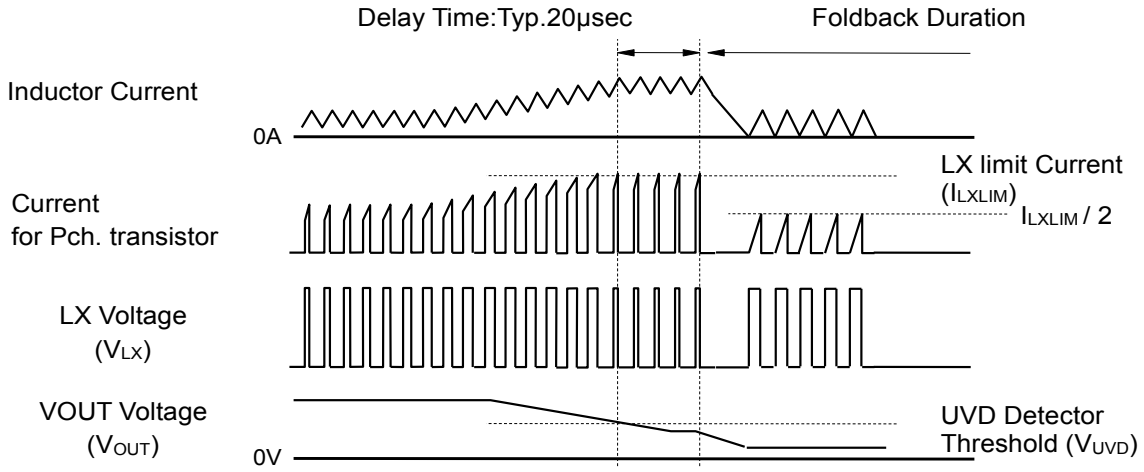
Timing Chart

Foldback Protection (RP510Lxx4G/4H, RP510L004J/4N)

If the device is in a state where an overcurrent is detected during protection delay time (t_{PROT}) or a state where the output voltage (V_{OUT}) or the feedback voltage (V_{FB}) becomes lower than UVD detector threshold (V_{UVD}) over about 20 µsec while the overcurrent is caused by an output short-circuit, the foldback protection is enabled. During the foldback protection, the inductor current is set to the upper limit of 1/2 of LX limit current (I_{LXLIM}) and the lower limit of 0mA. During the foldback protection, the device alternately operates the following Pch. and Nch. transistor as follows: the Pch. transistor is turned ON until the inductor current reach the upper limit and the Nch. transistor is turned ON until the inductor current reach 0mA. Therefore, the switching frequency is decreased and the upper limit of the output current (I_{OUT_SHORT}) during the foldback protection is limited to a current value calculated by the following equation.

$$I_{OUT_SHORT} = I_{LXLIM} / 4$$

When the short-circuit and the overcurrent states are released and the output current (I_{OUT}) becomes less than I_{OUT_SHORT}, the output voltage reaches the set output voltage. Then, the foldback protection is released. And also, the foldback protection is released when the device is reset by inputting CE pin to “Low” or by decreasing the input voltage to less than the UVLO detector threshold (V_{UVLO1}). If the foldback protection occurs by the short-circuit and the overcurrent states when I_{OUT} exceed I_{OUT_SHORT}, the device might not return to a normal state even if their states are released. Release of the foldback protection is required to reduce I_{OUT} less than I_{OUT_SHORT} or reset the device.



Foldback Protection Timing Chart at Low Output Voltage

Note: The current limit function and the overcurrent limit protection of the latch / foldback type, as described above, becomes possible to provide a high degree of safety to the device, not to secure reliability. And, I_{LXLIM} and t_{PROT} could be easily affected by self-heating or ambient environment. If the V_{IN} drops dramatically or becomes unstable due to short-circuit, protection operation and t_{PROT} could be affected.

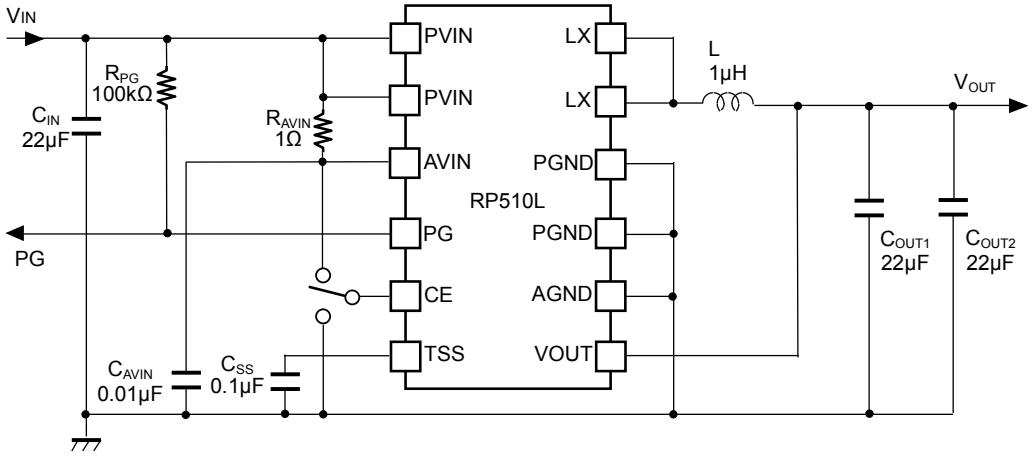
Reverse Current Limit Function

The reverse current limit function supervises the current on the Nch. transistor in every switching. When an overcurrent more than the threshold current (Typ. -2.0A) occur, the Nch. transistor is turned off to limit a lower of the inductor current. On the heavy-to-light load transient, the reverse current limit function may occur by the overcurrent. If this limit function occur, the reduction of the output voltage overshoot by reverse current will be limited.

APPLICATION INFORMATION

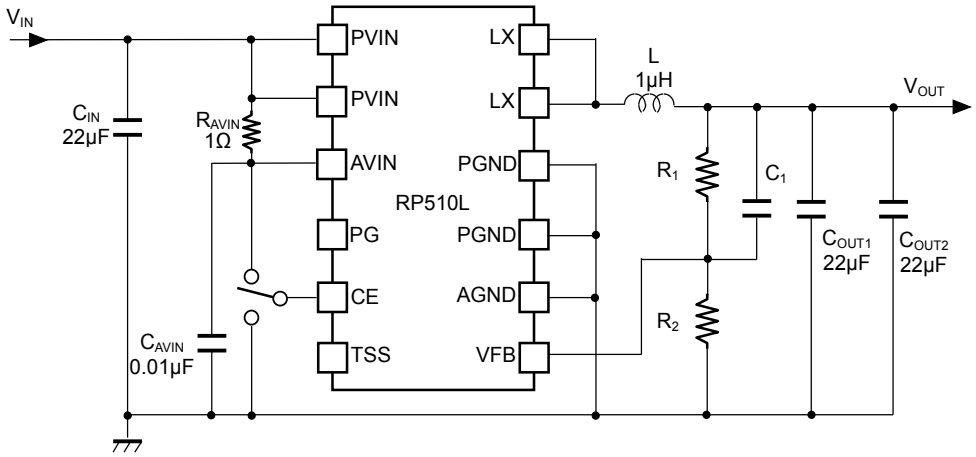
Typical Application Circuit

Conditions: Power Good enabled, Soft-start time of 30 ms



RP510Lxx1G/1H/4G/4H (Fixed Output Voltage Type)

Conditions: Power Good disabled, Soft-start time of 150 μs



RP510L001J/1N/4J/4N (Adjustable Output Voltage Type)

Cautions in selecting external components

- Choose a low ESR ceramic capacitor. The input capacitor (C_{IN}) between PVIN and PGND should be more than 22 µF, and the output capacitor (C_{OUT}) should be used by two or more parallel connection with ceramic capacitor of 22 µF.
- The phase compensation of this device is designed according to the C_{OUT} and L values. The inductance value of an inductor should be 1.0µH to gain stability.
- Choose an inductor that has small DC resistance, has enough permissible current and is hard to cause magnetic saturation. If the inductance value of the inductor becomes extremely small under the load conditions, the peak current of LX may increase along with the load current. As a result, the overcurrent protection circuit may start to operate when the peak current of LX reaches to LX limit current. Therefore, choose an inductor with consideration for the value of I_{LXMAX}. See the following page of *Calculation Conditions of LX Pin Maximum Output Current (I_{LXMAX})*.
- As for the adjustable output voltage type (RP510L001J/1N/4J/4N), the output voltage (V_{OUT}) is adjustable by changing the resistance values of R1 and R2.

  V_{SET}[(2)]$= V_{FB} \times (R1 + R2) / R2$ $\quad (0.8\ V \leq V_{SET} \leq 3.3\ V)$

  If R2 are too large, the impedance of V_{FB} also become large, as a result, the device could be easily affected by noise. For this reason, R2 should be 30kΩ or less. If the operation becomes unstable dues to the high impedances, the impedances should be decreased.
  C1 can be calculated by the following equation. Please use the value close to the calculation result.

  $C1 = 5 \times 10^{-7} / R2$ [F]

  The recommended component values for R1, R2, and C1 are as follows.

Set Output Voltage (V_{SET}) vs. Resistor (R1, R2), Capacitor (C1)

Set Output Voltage V_{SET} [V]	Resistor [kΩ]		Capacitor [pF]
	R1	R2	C1
0.8	10	30	16
1.2	20	20	25
1.8	40	20	25
2.5	95	30	16
3.3	90	20	25

(2) V_{SET}: set output voltage

Calculation Conditions of LX Pin Maximum Output Current (I_{LXMAX})

The following equations explain the relationship to determine I_{LXMAX} at the ideal operation of the device in continuous mode.

I_{RP} : Ripple Current P-P value

R_{ONP} / R_{ONN} : ON resistance of Pch. / Nch. transistor

R_L : DC resistance of the inductor

First, when the Pch. transistor is “ON”, Equation 1 is satisfied.

$$V_{IN} = V_{OUT} + (R_{ONP} + R_L) \times I_{OUT} + L \times I_{RP} / t_{ON} \cdots\cdots \text{Equation 1}$$

Second, when the Pch. transistor is "OFF" (the Nch. transistor is "ON"), Equation 2 is satisfied.

$$L \times I_{RP} / t_{OFF} = R_{ONN} \times I_{OUT} + V_{OUT} + R_L \times I_{OUT} \cdots\cdots \text{Equation 2}$$

Put Equation 2 into Equation 1 to solve ON duty of the Pch. transistor ($D_{ON} = t_{ON} / (t_{OFF} + t_{ON})$):

$$D_{ON} = (V_{OUT} + R_{ONN} \times I_{OUT} + R_L \times I_{OUT}) / (V_{IN} + R_{ONN} \times I_{OUT} - R_{ONP} \times I_{OUT}) \cdots\cdots \text{Equation 3}$$

Ripple Current is described as follows:

$$I_{RP} = (V_{IN} - V_{OUT} - R_{ONP} \times I_{OUT} - R_L \times I_{OUT}) \times D_{ON} / f_{OSC} / L \cdots\cdots \text{Equation 4}$$

Peak current that flows through L, and Pch.and Nch. transistors is described as follows:

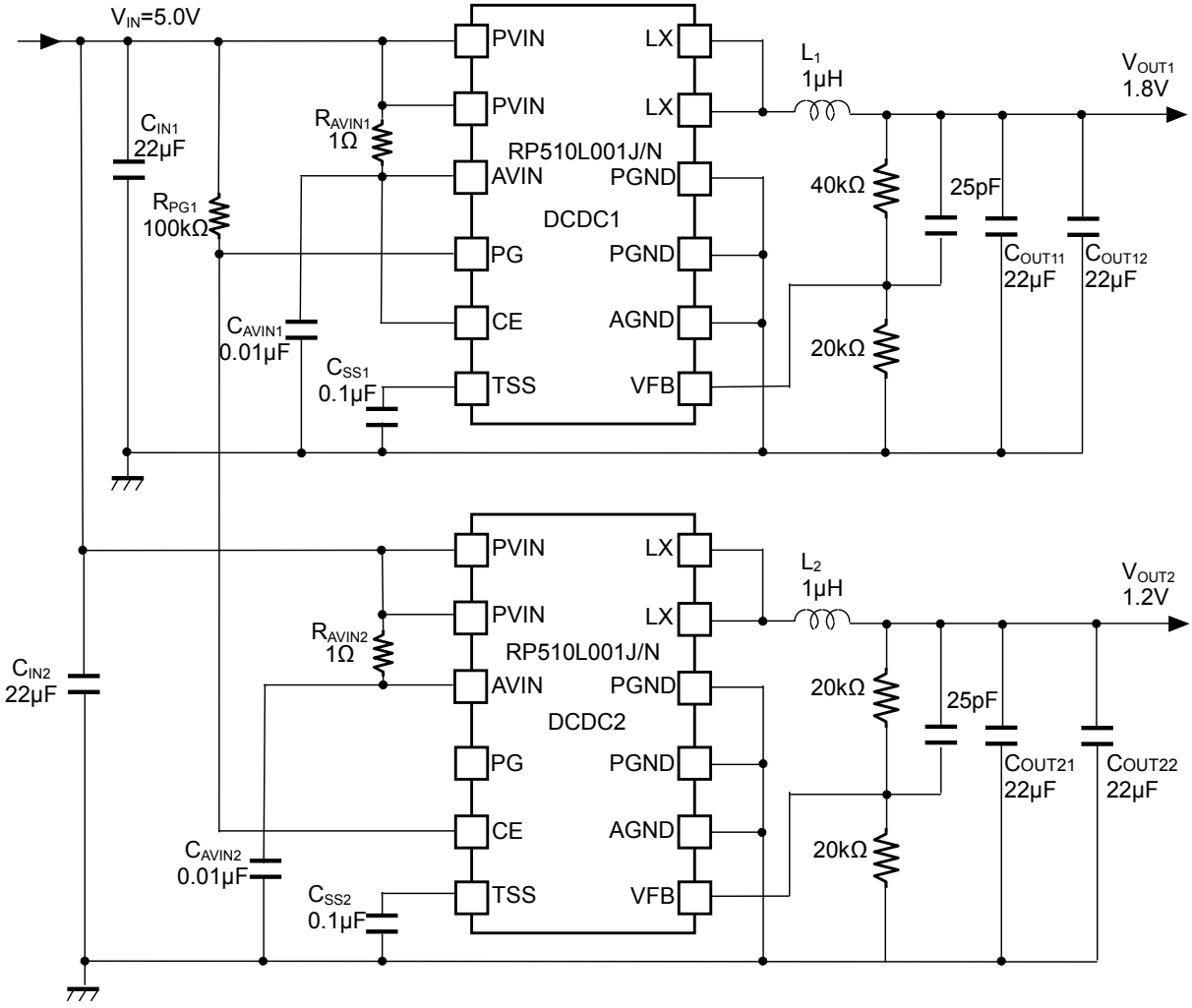
$$I_{LXMAX} = I_{OUT} + I_{RP} / 2 \cdots\cdots \text{Equation 5}$$

Example applications: Control sequencer

Sequencer control can establishes by using the soft-start time adjustment and the power good functions of the RP510L. The following figure indicates an application circuit example with using two RP510L (DCDC1 and DCDC2).

DCDC1 starts up prior to DCDC2. After DCDC1 reaches the output voltage of typ.1.44V (V_{SET} x 0.8), CE pin of DCDC2 receives "High" signal from PG pin of DCDC1, and the DCDC2's soft-start starts.

DCDC1 (RP510L001J/1N): V_{IN} = 5.0 V, V_{OUT} = 1.8 V, t_{START} = 30 ms, C_{SS} = 0.1 µF
DCDC2 (RP510L001J/1N): V_{IN} = 5.0 V, V_{OUT} = 1.2 V, t_{START} = 30 ms, C_{SS} = 0.1 µF



Sequence Control Application Circuit Example

TECHNICAL NOTES

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. A peripheral component or the device mounted on PCB should not exceed a rated voltage, a rated current or a rated power. When designing a peripheral circuit, please be fully aware of the following points.

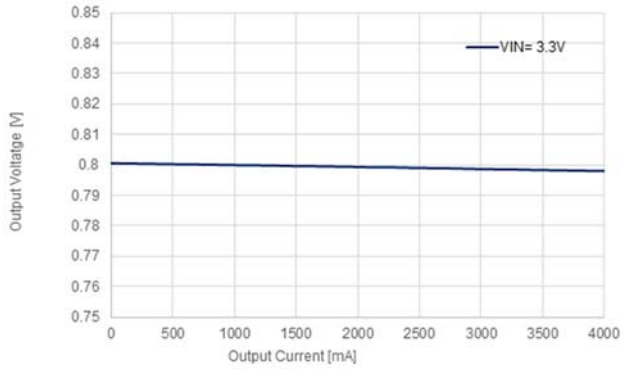
- AGND and PGND must be wired to the GND plane when mounting on boards.
- AVIN must be connected to between an input capacitor (C_{IN}) and PVIN via a low-pass filter (Recommended LPF: 1Ω, 10nF). Place a capacitor between AVIN and AGND as close as possible to the IC.
- Set the external components as close as possible to the IC and minimize the wiring between the components and the IC. Especially, place C_{IN} as close as possible to PVIN pin and PGND.
- Use the VIN and the GND lines as wide and short as possible to make low impedance, since noise pickup or unstable operation occurs when their impedance are too high.
- The VIN line, the GND line, the V_{OUT} line, an inductor, and L_X should make special considerations for the large switching current flows.
- For the feedback of output voltage, the wiring to the VOUT pin (RP510Lxxx1G/1H/4G/4H) or to a resistor for setting output voltage (R1) (RP510L001J/1N/4J/4N) must be taken from the connection with the output capacitor, and also the wiring should be separated from the wiring between the output capacitor and Load.
- Overcurrent protection circuit and latch / foldback type protection circuit may be affected by self-heating or power dissipation environment.
- When not using the soft-start time adjustment, always make TSS pin open.
- When not using the power good function, PG pin should be Open or connected to GND.

TYPICAL CHARACTERISTICS

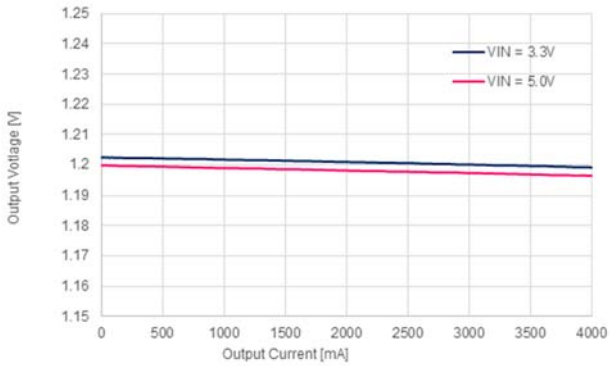
Typical Characteristics are intended to be used as reference data, they are not guaranteed.

1) Output Voltage vs. Output Current

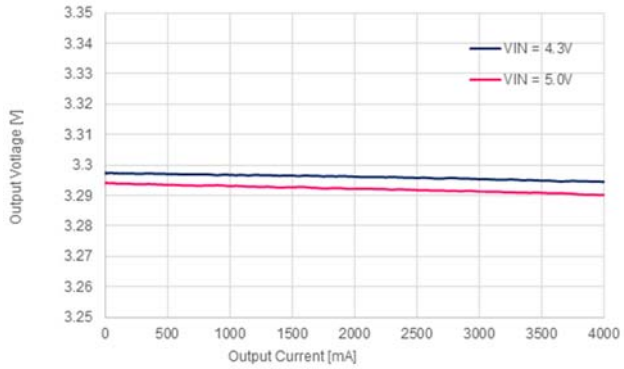
V_{OUT} = 0.8 V



V_{OUT} = 1.2 V

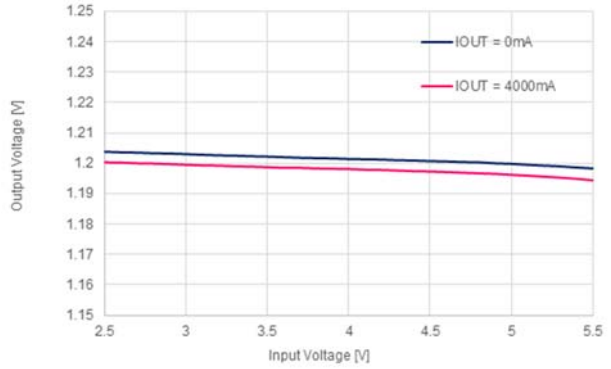


V_{OUT} = 3.3 V



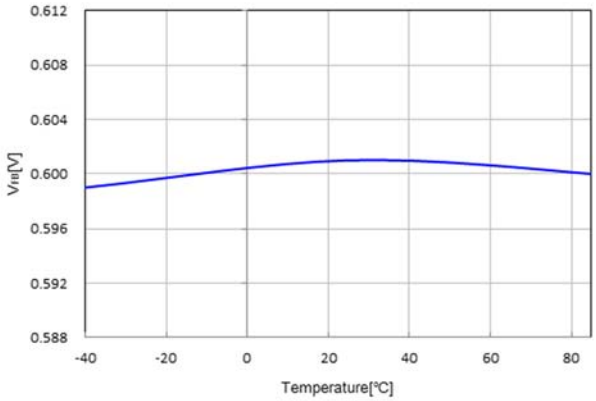
2) Output Voltage vs. Input Voltage

V_{OUT} = 1.2 V



3) Feedback Voltage vs. Temperature

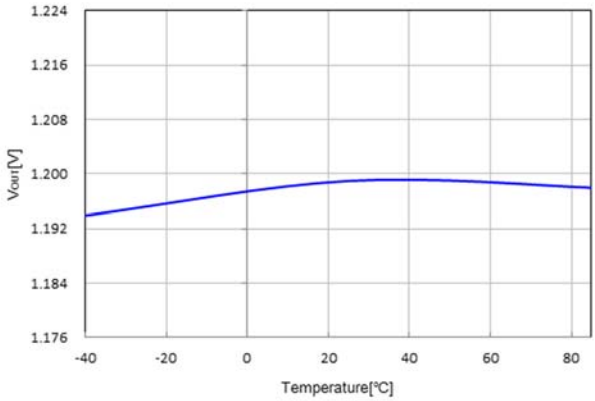
RP510L001J/1N/4J/4N/



4) Output Voltage vs. Temperature

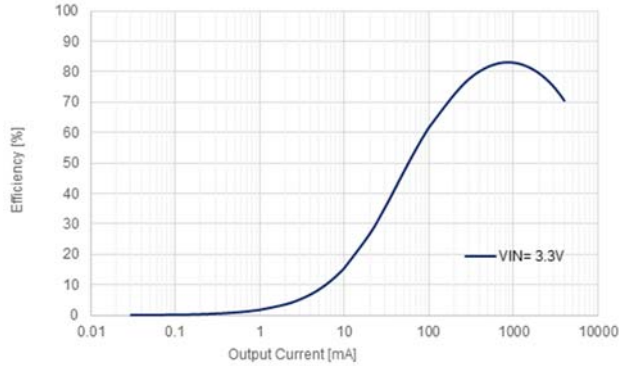
RP510Lxx1G/1H/4G/4H

V_{OUT} = 1.2 V

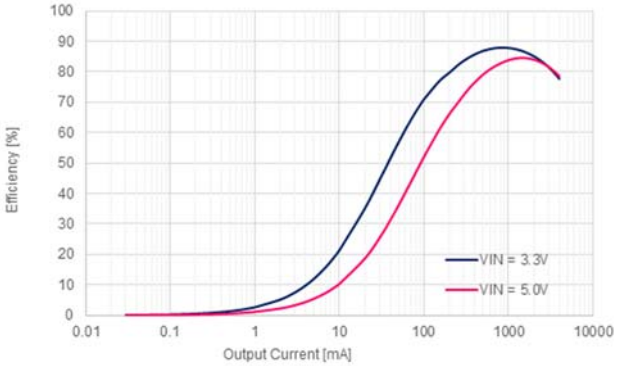


5) Efficiency vs. Output Current

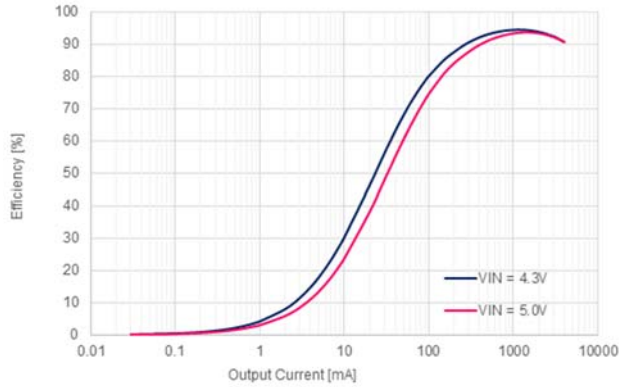
V_{OUT} = 0.8 V



V_{OUT} = 1.2 V

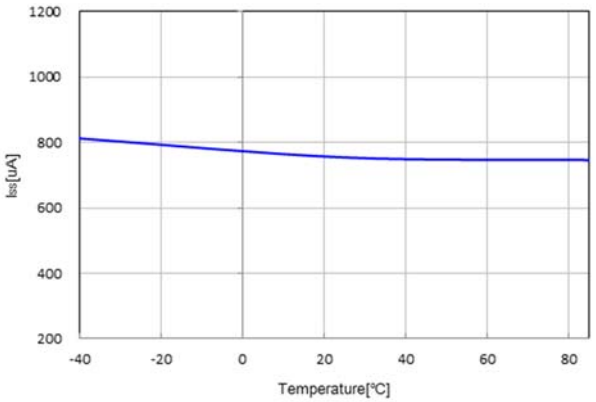


V_{OUT} = 3.3 V

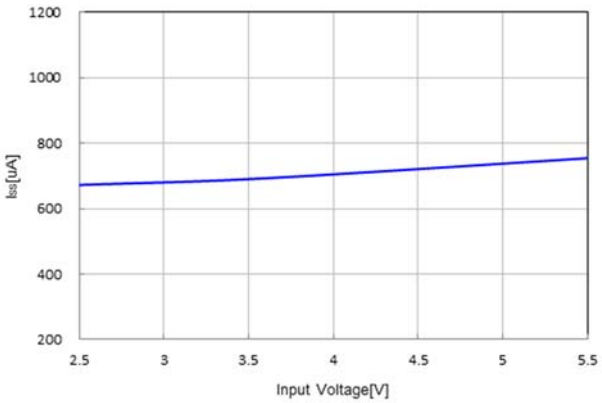


6) Current Consumption vs. Temperature

V_{IN} = 5.5 V

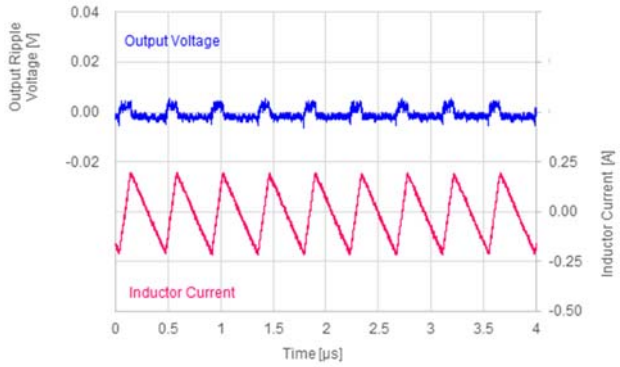


7) Current Consumption vs. Input Voltage

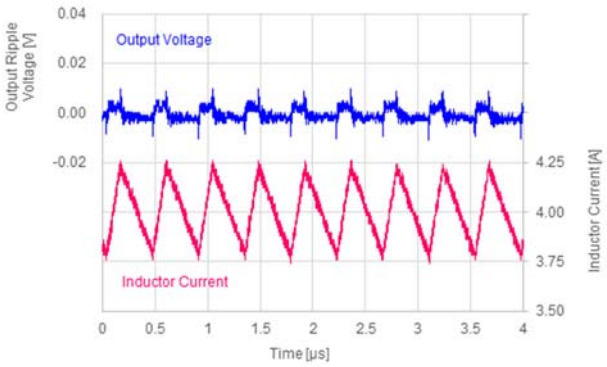


8) Output Voltage Waveform

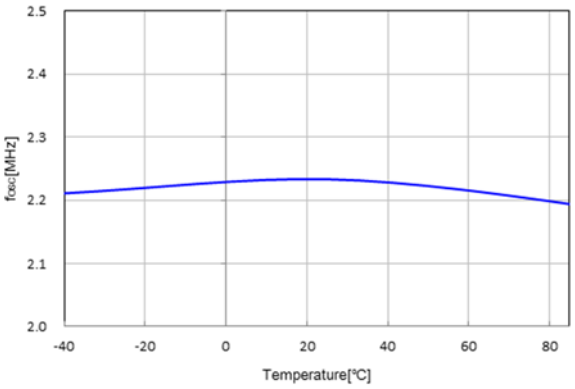
V_{OUT} = 1.2 V, I_{OUT} = 0mA



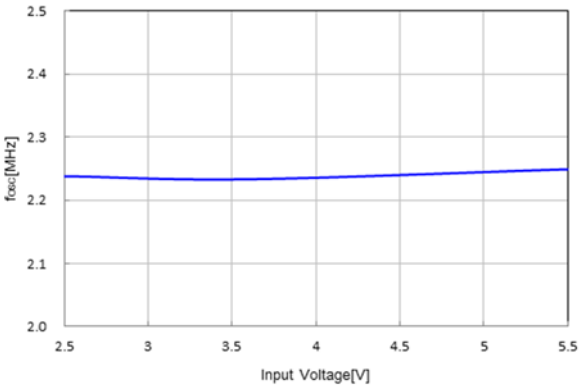
V_{OUT} = 1.2 V, I_{OUT} = 4000mA



9) Oscillation Frequency vs. Temperature

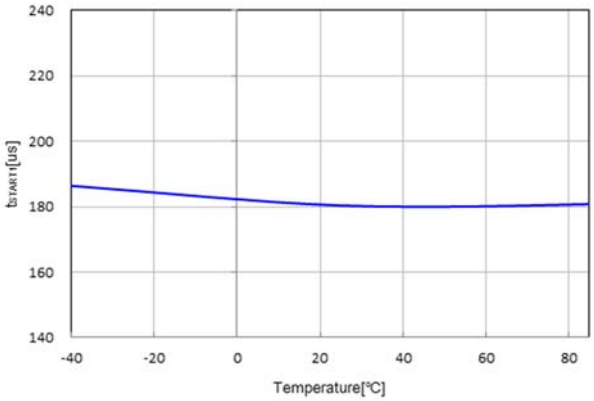


10) Oscillation Frequency vs. Input Voltage

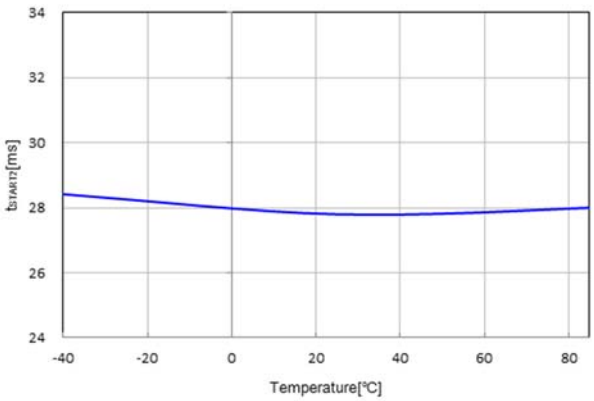


11) Soft-start time vs. Temperature

C_{SS} = open

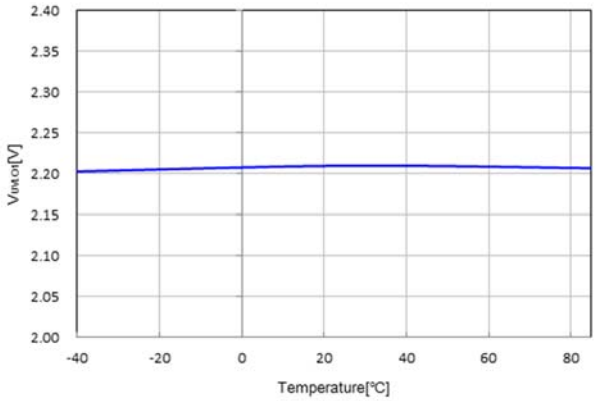


C_{SS} = 0.1µF

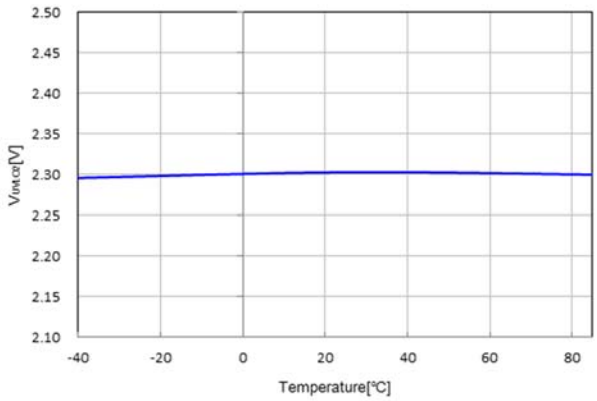


12) UVLO vs. Temperature

UVLO detection voltage

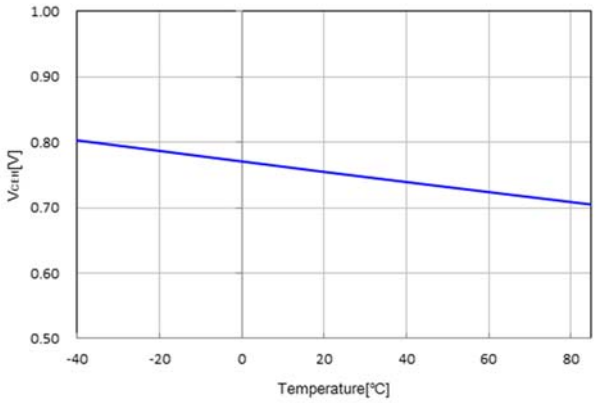


UVLO release voltage

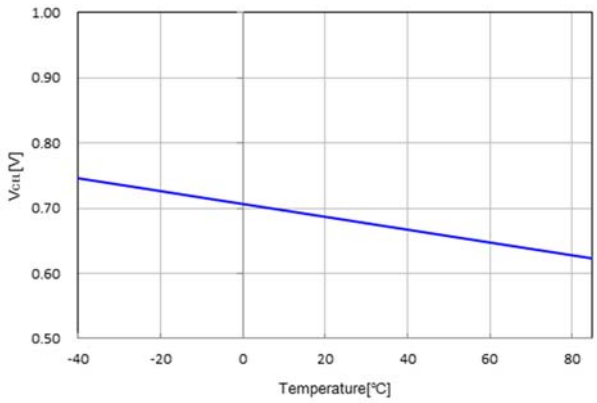


13) CE Input Voltage vs. Temperature

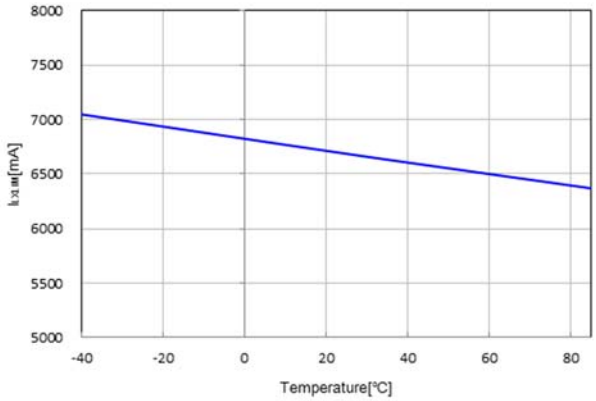
CE "H" input voltage
V_{IN} = 5.5 V



CE "L" input voltage
V_{IN} = 2.5 V

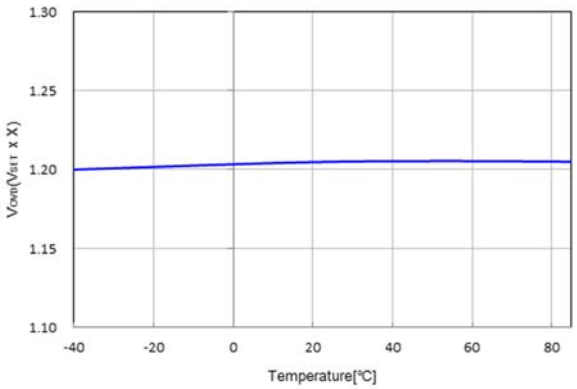


14) LX Limit Current vs. Temperature

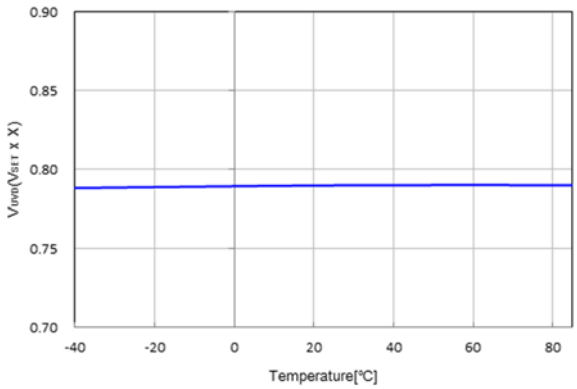


15) PG Detection Voltage vs. Temperature

Over Voltage Detection

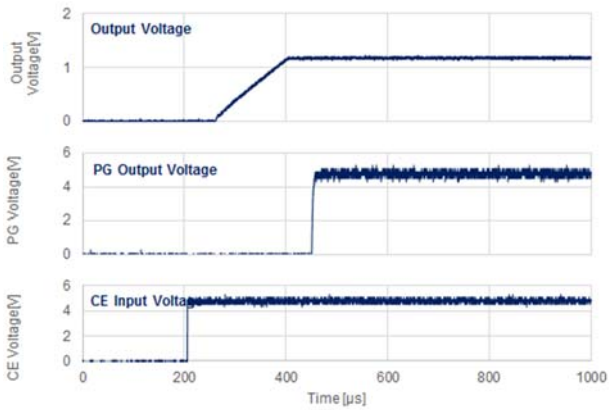


Under Voltage Detection

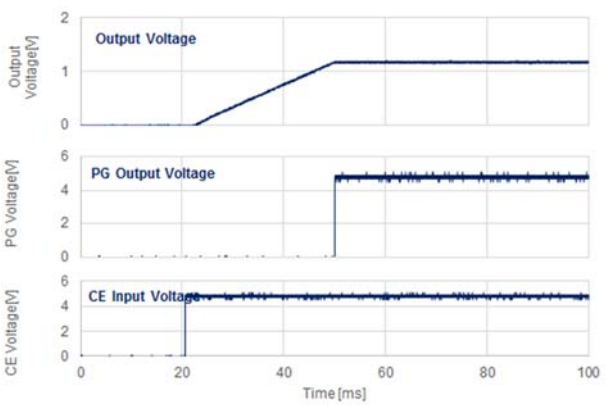


16) Soft-start Waveform

V_{OUT} = 1.2 V, C_{SS} = open



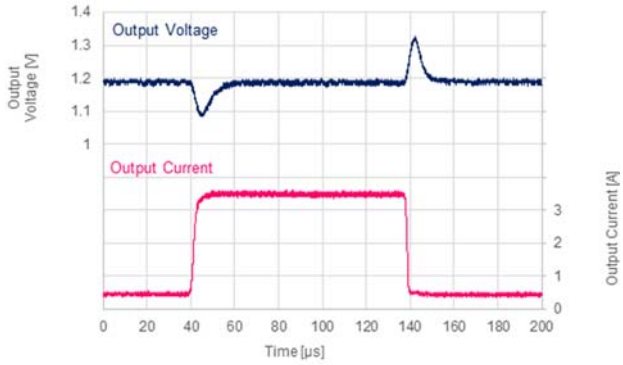
V_{OUT} = 1.2 V, C_{SS} = 0.1µF



17) Load Transient Response

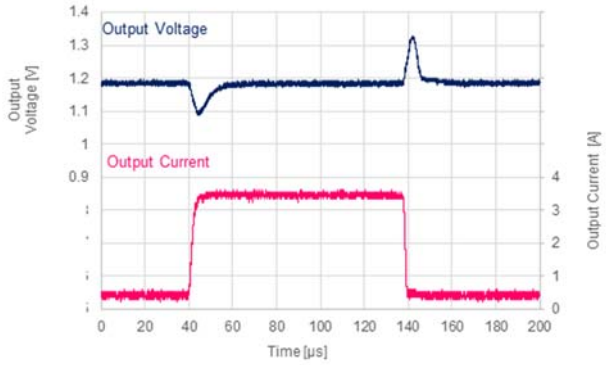
V_{IN} = 3.3 V, V_{OUT} = 1.2 V

I_{OUT} = 0.5 A ↔ 3.5 A



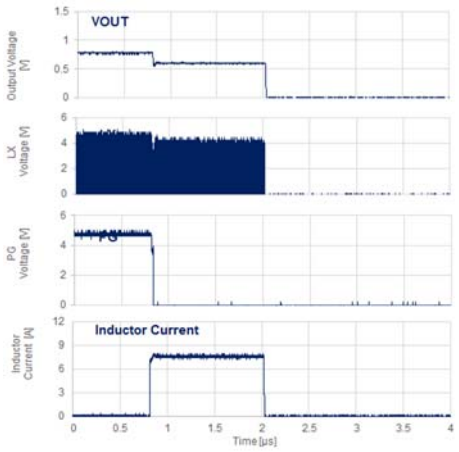
V_{IN} = 5.0 V, V_{OUT} = 1.2 V

I_{OUT} = 0.5 A ↔ 3.5 A

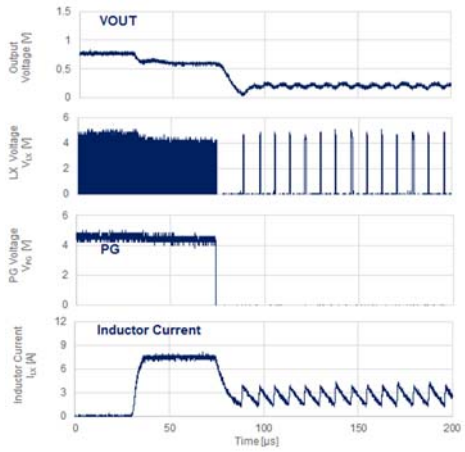


18) Output Short-circuit Waveform

RP510Lxx1G/1H/1J/1N (Latch Type)
V_{IN} = 5.0 V, V_{OUT} = 0.8 V

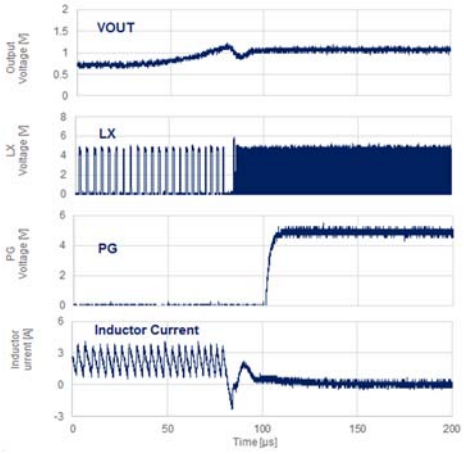


RP510Lxx4G/4H/4J/4N (Foldback Type)
V_{IN} = 5.0 V, V_{OUT} = 0.8 V



19) Output Short-circuit Release Waveform

RP510Lxx4G/4H/4J/4N (Foldback Type)
V_{IN} = 5.0 V, V_{OUT} = 0.8 V



Ver. A

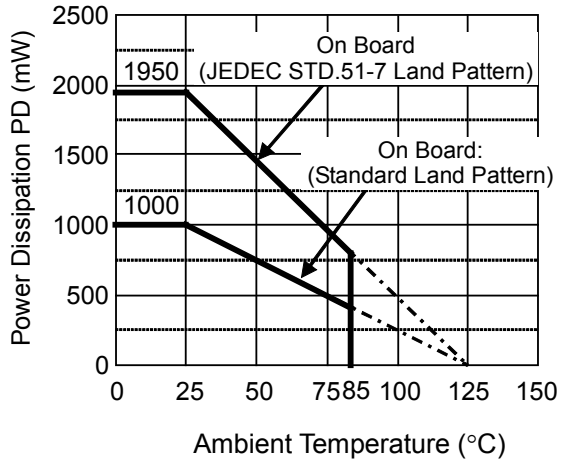
The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

Measurement Conditions

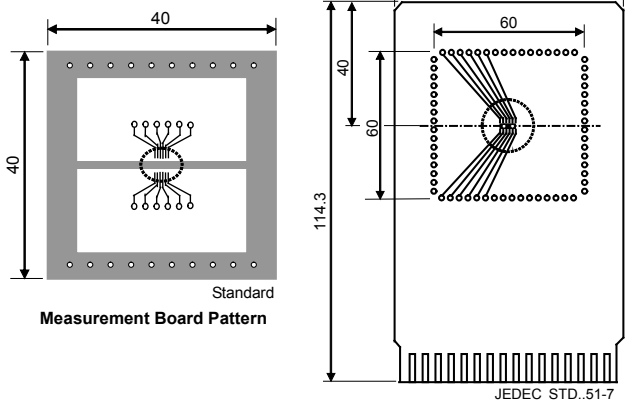
	Standard Test Land Pattern	JEDEC STD.51-7 Test Land Pattern
Environment	Mounting on Board (Wind Velocity=0m/s)	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass cloth epoxy plastic (Double sided)	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	40mm x 40mm x 1.6mm	76.2 mm × 114.3 mm × 1.6 mm
Copper Ratio	Top side: Approx. 50%, Back side: Approx. 50%	Outer Layers (First and Fourth Layers): Less than 10% of 60 mm Square Inner Layers (Second and Third Layers): 100% of 74.2 mm Square
Through-holes	ϕ 0.54mm x 32pcs	ϕ 0.85 mm × 64 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

	Standard Test Land Pattern	JEDEC STD.51-7 Test Land Pattern
Power Dissipation	1000mW	1950mW
Thermal Resistance	θja = (125 − 25°C) / 1.00 W = 100°C/W θjc = 18°C/W	θja = (125 − 25°C) / 1.95 W = 51.2°C/W θjc = 5.9°C/W



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

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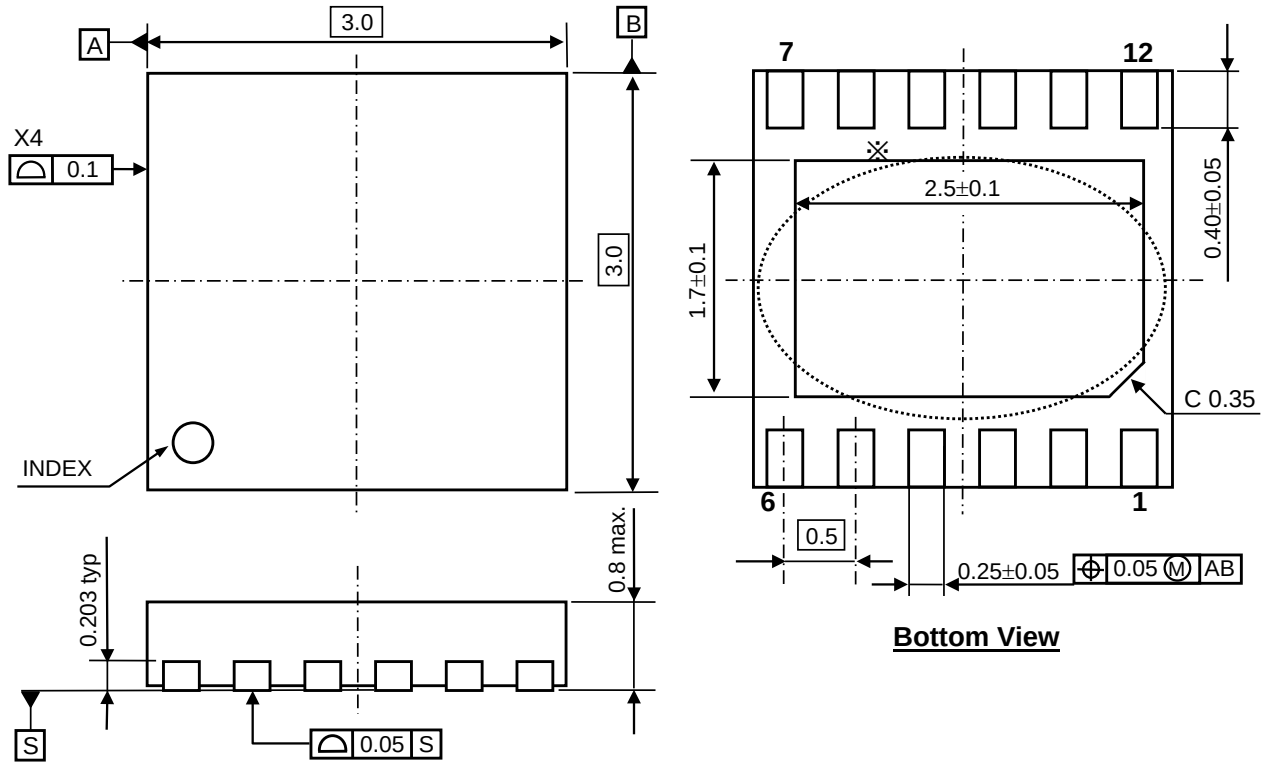
Ver. A



DFN3030-12 Package Dimensions (Unit: mm)

∗ The tab on the bottom of the package is substrate level (GND). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

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