RECOM

Whitepaper

Designing Robust Transistor Circuits with IGBTs and SIC MOSFETs

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Designing Robust Transistor Circuits with IGBTs and SIC MOSFETs

When evaluating new switching transistors circuits, often only the specifications of the transistor itself are considered. However, a very significant contributor in the robustness of final design is the driver circuit.

To explore the effect of the driver parameters, let us first consider ideal conditions using the following example of an IGBT transistor (IKW20N60H3)

From the datasheet, at 25°C:

Vge max = ± 20V

Gate emitter voltage threshold = 4.1V – 5.7V

With these values, a gate driver supply of +15V and GND would seem to be sufficient and the driver circuit would look something like this:

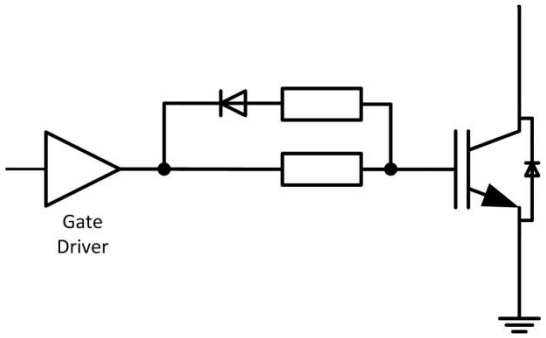


Figure 1: Simple gate drive circuit for an ideal IGBT

Looks pretty simple! However, when the parasitic elements are taken into account, the real-life model is more complex:

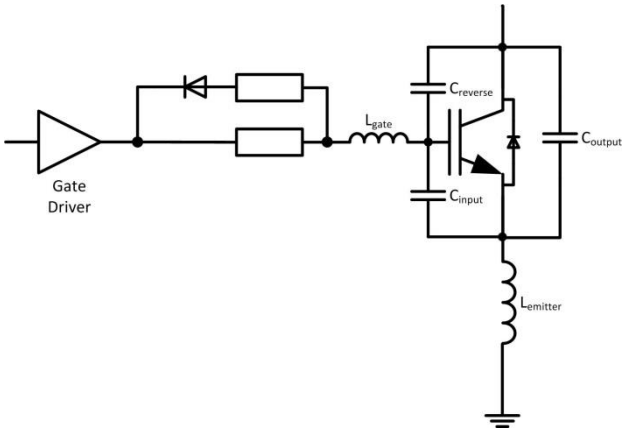


Figure 2: Realistic gate driver circuit including IGBT parasitic components

If we now take into account that the gate emitter threshold also varies over temperature range, it can be readily seen that the threshold voltage decreases with increasing temperature significantly (several mV / °K) and in the worst case is significantly lower than the typical minimum value of 4.1 V as measured at 25°C.

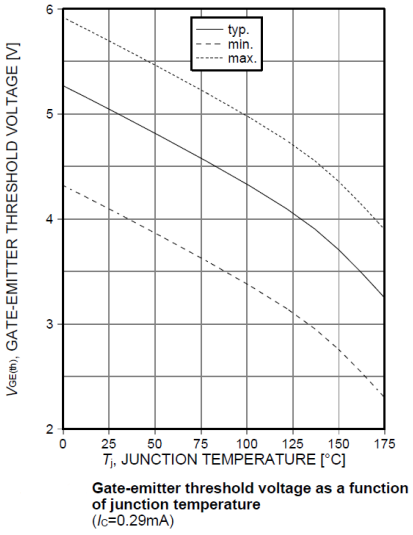


Figure 3: Gate-Emitter threshold voltage variation with temperature

The driver circuit must be designed to prevent unwanted turn-on in all operating conditions. Otherwise, this can lead to shoot-through short circuits, which can manifest itself in increased losses, increased component stress, shorter service life, worse EMC and in extreme cases, to the destruction of the transistor.

Essentially we have 2 kinds of unwanted switch-on timing:

- An unwanted turn-on due to the effect of the Miller capacitance ($C_{reverse}$).
- An unwanted turn-on due to the effect of the parasitic inductances (L_{gate} and $L_{emitter}$).

1. An unwanted turn-on due to the effect of the Miller capacitance:

As the Collector Emitter voltage rises, either when the low-side IGBT is turned off or in a bridge circuit, the high-side IGBT is turned on and current flows through the anti-parallel diode, the Miller capacitance, $C_{reverse}$, must be charged up.

The Miller capacitance charging current can be calculated as follows:

$$I_{C_{reverse}} = C_{reverse}.{}^{\partial V_{CE}}/_{\partial t}$$

The Miller capacitance is given in most transistor datasheets, but this is, however, just a rough value. The value of $C_{reverse}$ is strongly voltage dependent and also varies with temperature and current.

Most data sheets only define the Miller capacitance under certain ideal conditions, so measuring the value under real operating conditions is strongly recommended. The following graph shows the effect of V_{CE} on the reverse capacitance:

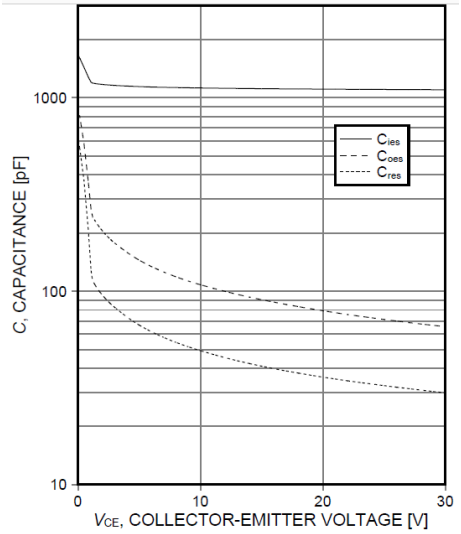
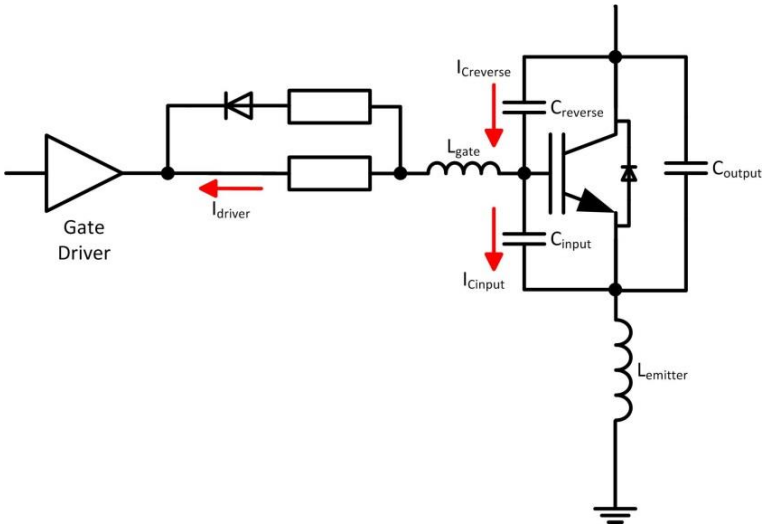


Figure 18. **Typical capacitance as a function of collector-emitter voltage** (V_{GE}=0V, f=1MHz)

Figure 4: Variation of $C_{reverse}$ with V_{CE} in an IGBT (IKW20N60H3)

The additional capacitive load of $C_{reverse}$ will not be a problem for most driver circuits; it only becomes an issue when the input capacitance C_{input} also becomes sufficiently charged by the current flowing through $C_{reverse}$ that the transistor turns on again.

The charging current of C_{input} can be defined from the following relationship: $I_{C_{input}} = I_{C_{reverse}} - I_{driver}$



I_{Driver} is dependent on the DC gate resistance and the AC resistance of L_{GATE}.

L_{gate} mainly depends on the package style (THT or SMD module) and the PCB layout.

Figure 5: Current flow during increasing V_{CE} Conditions

So what measures can be taken to avoid undesired turn-on due to the Miller capacitance current?

a) Limit the dV/dt. By slowing the rate of change of the VCE voltage, the $C_{reverse}$ current is reduced. However, this means higher switching losses.

b) Reduce the parasitic inductance LGATE. By suitable choice of layout and package, the $C_{reverse}$ current can be diverted away from charging up the gate-emitter capacitance, C_{input}. However, this restricts the design freedom of the PCB layouter.

c) Use a negative gate emitter voltage. If the driver output goes negative, the gate is held hard off and the safety distance between the gate turn-on threshold voltage and actual gate voltage is increased. Thus an unwanted turn-on is impossible even under worst case dv/dt conditions.

2. Unwanted turn-on caused by parasitic inductances:

In the ON state, current flows through the transistor and also through the emitter-side inductance of the load current. If the current is now turned abruptly off, a negative voltage is generated by emitter-side load inductance voltage according to the following relationship:

$$-V = L_{emitter} \cdot {}^{\partial I}/_{\partial t}$$

The voltage at the emitter is thus lower than the GND voltage.

If the gate driver output is at the same GND potential, this results in a positive gate - emitter voltage. If this voltage exceeds the threshold voltage, the transistor will then momentarily switch on again.

In bridge arrangements, the inductances of the other bridge branches and the PCB layout can add to the effective emitter-side load inductance.

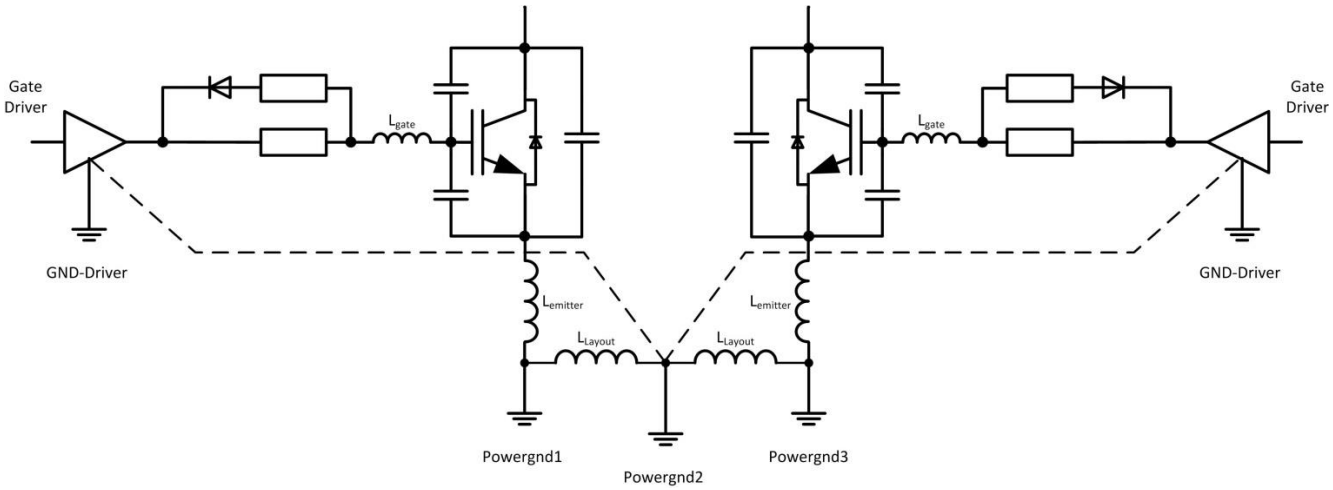


Figure 6: Low-side transistors in a bridge circuit showing effective power ground inductances

Non-isolated gate driver circuits in bridge arrangements can often exhibit significant potential differences between of the various connection points of Powergnd and the gate driver grounds, thereby leading to a significant impact on potentially unwanted turn-on effects due to the parasitic inductances.
In order to reduce the ground potential differences, it is necessary to connect the system ground to point Powergnd2 and also to use a star-earth connection to driver ground connections, GND-Driver. Furthermore, the inductance L_{Layout} must be nearly the same on both sides of the bridge.

Often the layout does not allow for absolute symmetry. If the system Powergnd is now connected to the point Powergnd1 instead of Powergnd2, then the right-hand branch to Powergnd3 will exhibit an increased gate-emitter voltage equal to:

$$-V = L_{emitter} \cdot L_{Layout} \cdot L_{Layout} \cdot {}^{\partial I}/_{\partial t}$$

The same imbalance is true if the system Powergnd is connected closer to the point Powergnd3 for the left-hand branch, of course.

How to check whether your gate driver design is safely under the gate emitter threshold voltage during operational switching operations?

It is not so simple as just attaching an oscilloscope probe and monitoring the gate voltage as direct access to the gate and emitter is difficult in practice and the readings will be affected by the capacitance loading of the probe itself. Thus, the measured values do not necessarily reflect reality. (Who wrongly measures, measures wrongly). Rather, you need to measure the inductances $L_{emitter}$, L_{gate} and in some cases even L_{Layout} and do the necessary calculations.

One way to find out if there are momentary unwanted turn-on effects in a bridge design is to measure the current in each branch of the bridge. Again, one must be careful that you do not change the switching behavior of IGBTs by measuring the current. Thus, there must be no additional resistances or inductances in the gate-emitter path. One method which has been proven to be reasonably accurate is to use a current shunt in the high side collector connection and an isolated oscilloscope.

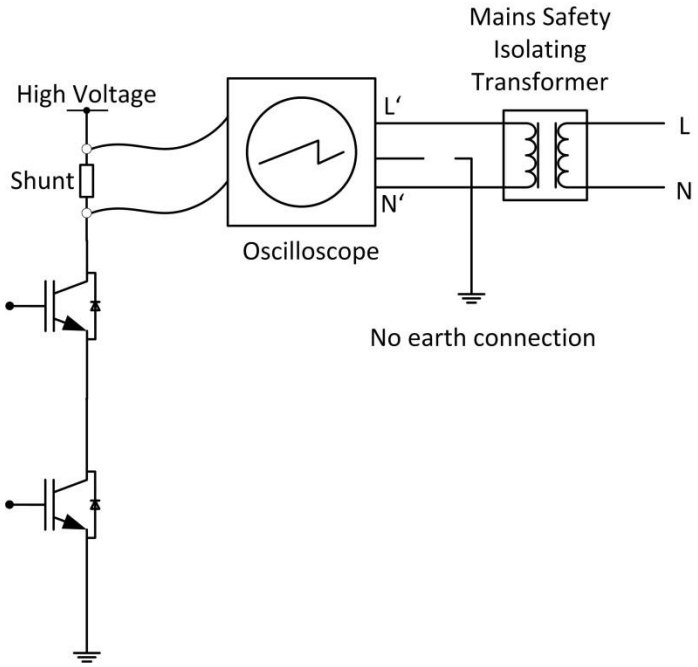


Figure 7: Measurement setup to check bridge current flow

Even if this measurement does not reveal any unwanted current peaks, you still cannot assume that the design is safe under all operating conditions. To be sure, you would have to have to select transistors having the minimum threshold voltages given in the datasheet and test at the maximum permissible temperature and maximum dI/dt and dv/dt levels.

So what can be done to minimize the unwanted effects of parasitic inductances?

a) Reduce dI/dt. Slower current decay rates result in lower voltages induced in the parasitic inductances and thus lower voltages between gate and emitter. However, this increases the switching losses.

b) Reduce the layout inductance. The lower the layout inductance (track or cable lengths), the smaller the parasitic voltage generated.

c) Use negative gate emitter voltages. By using a negative gate-emitter voltage instead of GND, the safety distance of the gate-emitter voltage to the gate emitter threshold voltage is increased.

d) Galvanically separate the gate drive from the power ground. Through the use of isolated gate drivers for each transistor, the influences of the layout inductance can be eliminated. For this purpose, the driver supply ground point is connected directly to the respective transistor emitters.

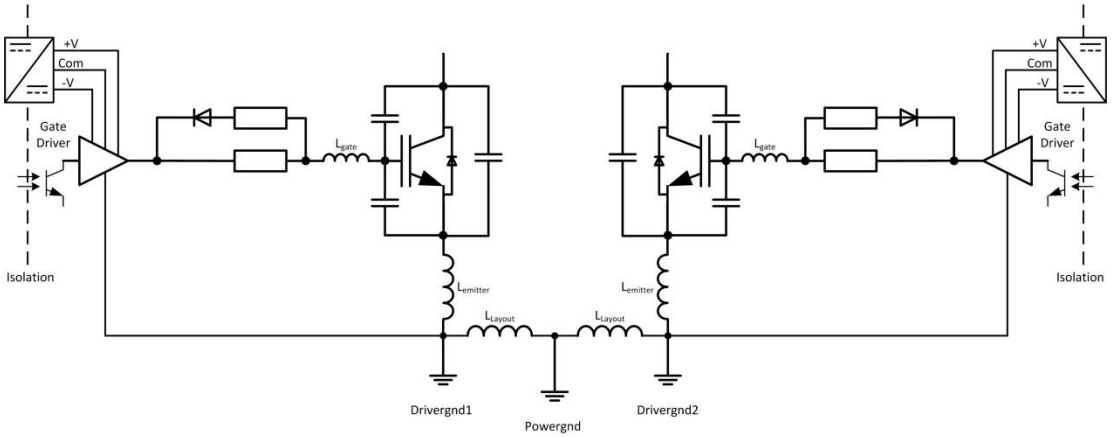


Figure 8: Galvanically isolated gate drivers

Now that L_{layout} is not part of the driver current loop, if the system Powergnd is now connected closer to Drivergnd 1 or Drivergnd2 it has less influence on the switching behaviour.

e) Use Kelvin contacts.

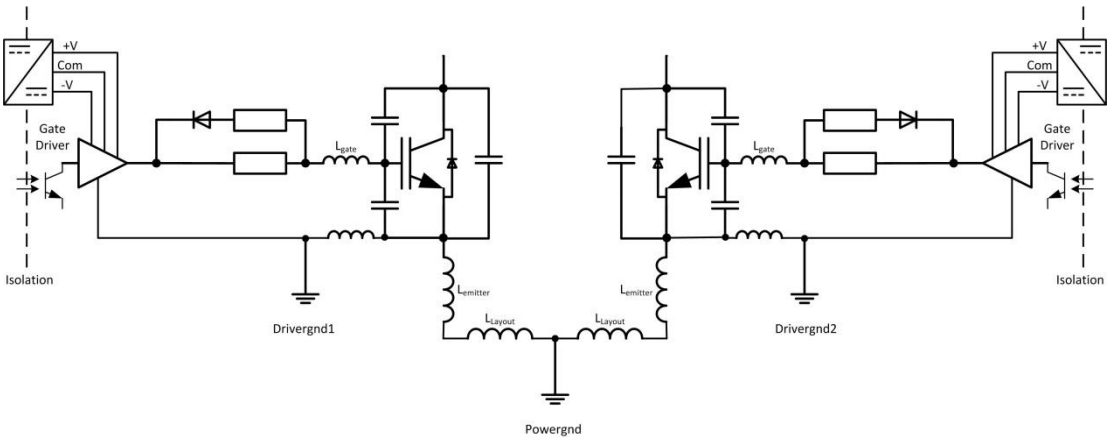


Figure 9: Galvanically isolated gate driver with Kelvin contacts

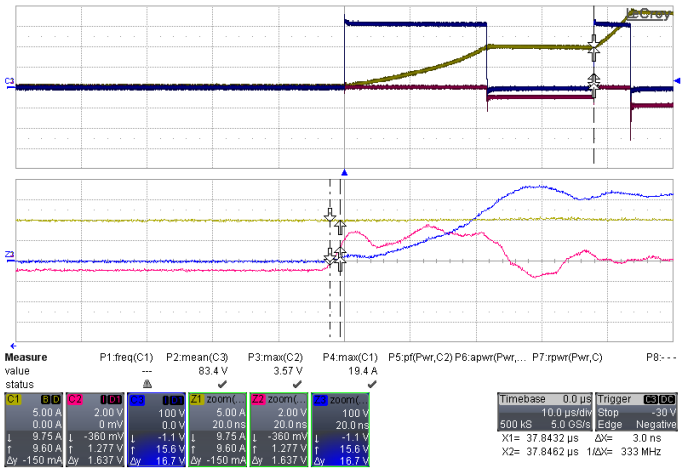
Several transistor manufacturers now offer packages in which a separate kelvin connection is provided for the emitter. Although this also has its own small parasitic inductance due to the connection path, the main load current does not flow through it, so no induced voltage is generated by any load current variations. This solution eliminates the effects of both the $L_{emitter}$ and L_{layout} parasitic inductances.

In summary: there are many ways to prevent undesired turn-on of an IGBT, but there are, however, just as many dangers that it happens! The safest way to prevent unwanted turn-on switching is to use an isolated dual supply for the gate driver with a negative turn-off voltage (+15V/-9 V has proven itself to be most appropriate), and to keep the parasitic inductances as low as possible. Ideally, one uses a package with Kelvin emitter connection.

Driver circuits for SiC MOSFETs:

Silicon Carbide, or SiC MOSFETs are increasingly finding new applications in power electronics. Bridge circuits for high-voltage applications (several hundred volts) were previously reserved for only the IGBT domain. MOSFETs based on silicon, especially Super Junction MOSFETs are not suitable for these applications due to the extremely poor parasitic body diode performance; when silicon MOSFETs experience an unwanted turn-on effect, the body diode quickly goes into thermal destruction. Often, even a single false switching operation on the conductive body diode either exceeds the maximum dI/dt of the body diode, and thus destroy the MOSFETs, or the switching operation incites the gate to oscillate, so that the maximum gate source voltage is exceeded and transistor is also destroyed (a more detailed explanation of why this phenomena occurs would require a separate article, but believe me, it happens!)

SiC MOSFETs have a far more robust body diode than Si MOSFETS. The maximum switching dI/dt of the body diode of super junction MOSFETs is around 60Aμs-1 for the latest generation of fast switching MOSFETs up to 900Aμs-1 for SJ MOSFETs with ultra-fast body diodes, but these values pale in comparison with SIC MOSFETs with up to 6000A s-1. Here are the means for detecting the switching speed close to the limits. During various tests on SIC MOSFETs from different manufacturers, the author has not been able to destroy the transistor by fast switching the body diode. The boost converter (Figure 10) is a DC/DC-converter without galvanic insulation.



Channel 1: inductor current,

Channel 2: transistor load current measured with a 100mOhm shunt resistor,

Channel 3: drain source voltage.

Figure 10: Double pulse test on a SIC body diode (SCT30N120 di/dT approximately 5500Aµs^{-1})

MOSFETs in general and SIC MOSFETs specifically have the advantage of lower switching losses compared to IGBTs. Especially when switching off, there is no typical IGBT "current tail" effect. Thus SIC MOSFETS are able to increase the efficiency in bridge applications through lower switching losses. Alternatively, the switching frequency can be increased without harming the efficiency and thus contribute to volume, weight and cost savings in the passive components, especially the inductors.

Basically, the same rules apply in the dimensioning of the gate driver as with the IGBT design. So can we simply re-purpose an existing IGBT driver for SIC MOSFETs? As a first analysis: yes. The higher switching speeds and lower switching losses will lead to a more efficient design, which also offers reduced power dissipation at partial load and you do not need to worry about the body diode.

However, the following section will explain why you might be better off with another driver, or at least one with a different drive voltage supply.

To make a general statement here is quite difficult because the technology is constantly developing and being used in different applications, but if we take an existing product as an example: a 1200V MOSFET with 80mOhm R_{DSon} such as the C2M0080120D or the SCT30N120. Both have roughly similar specifications:

Absolute maximum ratings, at 25°C:

VGS = -10 / + 25V

Gate source threshold voltage = 1.8V or 2V.

As you can see immediately, the threshold voltage is significantly lower than with the IGBT example, and again it decreases with increasing temperature.

A logical conclusion would be now that you take more negative bias at the gate in order to prevent unwanted turn-on effects. However, there are studies that show that the gate oxide layer suffers deterioration with high negative bias voltages: In April 2015, Alberto Castellazzi presented to the *SIC and GaN User Forum* results of investigations which were made at the University of Nottingham on this topic.

Over a period of 1000 hours, a selection of SIC MOSFETs were biased at 150°C and tested with -5V or -10V gate voltages and the drift in the threshold voltage recorded.

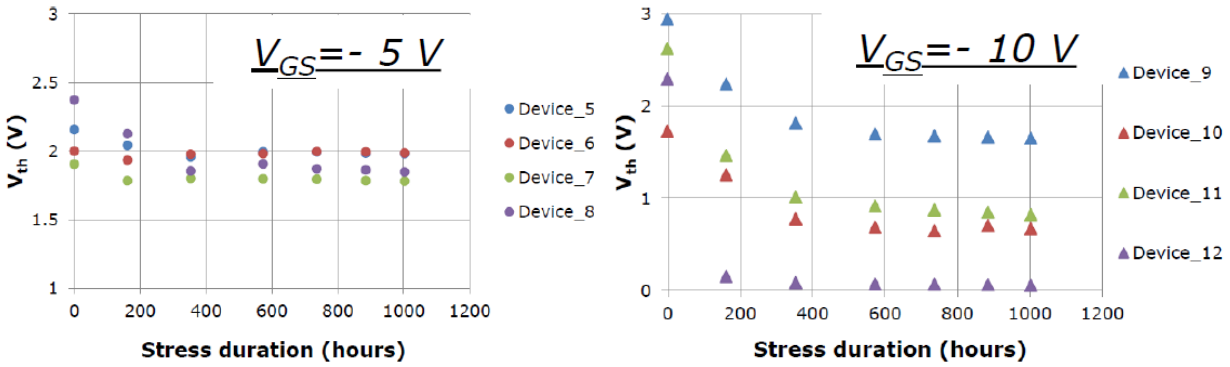


Figure 11: Change of the gate-source threshold voltage over time at negative gate voltages

When a negative gate voltage of -5V, the threshold voltage initially decreases slightly, then remains stable at around 1.8V after around 200 hours. At a voltage of -10V on the gate, the threshold voltage decreases significantly more and took twice as long to plateau out. In one example, (Device 12), the threshold voltage dropped from 2.2V down to 0V. The transistor thus became normally on and needed a negative voltage to switch off.

Based on these investigations, tt is therefore recommended not to switch the gate-source voltage hard off with a drive voltage more negative than -5 volts. The switch-on positive voltage could theoretically use the same +15V as with the IGBT design, since the threshold voltage is significantly lower and therefore the SiC MOSFET would be turned on safely.

However one looks at the output characteristic of the SiC MOSFET with different gate source voltages (Fig.12), you can clearly see that with a higher gate-source voltage, a considerably lower RDON is achieved.

Thus to fully exploit the transistor performance as much possible it is necessary that the gate-source voltage is closer to 20V. In this case, we recommend a gate driver supply voltage of +20V/-5V.

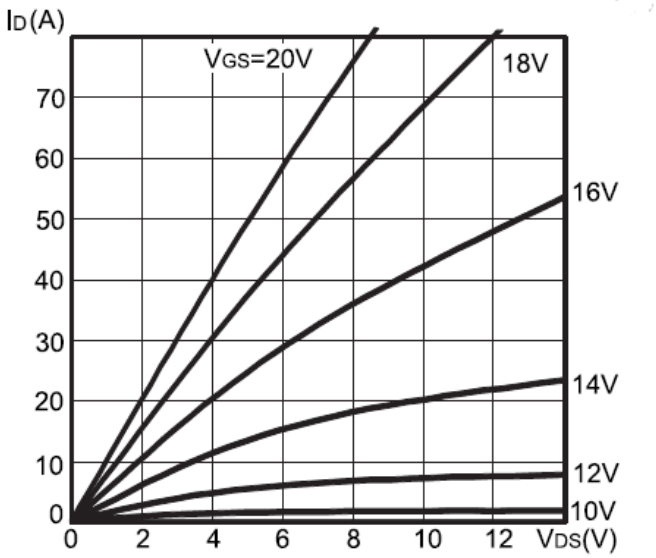


Figure 12: Output characteristic of a SiC MOSFET at 25°C