QPF0219

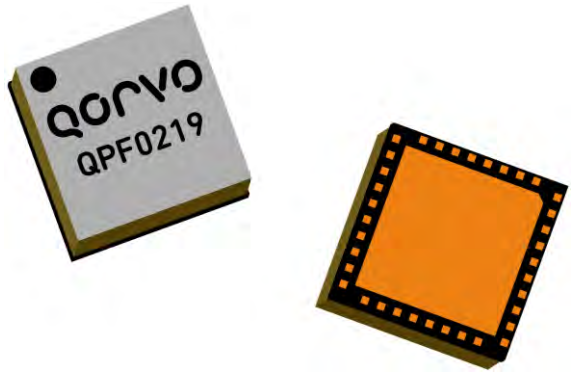
2 – 18 GHz 10 W T/R Module

Product Description

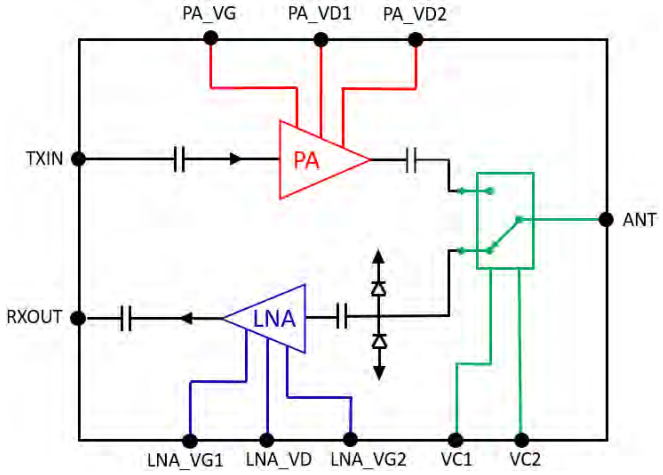
QPF0219 is a multi-chip Front-End Module (FEM) designed for 2-18 GHz Wide-Band radar applications. The FEM integrates a T/R switch, a limiter, a low-noise amplifier and a power amplifier. Transmit power is 10 W saturated with 20% PAE and large signal gain is 13 dB, small signal is 19dB. The receiver noise figure is 4 dB, small signal gain is 14 dB, P1dB is 21 dBm.

The multi-die FEM offers the optimal semiconductor technology for each functional block to maximize performance in challenging radar applications. Power amplifier and T/R switch are GaN-on-SiC while limiter and LNA are GaAs.

Package is a 8 x 8 mm air cavity QFN. QPF0219 offers exceptional performance in a compact footprint.



Functional Block Diagram



Product Features

- Frequency Range: 2 – 18 GHz
- RX Noise Figure: 4 dB
- RX Small Signal Gain: 14 dB
- RX P1dB: 21 dBm
- RX Output TOI: 30dBm (@ Pin = -14dBm / tone)
- TX Large Signal Gain: 13 dB
- TX Saturated Power: 40 dBm, CW or Pulsed
- TX PAE: 20% @ Pin = 27 dBm, CW or Pulsed
- Antenna Port Power Survivability: 40 dBm Pulsed
- Package Dimensions: 8 x 8 x 1.57 mm

Performance is typical at room temperature.
Please reference electrical specification table and data plots for more details.

Applications

- Electronic Warfare (EW)
- Communication Systems

Ordering Information

Part No.	Description
QPF0219	Shipping Tray, Qty 50
QPF0219TR7	Tape and Reel, 7 ", Qty 250
QPF0219EVB	Evaluation Board, Qty 1

Normal Operating Conditions

Parameter [1]	Value			Units
RX Drain Voltage (LNA_VD)		5		V
RX Drain Quiescent Current		100		mA
RX Gate Control (LNA_VG1) [2]	-1.0	-0.5	0	V
RX Gate Control (LNA_VG2)		1.3		V
TX Drain Voltage (PA_VD)		22		V
TX Drain Quiescent Current		1680		mA
TX Gate Voltage (PA_VG) [2]	-3.0	-2.5	0	V
Control Voltage Transmit (VC1 / VC2) [3]	-40 / 0		0	V
Control Voltage Receive (VC1 / VC2) [3]	0		-40	V
Operating Temperature Range	−40 °C		85 °C	°C

1. *Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.*
2. *Gate voltage varies due to process variations, can be adjusted to set required drain current.*
3. *Control voltage can use up to -20V, the power compression maybe compromised if low level is higher than -40 V.*

Absolute Maximum Ratings

Parameter	Min Value	Max Value	Units
PA Drain Voltage (PA_VD1, PA_VD2)	-	29.5	V
PA Drain Current (VD1 and VD2 Total)	-	2848	mA
PA Gate Voltage (PA_VG)	- 4	0	V
PA Gate Current	-	10	mA
LNA Drain Voltage (LNA_VD)	-	7	V
LNA Drain Current	-	144	mA
LNA Gate voltage (LNA_VG1)	- 2	0	V
LNA Gate voltage (LNA_VG2)	-3	LNA_VD	V
LNA Control Current (LNA_VG1, LNA_VG2 each)	-	10	mA
Switch Control Voltage (VC1, VC2)	0	-50	V
Switch Control Current	-	10	mA
Antenna Port Input Power (@ 85 °C, Pulse)	-	40	dBm
Antenna Port Input Power (@ 85 °C, CW)	-	33	dBm
TX Input Power (@ 85 °C, Pulse, Output VSWR 3:1)	-	32	dBm
TX Input Power (@ 85 °C, Pulse, Output 50 Ohm)	-	33	dBm
Storage Temperature	−55	150	°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Extended application of Absolute Maximum Rating conditions may reduce device reliability.

Electrical Specifications, Receive

Test conditions unless otherwise noted: LNA_VD = 5 V, _LNA_IDQ = 100 mA, VC1 = 0 V, VC2 = -40 V
Data de-embedded of fixture losses, 25 °C

Parameter	Min	Typical	Max	Units
Frequency	2		18	GHz
Small Signal Gain		14		dB
Noise Figure		4		dB
Input Return Loss		12		dB
Output Return Loss		14		dB
Saturated Output Power, CW		24		dBm
Output P1dB, CW		21		dBm
Output TOI @ Pin =-14 dBm / Tone		30		dBm
Switching Time (using module internal switch) [1]		60		nS
Gain Temperature Coefficient		−0.048		dB/°C

1. From 50% trigger signal to 90 % of RF rising edge or 10 % of RF falling edge.

Electrical Specifications, Transmit

Test conditions unless otherwise noted: PA_VD = 22 V, PA_IDQ = 1680 mA, VC1 = -40 V, VC2 = 0 V
Data de-embedded of fixture losses, 25 °C

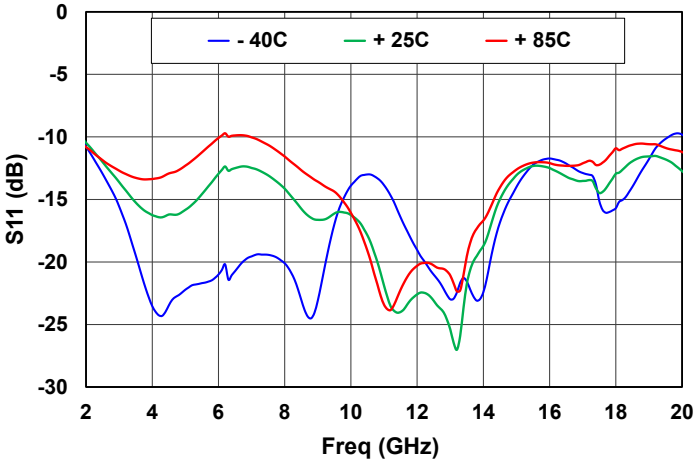
Parameter	Min	Typical	Max	Units
Frequency	2		18	GHz
Small Signal Gain		19		dB
Large Signal Gain @ Pin = 27 dBm [1]		13		dB
Input Return Loss		16		dB
Output Return Loss		5		dB
Output Power @ Pin = 27 dBm [1]		40		dBm
PAE (@ Pin = 27 dBm) [1]		20		%
Harmonic Suppression, 2nd, 2 to 15 GHz, Pin = 27 dBm		20		dBc
Harmonic Suppression, 2nd, 16 to 18 GHz, Pin = 27 dBm		40		dBc
Harmonic Suppression, 3rd, 2 to 9 GHz, Pin = 27 dBm		15		dBc
Harmonic Suppression, 3rd, 10 to 18 GHz, Pin = 27 dBm		35		dBc
Switching Time (using module internal switch) [2]		60		nS
Gate Leakage Current (VG leak, VD = 10 V, VG = -3.7 V)	- 8.4			mA
Gain Temperature Coefficient		−0.04		dB/°C

1. *Power and PAE shown are for CW mode, pulse mode showed similar data.*
2. *From 50% trigger signal to 90 % of RF rising edge or 10 % of RF falling edge.*

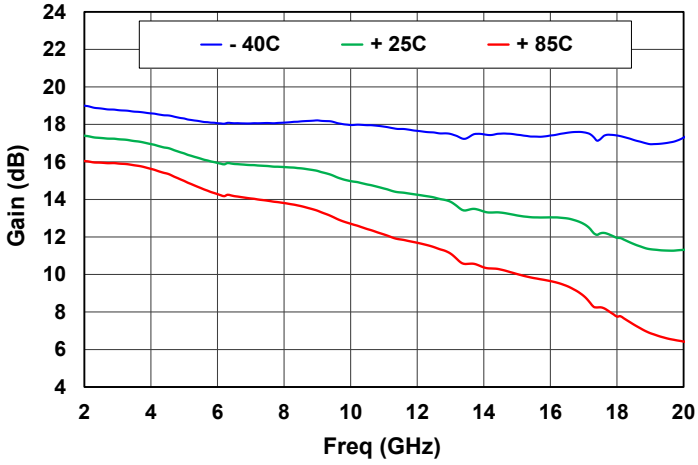
Small Signal Performance, Receive

Test Conditions unless otherwise stated: VDD = 5 V, LNA IDQ = 100 mA, 25 °C

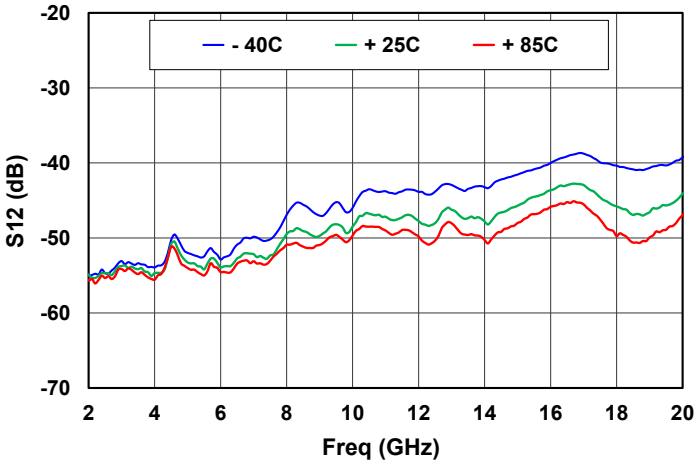
Input Return Loss vs Temp



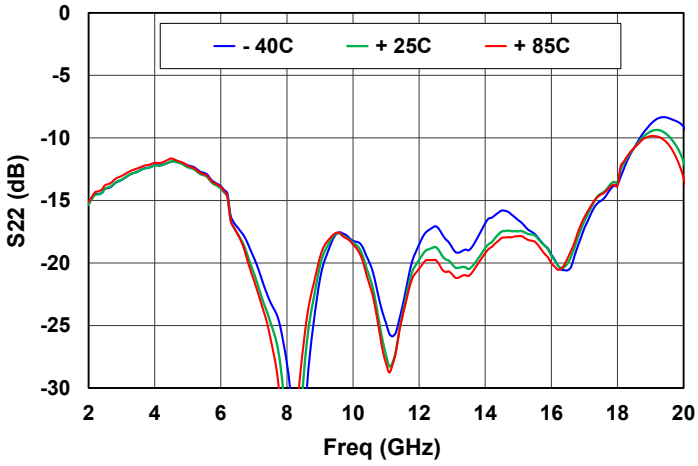
Gain vs Temp



Reverse Isolation vs Temp



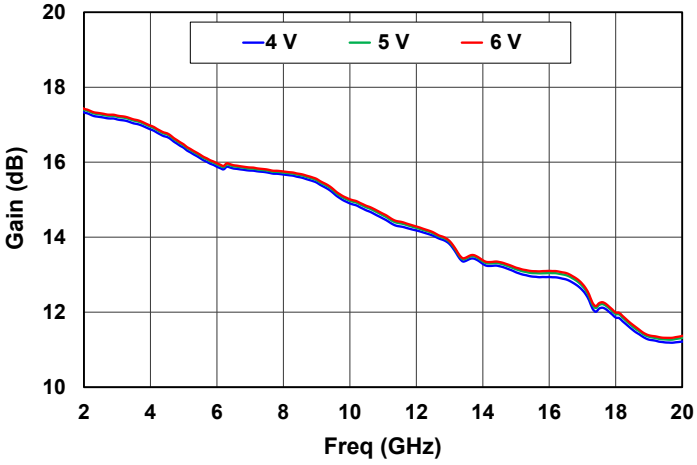
Output Return Loss vs Temp



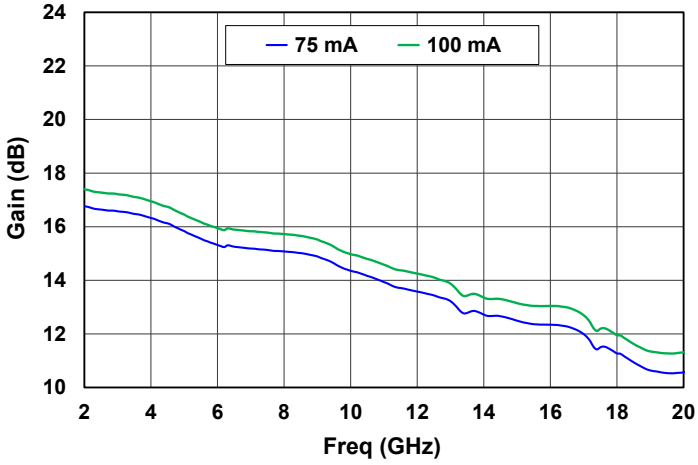
Small Signal Performance, Receive

Test Conditions unless otherwise stated: LNA_VD = 5 V, LNA IDQ = 100 mA, 25 °C

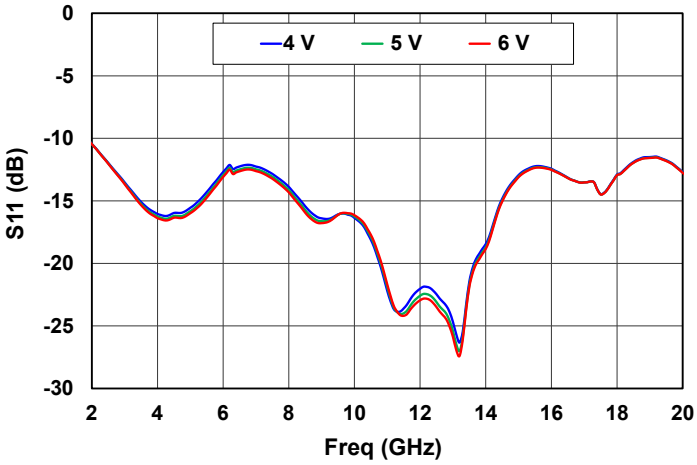
Gain vs Voltage



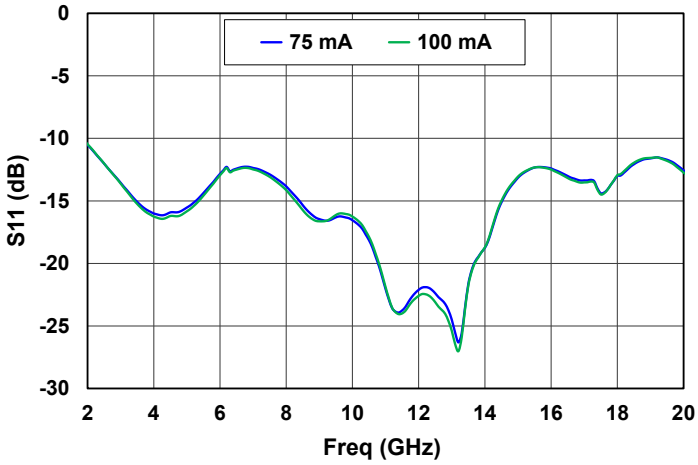
Gain vs Current



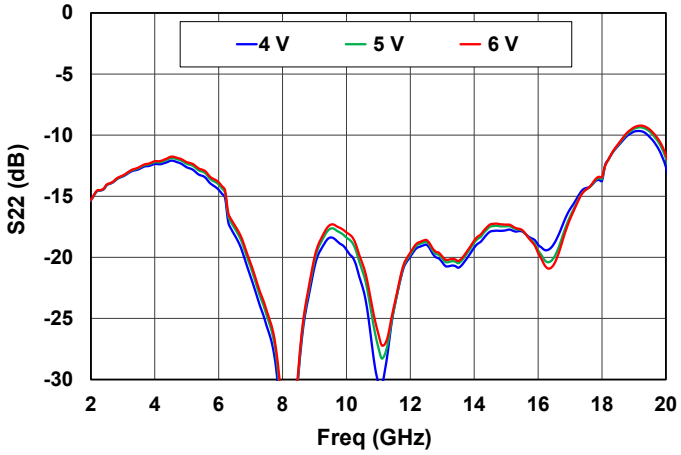
Input Return Loss vs Voltage



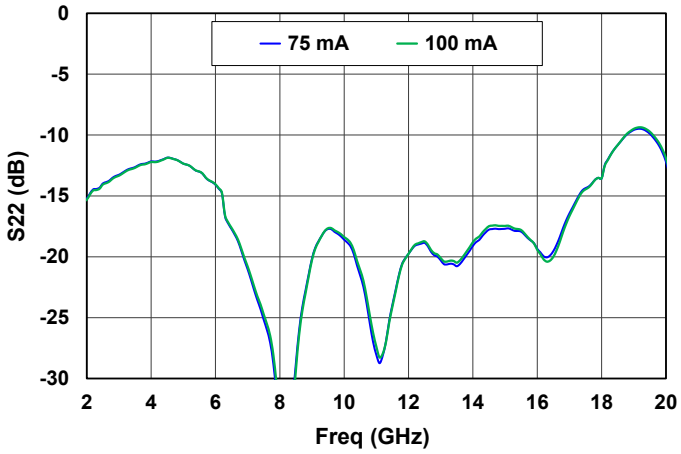
Input Return Loss vs Current



Output Return Loss vs Voltage

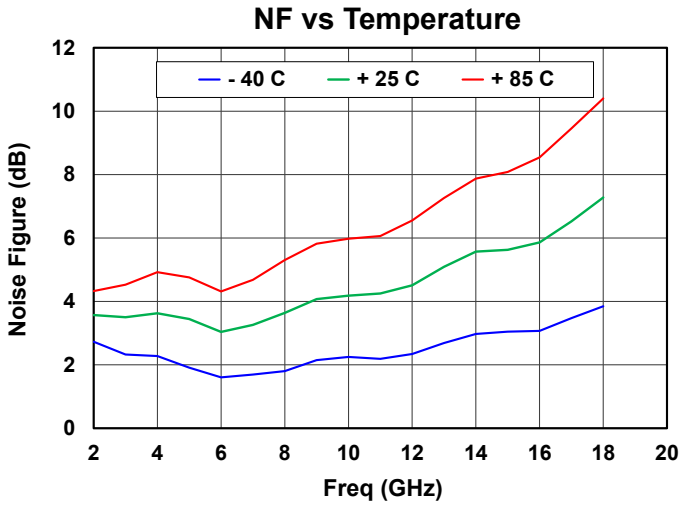


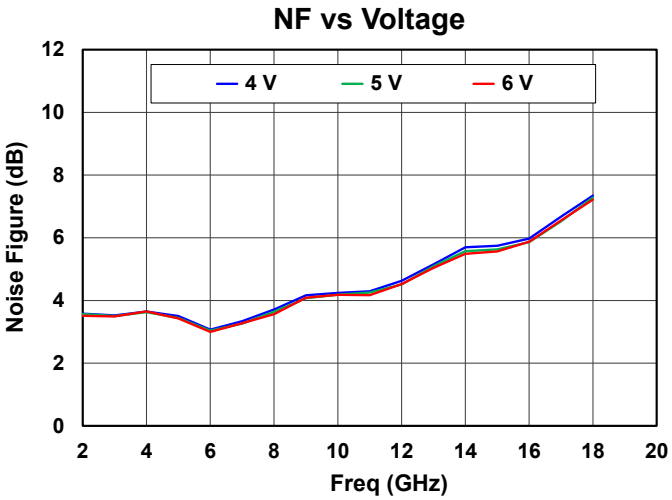
Output Return Loss vs Current

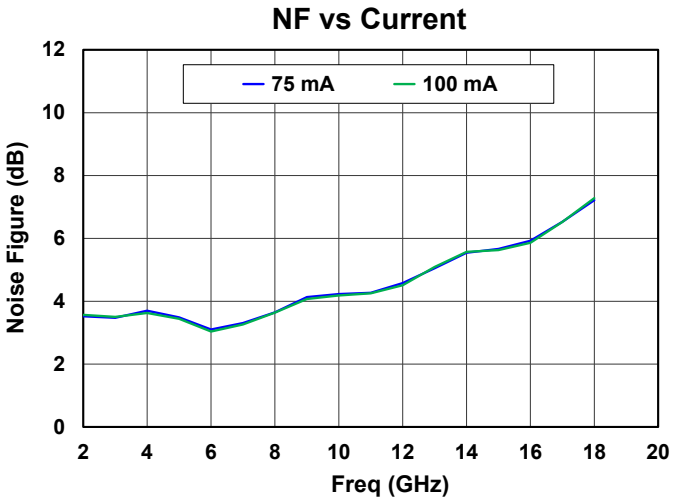


Noise Figure, Receive

Test Conditions unless otherwise stated: VDD = 5 V, LNA IDQ = 100 mA, 25 °C



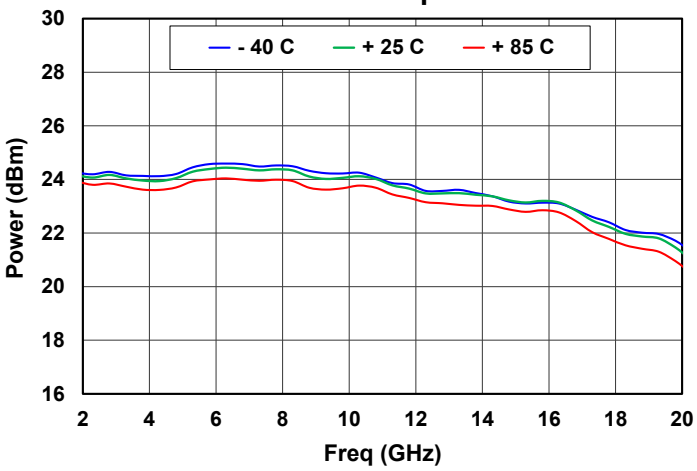




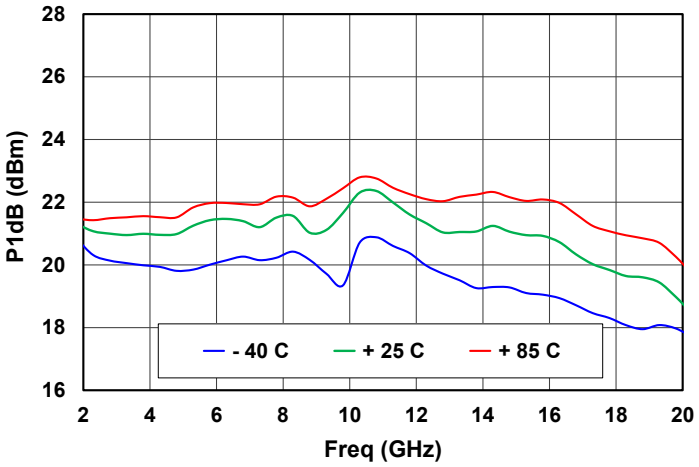
Power Performance, Receive

Test Conditions unless otherwise stated: VDD = 5 V, LNA IDQ = 100 mA, CW Mode, 25 °C

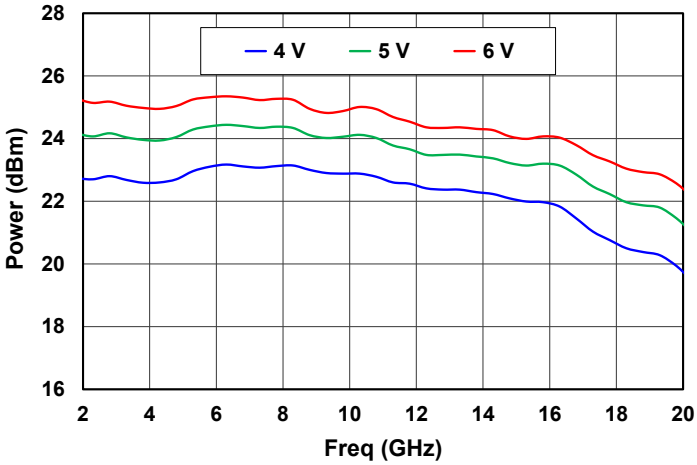
Power vs Temperature



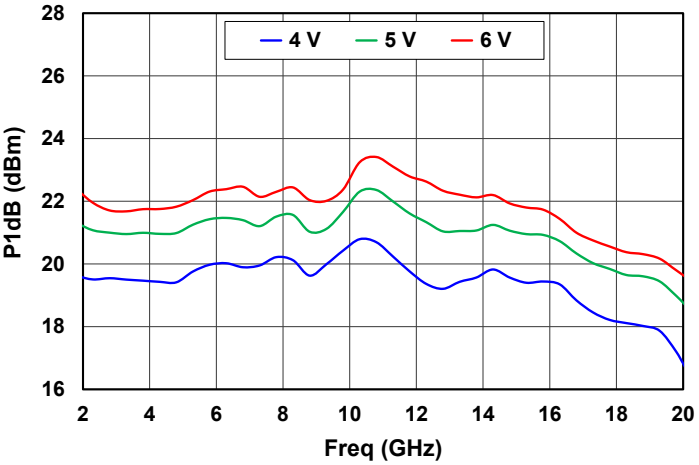
P1dB vs Temperature



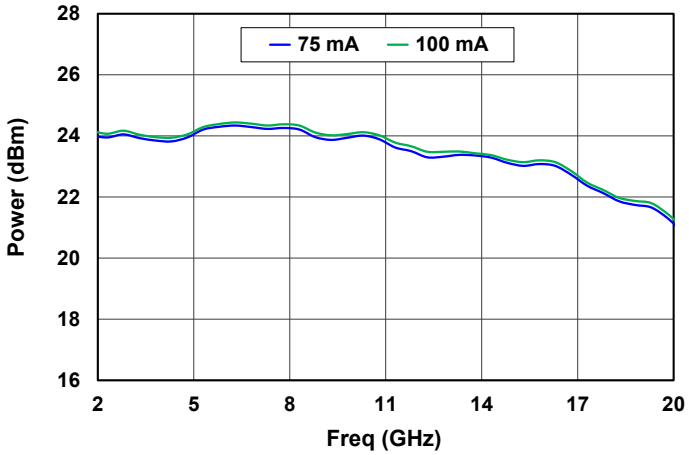
Power vs Voltage



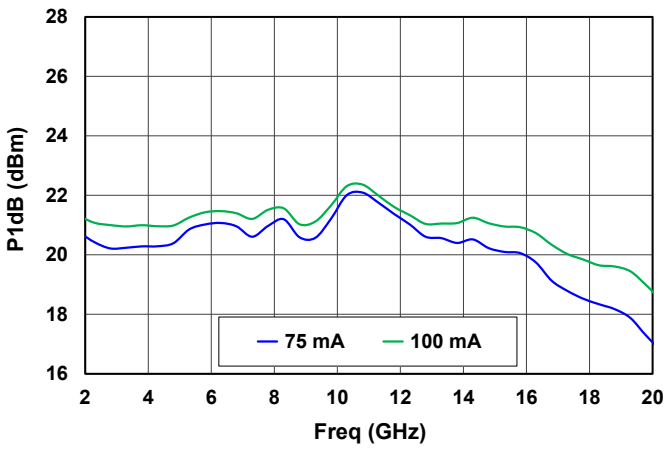
P1dB vs Voltage



Power vs Current

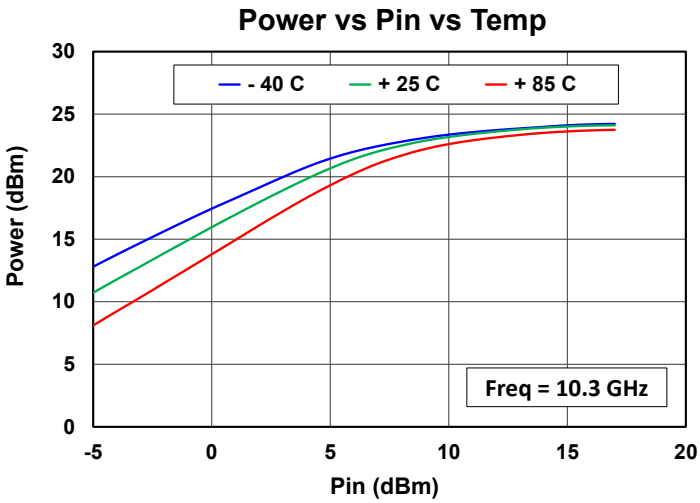


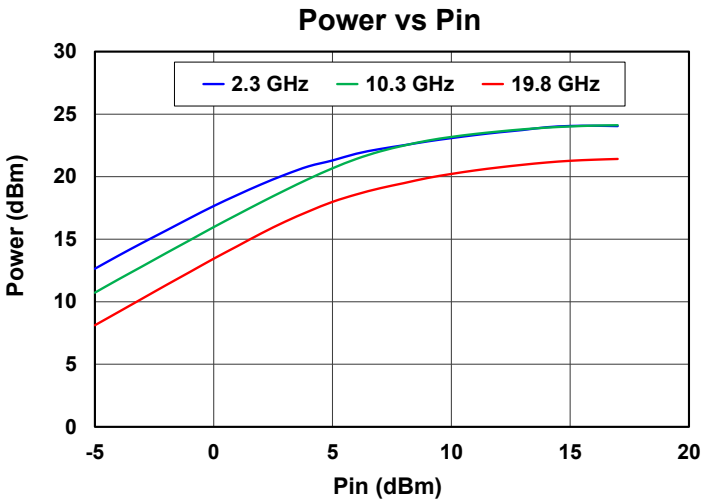
P1dB vs Current

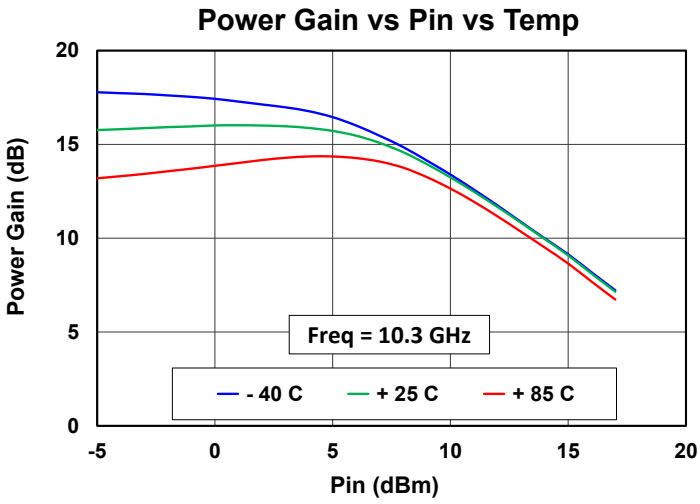


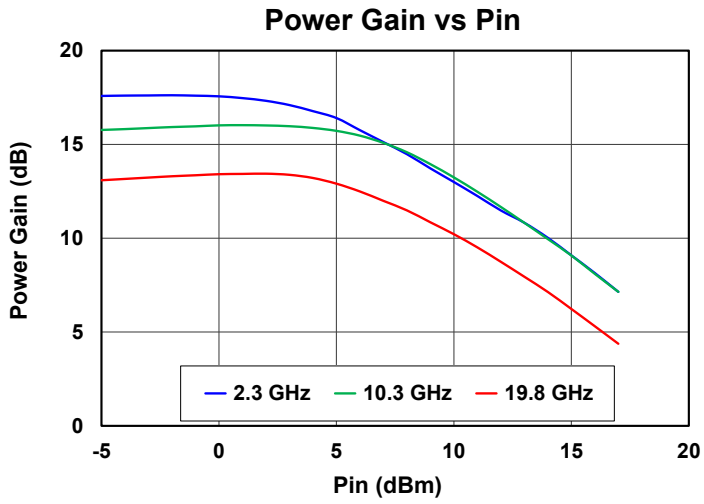
Power Sweep, Receive

Test Conditions unless otherwise stated: LNA_VD = 5 V, LNA IDQ = 100 mA, 25 °C



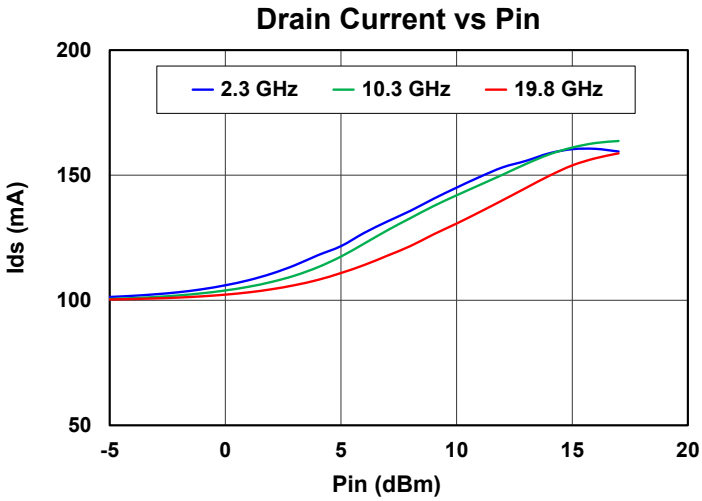


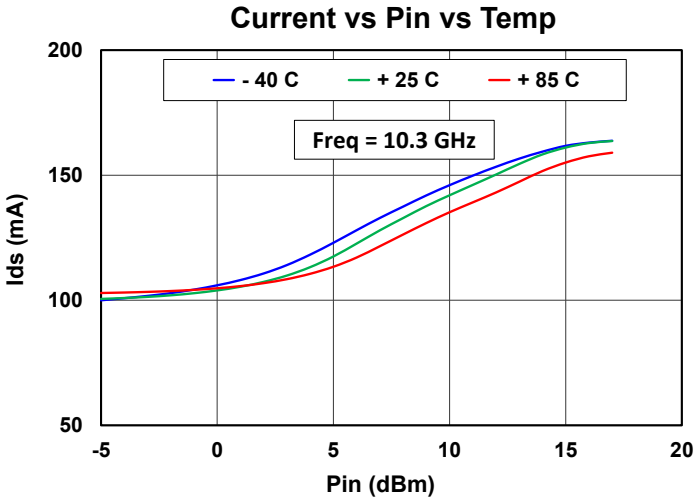


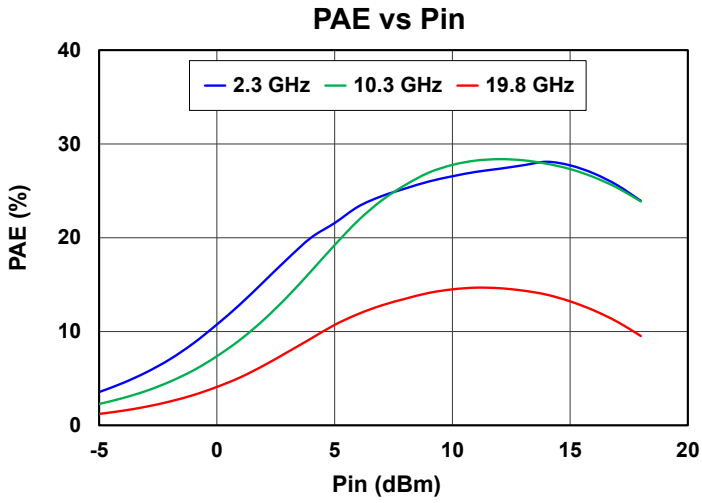


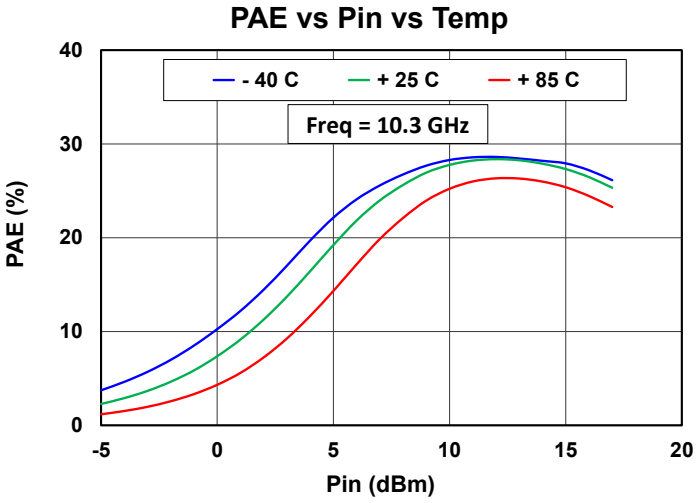
Power Sweep, Receive

Test Conditions unless otherwise stated: LNA_VD = 5 V, LNA IDQ = 100 mA, 25 °C



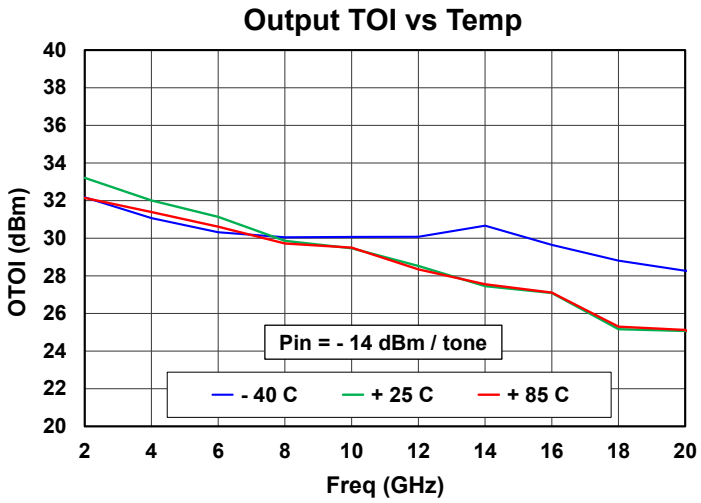


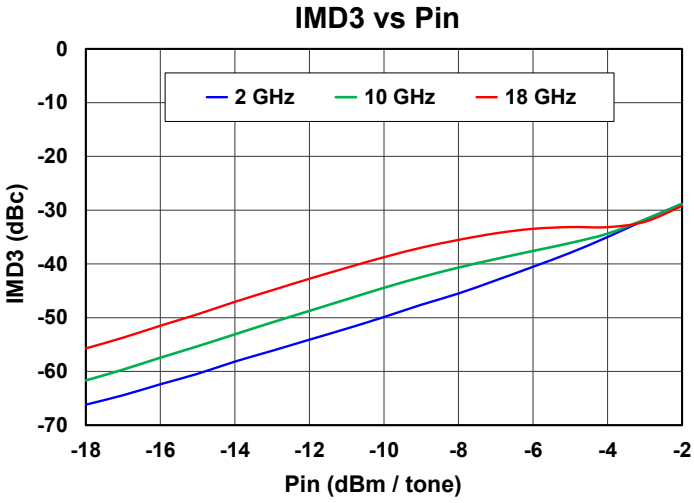


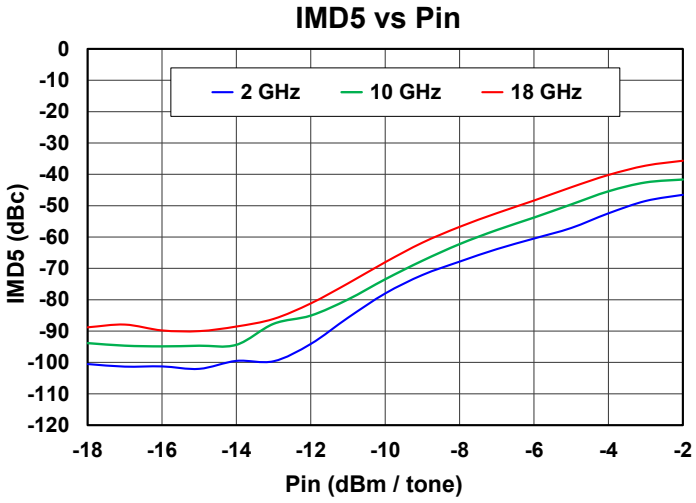


Performance Plots, Linearity, Receive

Test Conditions unless otherwise stated: LNA VD = 5 V, LNA IDQ = 100 mA, Tone spacing = 100 MHz, 25 °C

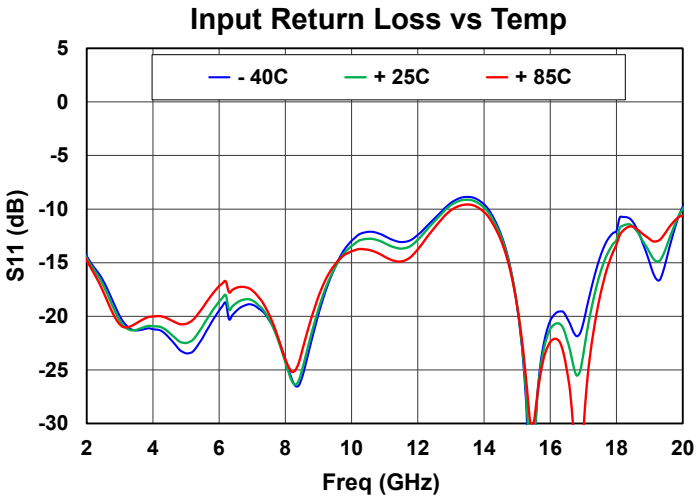


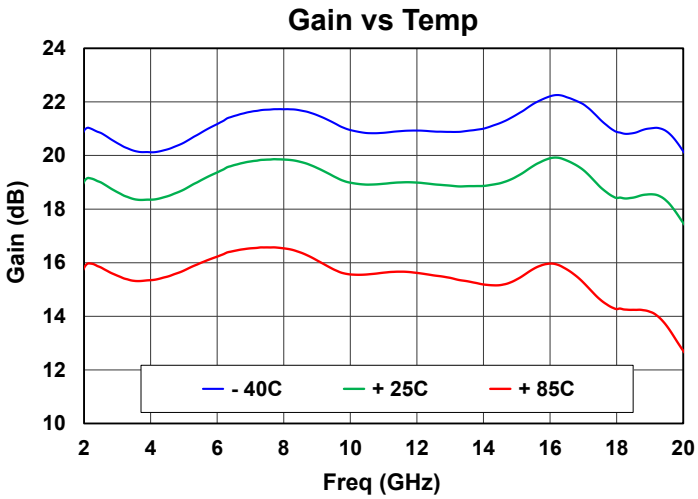


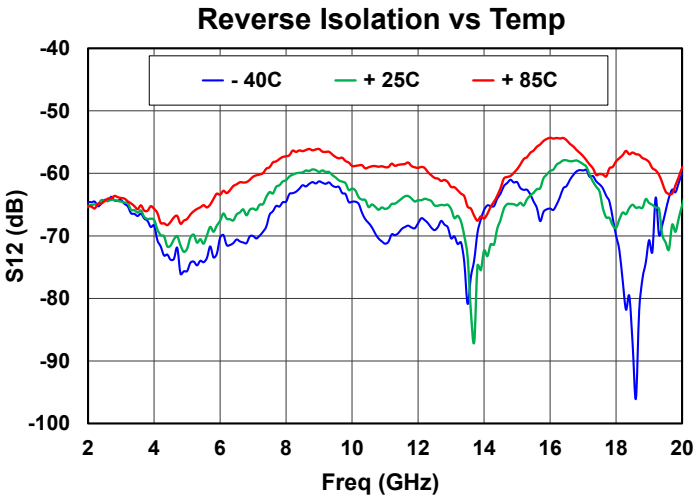


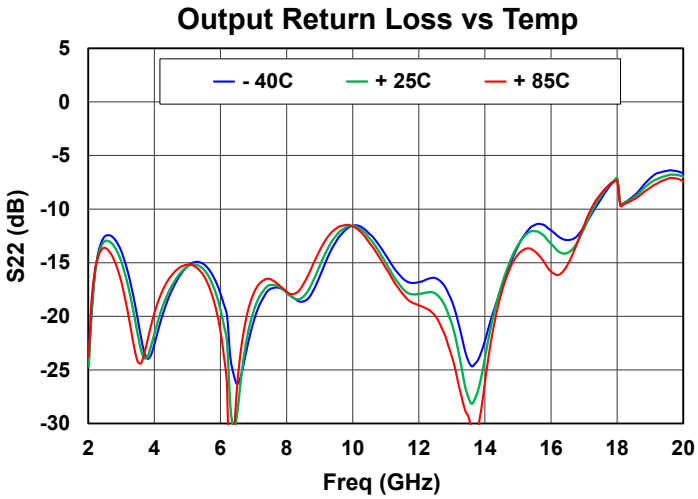
Small Signal Performance, Transmit

Test Conditions unless otherwise stated: VD = 22 V, PA IDQ = 1680 mA, 25 °C





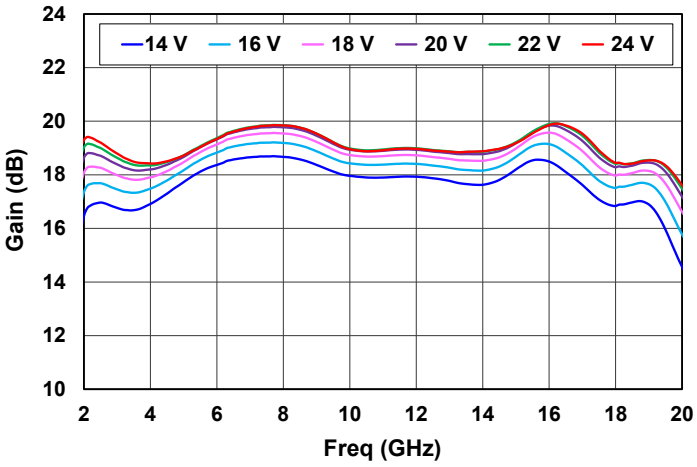




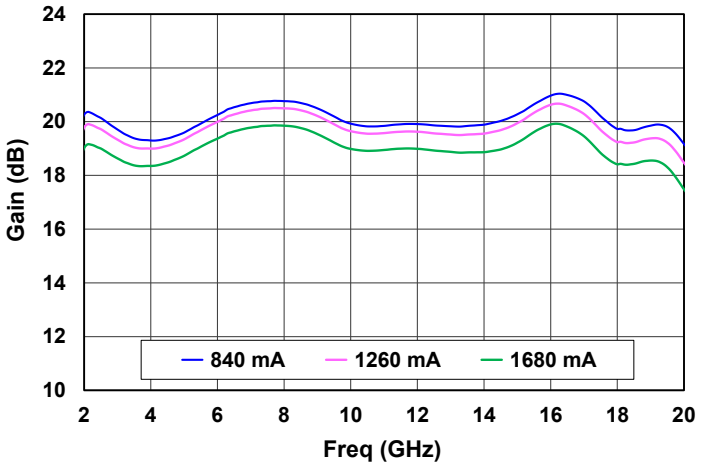
Small Signal Performance, Transmit

Test Conditions unless otherwise stated: PA_VD = 22 V, PA IDQ = 1680 mA, 25 °C

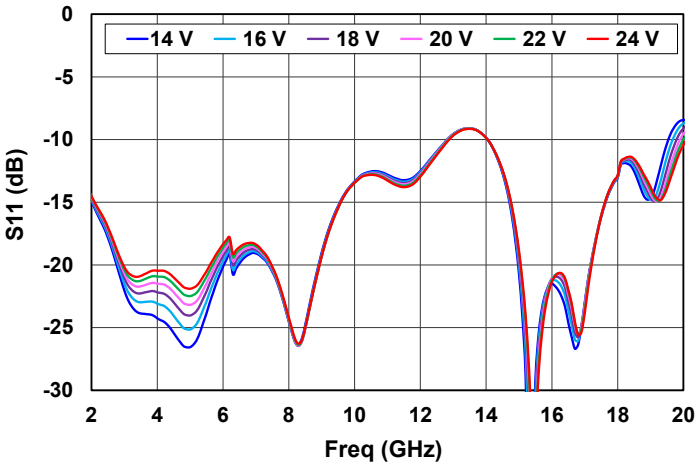
Gain vs Voltage



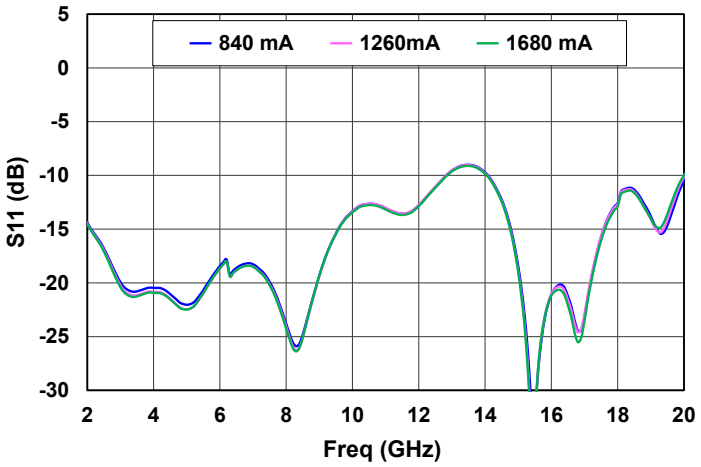
Gain vs Current



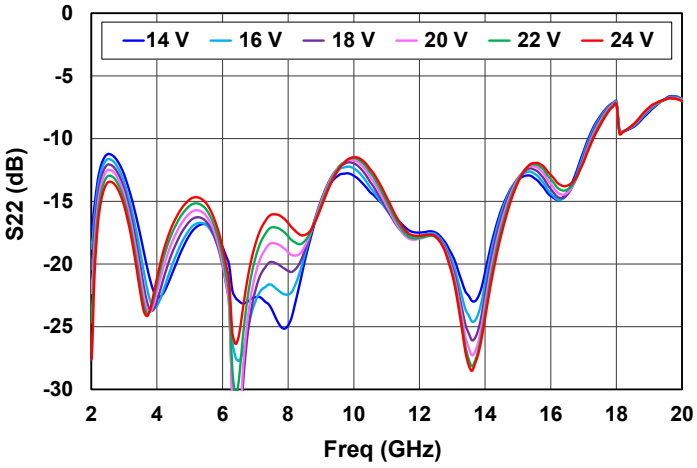
Input Return Loss vs Voltage



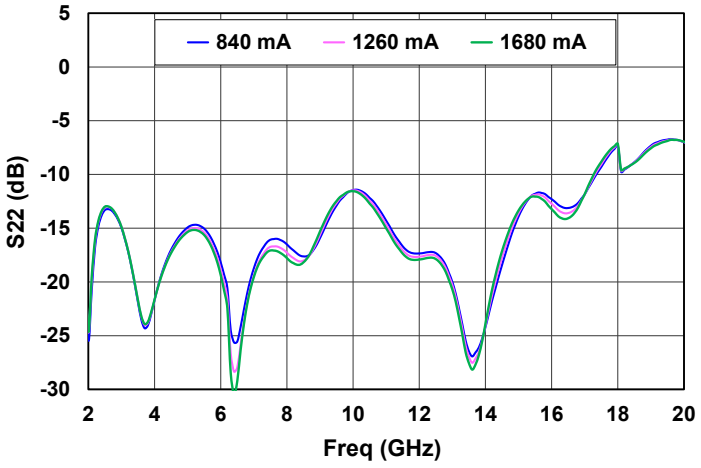
Input Return Loss vs Current



Output Return Loss vs Voltage



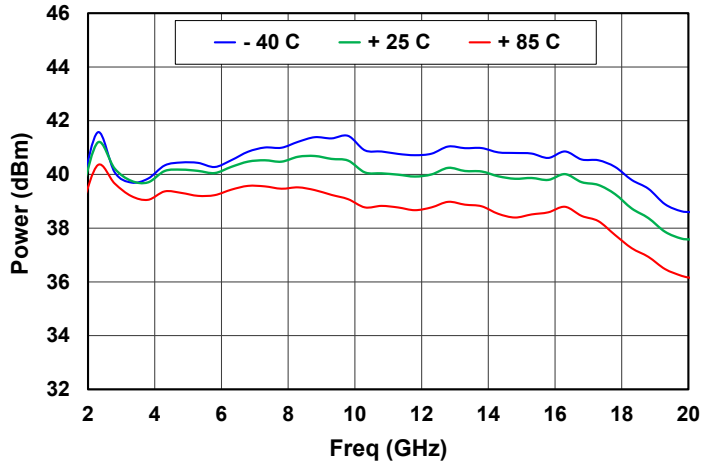
Output Return Loss vs Current



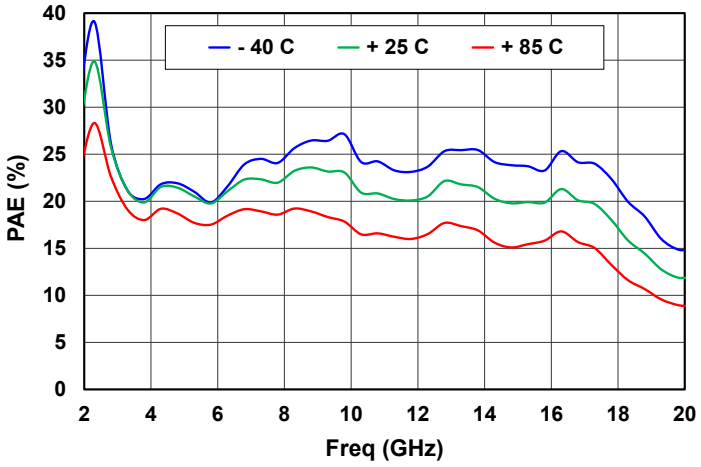
Power Performance, Large Signal, Transmit

Test Conditions unless otherwise stated: VD = 22 V, IDQ = 1680 mA, CW Mode, Pin = 27 dBm, 25 °C

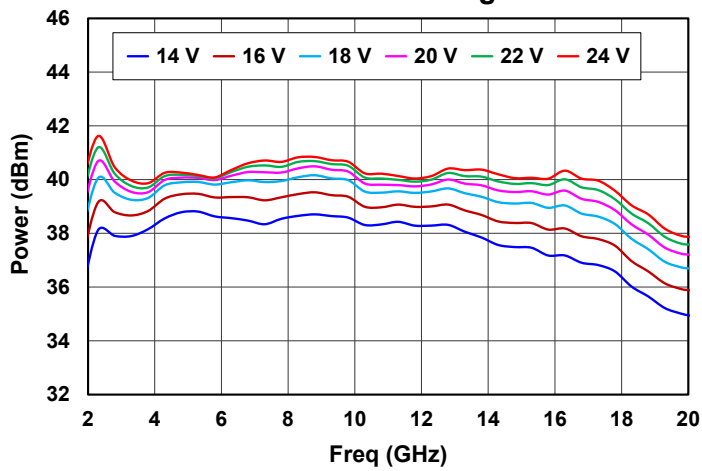
Power vs Temperature



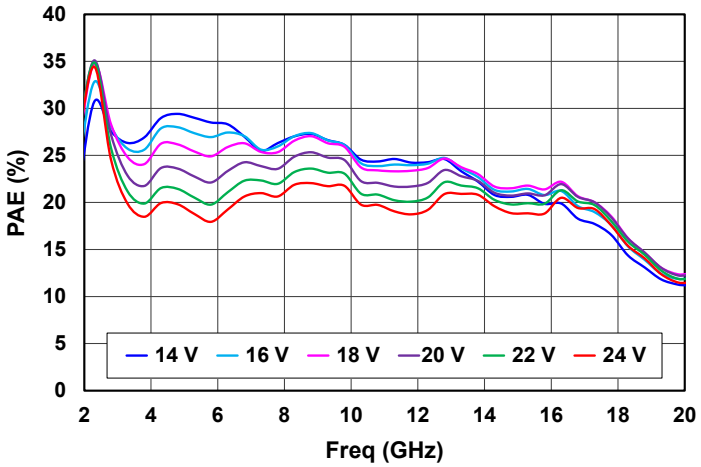
PAE vs Temperature



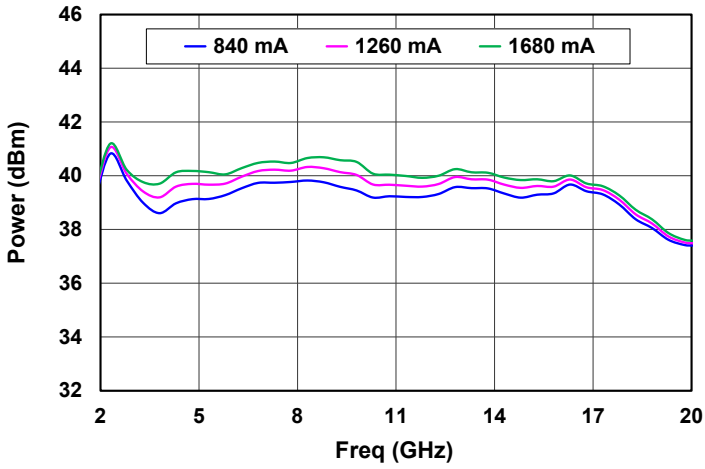
Power vs Voltage



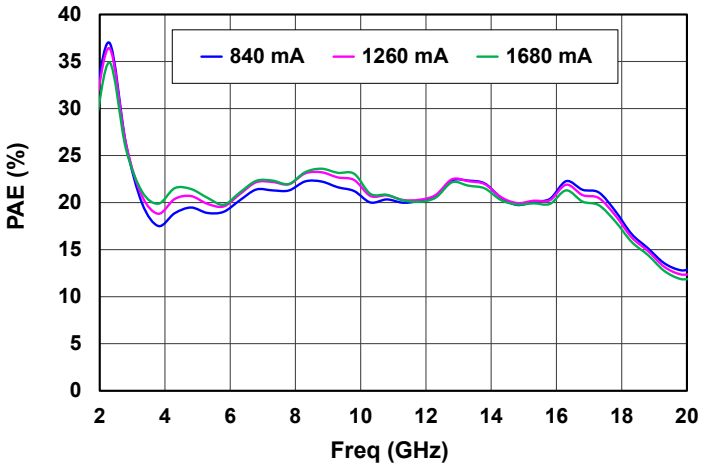
PAE vs Voltage



Power vs Current



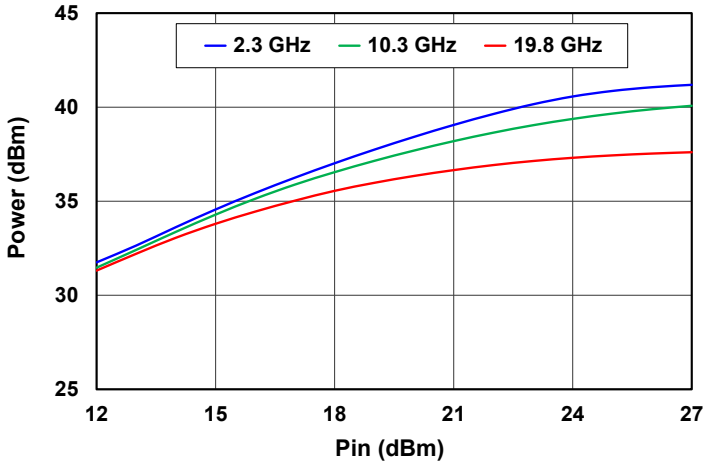
PAE vs Current



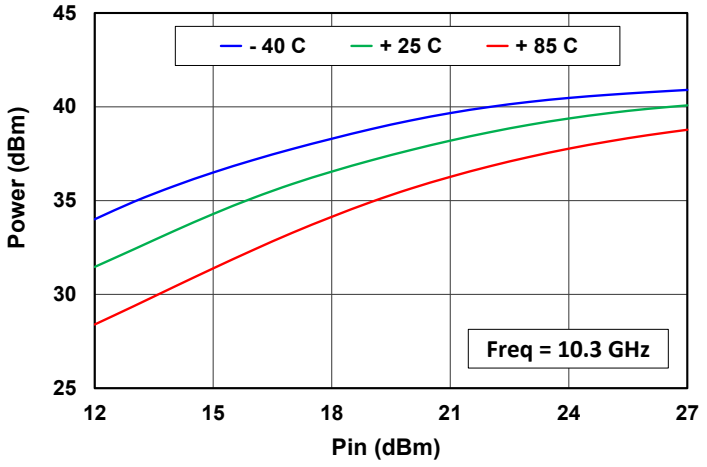
Power Performance, Power Sweep, Transmit

Test Conditions unless otherwise stated: VD = 22 V, IDQ = 1680 mA, CW Mode, 25 °C

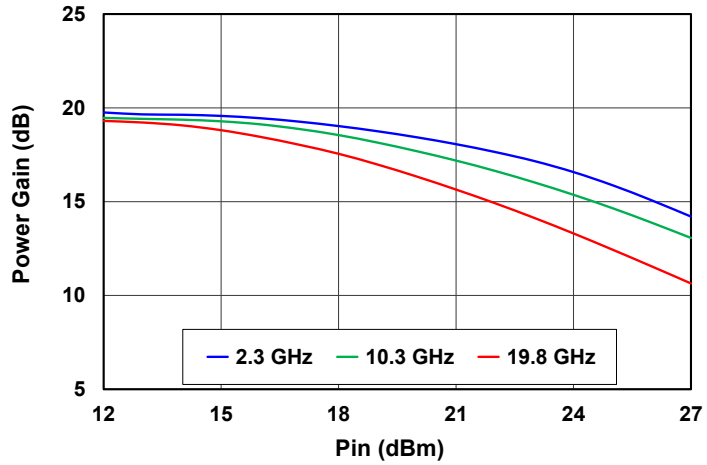
Power vs Pin



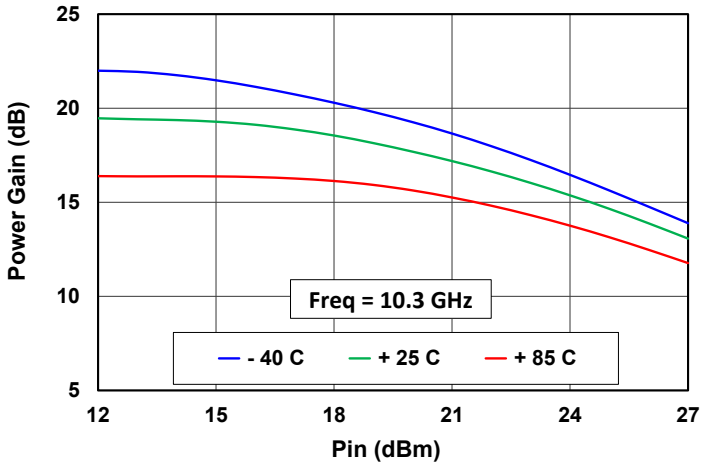
Power vs Pin vs Temp



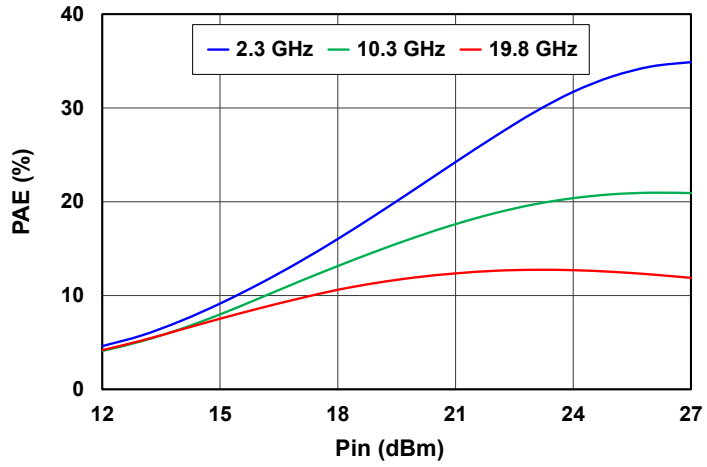
Power Gain vs Pin



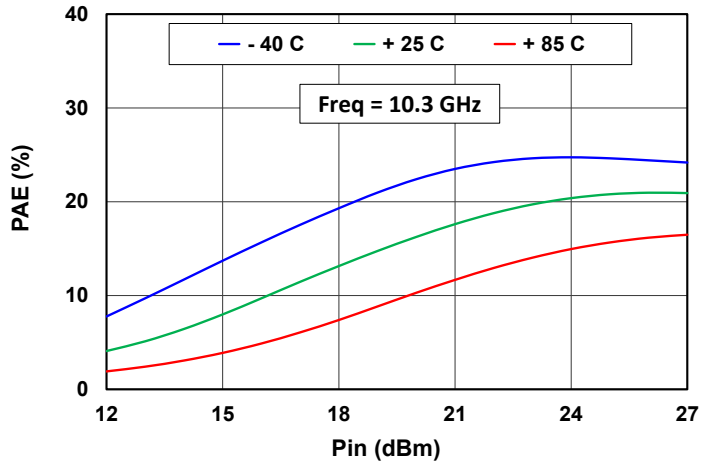
Power Gain vs Pin vs Temp



PAE vs Pin



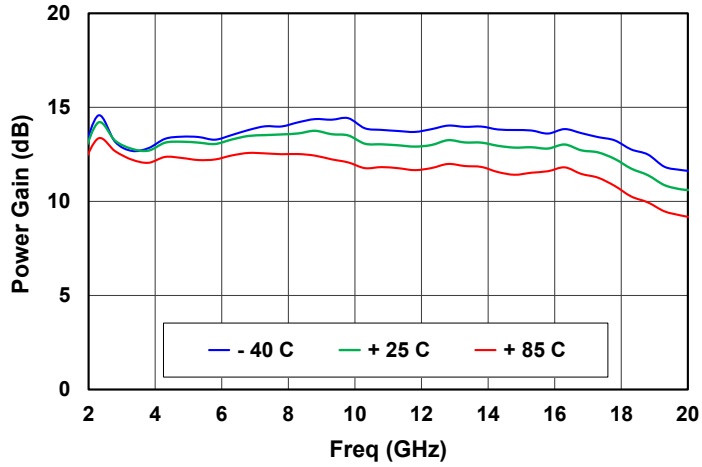
PAE vs Pin vs Temp



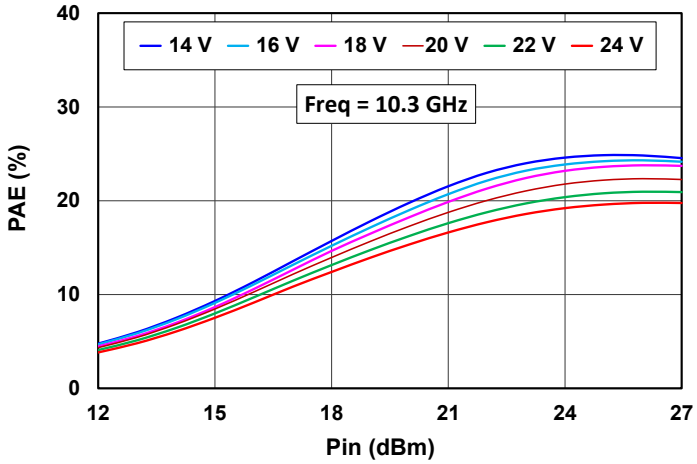
Power Performance, Large Signal, Transmit

Test Conditions unless otherwise stated: VD = 22 V, IDQ = 1680 mA, CW Mode, Pin = 27 dBm, 25 °C

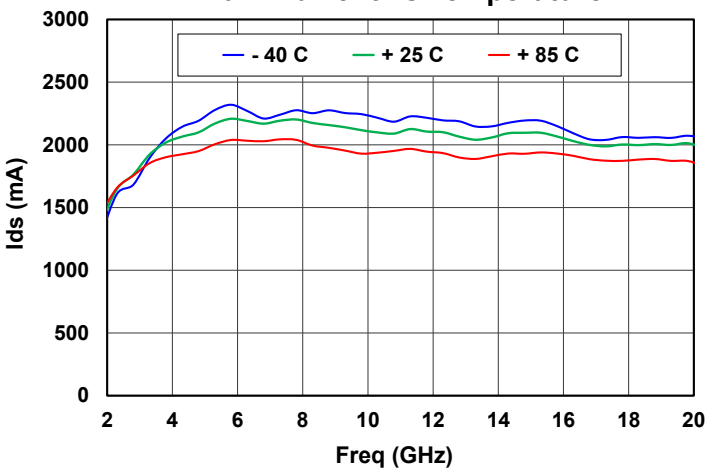
Power Gain vs Temperature



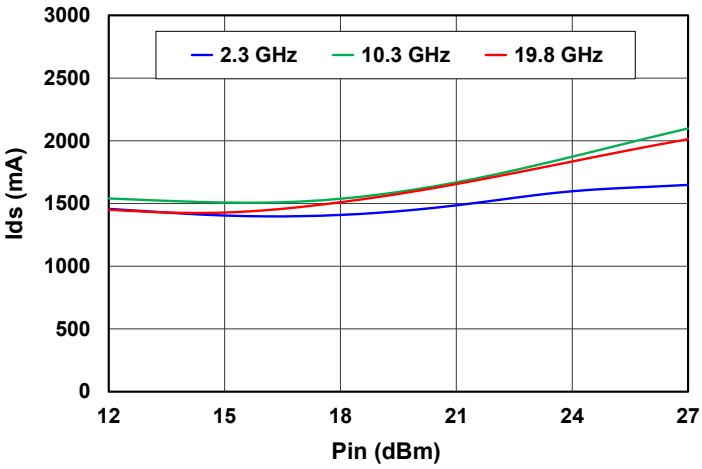
PAE vs Pin v Voltage



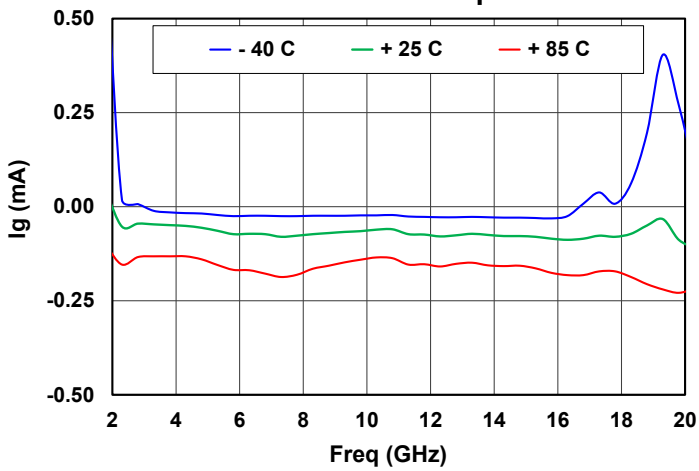
Drain Current vs Temperature



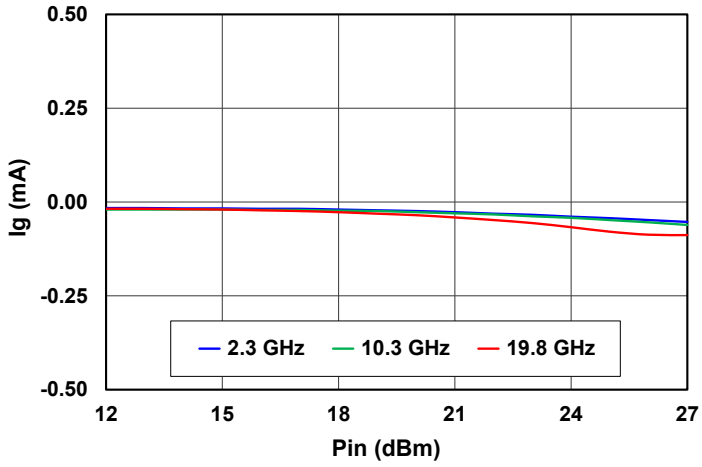
Drain Current vs Pin



Gate Current vs Temperature

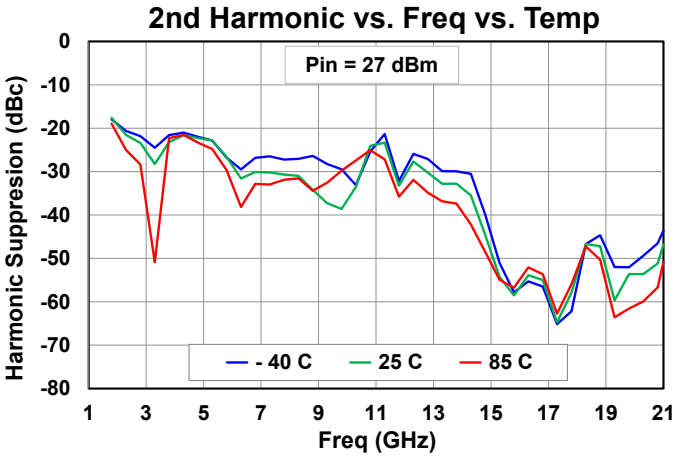


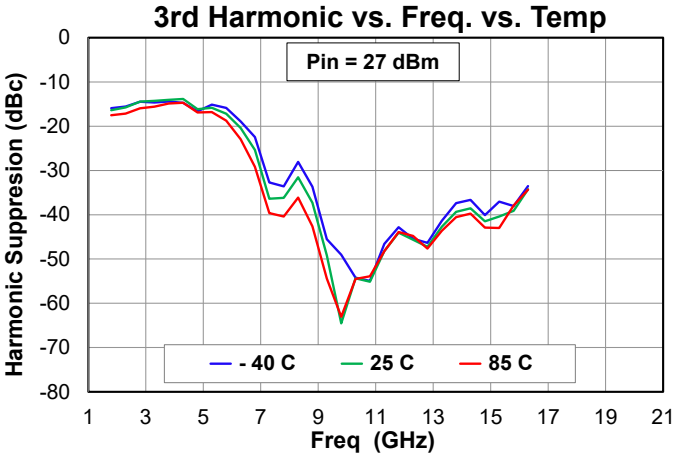
Gate Current vs Pin

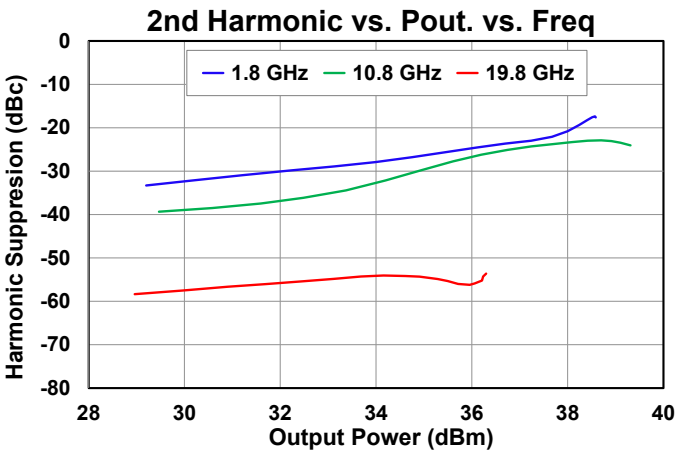


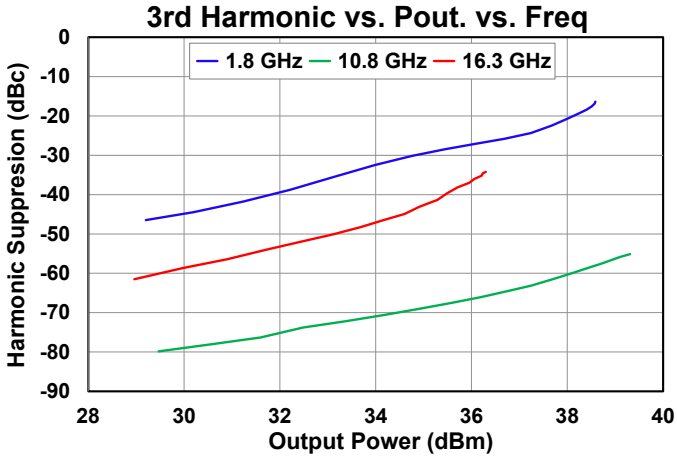
Performance Plots, Harmonics, Transmit

Test Conditions unless otherwise stated: VD = 22 V, IDQ = 1680 mA, CW Mode, 25 °C





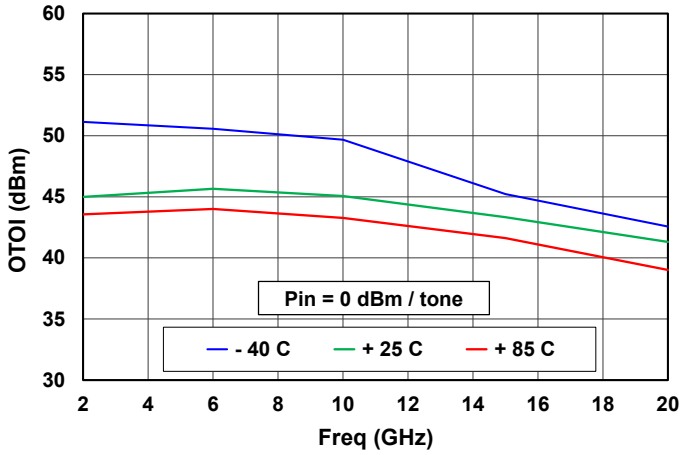




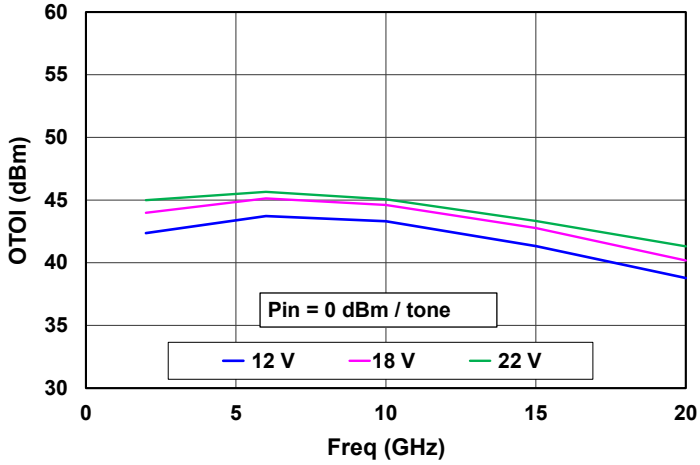
Performance Plots, Linearity, Transmit

Test Conditions unless otherwise stated: VD = 22 V, IDQ = 1680 mA, Tone Spacing = 100 MHz, CW Mode, 25 °C

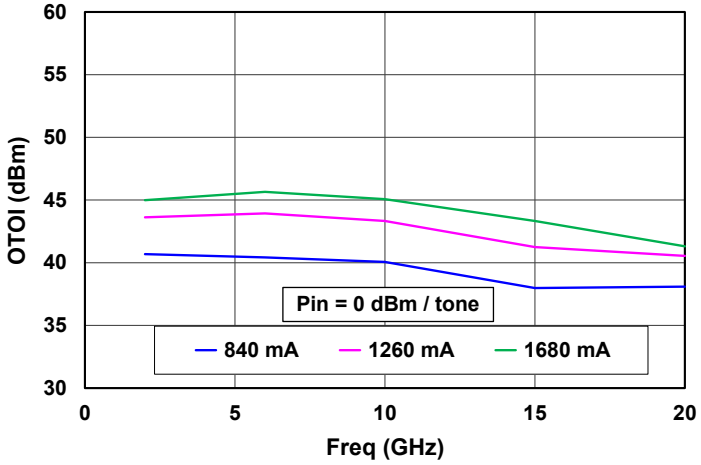
Output TOI vs Temp



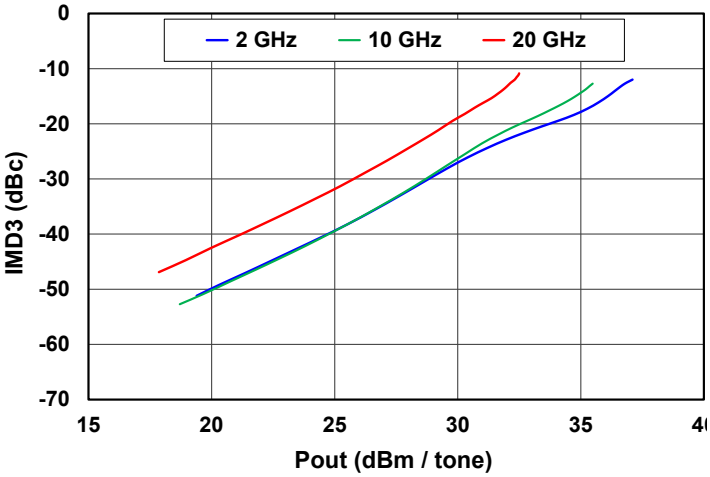
Output TOI vs Voltage



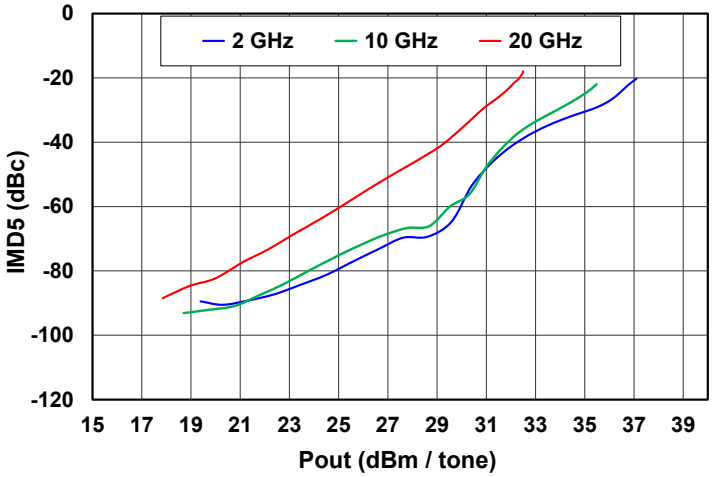
Output TOI vs Current



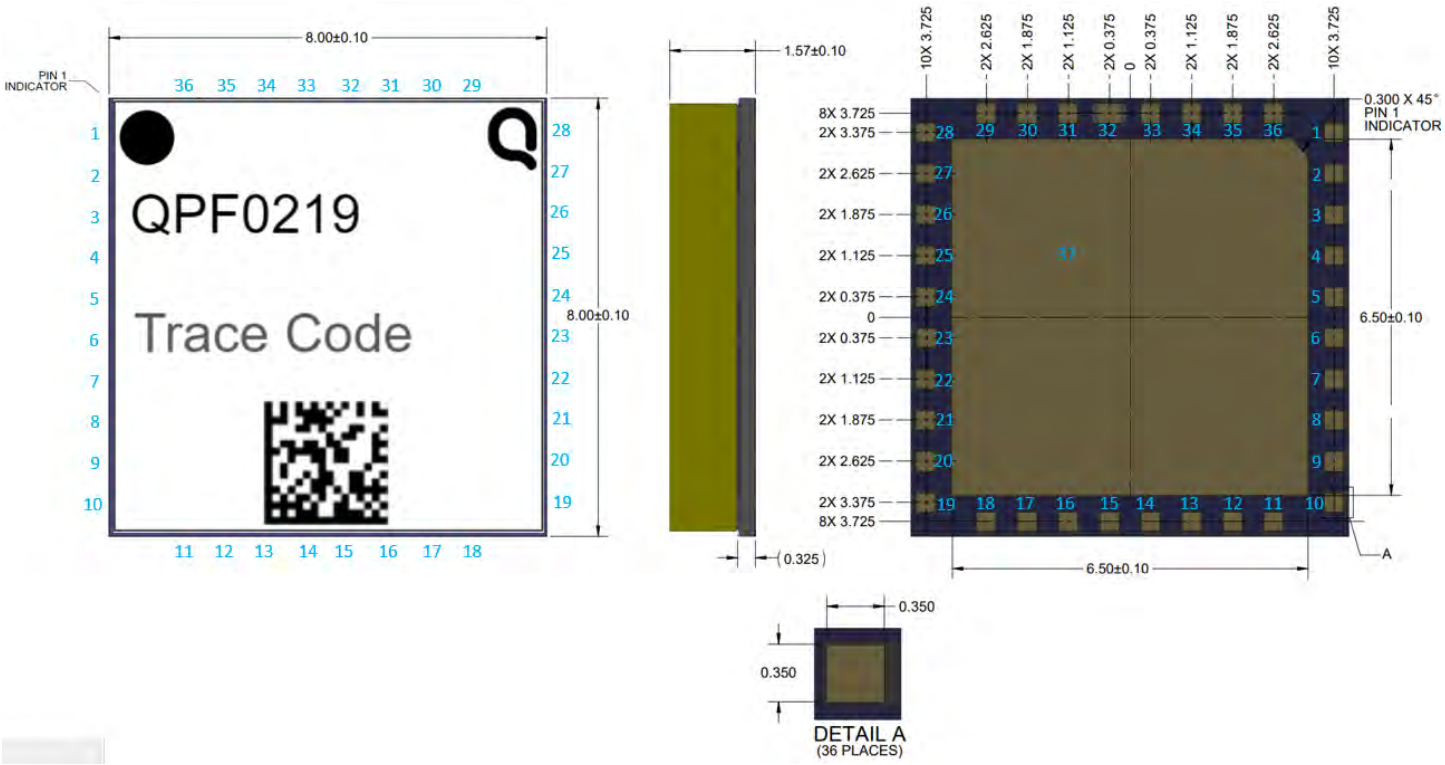
IMD3 vs Pout



IMD5 vs Pout



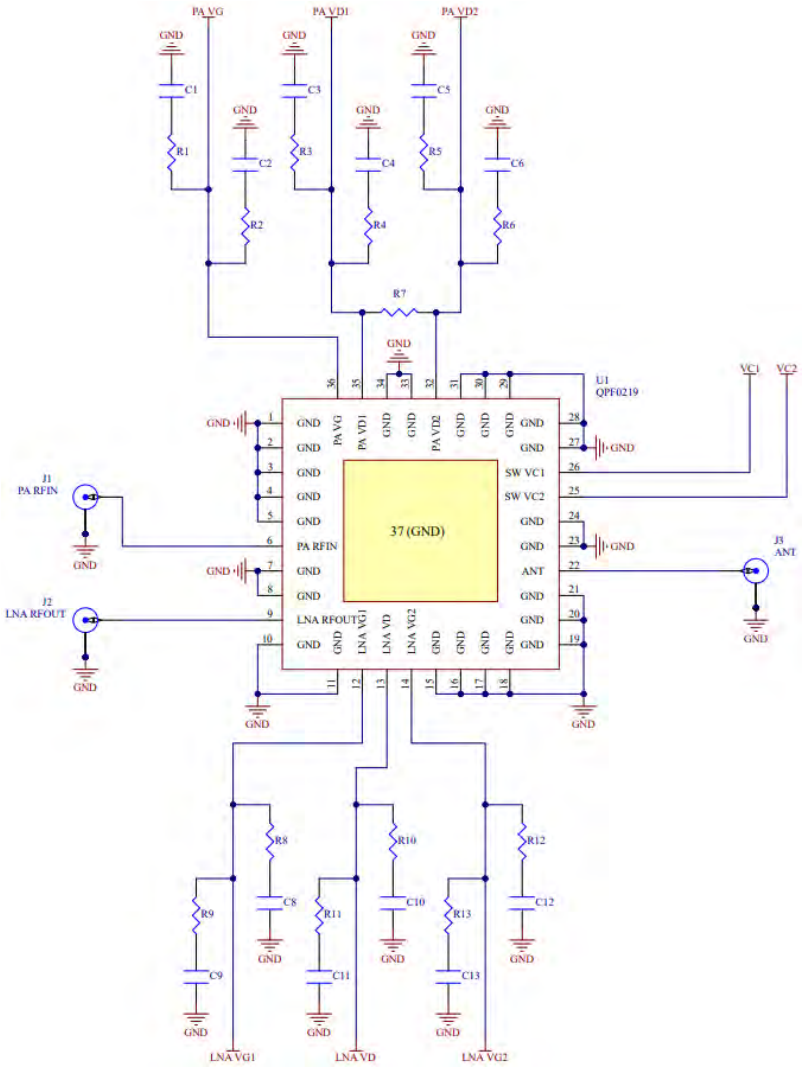
Mechanical Drawing & Pad Description



Dimensions in mm
Package is air cavity with gold plated leads, typical gold finish thickness is 0.1 um
Part Marking: QPF0219 = Part Number, Trace Code and 2DID can be used to trace part manufacturing records

Pin Number	Label	Description
1 - 5, 7, 8, 10, 11, 15 - 21, 23, 24, 27 – 31, 33, 34	GND	Ground
6	TXIN	Transmit Input, DC Blocked
9	RXOUT	Receive Output, DC Blocked
12	LNA_VG1	LNA Gate Control
13	LNA_VD	LNA Drain Supply
14	LNA_VG2	LNA Gate Control
22	ANT	RXIN / TXOUT, Common Port to Antenna, DC Coupled
25	VC2	Switch Control
26	VC1	Switch Control
32	PA_VD2	Transmit PA Drain Supply
35	PA_VD1	Transmit PA Drain Supply
36	PA_VG	Transmit PA Gate Control
37	GND	Package Base Ground

Application Circuit



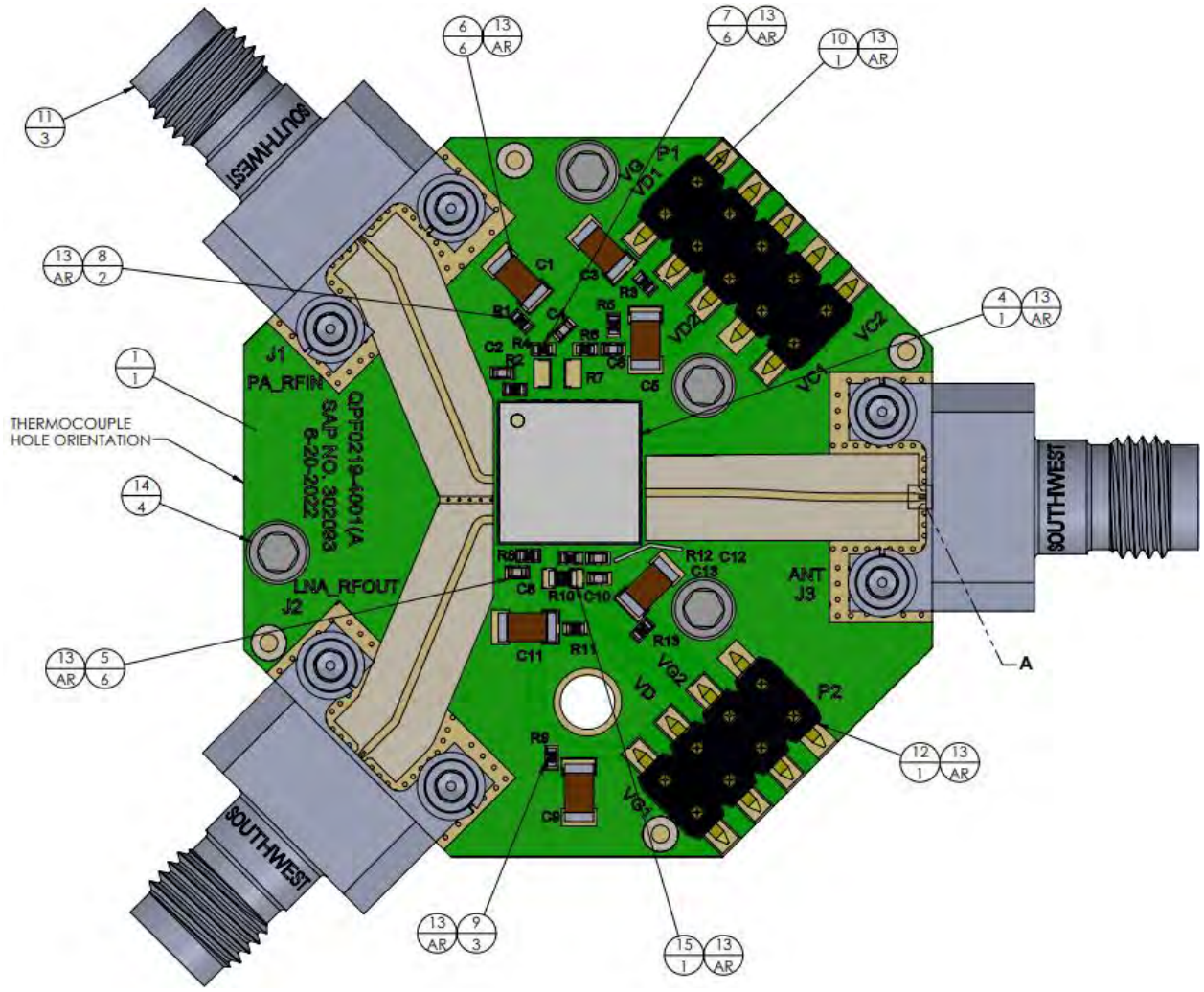
Bias-up Procedure

1. Set PA_VD current limit to 3000 mA, LNA_VD current limit to 200 mA, gate current limit to 10 mA, switch control current limit to 10mA each
2. Set LNA_VG1 to -1.5 V and PA_VG to − 5 V
3. Set LNA_VD = + 5 V, PA_VD = + 22 V
4. Set VC1 = - 40 V (or 0 V), VC2 = 0 V (or – 40 V) for Transmit (Receive), set LNA_VG2 = 1.3 V
5. Adjust PA_VG, LNA_VG1 to achieve required drain current for PA (- 2.5 V typical) and LNA (−0.5 V typical)
6. Apply RF signal

Bias-down Procedure

1. Turn off RF signal
2. Set LNA_VG1 = -1.5 V, PA_VG to −5 V
3. Set LNA_VG2 = 0 V
4. Set PA_VD = 0 V, LNA_VD = 0 V
5. Turn off VC1, VC2, PA_VD, LNA_VD
6. Turn off gate supplies

Evaluation Board and Assembly



Multilayer PCB, top RF layer is 8 mils thick Rogers 4003C (ε_r = 3.35). Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-01A-12.

Ref. Des.	Component	Value	Manuf.	Part Number
C2, C4, C6, C8, C10, C12	SMT Cap.	CAP, 0402, 0.01uF, 10%, 50V, X7R	Various	
C1, C3, C5, C9, C11, C13	SMT Cap.	CAP, 1206, 10uF, 20%, 50V, X7R	Various	
R9, R11, R13	SMT Res.	RES, 0402 10 Ohm, 5%, 1/10W	Various	
R1, R3	SMT Res.	RES, 0402 5.1 Ohm, 5%, 1/10W	Various	
R2, R4, R5, R6, R8, R12	SMT Res.	RES, 0402 0 Ohm	Various	
R10	SMT Res.	RES, 0603, 0 Ohm	Various	
R7	SMT Res.	Component not populated	-	
J1, J2, J3	RF Connectors	CONN, 2.92mm, end launch	Southwest Microwave	1092-01A-12

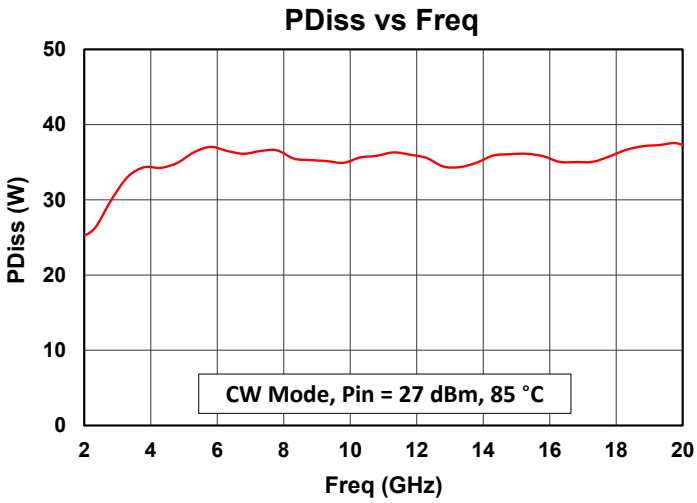
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
TX Channel Thermal Resistance (θ_{JC}) (1)	T_{base} = +85 °C, V_D = 22 V, I_{DQ} = 1260 mA P_{DISS} = 27.72 W Quiescent or small signal applicsations	2.58	ºC/W
TX Channel Temperature, T_{CH} (Under RF) (2,3)		156.52	°C
TX Channel Thermal Resistance (θ_{JC}) (1)	T_{base} = +85 °C, V_D = 22 V, I_{DQ} = 1680 mA, I_{D_Drive} = 1872 mA P_{OUT} = 36.22 dBm, P_{IN} = 27 dBm, Freq. = 19.8 GHz (worst case), P_{DISS} = 37.50 W (CW)	2.58	ºC/W
TX Channel Temperature, T_{CH} (Under RF) (2,3)		181.80	°C
RX Channel Thermal Resistance (θ_{JC}) (1,4)	T_{base} = +85 °C, V_{DD} = 5 V, I_{DQ} = 100 mA, CW P_{DISS} = 0.5 W (Quiescent or small signals CW)	26	ºC/W
RX Channel Temperature, T_{CH} (Under RF) (1,4)		98	°C
Median Lifetime (T_M) (3)		1.0E09	Hrs

Notes:
1. Thermal resistance is referenced to the back of the package.
2. Channel temperature is IR scan equivalent.
3. Refer to the following document for transmit channel thermal properties:
   GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates
4. LNA used GaAs Process, refer to below plot for operation life.

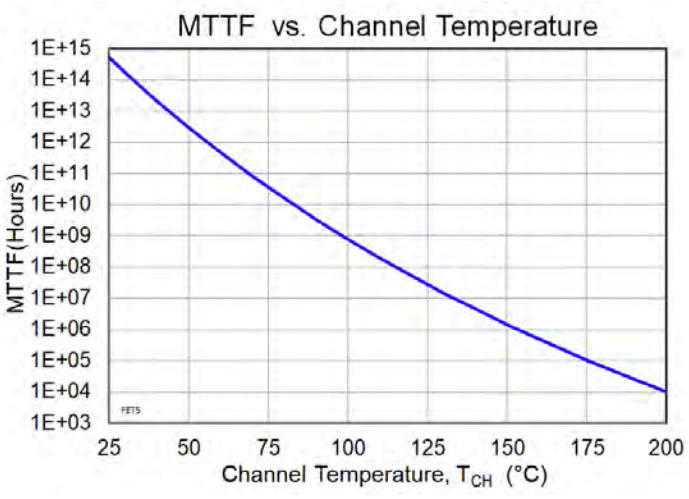
PA Power Dissipation

Test Conditions: VD = 22 V, 1680 mA
CW Mode, 85 °C



LNA Median Life

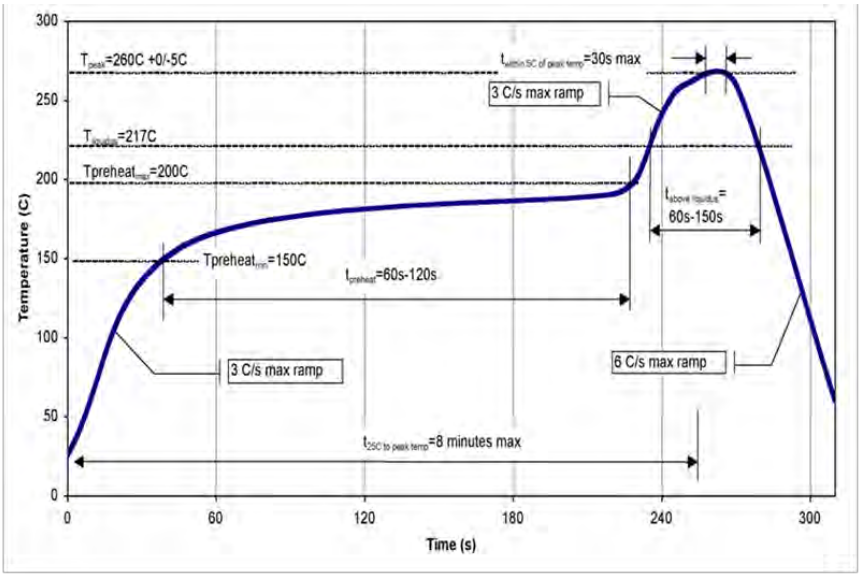
Test Conditions: VD = 4 V
Failure Criteria = 10% reduction in I_{D_MAX}



Solderability

1. Compatible with lead-free soldering process with 260° C peak reflow temperature.
2. This package is non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing is highly recommended.

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1B	ESDA / JEDEC JS-001-2017
ESD – Charged Device Model (CDM)	C2a	ESDA / JEDEC JS-002-2014
MSL – Convection Reflow 260 °C	MSL5a	JEDEC standard IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.
This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Tel: **1-844-890-8163**

Web: www.qorvo.com

Email: customer.support@qorvo.com

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