# QPD1009

## 15W, 50V, DC – 4 GHz, GaN RF Transistor

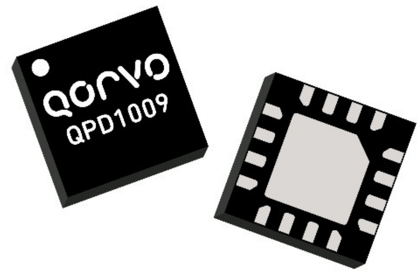
## General Description

The Qorvo QPD1009 is a 15 W ($P_{3dB}$) discrete GaN on SiC HEMT which operates from DC to 4 GHz. The device is constructed with Qorvo's proven QGaN25HV process, which features advanced field plate techniques to optimize power and efficiency at high drain bias operating conditions. This optimization can potentially lower system costs in terms of fewer amplifier line-ups and lower thermal management costs.

The device is housed in an industry-standard 3 x 3 mm surface mount QFN package.

Lead-free and ROHS compliant

Evaluation boards are available upon request.

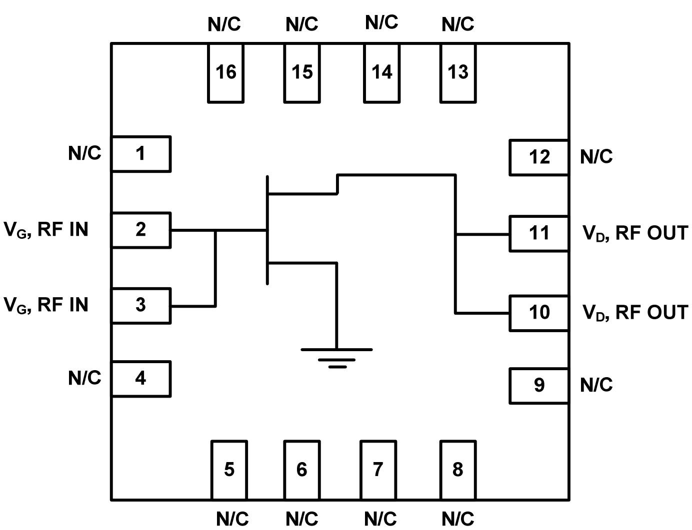



3 x 3 x 0.100 mm

## Product Features

- Frequency: DC to 4 GHz
- Output Power ($P_{3dB}$): 17 W at 2 GHz
- Linear Gain: 24 dB at 2 GHz
- Typical $PAE_{3dB}$: 72% at 2 GHz
- Operating Voltage: 50 V
- Low thermal resistance package
- CW and Pulse capable
- 3 x 3 mm package

## Functional Block Diagram




## Applications

- Military radar
- Civilian radar
- Land mobile and military radio communications
- Test instrumentation
- Wideband or narrowband amplifiers
- Jammers

## Ordering info

| Part No. | ECCN | Description |
|---|---|---|
| QPD1009 | EAR99 | DC – 4 GHz RF Transistor |
| QPD1009-EVB1 | EAR99 | 0.96 – 1.215 GHz EVB |

## Absolute Maximum Ratings[1]

| Parameter | Rating | Units |
|---|---|---|
| Breakdown Voltage, $BV_{DG}$ | +145 | V |
| Gate Voltage Range, $V_G$ | -7 to 0 | V |
| Drain Current, $I_{DSS}$ | 1600 | mA |
| Gate Current Range, $I_G$ | See page 4. | mA |
| Power Dissipation, CW, $P_{DISS}$ | 16 | W |
| RF Input Power at 2 GHz, CW, 50 Ω, T = 25 °C | +27 | dBm |
| Channel Temperature, $T_{CH}$ | 275 | °C |
| Mounting Temperature (30 Seconds) | 320 | °C |
| Storage Temperature | –40 to +150 | °C |

Notes:

1. . Operation of this device outside the parameter ranges given above may cause permanent damage.

## Recommended Operating Conditions[1]

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Operating Temp. Range | –40 | +25 | +85 | °C |
| Drain Voltage Range, $V_D$ | +12 | +50 | +60 | V |
| Drain Bias Current, $I_{DQ}$ | – | 26 | – | mA |
| Drain Current, $I_D$ | – | 700 | – | mA |
| Gate Voltage, $V_G$ | – | –2.8 | – | V |
| Channel Temperature ($T_{CH}$) | – | – | 250 | °C |
| Power Dissipation, CW ($P_D$)[2] | – | – | 14.4 | W |
| Power Dissipation, Pulsed ($P_D$)[2, 3] | – | – | 17.5 | W |

Notes:

1. Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.
2. Package at 85 °C
3. Pulse Width = 128 uS, Duty Cycle = 10%

## Pulsed Characterization – Load Pull Performance – Power Tuned

| Parameters | Typical Values | | | | | Unit |
|---|---|---|---|---|---|---|
| Frequency, F | 1 | 2 | 3 | 3.5 | 4 | GHz |
| Linear Gain, $G_{LIN}$ | 27 | 23.7 | 20.9 | 19.7 | 18.7 | dB |
| Output Power at 3dB compression point, $P_{3dB}$ | 41.9 | 42.4 | 42.4 | 42.2 | 41.8 | dBm |
| Power-Added-Efficiency at 3dB compression point, $PAE_{3dB}$ | 64.1 | 67.3 | 61.4 | 56.9 | 50.0 | % |
| Gain at 3dB compression point | 24 | 20.7 | 17.9 | 16.7 | 15.7 | dB |

Notes:
1. Test conditions unless otherwise noted: $V_D$ = +50 V, $I_{DQ}$ = 26 mA, Temp = +25 °C

## Pulsed Characterization – Load Pull Performance – Efficiency Tuned

| Parameters | Typical Values | | | | | Unit |
|---|---|---|---|---|---|---|
| Frequency | 1 | 2 | 3 | 3.5 | 4 | GHz |
| Linear Gain, $G_{LIN}$ | 26.8 | 24.0 | 21.8 | 20.5 | 19.3 | dB |
| Output Power at 3dB compression point, $P_{3dB}$ | 40 | 41.9 | 40.9 | 40.7 | 41.2 | dBm |
| Power-Added-Efficiency at 3dB compression point, $PAE_{3dB}$ | 77.8 | 72.4 | 69.6 | 63.3 | 54.6 | % |
| Gain at 3dB compression point, $G_{3dB}$ | 23.8 | 21.0 | 18.8 | 17.5 | 16.3 | dB |

Notes:
1. Test conditions unless otherwise noted: $V_D$ = +50 V, $I_{DQ}$ = 26 mA, Temp = +25 °C

## RF Characterization – 0.96 – 1.215 GHz EVB Performance At 1.09 GHz[1]

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Linear Gain, $G_{LIN}$ | – | 19.5 | – | dB |
| Output Power at 3dB compression point, $P_{3dB}$ | – | 41.4 | – | dBm |
| Drain Efficiency at 3dB compression point, $DEFF_{3dB}$ | – | 53.9 | – | % |
| Gain at 3dB compression point, $G_{3dB}$ | – | 16.5 | – | dB |

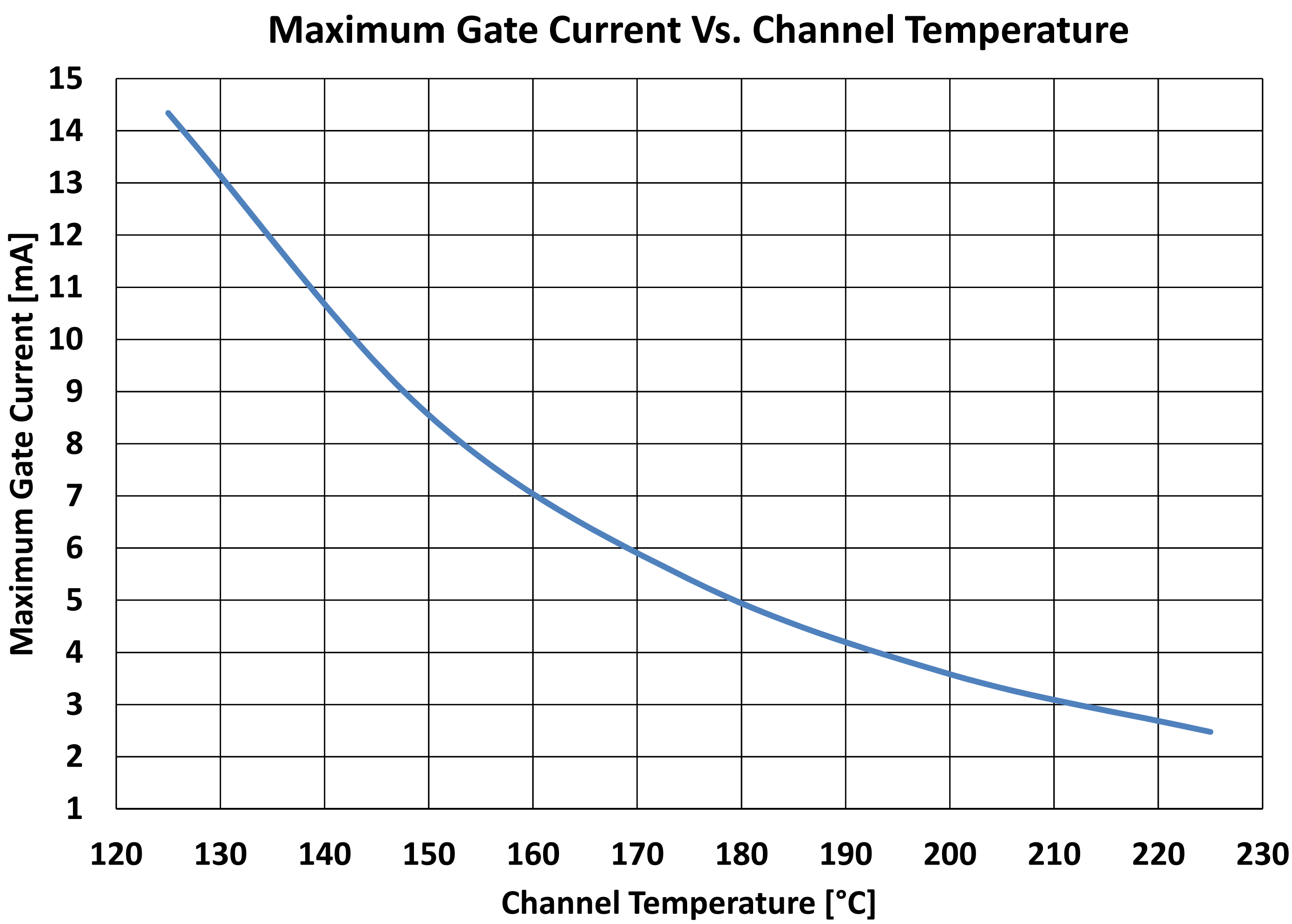
Notes:
1. $V_D$ = +50 V, $I_{DQ}$ = 26 mA, Temp = +25 °C, Pulse Width = 128 uS, Duty Cycle = 10%

## RF Characterization – Mismatch Ruggedness at 1.09 GHz

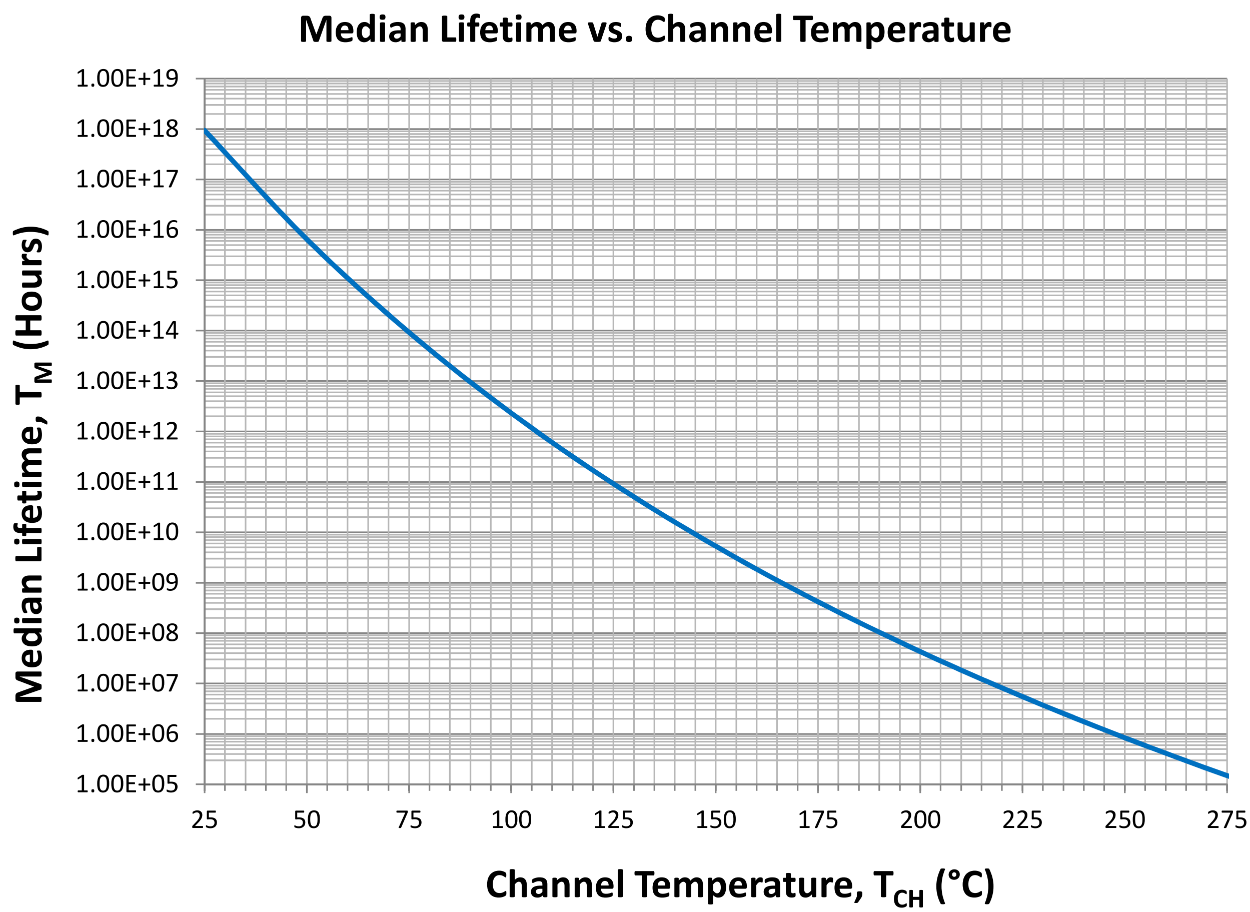
| Symbol | Parameter | dB Compression | Typical |
|---|---|---|---|
| VSWR | Impedance Mismatch Ruggedness | 3 | 10:1 |

Test conditions unless otherwise noted: $T_A$ = 25 °C, $V_D$ = 50 V, $I_{DQ}$ = 26 mA
Driving input power is determined at pulsed compression under matched condition at EVB output connector.

## Maximum Gate Current

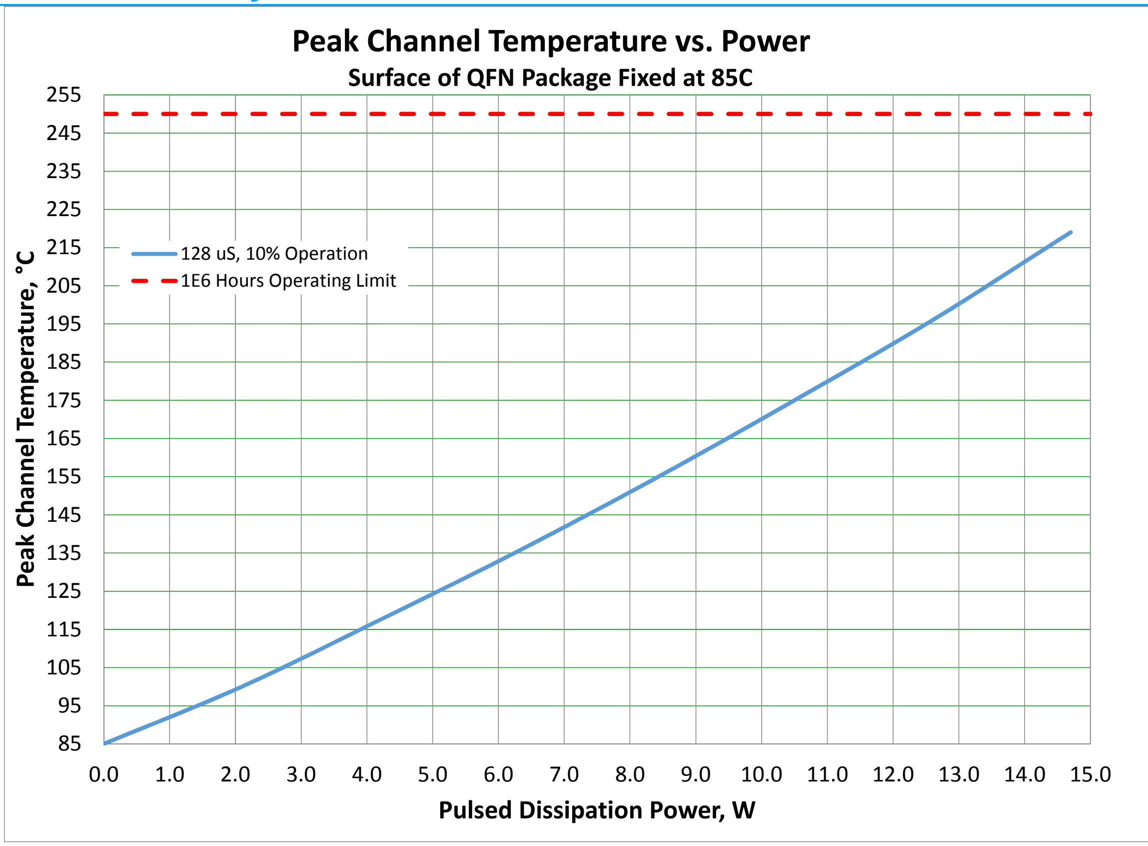


## Median Lifetime[1]



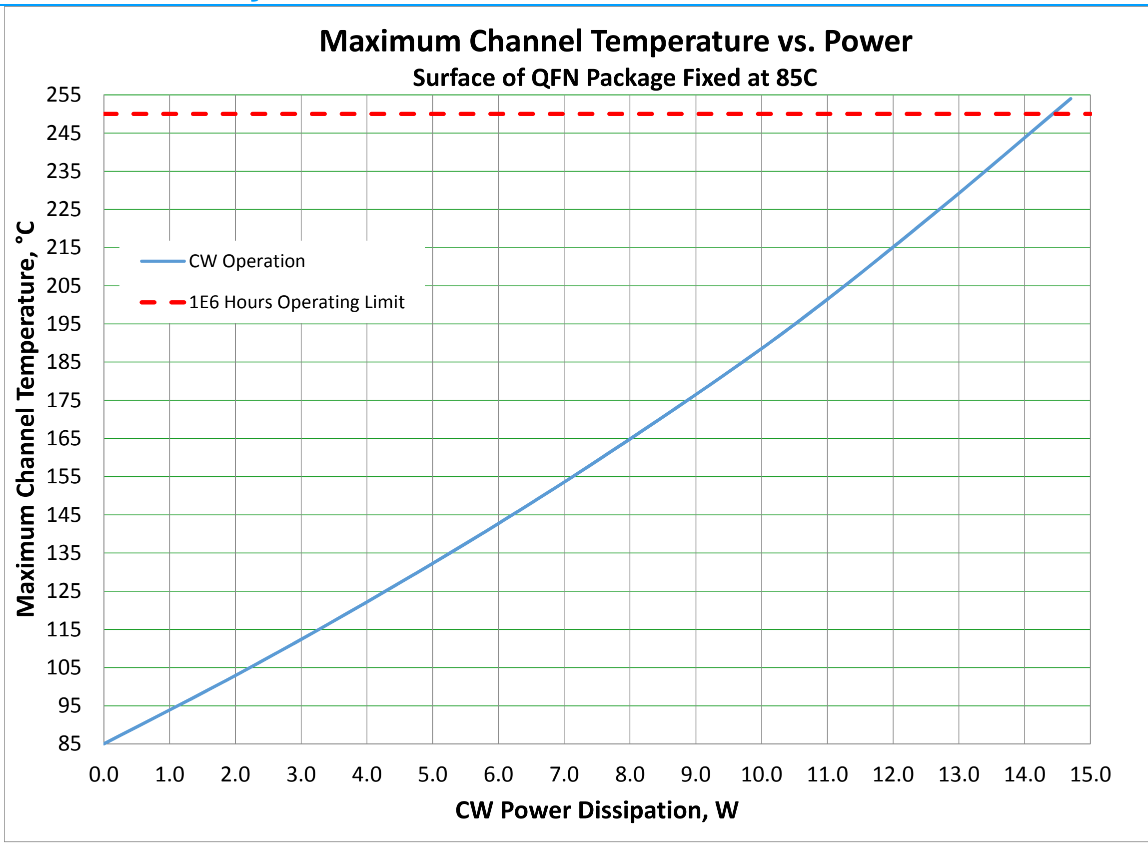

[1] For pulsed signals, average lifetime is average lifetime at maximum channel temperature divided by duty cycle.

## Thermal and Reliability Information - Pulsed




| Parameter | Conditions | Values | Units |
|---|---|---|---|
| Thermal Resistance ($\theta_{JC}$) | 85 °C Case<br>4.2 W Pdiss, 128 uS PW, 10% | 7.1 | °C/W |
| Maximum Channel Temperature ($T_{CH}$) | | 118 | °C |
| Median Lifetime ($T_M$) | | 2.3E12 | Hrs |
| Thermal Resistance ($\theta_{JC}$) | 85 °C Case<br>6.3 W Pdiss, 128 uS PW, 10% | 8.0 | °C/W |
| Maximum Channel Temperature ($T_{CH}$) | | 136 | °C |
| Median Lifetime ($T_M$) | | 2.6E11 | Hrs |
| Thermal Resistance ($\theta_{JC}$) | 85 °C Case<br>8.4 W Pdiss, 128 uS PW, 10% | 8.3 | °C/W |
| Maximum Channel Temperature ($T_{CH}$) | | 155 | °C |
| Median Lifetime ($T_M$) | | 3.2E10 | Hrs |
| Thermal Resistance ($\theta_{JC}$) | 85 °C Case<br>10.5 W Pdiss, 128 uS PW, 10% | 8.6 | °C/W |
| Maximum Channel Temperature ($T_{CH}$) | | 175 | °C |
| Median Lifetime ($T_M$) | | 4.2E9 | Hrs |
| Thermal Resistance ($\theta_{JC}$) | 85 °C Case<br>12.6 W Pdiss, 128 uS PW, 10% | 8.8 | °C/W |
| Maximum Channel Temperature ($T_{CH}$) | | 196 | °C |
| Median Lifetime ($T_M$) | | 6.2E8 | Hrs |
| Thermal Resistance ($\theta_{JC}$) | 85 °C Case<br>14.7 W Pdiss, 128 uS PW, 10% | 9.1 | °C/W |
| Maximum Channel Temperature ($T_{CH}$) | | 219 | °C |
| Median Lifetime ($T_M$) | | 9.0E7 | Hrs |

## Thermal and Reliability Information - CW

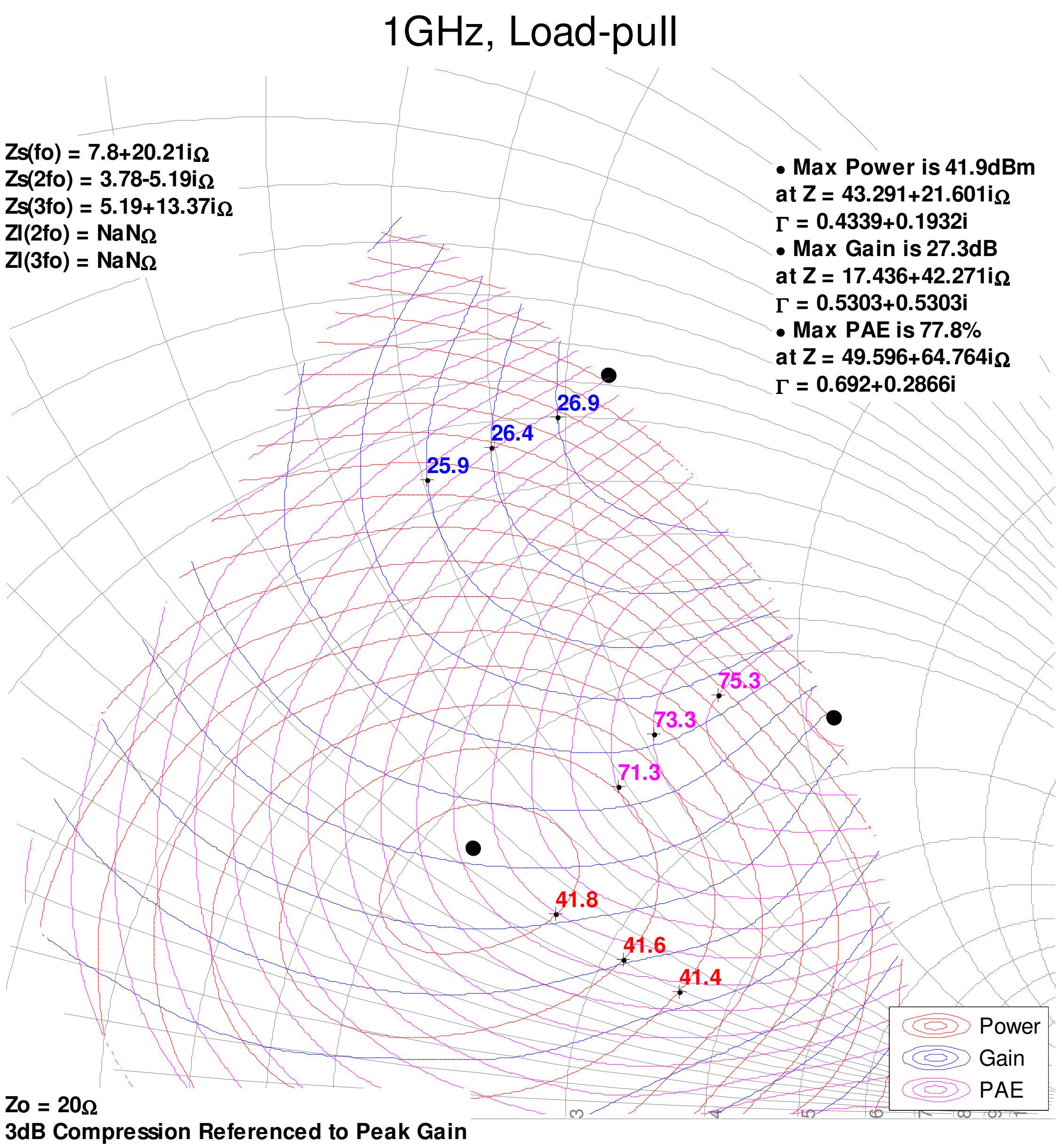



| Parameter | Conditions | Values | Units |
|---|---|---|---|
| Thermal Resistance ($\theta_{JC}$) | 85 °C Case<br>4.2 W Pdiss, CW | 9.3 | °C/W |
| Maximum Channel Temperature ($T_{CH}$) | | 124 | °C |
| Median Lifetime ($T_M$) | | 1.1E11 | Hrs |
| Thermal Resistance ($\theta_{JC}$) | 85 °C Case<br>6.3 W Pdiss, CW | 9.7 | °C/W |
| Maximum Channel Temperature ($T_{CH}$) | | 146 | °C |
| Median Lifetime ($T_M$) | | 8.4E9 | Hrs |
| Thermal Resistance ($\theta_{JC}$) | 85 °C Case<br>8.4 W Pdiss, CW | 10 | °C/W |
| Maximum Channel Temperature ($T_{CH}$) | | 169 | °C |
| Median Lifetime ($T_M$) | | 7.8E8 | Hrs |
| Thermal Resistance ($\theta_{JC}$) | 85 °C Case<br>10.5 W Pdiss, CW | 10.5 | °C/W |
| Maximum Channel Temperature ($T_{CH}$) | | 195 | °C |
| Median Lifetime ($T_M$) | | 6.8E7 | Hrs |
| Thermal Resistance ($\theta_{JC}$) | 85 °C Case<br>12.6 W Pdiss, CW | 11 | °C/W |
| Maximum Channel Temperature ($T_{CH}$) | | 224 | °C |
| Median Lifetime ($T_M$) | | 6.6E6 | Hrs |
| Thermal Resistance ($\theta_{JC}$) | 85 °C Case<br>14.7 W Pdiss, CW | 11.5 | °C/W |
| Maximum Channel Temperature ($T_{CH}$) | | 254 | °C |
| Median Lifetime ($T_M$) | | 6.4E5 | Hrs |

## Load Pull Smith Charts[1, 2, 3]

Notes:

1. Vd = 50 V, $I_{DQ}$ = 26 mA, Pulsed signal with 128 uS pulse width and 10 % duty cycle. Performance is at indicated input power.
2. See page 18 for load pull and source pull reference planes. 20-Ω load pull TRL fixtures are built with 20-mil RO4350B material.
3. NaN means the impedances are either undefined or varying in load-pull system.



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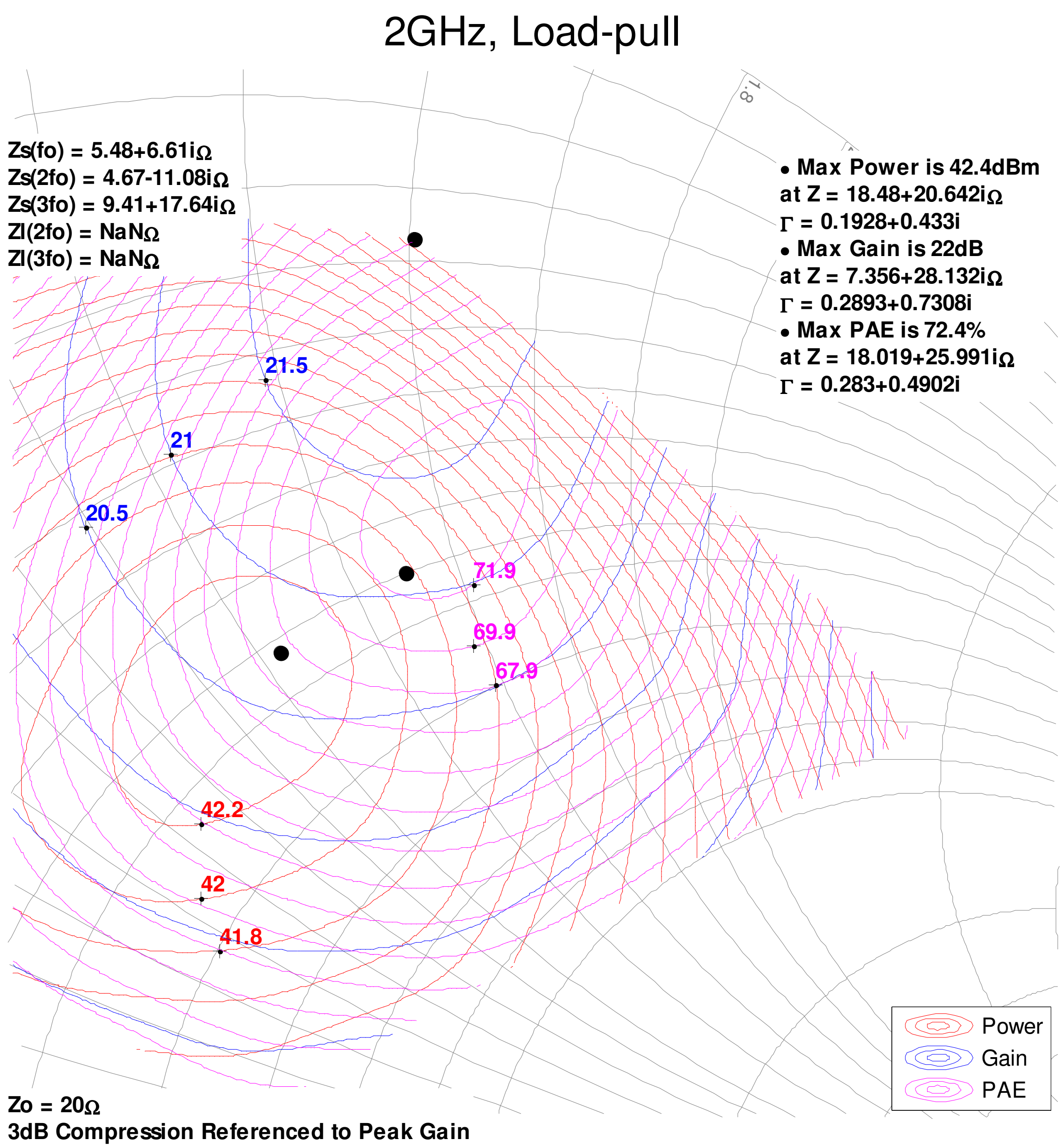

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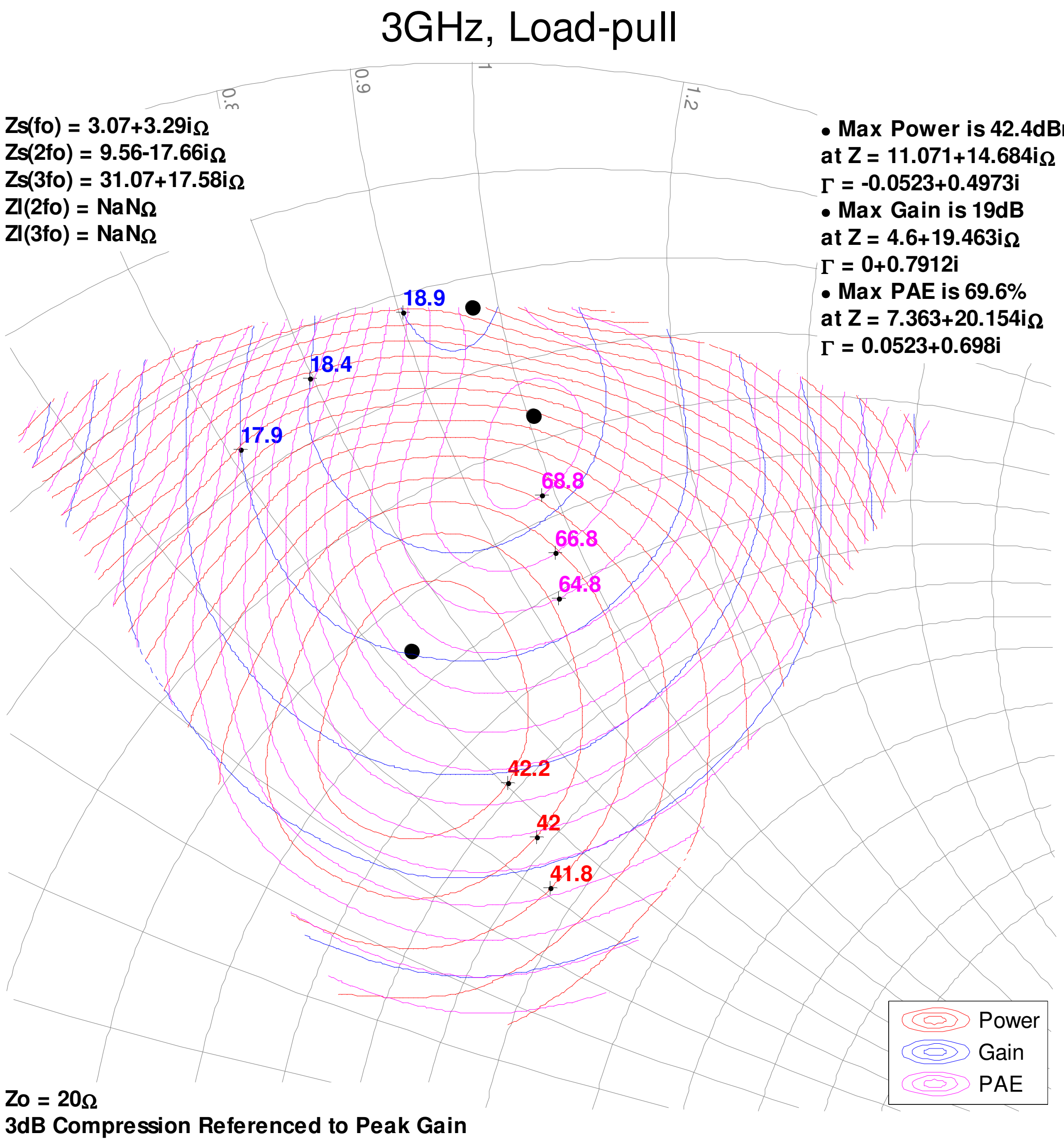

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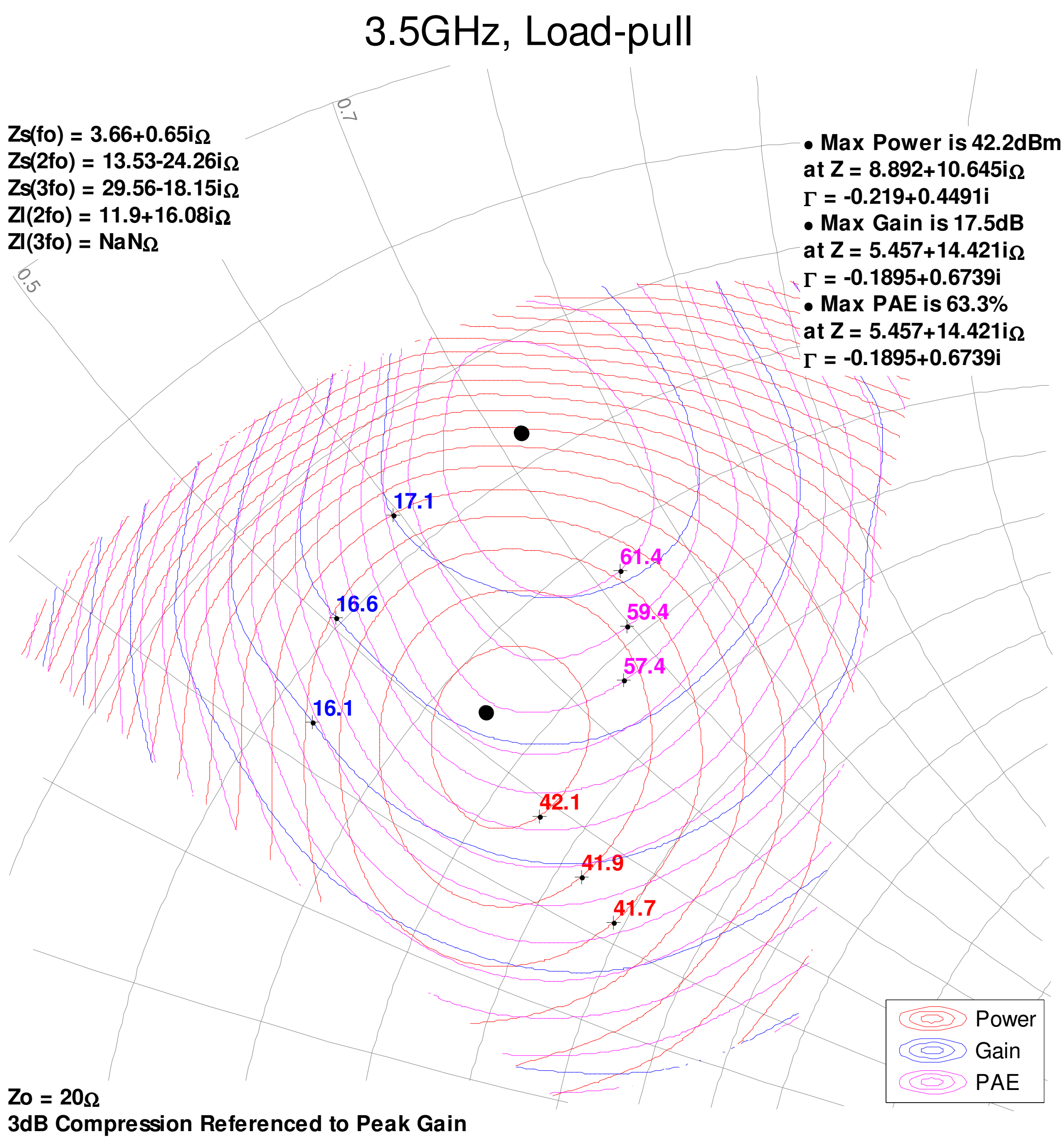

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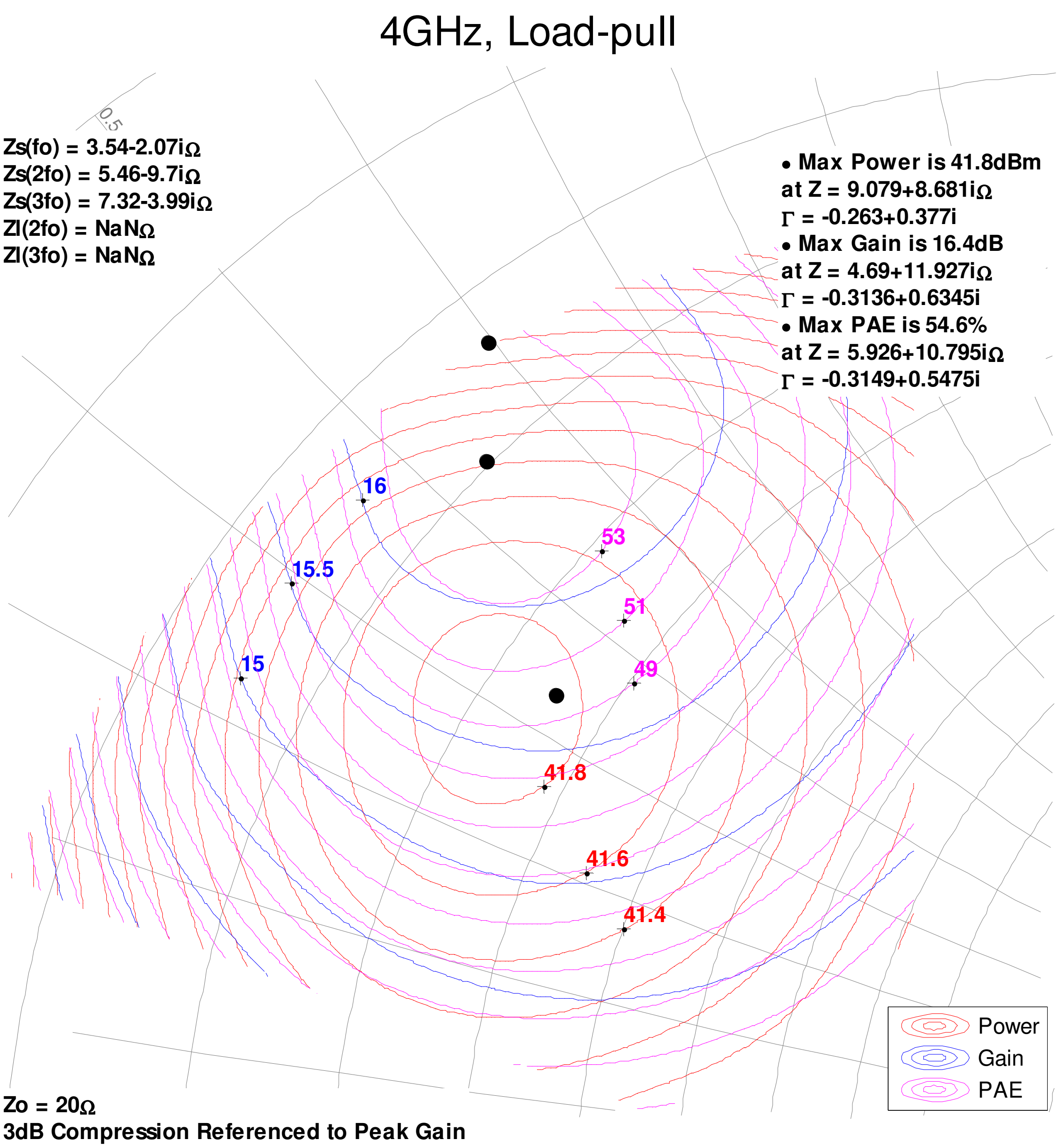
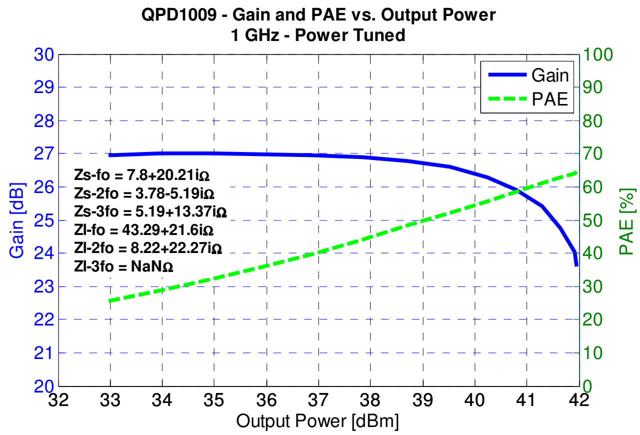
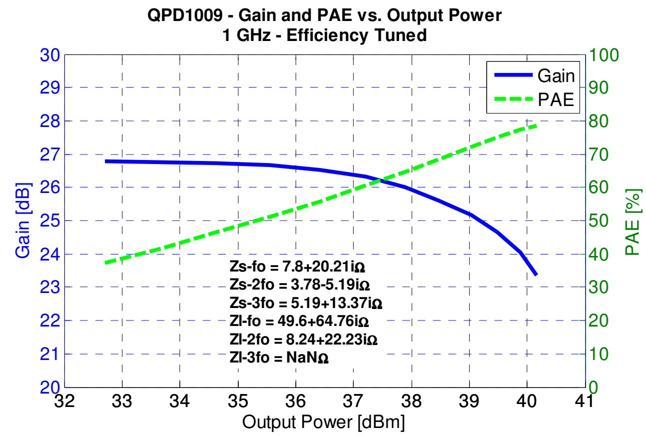
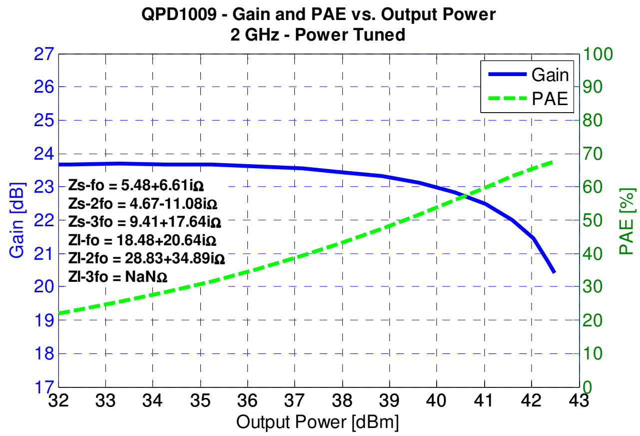


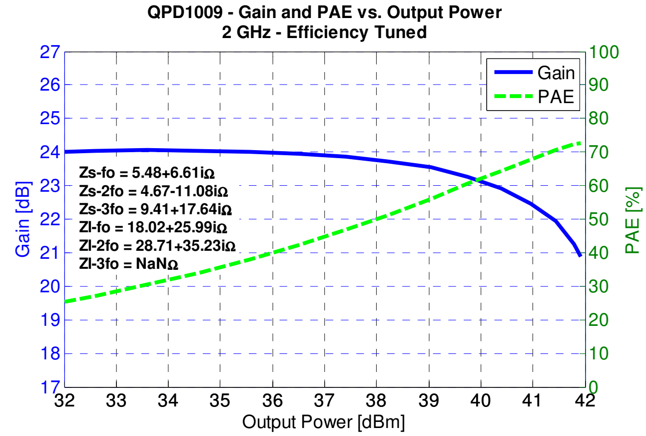
## Typical Performance – Load Pull Drive-up

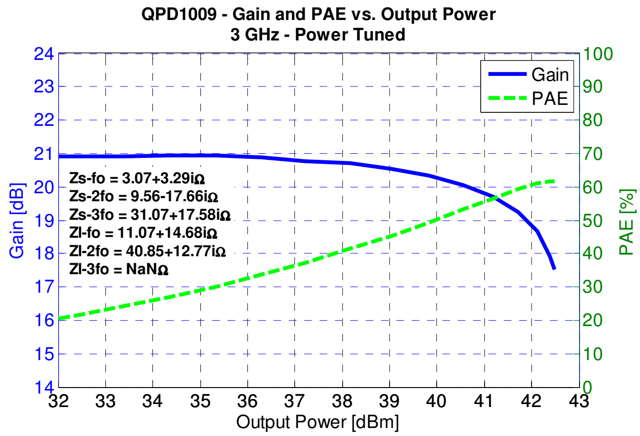
Notes:
1. Pulsed signal with 128 uS pulse width and 10 % duty cycle, Vd = 50 V, $I_{DQ}$ = 26 mA
2. See page 18 for load pull and source pull reference planes where the performance was measured.

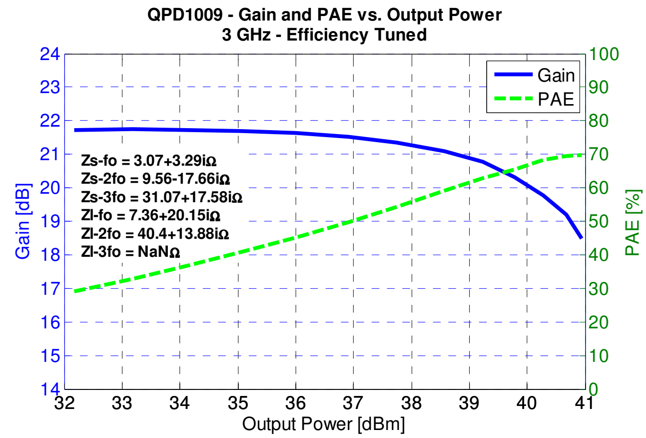


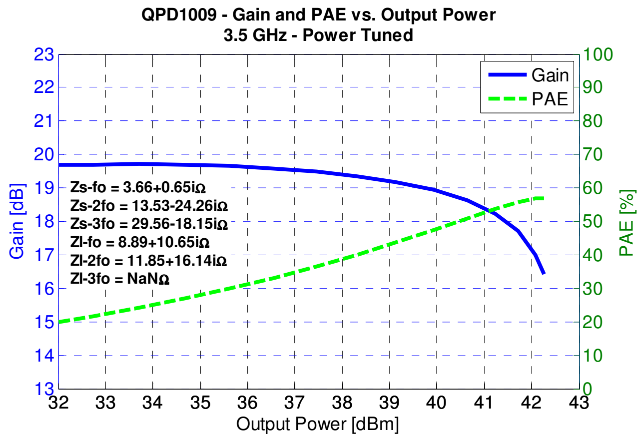



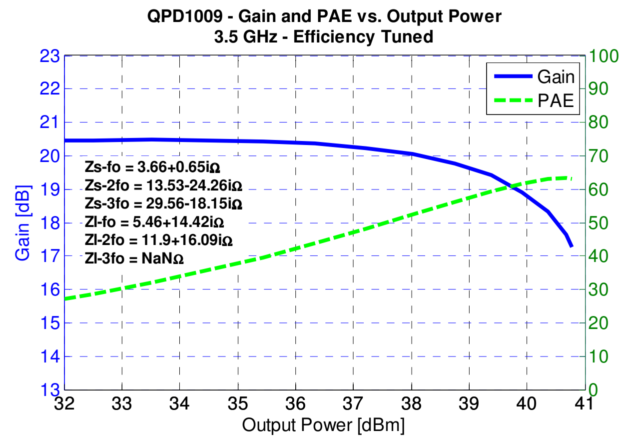



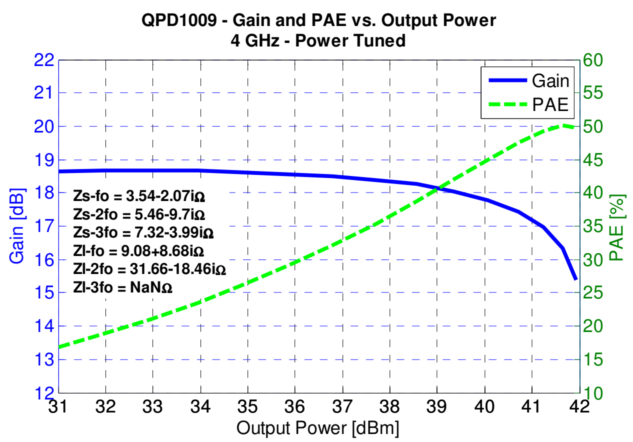



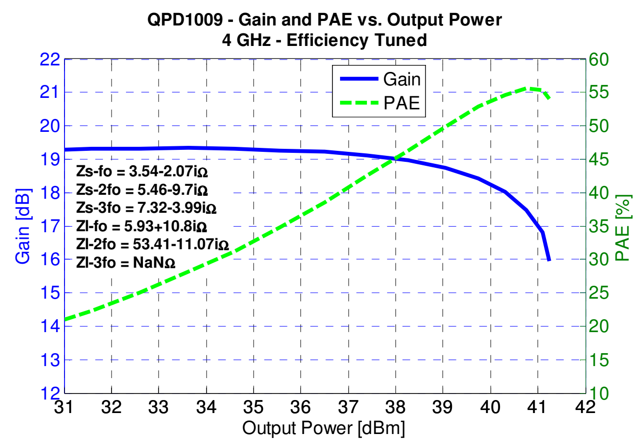
## Typical Performance – Load Pull Drive-up

Notes:
3. Pulsed signal with 128 uS pulse width and 10 % duty cycle, Vd = 50 V, $I_{DQ}$ = 26 mA
4. See page 18 for load pull and source pull reference planes where the performance was measured.



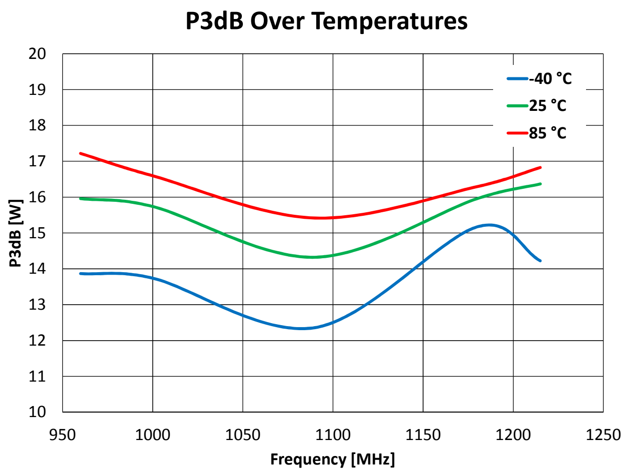



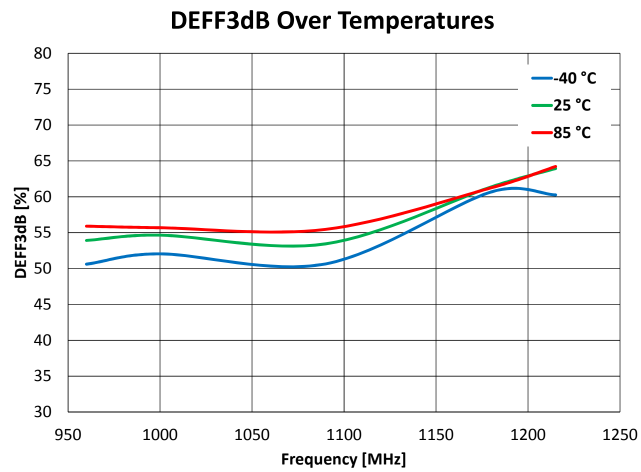



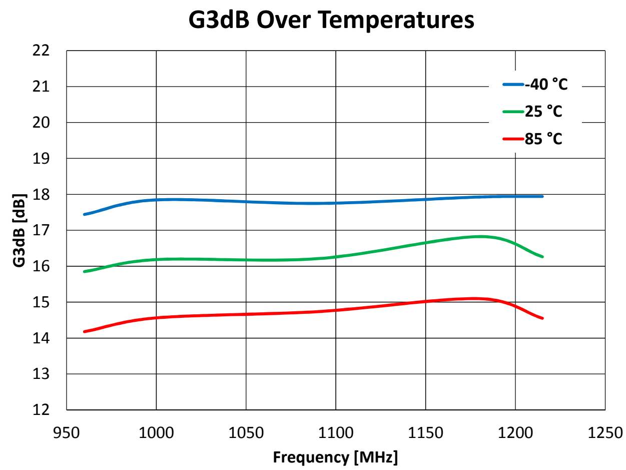



## Power Driveup Performance Over Temperatures Of 0.96 – 1.215 GHz EVB[1]

[1] Vd = 50 V, $I_{DQ}$ = 26 mA, Pulse Width = 128 uS, Duty Cycle = 10 %

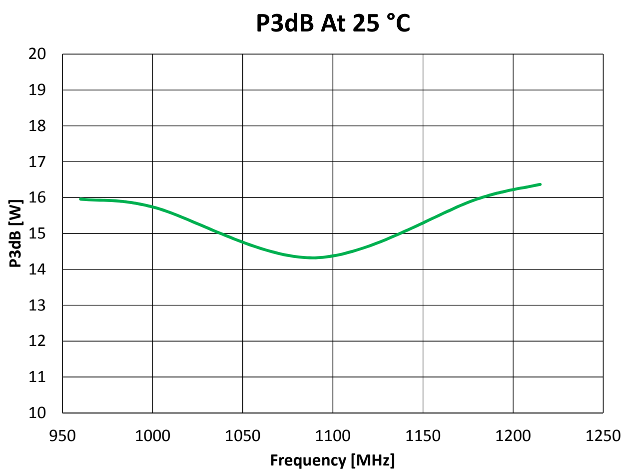


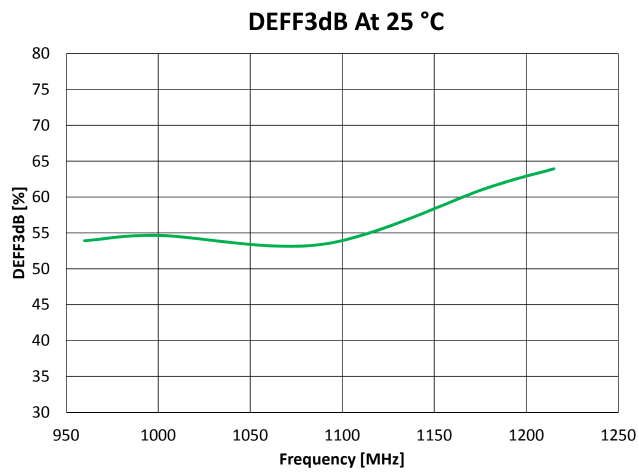



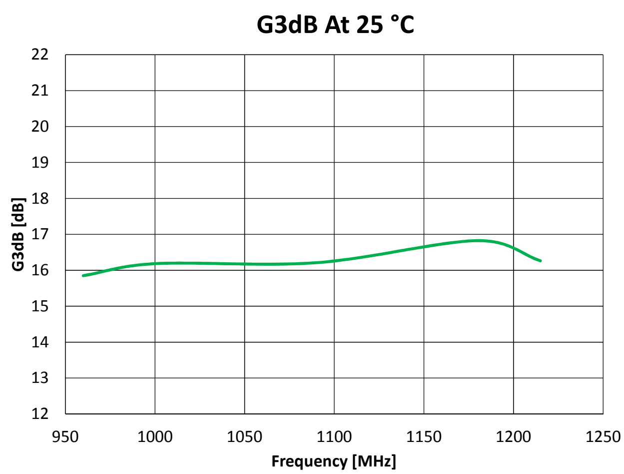



## Power Driveup Performance At 25 ℃ Of 0.96 – 1.215 GHz EVB[1]

[1] Vd = 50 V, $I_{DQ}$ = 26 mA, Pulse Width = 128 uS, Duty Cycle = 10 %

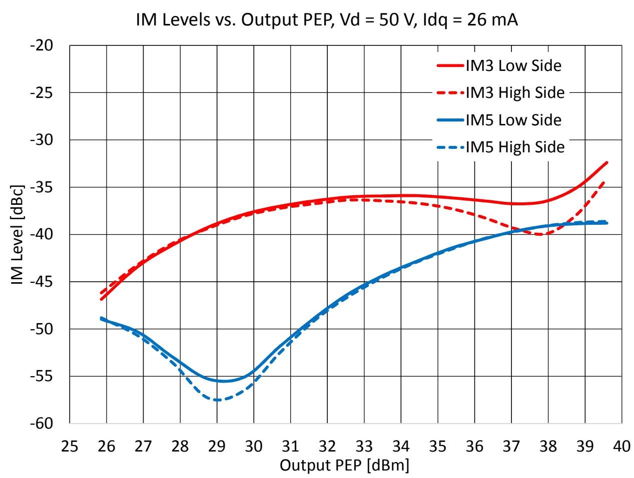


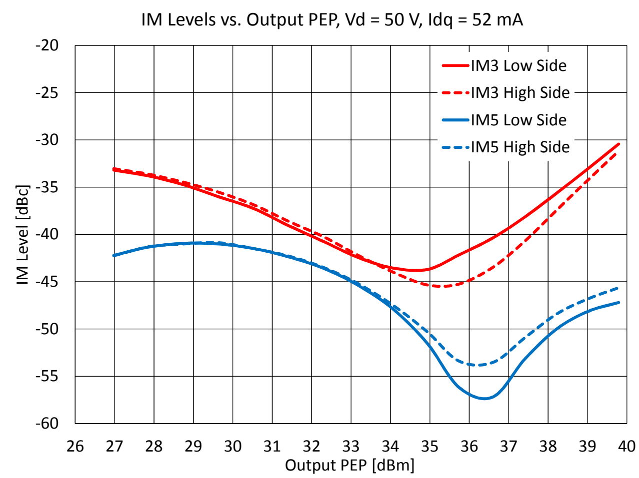



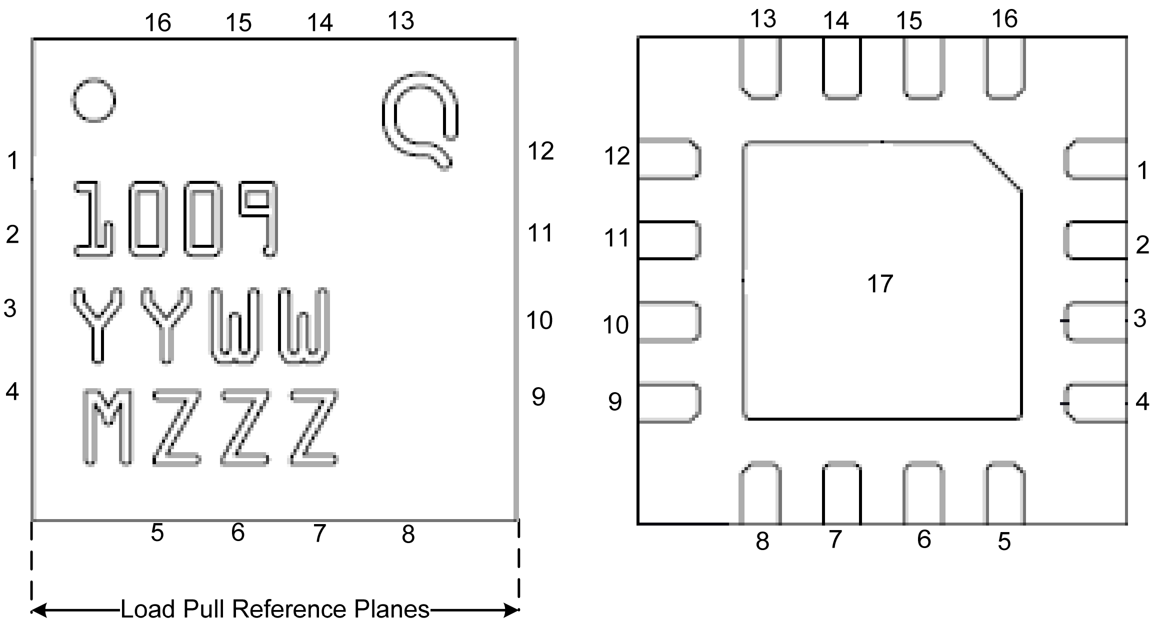
## Two-Tone Performance At 25 °C Of 0.96 – 1.215 GHz EVB[1]

[1] Center frequency = 1.09 GHz, Tone Separation = 1 MHz



## Pin Layout [1]

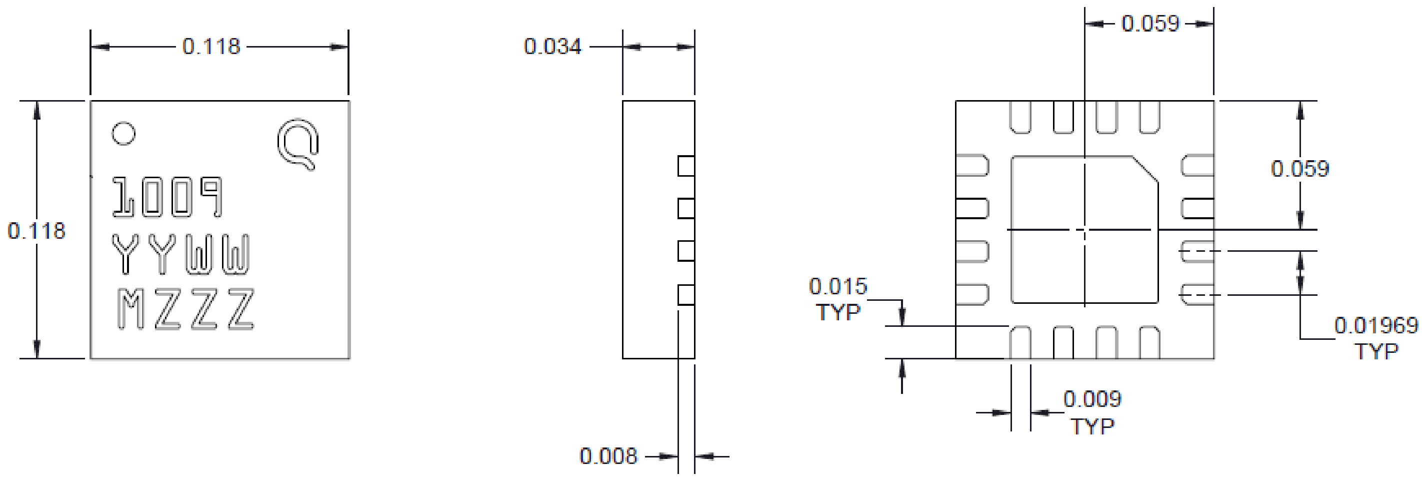



Notes:
1. The QPD1009 will be marked with the “1009” designator and a lot code marked below the part designator. The “YY” represents the last two digits of the calendar year the part was manufactured, the “WW” is the work week of the assembly lot start, the “MXXX” is the production lot number, and the “ZZZ” is an auto-generated serial number.

## Pin Description

| Pin | Symbol | Description |
|---|---|---|
| 2, 3 | VG / RF IN | Gate voltage / RF Input |
| 10, 11 | VD / RF OUT | Drain voltage / RF Output |
| 1, 4, 5 – 9, 12 - 16 | NC | Not Connected |
| 17 | Flange | Source to be connected to ground |

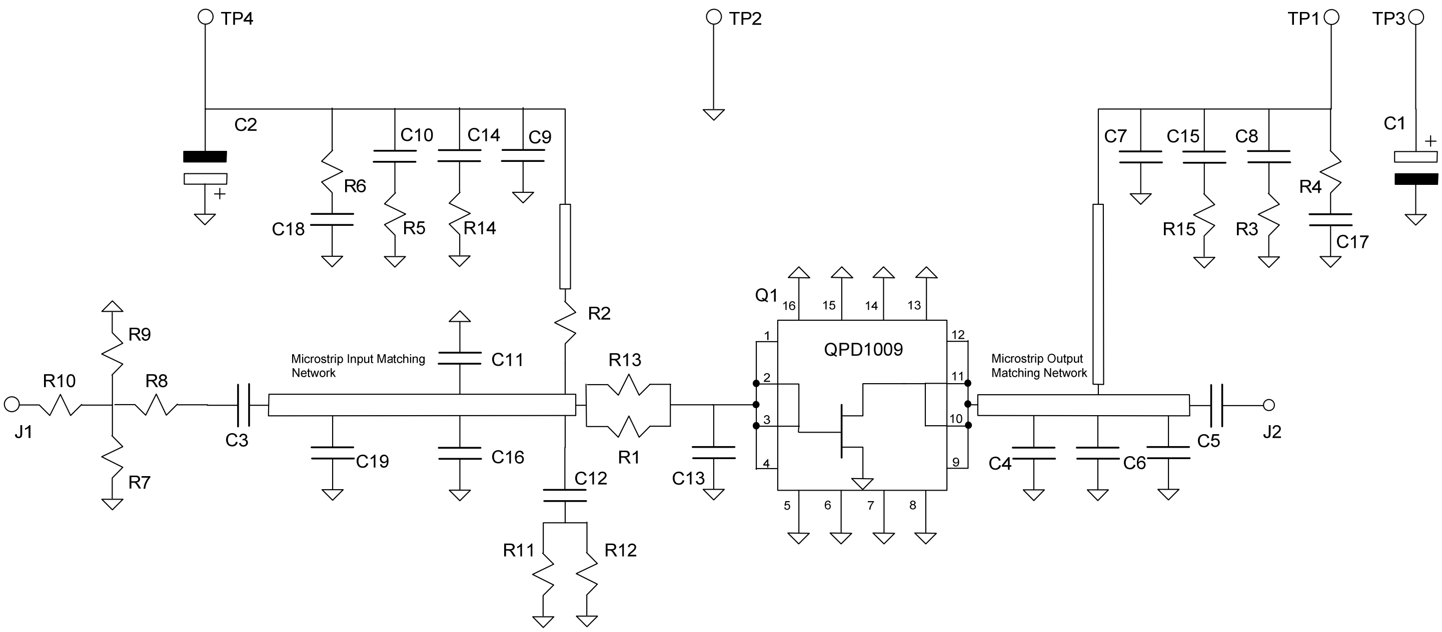
## Mechanical Drawing[1]




Notes:

1. All dimensions are in inches. Otherwise noted, the tolerance is ±0.005 inches.

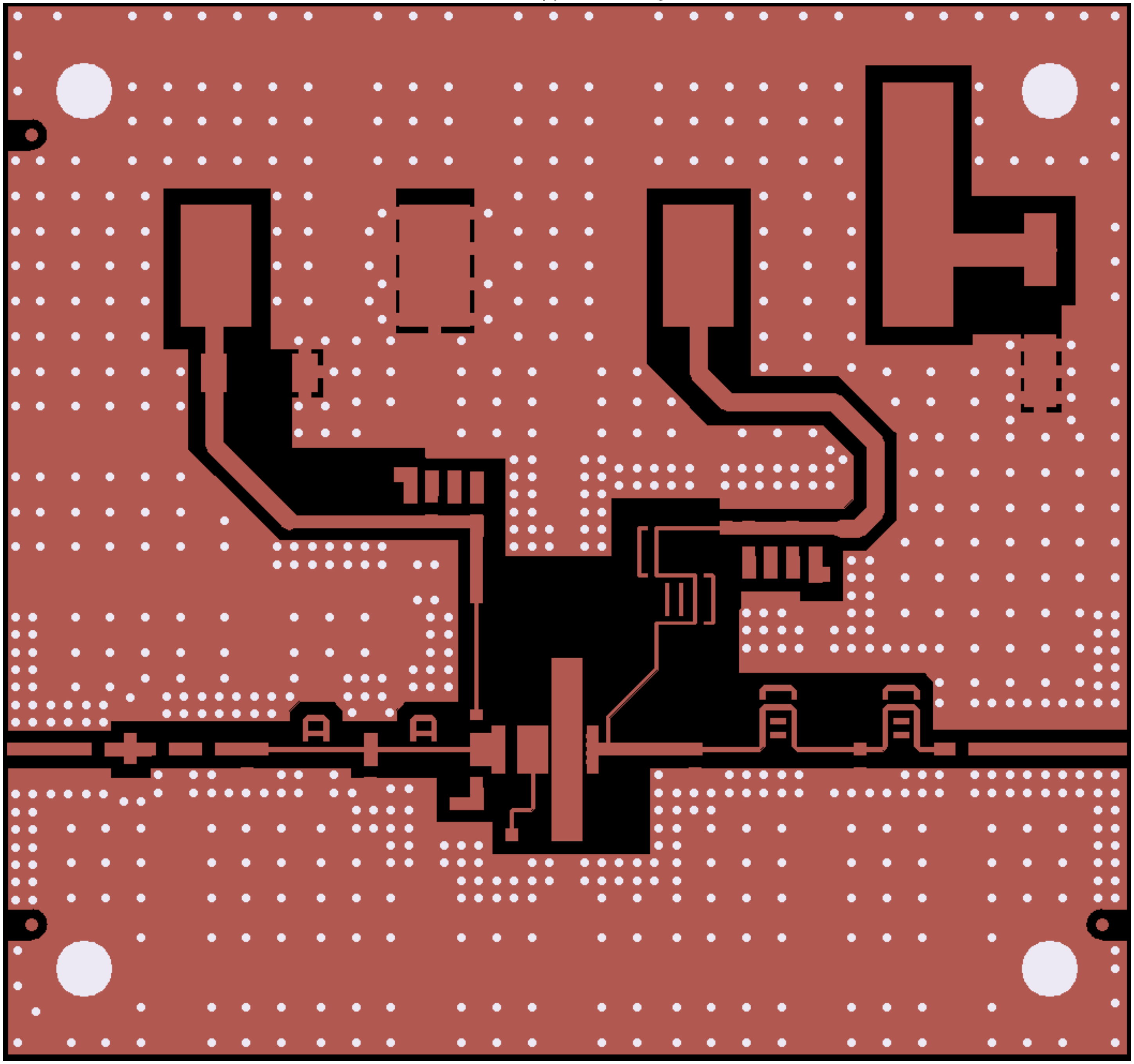
## Schematic - 0.96 – 1.215 GHz EVB



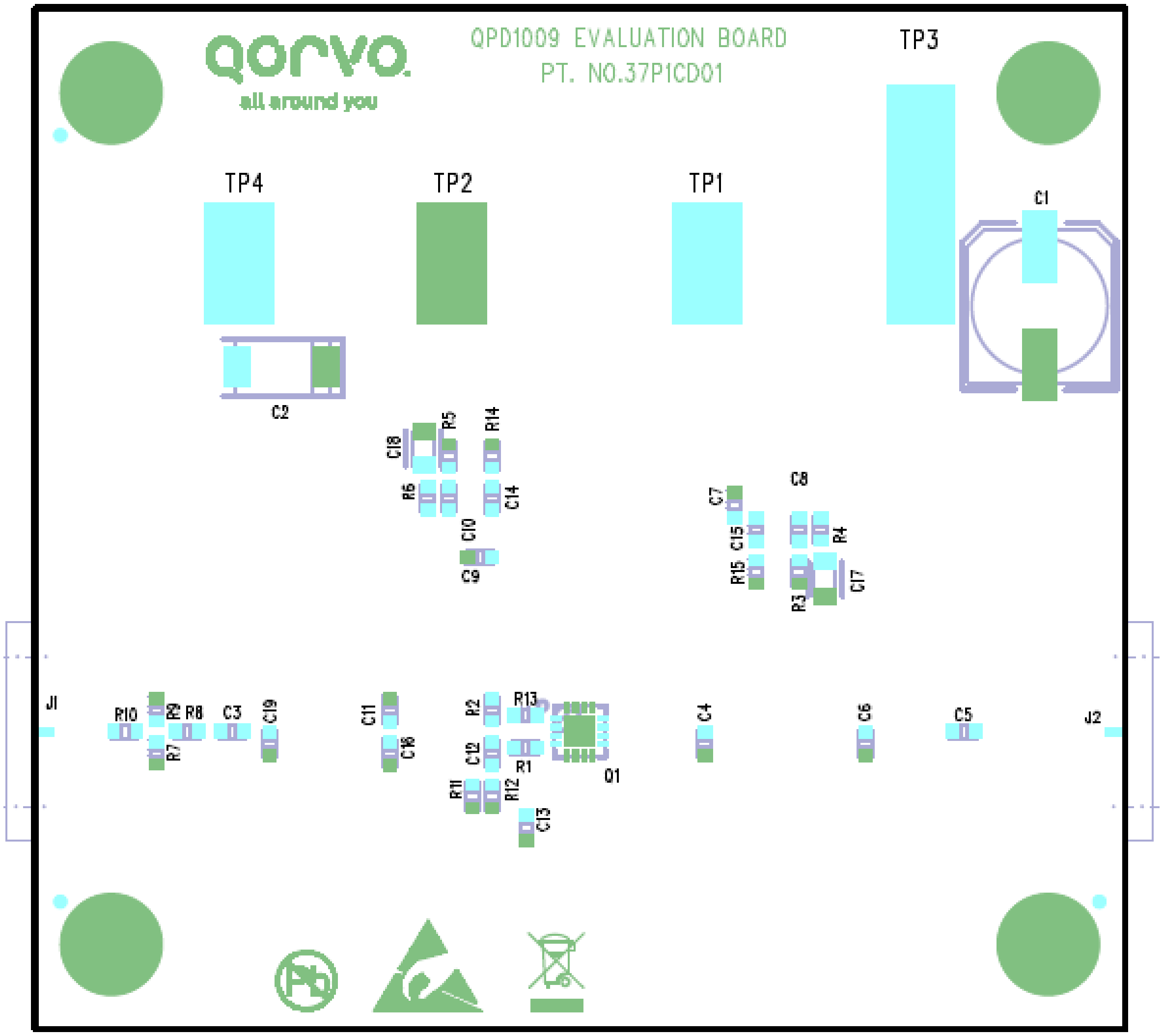

| Bias-up Procedure | Bias-down Procedure |
|---|---|
| 1. Set $V_G$ to -4 V. | 1. Turn off RF signal. |
| 2. Set $I_D$ current limit to 30 mA. | 2. Turn off $V_D$ |
| 3. Apply 50 V $V_D$. | 3. Wait 2 seconds to allow drain capacitor to discharge |
| 4. Slowly adjust $V_G$ until $I_D$ is set to 26 mA. | 4. Turn off $V_G$ |
| 5. Set $I_D$ current limit to 1.5 A | |
| 6. Apply RF. | |

## PCB Layout - 0.96 – 1.215 GHz EVB

Board material is RO4360G2 0.020” thickness with 1 oz copper cladding.



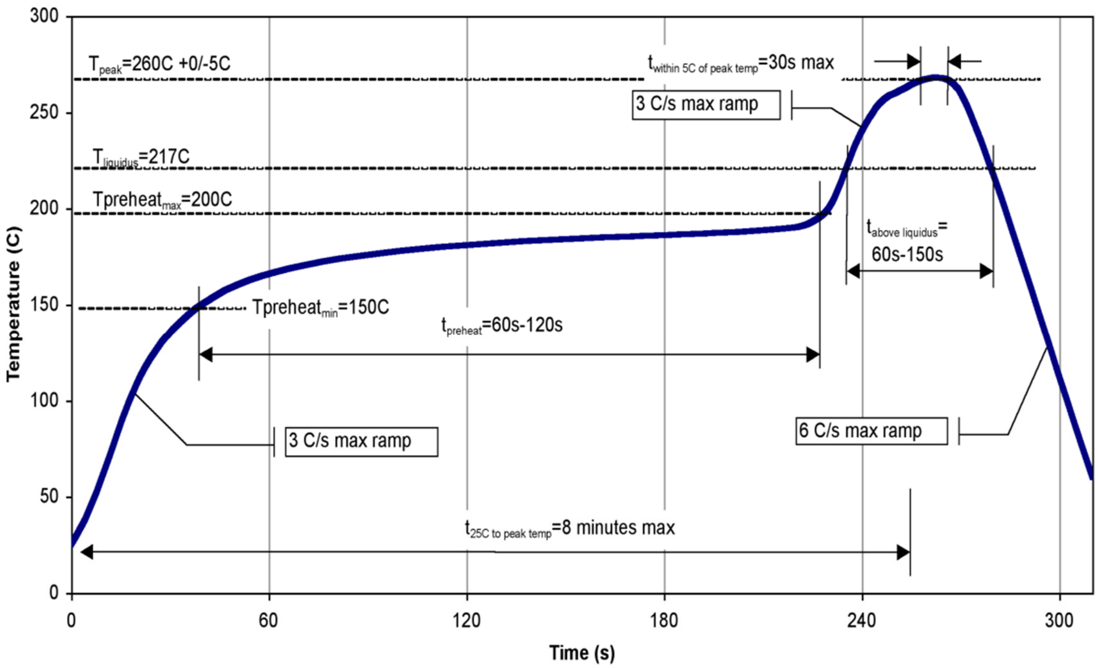
## Component Placement - 0.96 – 1.215 GHz EVB



## Bill Of material - 0.96 – 1.215 GHz EVB

| Ref Des | Value | Description | Manufacturer | Part Number |
|---|---|---|---|---|
| C14, 15 | 100 pF | C0G 100V 5% 0603 Capacitor | AVX | 06031A101JAT2A |
| C8 - 10 | 1 nF | X7R 100V 5% 0603 Capacitor | AVX | 06031C102JAT2A |
| C17 - 18 | 100 nF | X7R 100V 5% 0805 Capacitor | AVX | 08051C104JAT2A |
| C4 | 0.2 pF | RF NPO 250VDC ± 0.05 pF Capacitor | ATC | ATC600S0R2AT250X |
| C13 | 1.0 pF | RF NPO 250VDC ± 0.05 pF Capacitor | ATC | ATC600S1R0AT250X |
| C6 | 1.5 pF | RF NPO 250VDC ± 0.05 pF Capacitor | ATC | ATC600S1R5AT250X |
| C19 | 6.8 pF | RF NPO 250VDC ± 0.1 pF Capacitor | ATC | ATC600S6R8BT250X |
| C11, 16 | 7.5 pF | RF NPO 250VDC ± 0.1 pF Capacitor | ATC | ATC600S7R5BT250X |
| C3, 5, 7, 9, 12 | 56 pF | RF NPO 250VDC 1% Capacitor | ATC | ATC600S5650FT250X |
| C1 | 33 uF | 80V SVP Capacitor | Panasonic | EEEFK1K330P |
| C2 | 10 uF | 16V Tantalum Capacitor | AVX | TPSC106KR0500 |
| J1 - 2 | | SMA Panel Mount 4-hole Jack | Gigalane | PSF-S00-000 |
| R4, 6 | 1 Ohm | 0603 1% Thick Film Resistor | ANY | |
| R1, 2, 8, 10, 13, 14, 15 | 5.1 Ohm | 0603 1% Thick Film Resistor | ANY | |
| R3, 5 | 33 Ohm | 0603 1% Thick Film Resistor | ANY | |
| R11, 12 | 150 Ohm | 0603 1% Thick Film Resistor | ANY | |
| R7, 9 | 430 Ohm | 0603 1% Thick Film Resistor | ANY | |

## Recommended Solder Temperature Profile



## Product Compliance Information

### ESD Sensitivity Ratings

Caution! ESD Sensitive Device

### ESD Rating

| | |
|---|---|
| ESD Rating: | TBD |
| Value: | TBD |
| Test: | Human Body Model (HBM) |
| Standard: | JEDEC Standard JESD22-A114 |

### MSL Rating

| | |
|---|---|
| MSL Rating: | TBD |
| Test: | 260 °C convection reflow |
| Standard: | JEDEC Standard IPC/JEDEC J-STD-020 |

### Solderability

Compatible with lead free soldering processes, 260 °C maximum reflow temperature.

Package lead plating: NiAu

The use of no-clean solder to avoid washing after soldering is recommended.

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Qorvo:

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