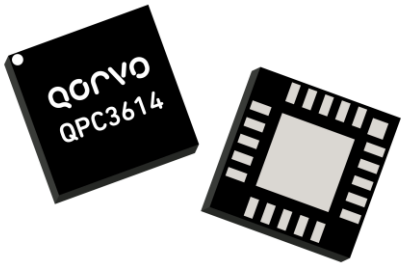
# QPC3614

## 75Ω 5 −1500MHz Digital Step Attenuator

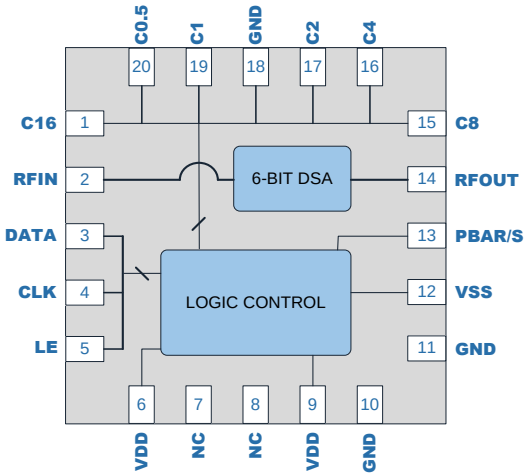
## Product Overview

The QPC3614 is a 75Ω 6-bit digital step attenuator (DSA) that features high linearity over the entire 31.5 dB gain control range in 0.5 dB steps and has a low insertion loss of 1.2dB at 1 GHz. The QPC3614 features three modes of control: serial, latched parallel, and direct parallel programming. Patented circuit architecture provides overshoot-free transient switching performance. QPC3614 is available in a 20-pin 4.2mm x 4.2mm x 0.90mm QFN package.




20 Pin 4.2 x 4.2mm QFN Package

## Functional Block Diagram




Top View

## Key Features

- 6-Bit, 31.5dB Range, 0.5dB Step
- Patented Circuit Architecture
- Overshoot-free Transient Switching Performance
- Frequency Range 5MHz to 1500MHz
- High Linearity, IIP3 65dBm Typical at 1GHz
- Serial and Parallel Control Interface
- Fast Switching Speed, <500nsec Typical
- RF Pads Have No DC Voltage; Can be DC Grounded Externally
- Option to Turn Off Negative Voltage Generator and Supply $V_{SS}$ Externally
- Power-up Default Setting Is Maximum Attenuation

## Applications

- Optical Nodes
- Point-to-Point
- MDU Amplifiers
- Pre-amplifier Attenuation
- Inter-stage Attenuation
- Return Attenuation
- AGC
- Tilt Control

## Ordering Information

| Part No. | Description |
|---|---|
| QPC3614SQ | Sample bag with 25 pieces |
| QPC3614SR | 7" Reel with 100 pieces |
| QPC3614TR13 | 13" Reel with 2500 pieces |
| QPC3614PCK | 5 - 1500 MHz PCBA with 5 pc. sample bag |

## Absolute Maximum Ratings

| Parameter | Rating |
|---|---|
| Supply Voltage ($V_{DD}$) | -0.5 to + 6.0V |
| Supply Voltage ($V_{SS}$) | -6.0 to + 0.5V |
| All Other DC and Logic Pads (Supply Voltage Must Be Applied Prior to Any Other Pin Voltage) | -0.5 to VDD |
| Maximum Input Power at RFIN Pad at 85 °C Case Temperature | +30dBm |
| Maximum Input Power at RFOUT Pad at 85 °C Case Temperature | +27dBm |
| Storage Temperature Range | -40 to +150°C |

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

## Recommended Operating Conditions

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Supply Voltage, $V_{DD}$ | +2.7 | +5.0 | +5.5 | V |
| Supply Voltage, $V_{SS}$ | -5.5 | -5.0 | -4.5 | V |
| Temperature Range | -40 | | +85 | °C |
| Junction Temperature | | | +125 | °C |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

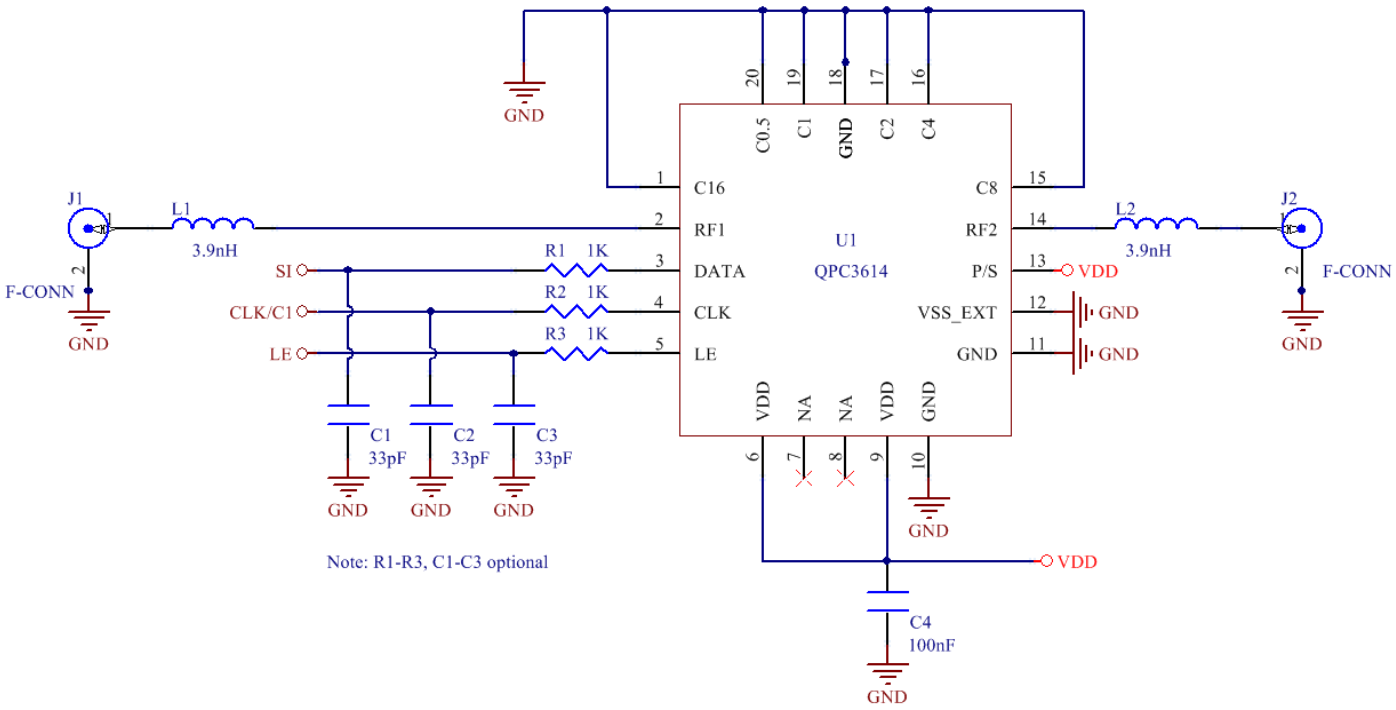
## Electrical Specifications

| Parameter | Condition (1) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Current ($I_{DD}$) | Steady state operation, current draw during attenuation state transitions is higher. | | 190 | | µA |
| Supply Current ($I_{SS}$) | Steady state operation, current draw during attenuation state transitions is higher. | | 110 | | µA |
| Frequency Range | | 5 | | 1500 | MHz |
| Insertion Loss | 1GHz | | 1.2 | | |
| Maximum Attenuation | | | 31.5 | | dB |
| Absolute Attenuation Error | | | ±(0.2 + 4%) | | dB |
| Input IP3 | 1GHz, Two tones, 13dBm/tone | | 65 | | dBm |
| Input P0.1dB(2) | | | 30 | | dBm |
| MER | 75dBmV composite, 885MHz | | 40 | | dB |
| CCN | 75dBmV composite, 885MHz | | 49 | | dB |
| Return Loss | 5MHz – 1200MHz, all states | | 18 | | dB |
| Input and Output Impedance | | | 75 | | Ω |
| Switching Speed | 50% control to 10% / 90% RF | | 150 | | nsec |
| Digital Logic Low | | | | 0.63 | V |
| Digital Logic High | | 1.17 | | | V |
| Thermal Resistance, θjc | Junction to case | | 67 | | °C/W |

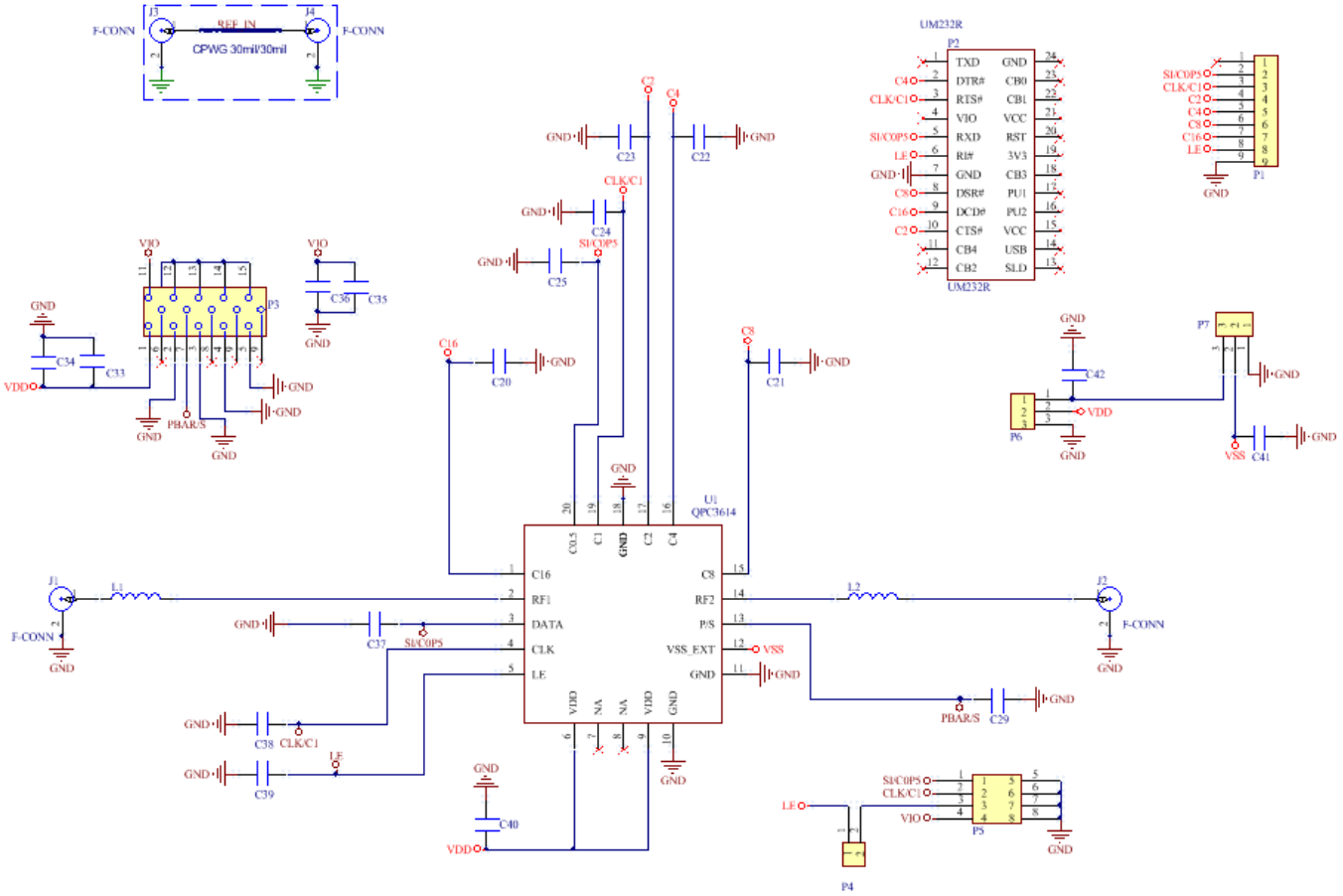
Notes:

1. Typical performance at these conditions: Temp = +25°C, 1000MHz, $V_{DD}$ = +5V, $V_{SS}$ = 0V, 75Ω system.
2. Figure of merit – exceeds maximum input power of device.
3. MER Test Conditions: 190 QAM256 Channels, 57-1215MHz, ITU-T J.83, Annex B
4. CCN test procedure according to ANSI/SCTE 17. System BW 5.36MHz.

## Typical Application Schematic – Serial Mode; 5 − 1500MHz



## Evaluation Board Schematic; 5 – 1500MHz

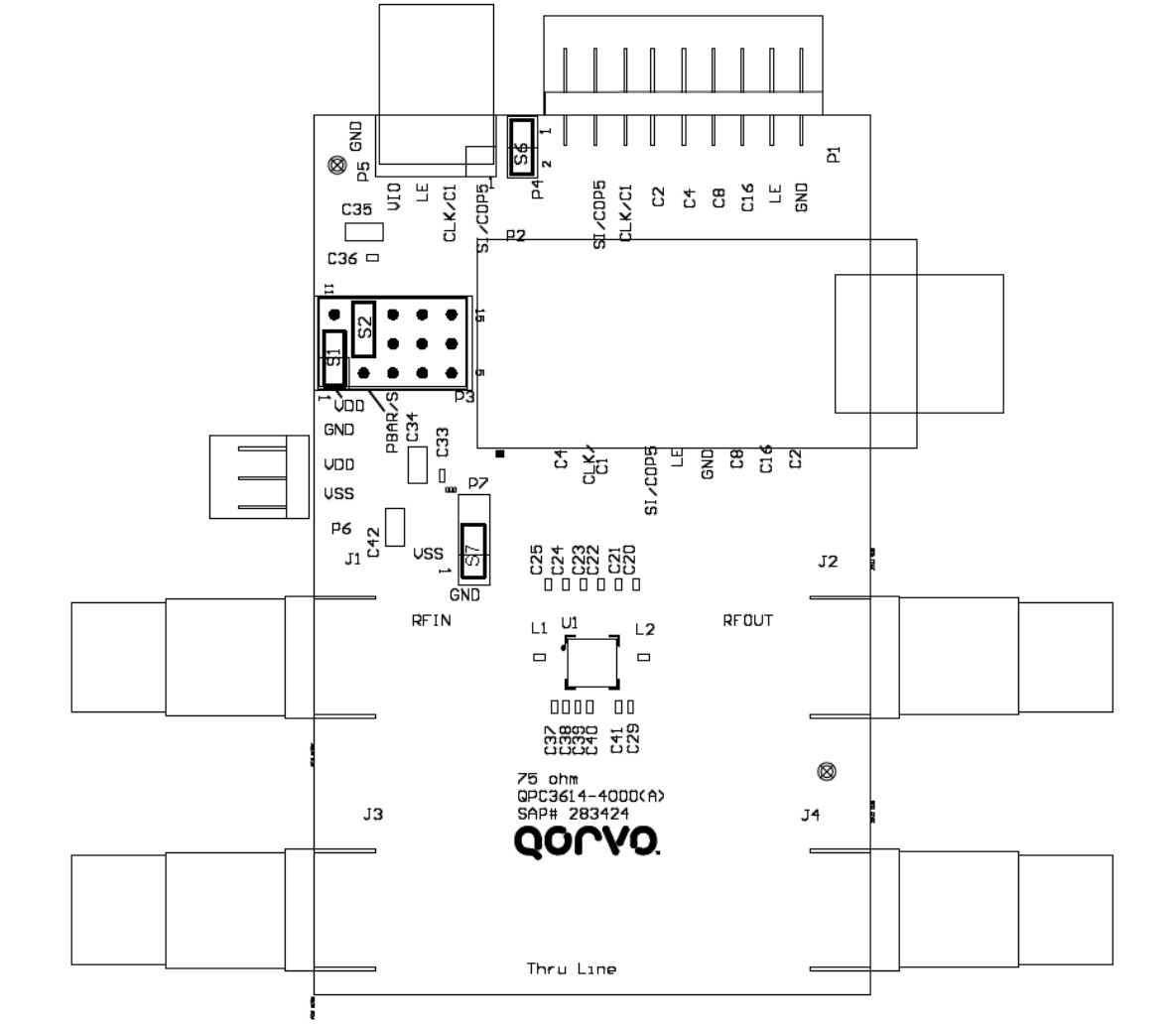


| Ref. Designator | Description | Manufacturer | Part Number |
|---|---|---|---|
| PCB | QPC3614−4000 | Viasystems | QPC3614-4000(A) |
| U1 | Digital Step Attenuator, 5 MHz to 1500 MHz | Qorvo | QPC3614SB |
| C34, C42 | CAP, 1 µF, 10%, 25 V, X7R, 1206 | Taiyo Yuden (USA), Inc. | CE TMK316BJ105KL-T |
| J1 - J4 | CONN, F FEM, EDGE MOUNT, 75 Ω, 0.065” | Genesis Technology USA | GT20-300204 |
| P1 | CONN, HDR, ST, 9-PIN, 0.100” | Samtec Inc. | TSW-109-07-G-S |
| P3 | CONN, HDR, ST, 3 x 5, 0.100”, T/H | Samtec Inc. | TSW-105-07-L-T |
| P4 | CONN, HDR, ST, 2-PIN, 0.100” | Samtec Inc. | TSW-102-07-G-S |
| P5 | CONN, HDR, 2 x 4, RA, 0.100”, T/H | Samtec Inc. | TSW-104-08-G-D-RA |
| P2 | CONN, SKT, 24-PIN DIP, 0.600”, T/H | Aries Electronics Inc. | 24-6518-10 |
| P6 | CONN. HDR, SRT, PLRZD, 3-PIN, 0.100” | ITW Pancon | MPSS100-3-C |
| P7 | CONN, HDR, ST, 2-PIN, 0.100” | Samtec Inc. | TSW-102-07-G-S |
| M1 (See Note 1) | MOD, USB TO SERIAL UART, SSOP-28 | Future Technology Devices Int’l | UM232R |
| S1, S2, S7 | JMPR, 2-PIN | 3M Interconnect Solutions | 929950-00 |
| C40, C41 | CAP, 1000pF, 10%, 50V, X8L, 0402 | Murata Electronics | GCM155L81H102KA37D |
| L1, L2 | IND, 3.9nH, +/-0.3nH, M/L, 0402 | Murata Electronics | LQG15HN3N9S02D |
| C20 - C25, C29, C33, C35 - C39, S6 | DNP | N/A | N/A |

Notes:

1. M1 should be mounted into P2 with respect to the Pin 1 alignment of M1 and P2.
2. Jumpers S1 and S2 should be installed on P3. Jumper S6 is DNP.
3. Jumper S7 should be installed on P7.

## Evaluation Board Assembly Drawing

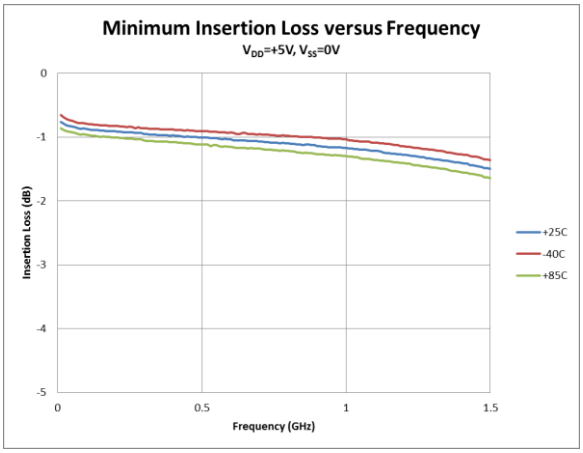


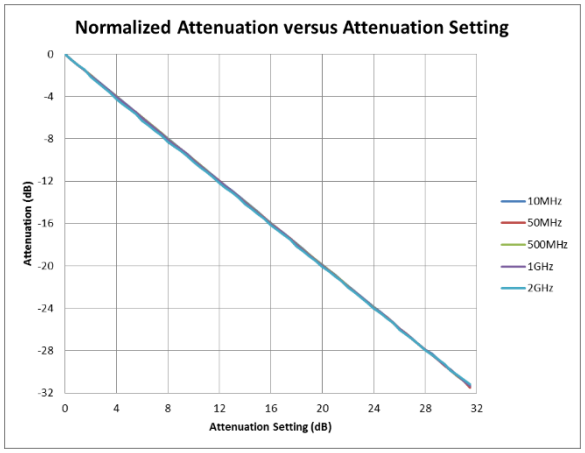

## On Board Jumpers

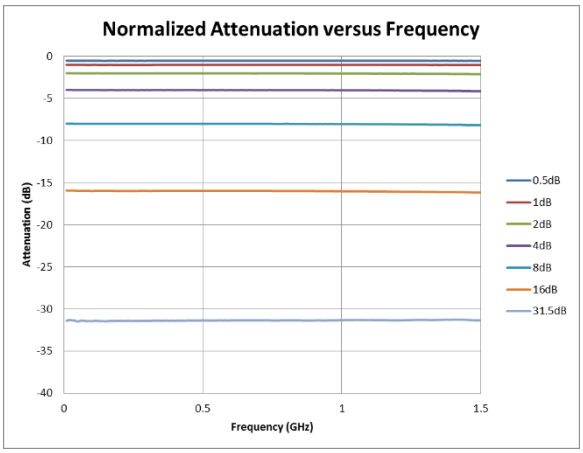
| Jumpers | Connector | Signal | Position | U1 Connection | Comment |
|---|---|---|---|---|---|
| S1 | P3 | Logic Voltage | 0 (Default) | VDD From P6 | |
| | | | 1 | VIO From P5 | |
| S2 | | PBar/S | 0 | GND | Parallel Mode |
| | | | 1 (Default) | U1_VDD | Serial Mode |
| S6 | P4 | LE | OPEN (Default) | LE (from UM232R) | Only install for external SPI control through P5 |
| | | | INSTALLED | LE (from P5.3) | |
| S7 | P7 | VSS | 0 (Default) | VSS to GND | Use to tie VSS to Ground to enable internal NVG or connect to P6 for external negative supply. |
| | | | 1 | VSS From P6 | |

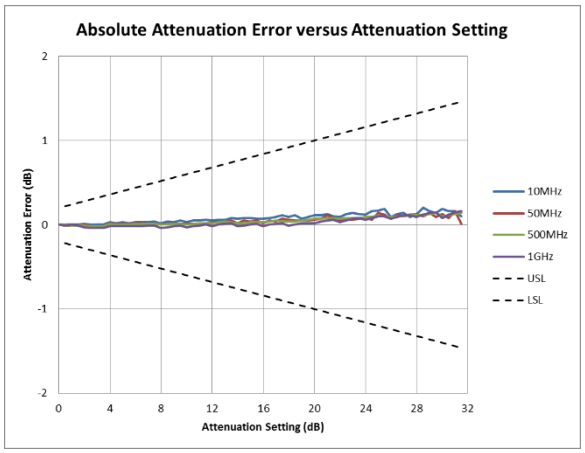
## Performance Plots

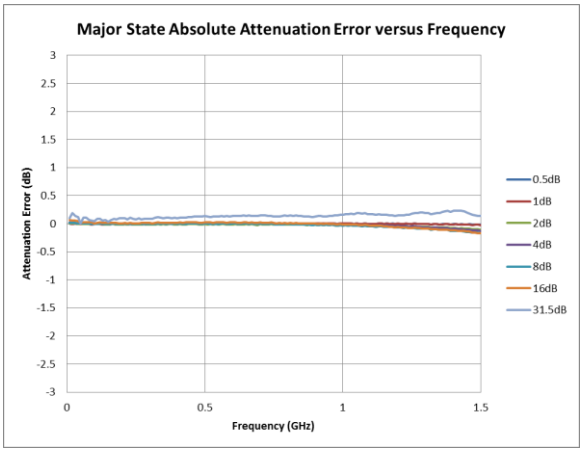
Test conditions unless otherwise noted: $V_{DD}$ =+5V, $V_{SS}$ = 0V, Temp= +25°C, $Z_o$ = 75Ω

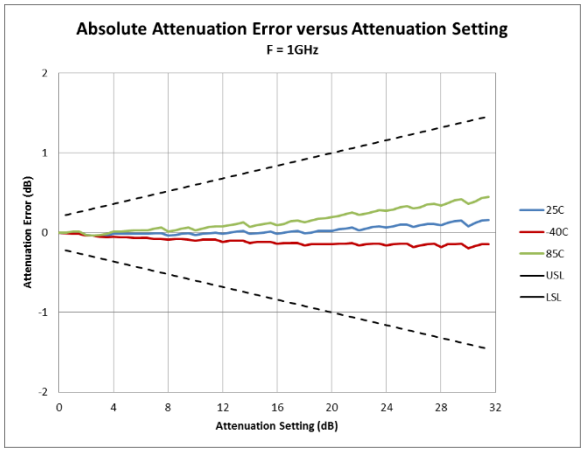


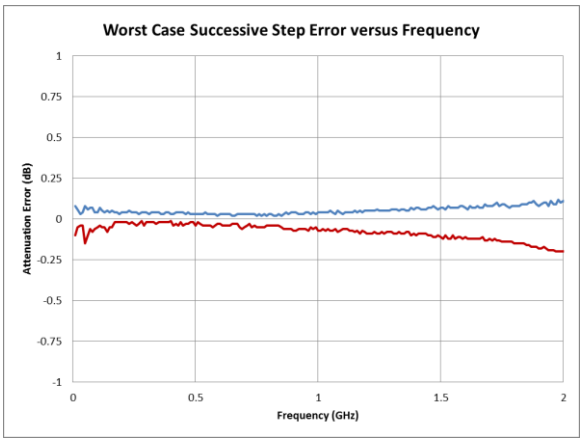



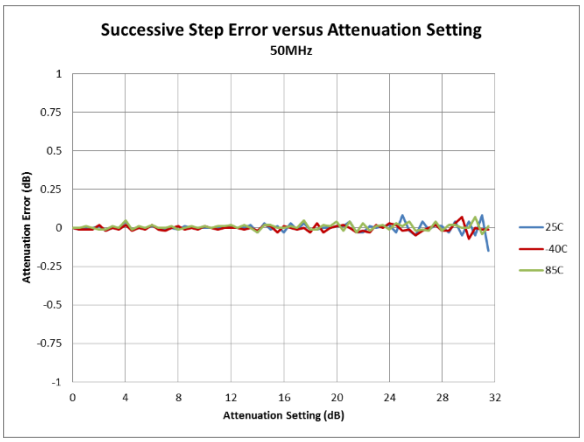



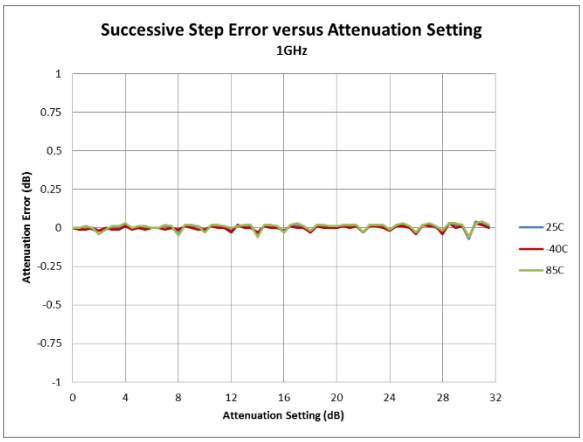



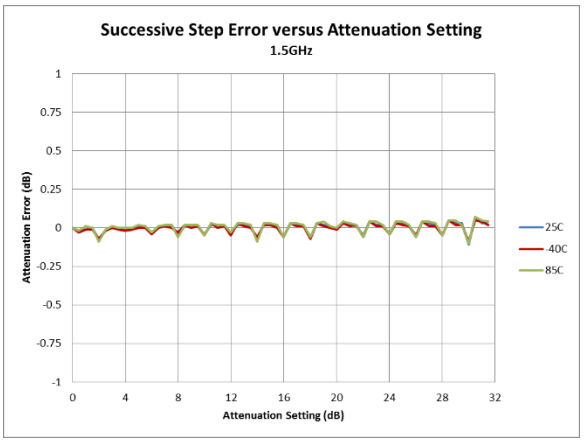
## Performance Plots (cont'd.)

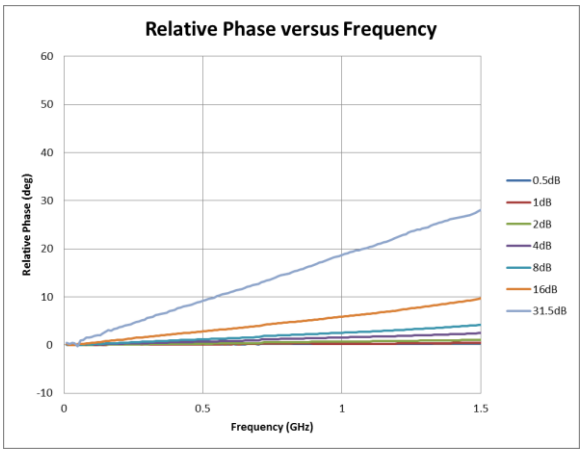
Test conditions unless otherwise noted: $V_{DD}$ =+5V, $V_{SS}$= 0V Temp= +25°C, $Z_o$ = 75Ω

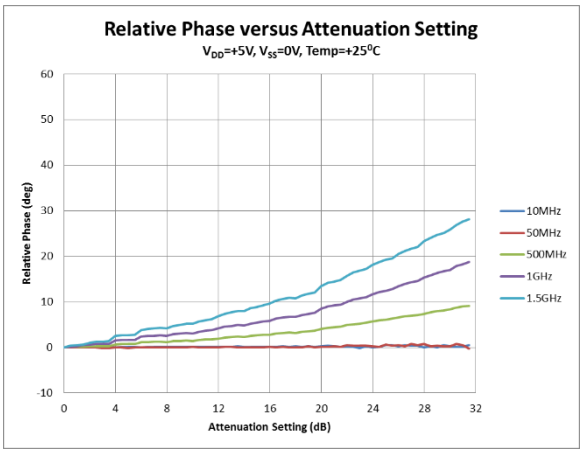


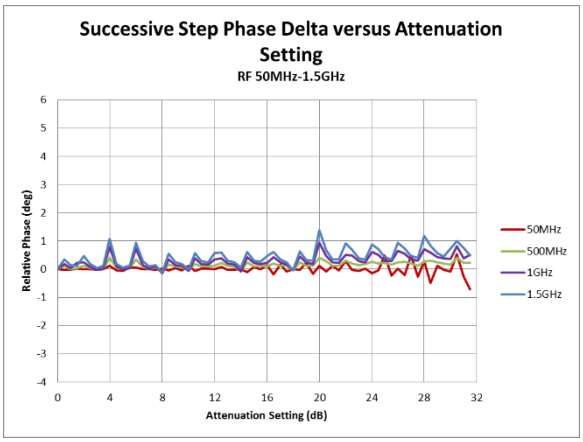



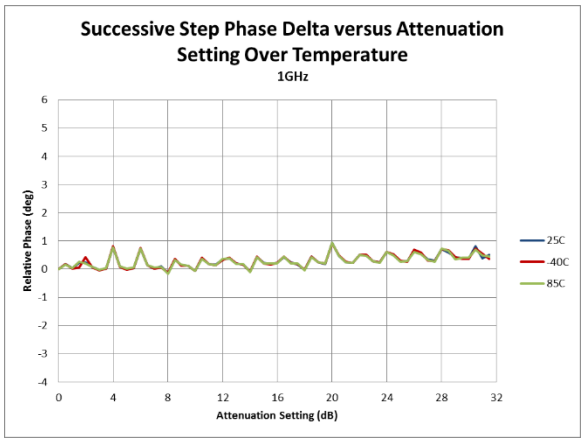



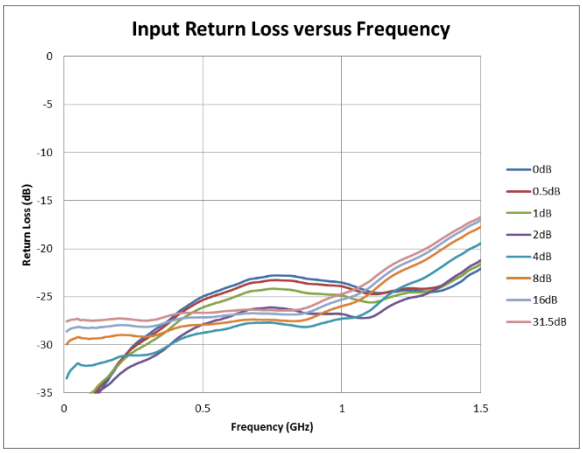



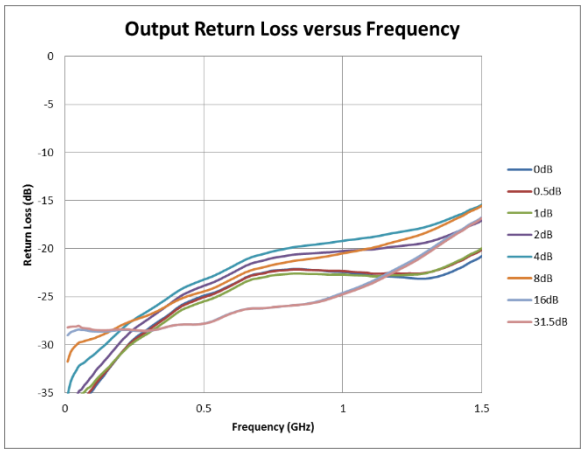
## Performance Plots (cont'd.)

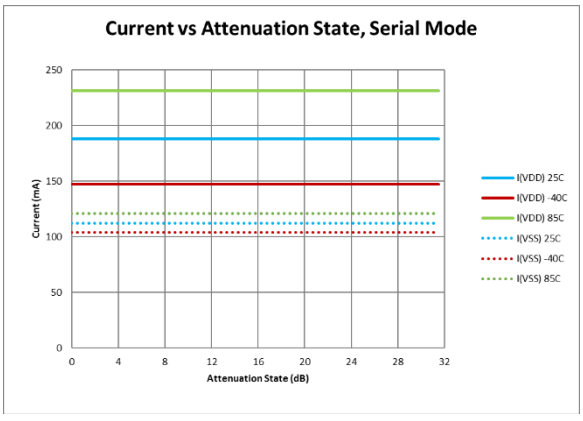
Test conditions unless otherwise noted: $V_{DD}$ =+5V, $V_{SS}$= 0V Temp= +25°C, $Z_o$ = 75Ω

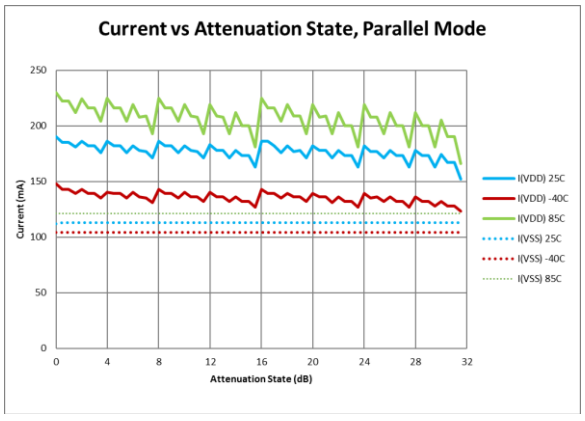


## Performance Plots (cont'd.)

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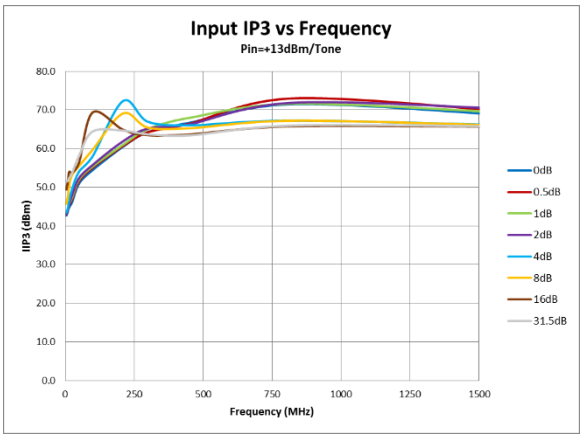
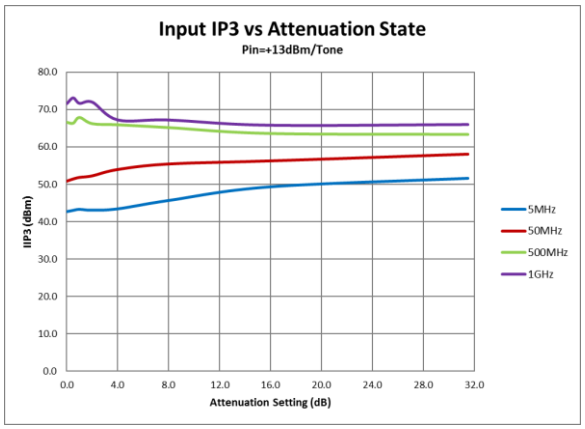
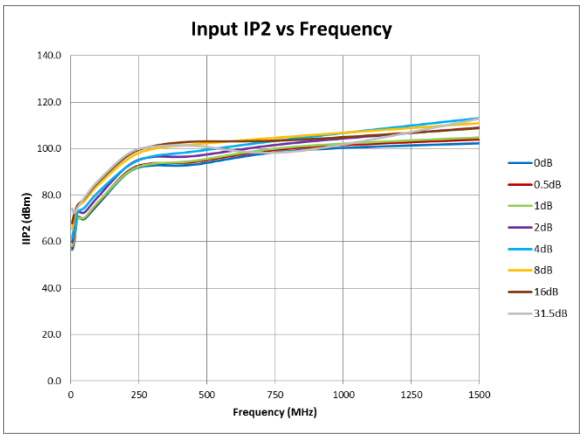
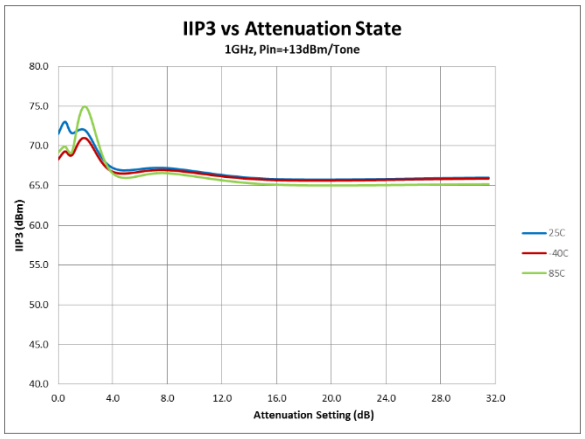
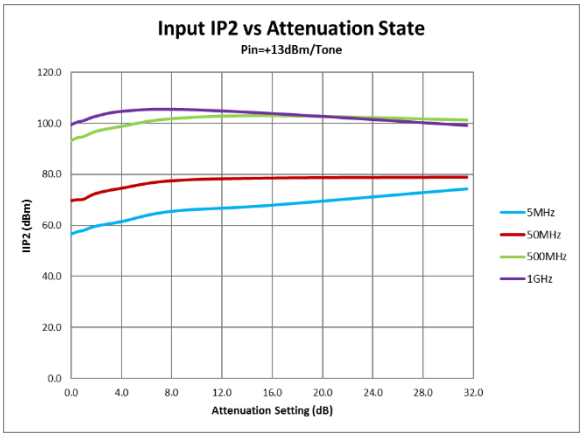
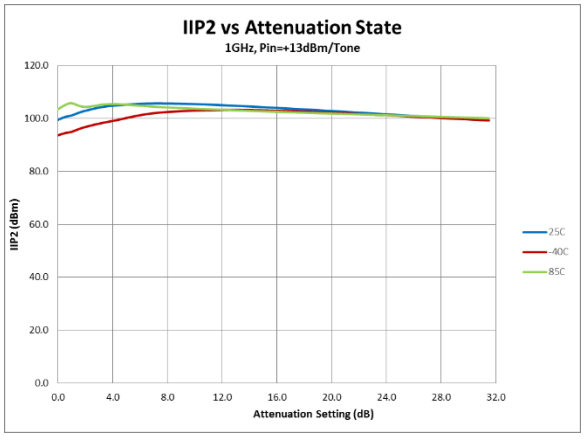


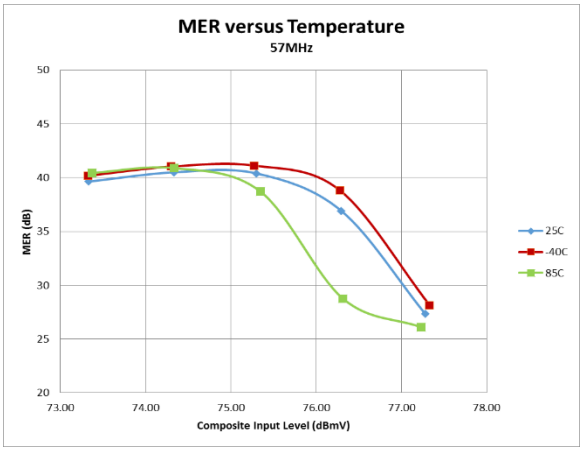



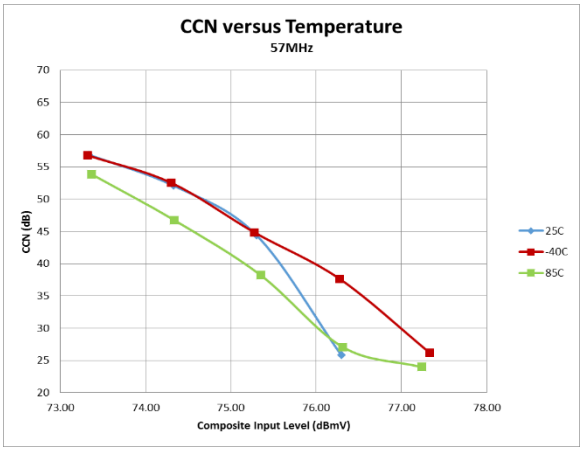



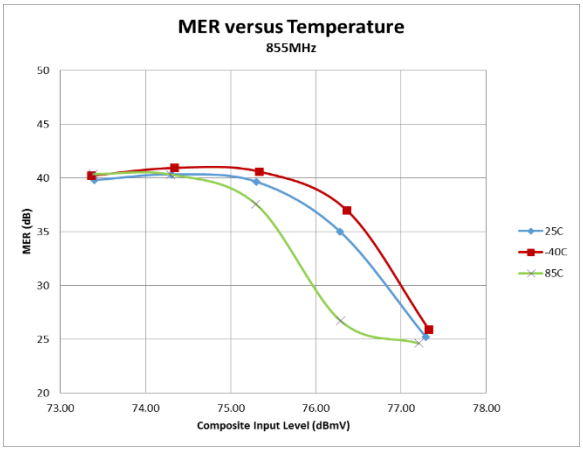



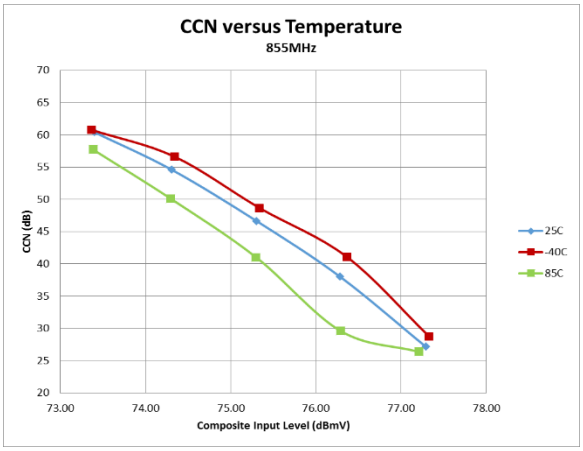
## Performance Plots (cont'd.)

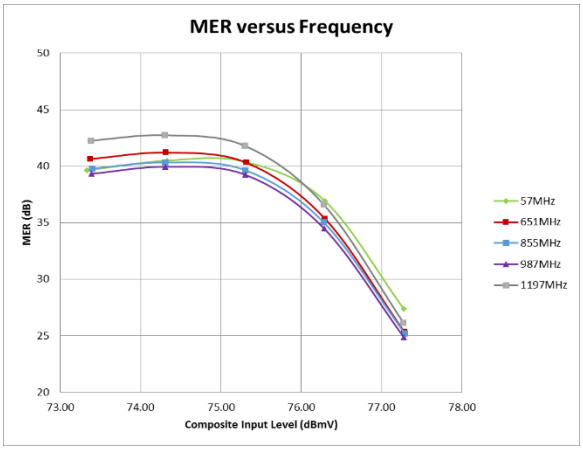
Test conditions unless otherwise noted: $V_{DD}$ =+5V, $V_{SS}$= 0V Temp= +25°C, $Z_o$ = 75Ω

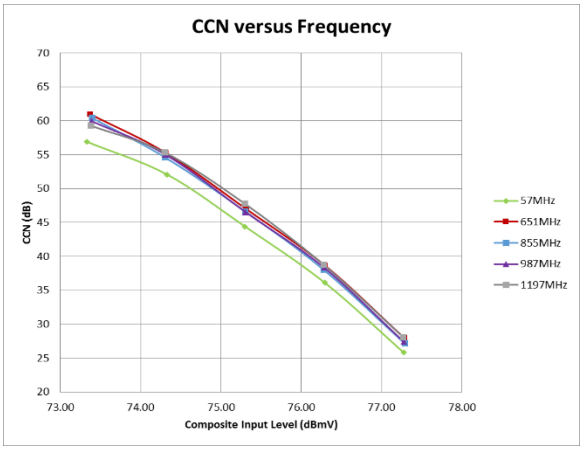



MER/CCN Test Conditions:

1. 190 QAM256 Channels, 57-1215MHz, ITU-T J.83, Annex B
2. CCN test procedure according to ANSI/SCTE 17. System BW 5.36MHz.
3. 0dB Attenuation Setting

## Evaluation Board Programming Using USB Interface

**Serial Mode**
All programming jumpers on the evaluation board are set to the default values indicated in the table. Refer to the Control Bit Generator (CBG) Software Reference Manual for instructions on how to setup the software for use. Apply supply voltage to P6. Select 'QPC3614' for serial operation from the parts list of the CBG user interface. Set the attenuation value using the CBG user interface.

**Direct Parallel Mode**
Evaluation board programming jumper S2 is set to '0'. Refer to the Control Bit Generator (CBG) Software Reference Manual for instructions on how to setup the software for use. Apply the supply voltage to P6. Select 'QPC3614-P' from the parts list of the CBG user interface. Set the attenuation value using the CBG user interface.

## Evaluation Board Programming Using External Bus

**Serial Mode**
This configuration allows the user to control the attenuator through the P5 connector using an external harness. Remove the USB interface board if it is currently installed on the evaluation board. Connect a user-supplied harness to the P5 connector. Note that the top row of P5 contains the serial bus signals and the bottom row is ground. Programming jumper S2 is set to '1' to select serial mode. Jumper S6 is installed and allows the LE signal to be routed from the P5 connector to the attenuator. Apply the supply voltage to P6. Send the appropriate signals onto the serial bus lines in accordance with the Serial Addressable Mode Timing Diagram.

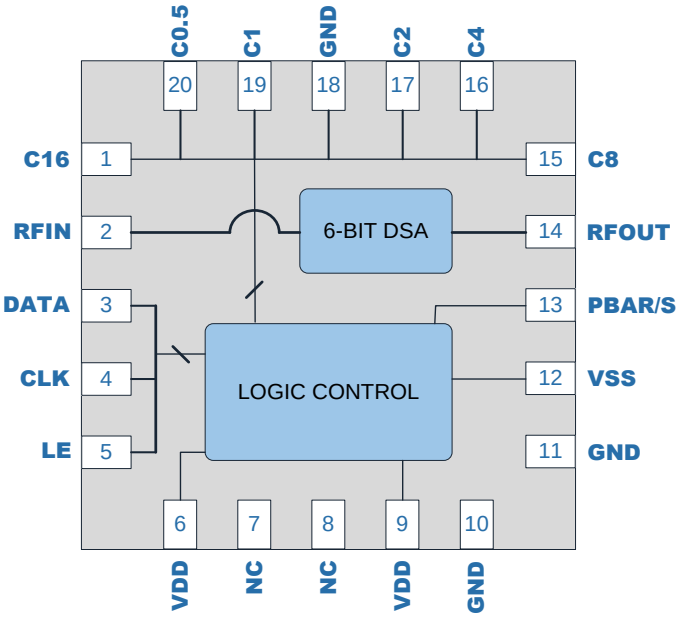
**Latched Parallel Mode**
This configuration allows the user to control the attenuator through the P1 connector using an external harness. Remove the USB interface if it is currently installed on the evaluation board. Connect a user-supplied harness to the P1 connector. The parallel bus signal names for P1 are indicated on the evaluation board. Programming jumper S2 is set to '0' to select parallel mode. Apply the supply voltage to P6. Send the appropriate signals onto the parallel bus lines in accordance with the Latched Parallel Mode Timing Diagram.

**Direct Parallel Mode**
This configuration allows the user to control the attenuator through the P1 connector using an external harness. When using this mode the LE signal is held at logic high so that the attenuation will change immediately when there is a change in logic state for any of the parallel bus signals. Remove the USB interface if it is currently installed on the evaluation board. Connect a user-supplied harness to the P1 connector. The parallel bus signal names for P1 are indicated on the evaluation board. Programming jumper S2 is set to '0' to select parallel mode. Apply the supply voltage to P6. Send the appropriate signals onto the parallel bus lines.

## Default Power-up State

This default attenuation state is maximum (31.5 dB) when supply voltage is applied to the attenuator in both serial and parallel modes. If a different attenuation state is desired during power-up, apply signals according to the Parallel Mode Truth Table to the C0.5 – C16 pins. The attenuator will power-up to the state applied to the parallel bus during turn on. The LE signal must be held to logic '0' during power-up. Note that the FDTI USB controller module on the Qorvo EVB can hold the parallel pins to a different state during power up. Removing the plug in module will allow normal expected power default operation.

## Pad Configuration and Description




Top View

| Pin | Label | Description |
|---|---|---|
| 1 | C16 | 16dB Parallel Control Bit |
| 2 | RFIN | RF Input Pin: Incident RF power must enter this pin for rated thermal performance and reliability. Do not apply DC power to this pin. Pin may be DC grounded externally and is grounded through resistors. |
| 3 | DATA | Serial Bus Data Input |
| 4 | CLK | Serial Bus Clock Input |
| 5 | LE | Latch Enable: The leading edge of signal on LE causes the attenuator to change state for serial and latched parallel modes. For direct parallel mode keep LE at logic high level. |
| 6 | VDD | Supply Voltage |
| 7 | NC | No Connection |
| 8 | NC | No Connection |
| 9 | VDD | Supply Voltage |
| 10 | GND | Ground Pin |
| 11 | GND | Ground Pin |
| 12 | VSS | External Negative Supply Voltage. Ground VSS pin to use internal negative voltage generator |
| 13 | PBAR/S | Mode Select Pin, Logic Low = Parallel, Logic High = Serial |
| 14 | RFOUT | RF Output Pin: Pin may be DC grounded externally and is grounded thru resistors internal to the part. |
| 15 | C8 | 8dB Parallel Control Bit |
| 16 | C4 | 4dB Parallel Control Bit |
| 17 | C2 | 2dB Parallel Control Bit |
| 18 | GND | Ground Pin |
| 19 | C1 | 1dB Parallel Control Bit |
| 20 | C0.5 | 0.5dB Parallel Control Bit |
| Backside Paddle | RF/DC GND | RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint. |

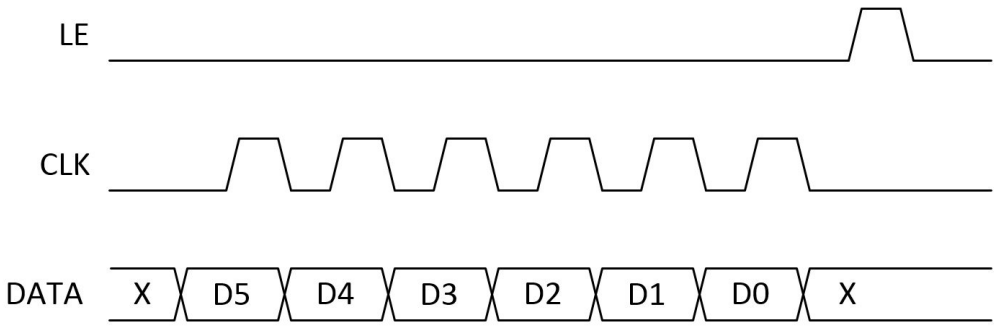
## Serial Mode Attenuation Word Truth Table

| Attenuation Word | | | | | | | Attenuation State |
|---|---|---|---|---|---|---|---|
| D5 | D4 | D3 | D2 | D1 | D0 (LSB) | | |
| L | L | L | L | L | L | | 0 dB / Reference Insertion Loss |
| L | L | L | L | L | H | | 0.5 dB |
| L | L | L | L | H | L | | 1 dB |
| L | L | L | H | L | L | | 2 dB |
| L | L | H | L | L | L | | 4 dB |
| L | H | L | L | L | L | | 8 dB |
| H | L | L | L | L | L | | 16 dB |
| H | H | H | H | H | H | | 31.5 dB |

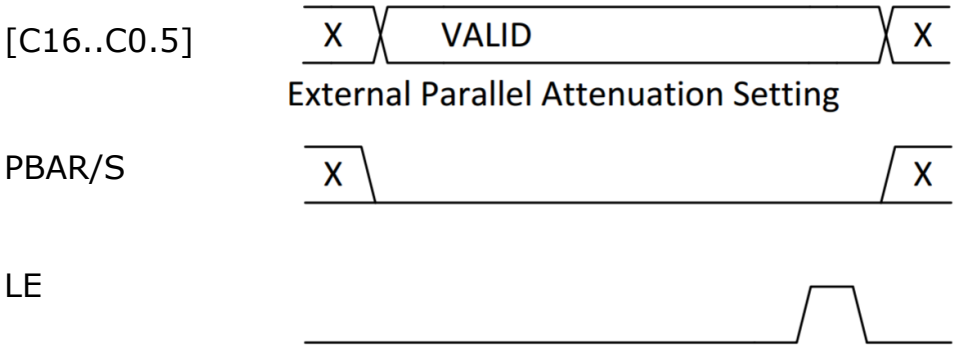
## Parallel Mode Attenuation Word Truth Table

| Attenuation Word | | | | | | | Attenuation State |
|---|---|---|---|---|---|---|---|
| C16 | C8 | C4 | C2 | C1 | C0.5 (LSB) | | |
| L | L | L | L | L | L | | 0 dB / Reference Insertion Loss |
| L | L | L | L | L | H | | 0.5 dB |
| L | L | L | L | H | L | | 1 dB |
| L | L | L | H | L | L | | 2 dB |
| L | L | H | L | L | L | | 4 dB |
| L | H | L | L | L | L | | 8 dB |
| H | L | L | L | L | L | | 16 dB |
| H | H | H | H | H | H | | 31.5dB |

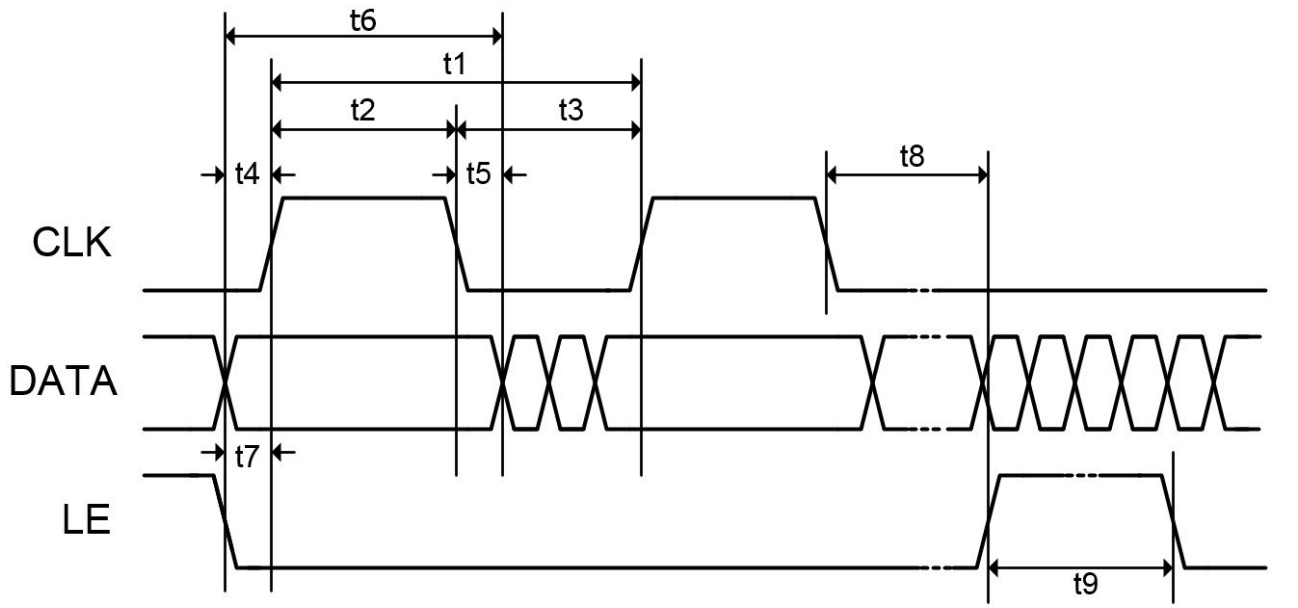
## Serial Mode Timing Diagram




## Latched Parallel Mode Timing Diagram

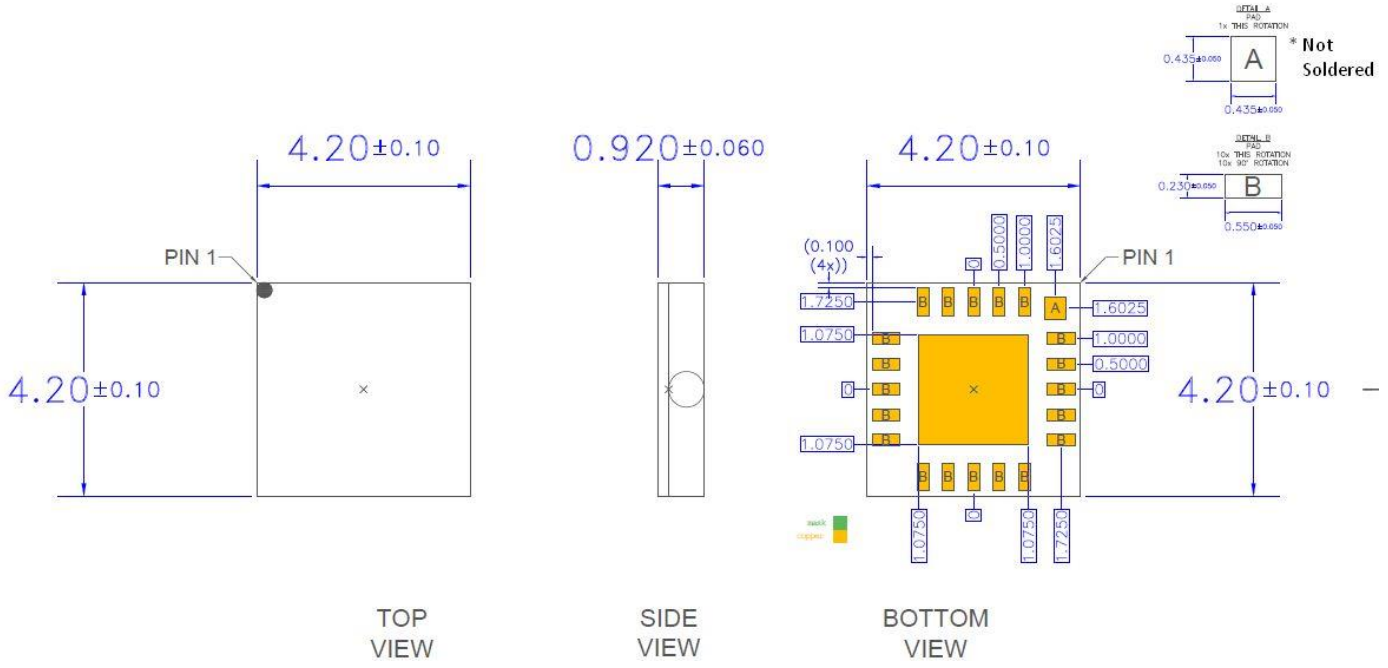


## Serial BUS Timing Specifications



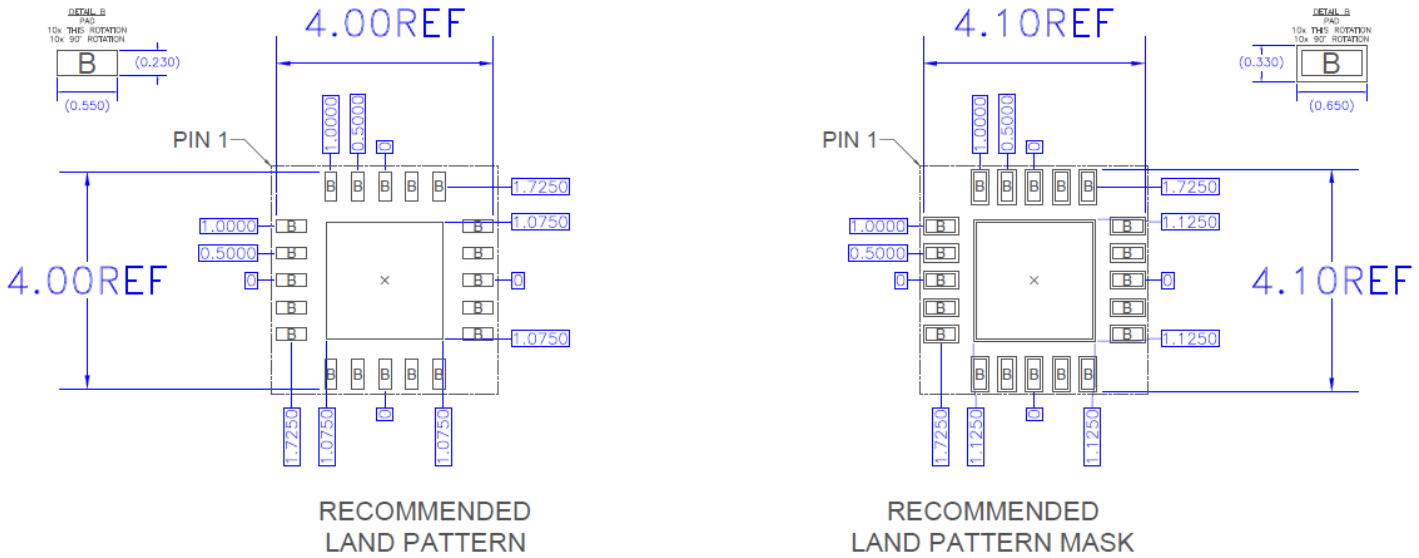

| Parameter | Limit | Unit | Comment |
|---|---|---|---|
| t1 | 25 | MHz max | CLK Frequency |
| t2 | 20 | ns min | CLK High |
| t3 | 20 | ns min | CLK Low |
| t4 | 5 | ns min | Data to CLK Setup Time |
| t5 | 5 | ns min | Data to CLK Hold Time |
| t6 | 30 | ns min | Data Valid |
| t7 | 5 | ns min | LE to CLK Setup Time |
| t8 | 5 | ns min | CLK to LE Setup Time |
| t9 | 10 | ns min | LE Pulse Width |

## Package Dimensions

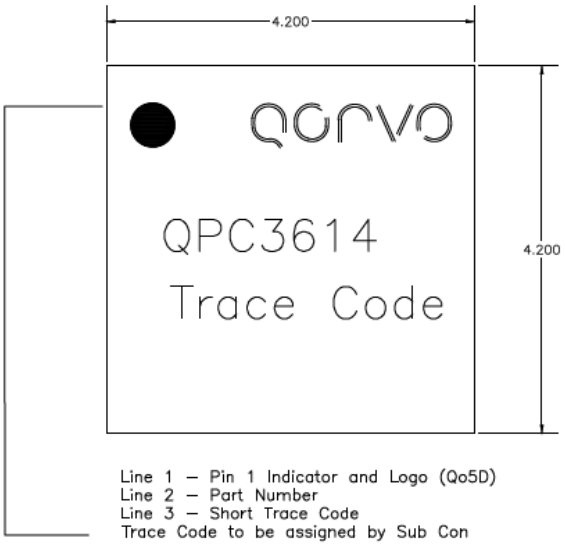



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
4. Contact plating: NiPdAu

## Recommended Mounting Pattern



## Package Marking



## Handling Precautions

| Parameter | Rating | Standard |
|---|---|---|
| ESD – Human Body Model (HBM) | 1C | ESDA / JEDEC JS-001-2012 |
| ESD – Charged Device Model (CDM) | C3 | JEDEC JESD22-C101F |
| MSL – Moisture Sensitivity Level | MSL3 | IPC/JEDEC J-STD-020 |

Caution!
ESD-Sensitive Device

## Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: NiPdAu

## RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free


## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

**Tel:** **1-844-890-8163**

**Web:** **www.qorvo.com**

**Email:** **customer.support@qorvo.com**

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