

APPNOTE NUMBER – AN1138

PI3WVR13612 DP1.4/HDMI2.0 Mux/Demux Application Guidelines

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1. Introduction

PI3WVR13612 is video switch that supports wide input voltage range. It can be employed in DP1.3/4 or HDMI2.0 switch application. This application note explains how it can be used for either DP1.3/4 or HDMI2.0 mux applications.

2. Application Guidelines

The PI3WVR13612 is a passive switch, and therefore it can be used in both source and sink applications. The switch can be used as MUX and DEMUX.

2.1 DP 2 to 1 Application

Below is a source application diagram of PI3WVR13612 as a DP1.4 2-to-1 Mux

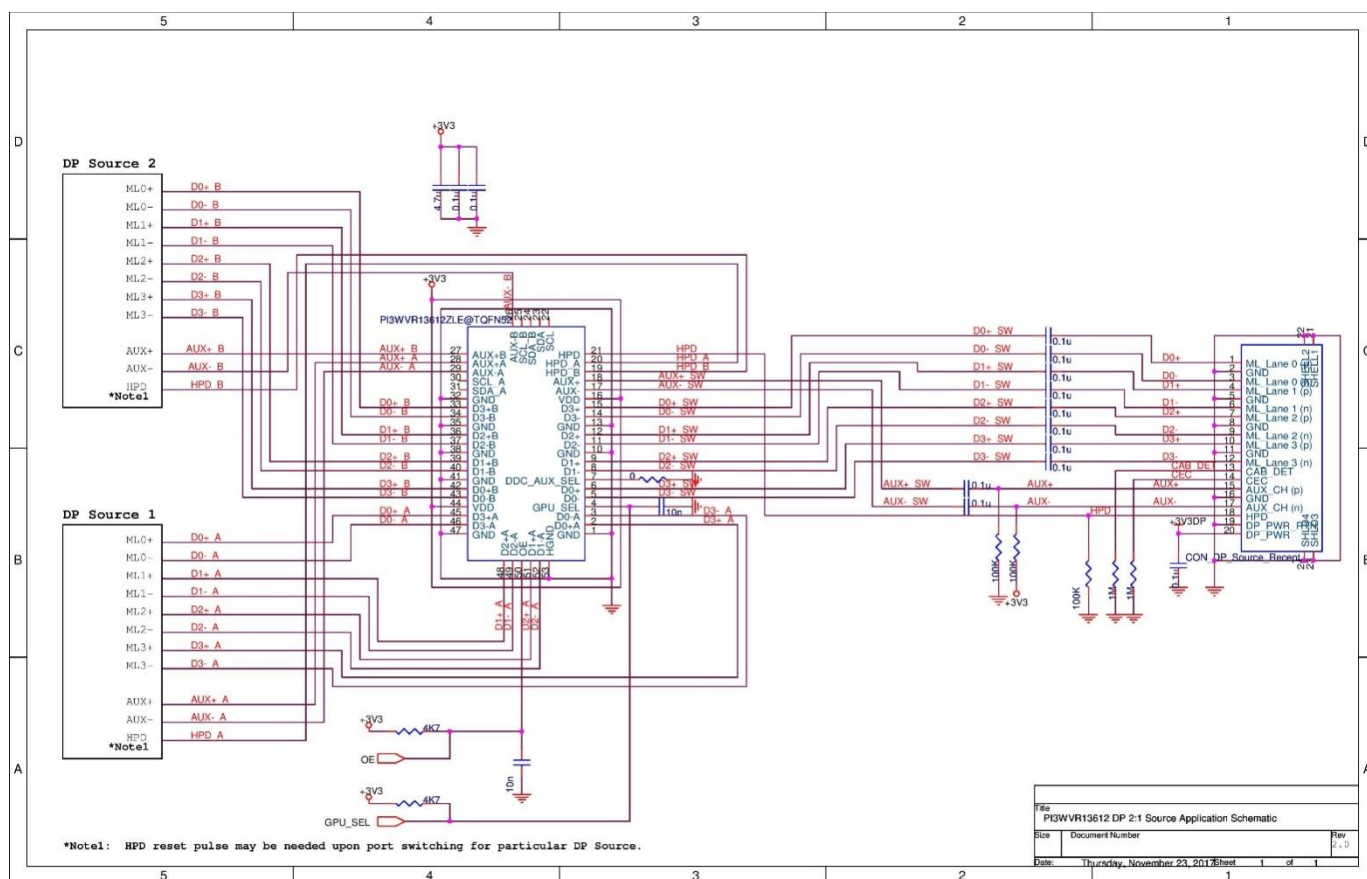


Figure 1: DP 2 to 1 Source Application Diagram

2.1.1 GPU_SEL Pin

In order to achieve better high-speed signal isolation, a decoupling capacitor of 10n-100nF at GPU_SEL pin is recommended.

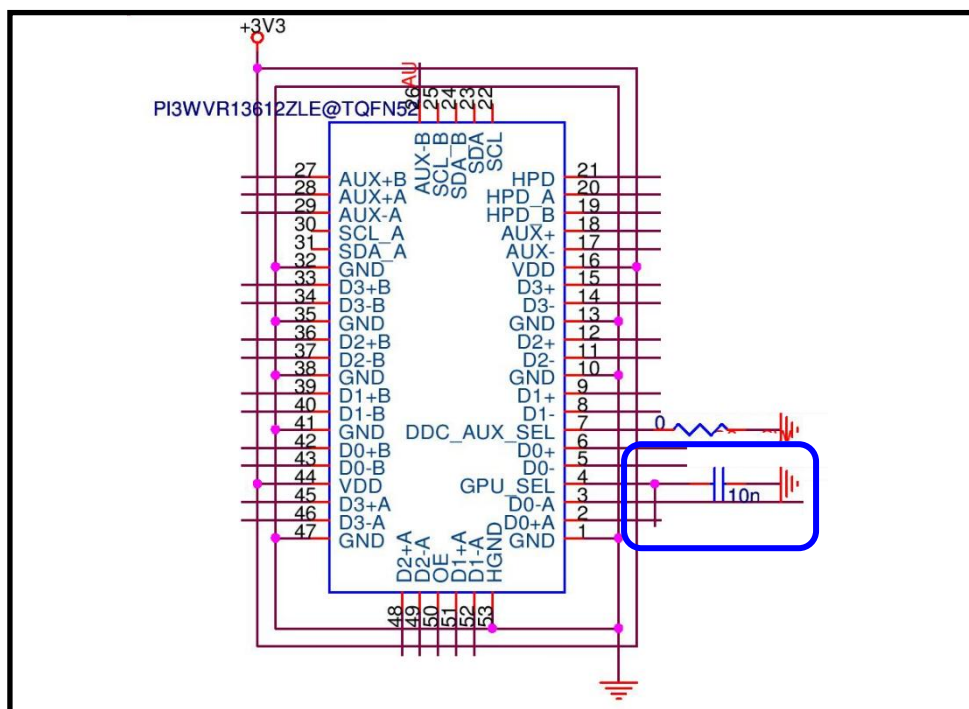


Figure 2: GPU_SEL Decoupling Design

2.1.2 OE Pin Design

OE pin of PI3WVR13612 is active HIGH. It should be pulled to VDD for output enabled. To save power, it can be controlled by GPIO.

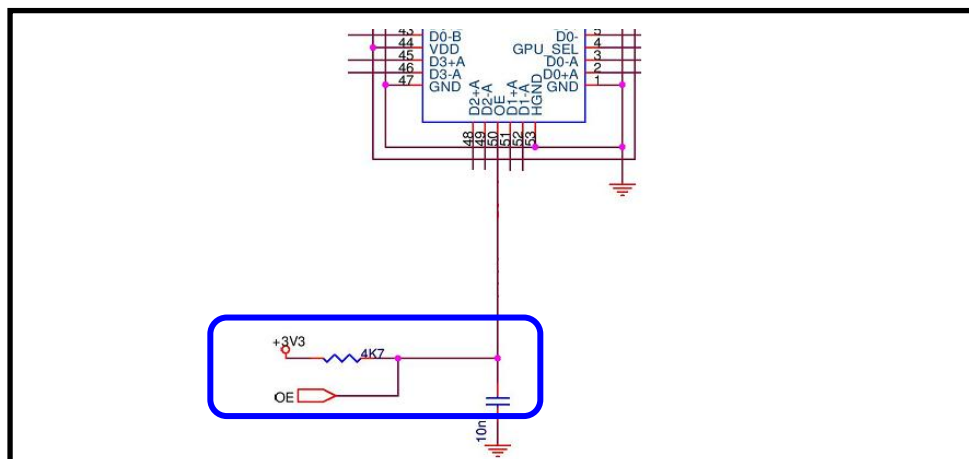


Figure 3: OE Controlled by GPIO

Similar to GPU_SEL pin, a decoupling capacitor of 10n-100nF at OE pin is recommended for better isolation.

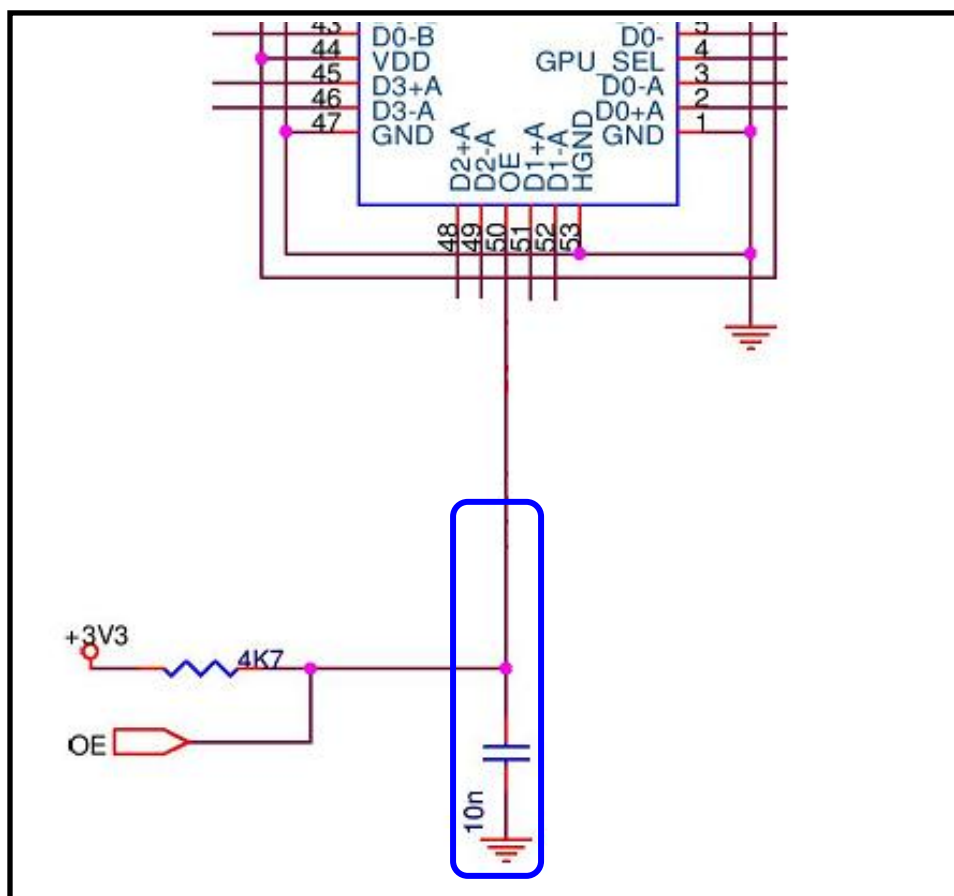


Figure 4: OE Decoupling Design

2.1.3 AUX Design

Per DP specification, AUX channels are AC coupled by 0.1μF capacitors followed by a 100kΩ pull-down resistor for AUX+ and a 100kΩ pull-up resistor for AUX-.

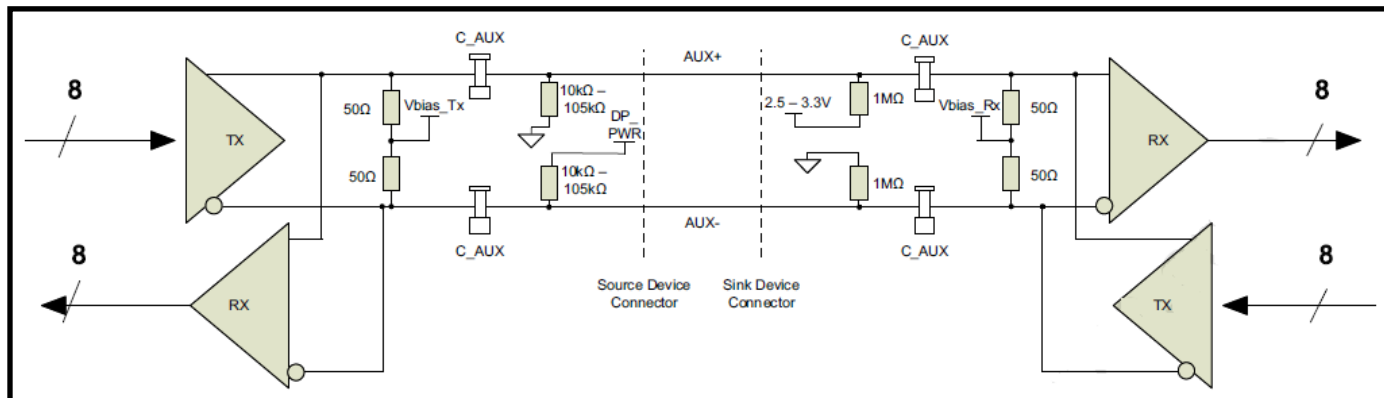


Figure 5: Standard AUX Design

2.1.4 Main-link Design

AC coupling capacitors are required for main-link channels as well. If main-link signals from DP source chipset are AC coupled before entering PI3WVR13612, external capacitor is not required.

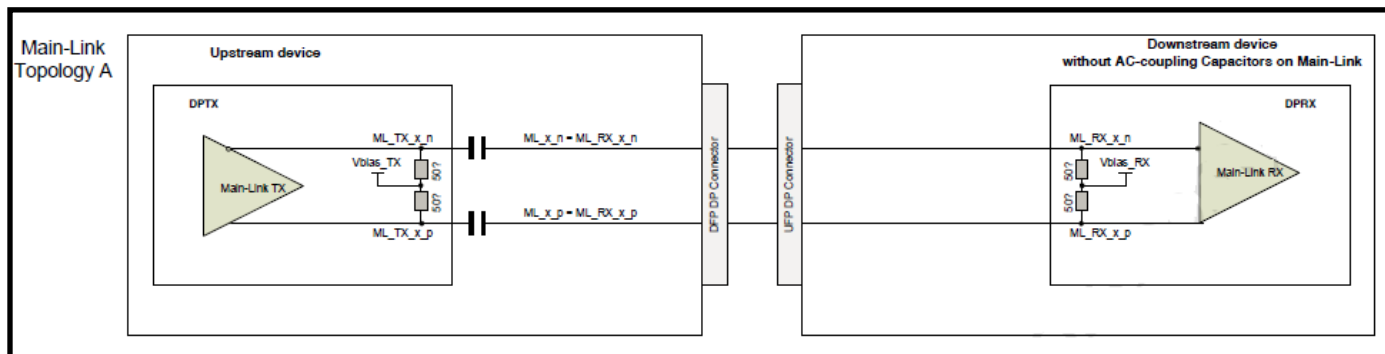


Figure 6: Standard Main-link Design

ESD protector is also recommended for preventing PI3WVR13612 and source chipset from being damaged. 2-pin ESD protector <https://www.diodes.com/assets/Datasheets/DESD3V3Z1BCSF.pdf> is preferable for better control of PCB impedance.

2.1.5 HPD Signal

In DP source application, as shown in figure 7, 100kΩ pull-down resistor is implemented at HPD in order to have a known state for DP source device when no sink device is attached to it.

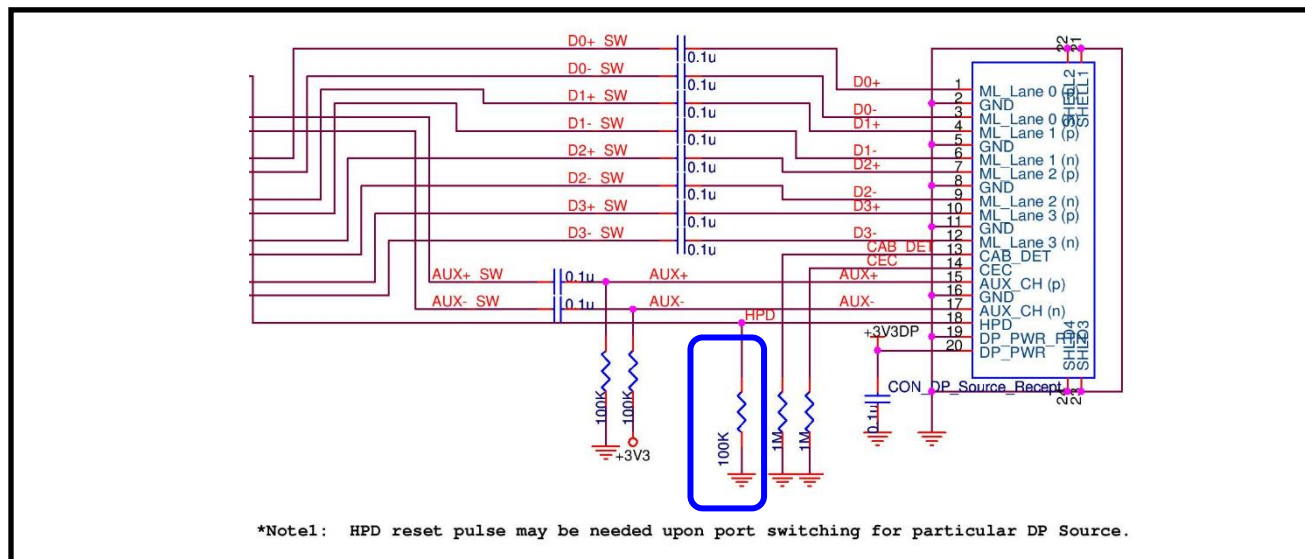


Figure 7: HPD Signal pull-down requirement in DP 2 to 1 Source Application

2.2 DP1.4 1 to 2 Application

Below is a source application diagram of PI3WVR13612 DP 1 to 2 switch.

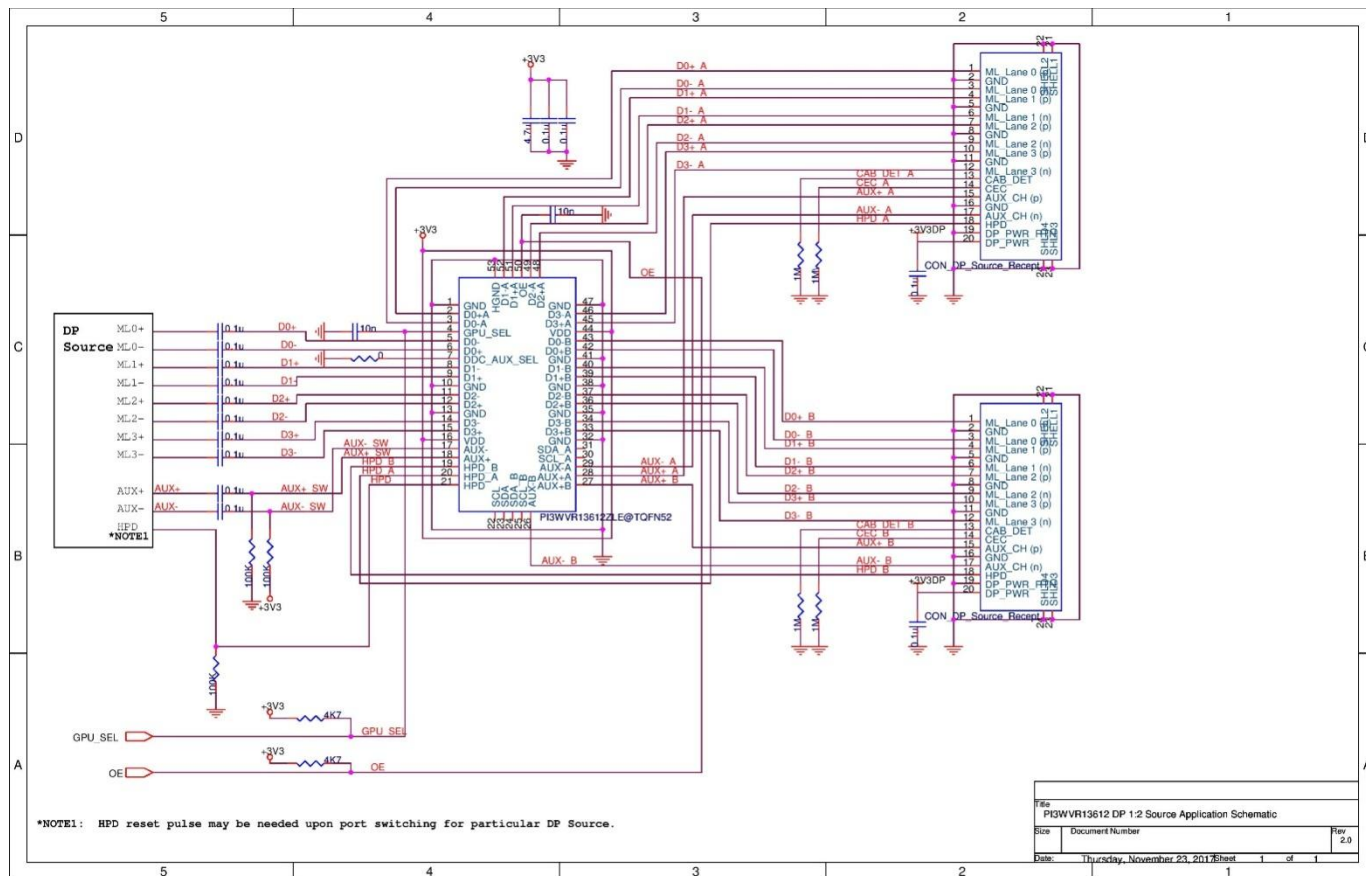


Figure 8: DP 1 to 2 Source Application Diagram

2.2.1 GPU_SEL Pin Design

As shown in figure 2, a decoupling capacitor of 10n-100nF at GPU_SEL pin is recommended for better high-speed signal isolation.

2.2.2 OE Pin Design

OE pin of PI3WVR13612 is active HIGH. It should be pulled to VDD for output enabled. To save power, it can be controlled by GPIO.

Similar to GPU_SEL pin, a decoupling capacitor of 10n-100nF at OE pin is recommended for better isolation.

2.2.3 AUX Design

Please refer to Section 2.1.3

2.2.4 Main-link Design

Please refer to Section 2.1.4.

2.2.5 HPD Signal

In DP source application, as shown in figure 9, 100k Ω pull-down resistor is implemented at HPD in order to have a known state for DP source device when no sink device is attached to it.

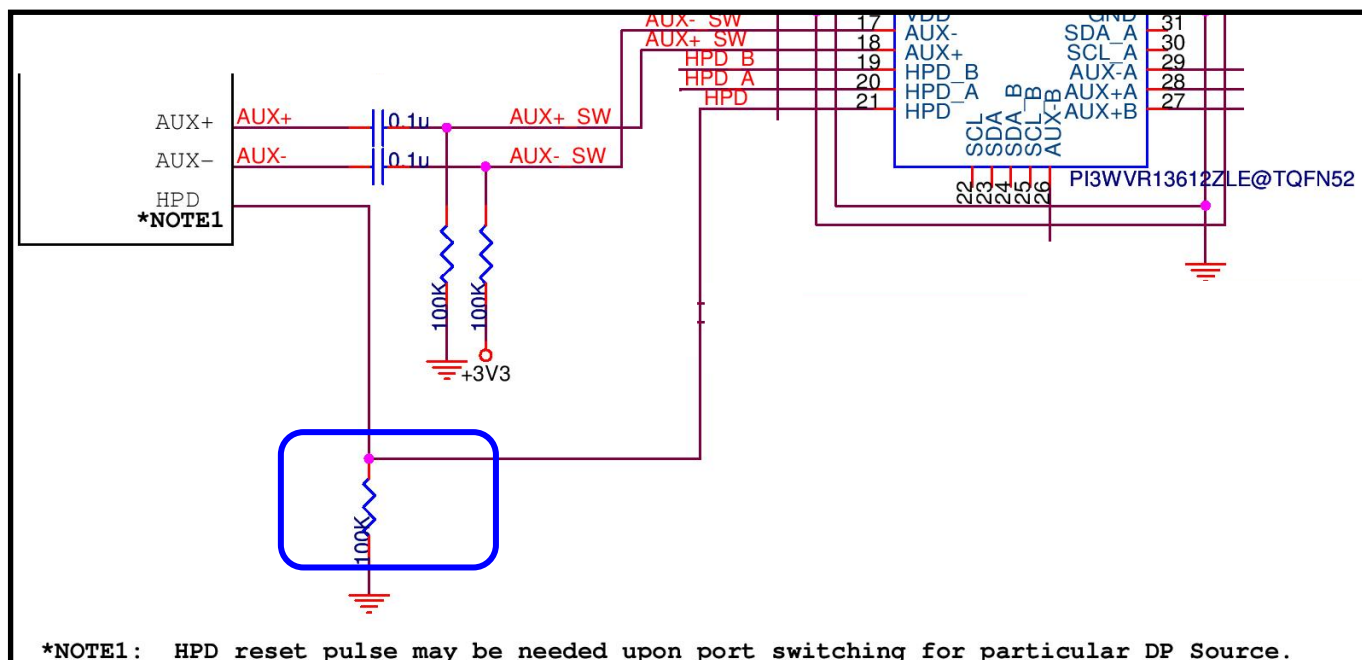


Figure 9: HPD Signal pull-down requirement in DP 1 to 2 Source Application

2.3 HDMI 2 to 1 Application

Below is a source application diagram of PI3WVR13612 HDMI2.0 2 to 1 Mux.

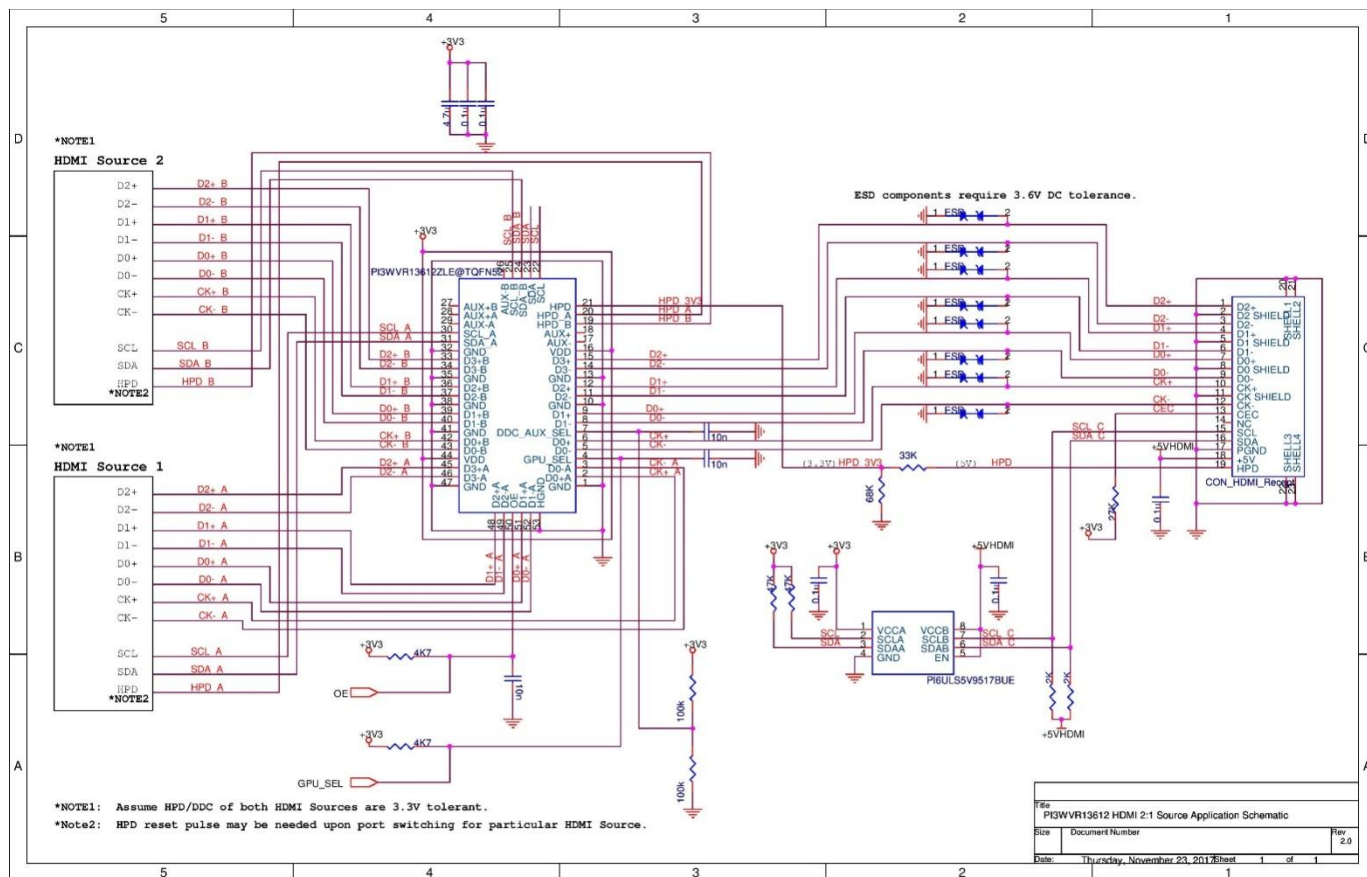


Figure 10: HDMI2.0 2 to 1 Source Application Diagram

2.3.1 GPU_SEL and DDC_AUX_SEL Pin Design

As shown in Figure 11, a decoupling capacitor of 10n-100nF at each of GPU_SEL and DDC_AUX_SEL pins is recommended for better high-speed signal isolation.

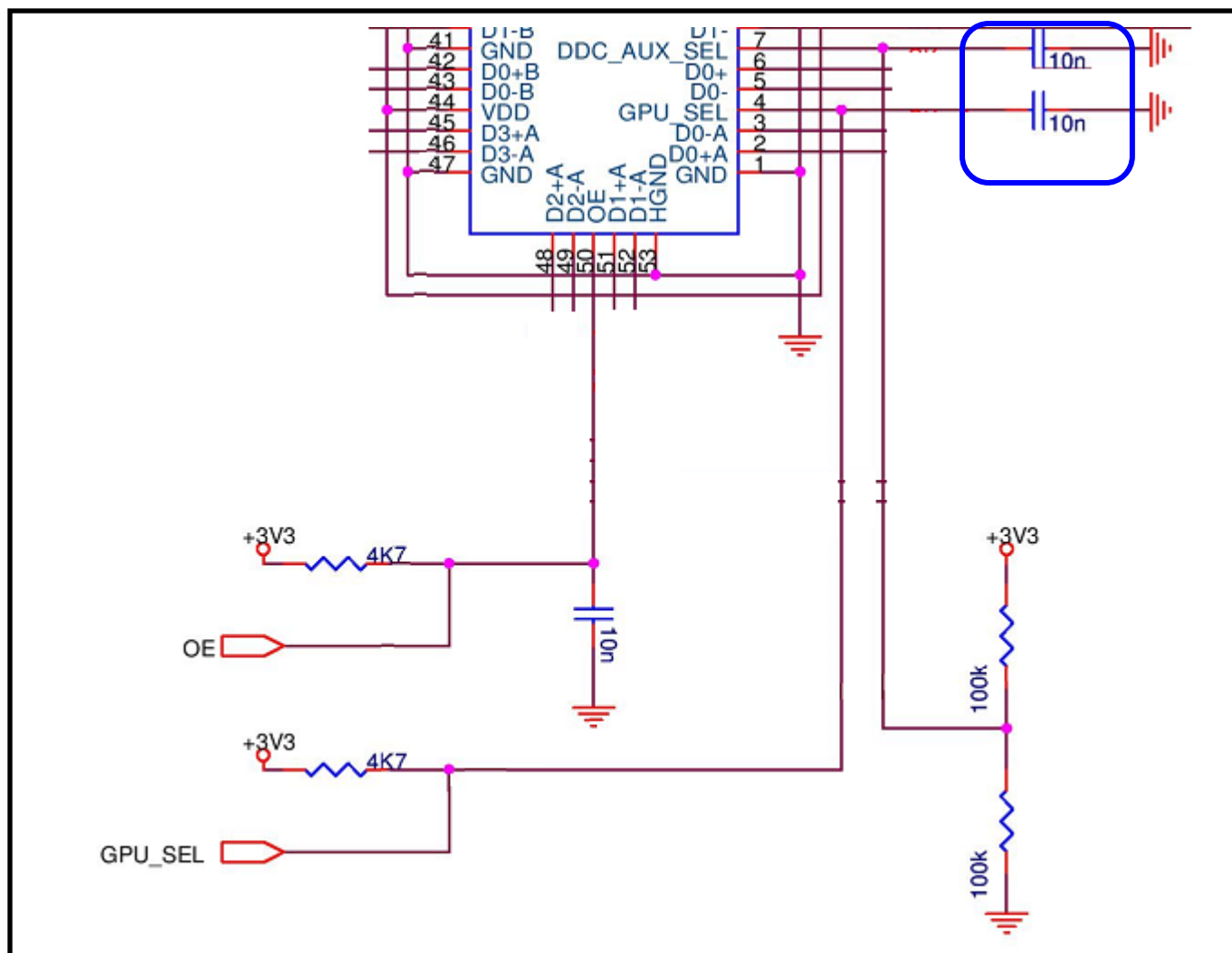


Figure 11: GPU_SEL and DDC_AUX_SEL Decoupling Design

2.3.2 OE Pin Design

A 10n-100nF capacitor is also recommended for OE pin. Since HPD from HDMI connector is 5V, if OE pin is controlled by HPD signal, voltage divider must be considered. 33kΩ and 68kΩ resistors are to form a voltage divider in the above application diagram.

2.3.3 DDC Design

As DDC path of PI3WVR13612 is 4V tolerant, SCL and SDA signals from PI3WVR13612 cannot be connected to HDMI connector directly. DDC level shifters must be added in between.

2.3.4 TMDS Design

Per HDMI specification, TMDS path is DC coupled. HDMI input and HDMI output are connected to PI3WVR13612 directly. To provide high-speed path from ESD damage, ESD protectors are recommended. 2-pin ESD protector, i.e. DESD3V3Z1BCSF, is more preferable for better control of PCB impedance.

2.3.5 HPD Signal

In HDMI source application, as shown in figure 12, 100kΩ pull-down resistor is implemented at HPD in order to have a known state for HDMI source device when no sink device is attached to it. Since PI3WVR13612 HPD pin is 4V tolerant, voltage divider must be considered. 33kΩ and 68kΩ resistors are to form a voltage divider.

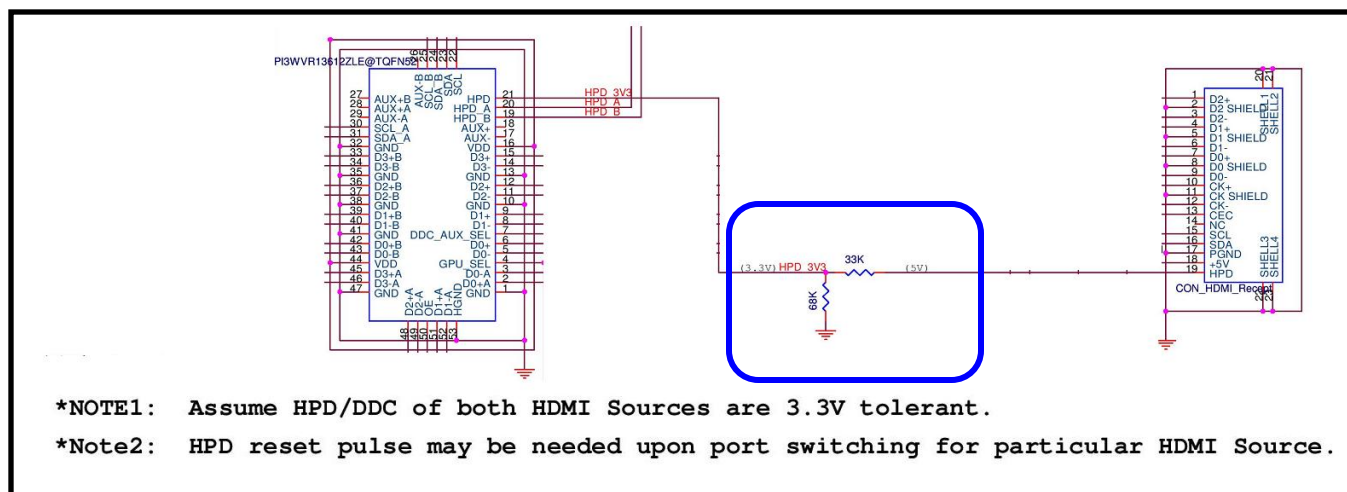


Figure 12: HPD Signal pull-down requirement in HDMI 2 to 1 Source Application

3. References

- (1) VESA DisplayPort (DP) Standard Version 1.4, Video Electronics Standards Association, February 23, 2016
- (2) High-Definition Multimedia Interface Specification Version 2.0b, HDMI Forum, March 3, 2016
- (3) High-Definition Multimedia Interface Specification Version 2.0n Compliance Test Specification, HDMI Forum, January 4, 2016
- (4) DESD3V3Z1BCSF datasheet, Diodes Incorporated, Document Number: DS39330 Rev.1-0, November 2016

Revision History

Revision	Date	Description
1.0	15 June, 2017	1. Initial release
1.1	28 August, 2017	1. Updated application schematics.
1.2	12 Sept., 2017	1. Errata and application schematics are updated.
2.0	24 Nov., 2017	This Doc. 1. Updated application schematics.

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