

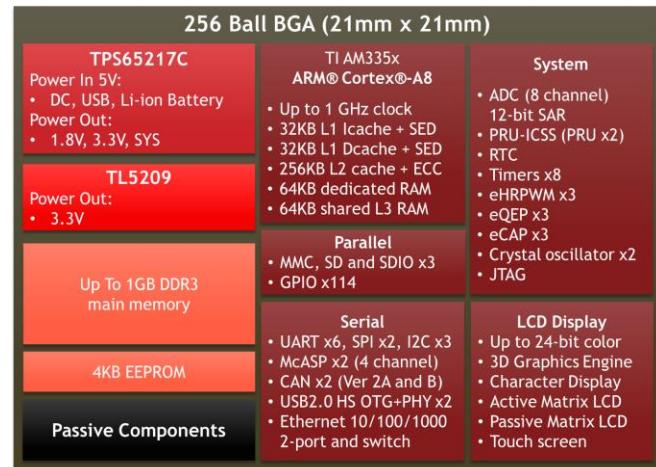
## Introduction

The OSD335x-SM Family of System-In-Package (SiP) products are building blocks designed to allow easy and cost-effective implementation of systems based on Texas Instruments' powerful Sitara™ AM335x line of processors. The OSD335x-SM integrates the AM335x along with the TI TPS65217C PMIC, the TI TL5209 LDO, up to 1 Gigabyte (GB) of DDR3 Memory, a 4 Kilobyte (KB) EEPROM for non-volatile configuration storage and resistors, capacitors, and inductors into a single 21mm x 21mm design-in-ready package.

With this level of integration, the OSD335x-SM Family of SiPs allows designers to focus on the key aspects of their system without spending time on the complicated high-speed design of the processor/DDR3 interface or the PMIC power distribution. It also reduces the overall size and complexity of the design and the supply chain. The OSD335x-SM can significantly decrease the time to market for AM335x-based products.

## Features

- TI AM335x, TPS65217C, TL5209, DDR3, EEPROM and passive components integrated into a single package
- TI AM335x Features:
  - ARM® Cortex®-A8 up to 1GHz
  - 8 channel 12-bit SAR ADC
  - Ethernet 10/100/1000 x 2
  - USB 2.0 HS OTG + PHY x2
  - MMC, SD and SDIO x3
  - LCD Controller
  - SGX 3D Graphics Engine
  - PRU Subsystem
- Access to all AM335x Peripherals: CAN, SPI, UART, I2C, GPIO, etc.
- Up to 1GB DDR3



OSD335x-SM Block Diagram

- PWR In: AC Adapter, USB or Single cell (1S) Li-Ion / Li-Po Battery
- PWR Out: 1.8V, 3.3V and SYS
- Selectable AM335x I/O Voltage: 1.8V or 3.3V

## Benefits

- Integrates over 100 components into one package
- Compatible with AM335x development tools and software
- Wide BGA ball pitch allows for low-cost assembly.
- Significantly reduces design time
- Decreases layout complexity
- 60% reduction in board space vs discrete implementation
- Increased reliability through reduced number of components

## Package

- 256 Ball BGA (21mm X 21mm)
- 16 X 16 grid, 1.27mm pitch
- Temp Range: 0 to 85°C, -40 to 85°C

## Table of Contents

1	Revision History .....	4
2	Block Diagram .....	5
2.1	Passives .....	6
3	Product Number Information .....	7
4	Reference Documents .....	9
4.1	Data Sheets .....	9
4.2	Other References .....	9
5	Ball Map .....	10
5.1	Ball Description .....	15
5.2	Not Connected Balls .....	18
5.3	Reserved Signals .....	18
6	OSD335x-SM Components .....	19
6.1	AM335x Processor .....	19
6.1.1	I/O Voltages .....	19
6.2	DDR3 Memory .....	19
6.3	EEPROM .....	21
6.3.1	EEPROM Contents .....	21
6.3.2	EEPROM Write Protection .....	21
7	Power Management .....	22
7.1	Input Power .....	22
7.1.1	VIN_AC .....	22
7.1.2	VIN_USB .....	22
7.1.3	VIN_BAT .....	22
7.2	Output Power .....	22
7.2.1	SYS_VOUT: Switched VIN_AC, VIN_USB, or VIN_BAT .....	22
7.2.2	SYS_VDD1_3P3V .....	23
7.2.3	SYS_VDD2_3P3V .....	23
7.2.4	SYS_VDD3_3P3V .....	23
7.2.5	SYS_RTC_1P8V .....	23
7.2.6	SYS_VDD_1P8V .....	23
7.2.7	SYS_ADC_1P8V .....	23

7.3	Internal Power .....	23
7.3.1	VDDS_DDR .....	23
7.3.2	VDD_MPU .....	24
7.3.3	VDD_CORE .....	24
7.3.4	VDDS_PLL .....	24
7.4	Total Current Consideration .....	24
7.5	Control and Status .....	25
7.5.1	Minimum Processor-PMIC interface Connections .....	25
7.5.2	Minimum RTC Power Connections .....	27
8	Electrical & Thermal Characteristics .....	28
9	Packaging Information .....	29
9.1	Mechanical Dimensions .....	29
9.2	Reflow Instructions .....	30
9.3	Storage Recommendations .....	30

# OSD335x-SM Family

Rev. 6 2/16/2018



## 1 Revision History

Revision Number	Revision Date	Changes	Author
1.0	19 Sept 2017	Initial Release	Greg Sheridan, Erik Welsh
2.0	16 Oct 2017	Added notes for power rails and updated minimum interface connections	Neeraj Dantu
3.0	21 Nov 2017	Updated SYS_VDD2_3P3V max current	Greg Sheridan
4.0	28 December 2017	Updated Mechanical Drawing for Clarity. Fixed table 2.1	Greg Sheridan
5.0	27 January 2018	Adjusted page numbering so they match with PDF page number	Greg Sheridan
6.0	16 February 2018	Updated voltage measurements and notes on EEPROM	Neeraj Dantu

## 2 Block Diagram

The OSD335x-SM family of devices consist of 5 main components serving 4 distinct functions. The main processor is a Texas Instruments Sitara™ AM335x ARM® Cortex®-A8. The power system has 2 devices from Texas Instruments, the TPS65217C Power Management IC (PMIC) and the TL5209 LDO. The system memory uses up to 1GB DDR3 memory. The last main component is the 4KB EEPROM for configuration data. Figure 2.1 shows a detailed block diagram of the OSD335x and breaks out the key functions of the AM335x processor.

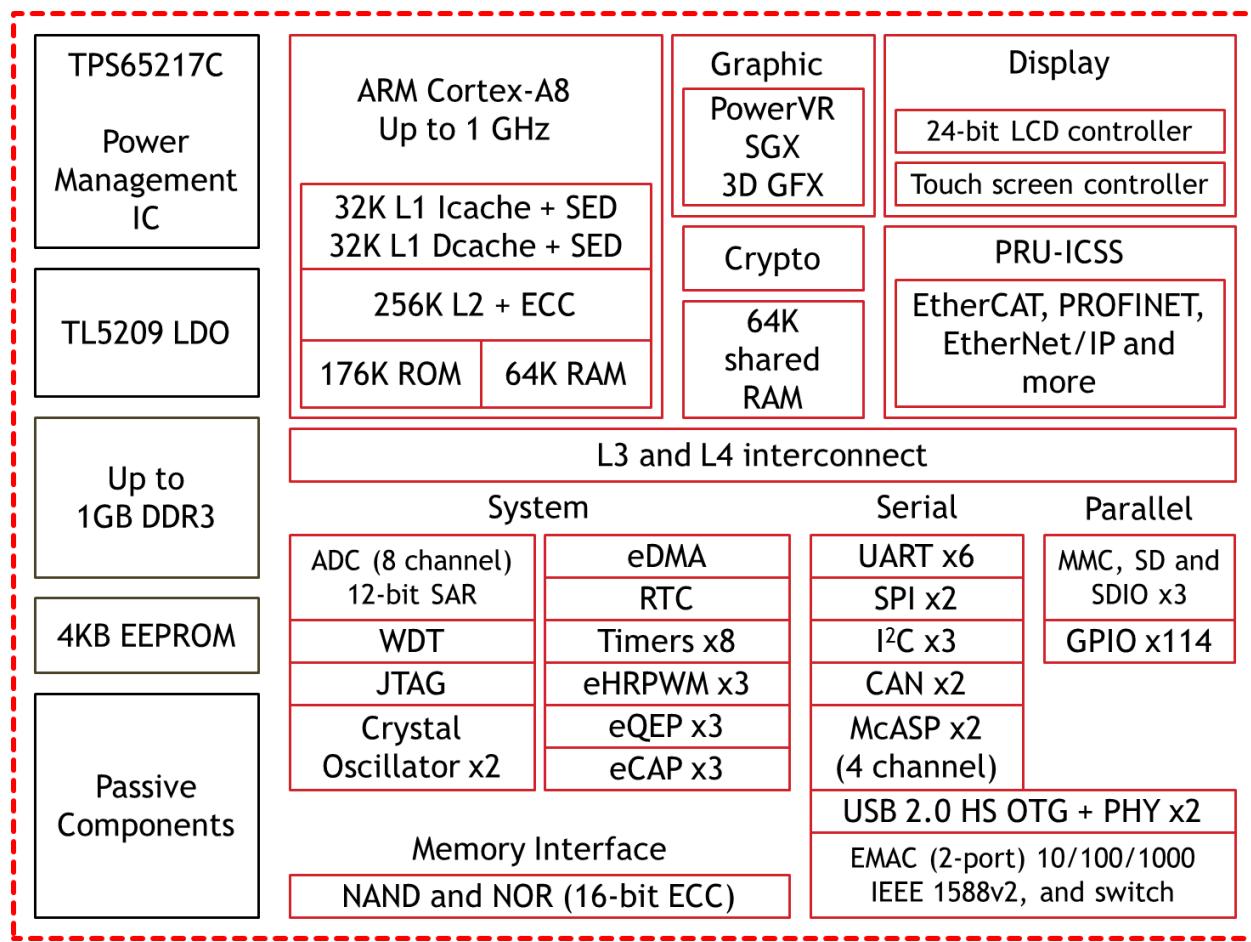


Figure 2.1. OSD335x-SM Detailed Block Diagram

# OSD335x-SM Family

Rev. 6 2/16/2018

## 2.1 Passives

Besides the five major components, the OSD335x-SM also integrates capacitors, resistors, inductors, and ferrite beads (Passives). Table 2.1 lists the information to design around the OSD335x-SM. This includes the approximate bulk capacitance on input and output power rails as well as all pull-up resistor locations and values. The OSD335x-SM does not require any external decoupling / bypass capacitors in most applications.

Table 2.1. OSD335x-SM Passives

From	To	Device	Description	Type	Value
<b>VIN_AC</b>	DGND	TPS65217C	VIN_AC input capacitance	C	10uF <sup>(1)</sup>
<b>VIN_USB</b>	DGND	TPS65217C	VIN_USB input capacitance	C	10uF <sup>(1)</sup>
<b>VIN_BAT</b>	DGND	TPS65217C	VIN_BAT input capacitance	C	10uF <sup>(1)</sup>
<b>SYS_VOUT</b>	DGND	TPS65217C	SYS_VOUT output capacitance	C	10uF <sup>(1)</sup>
<b>SYS_VDD1_3P3V</b>	DGND	TL5209	SYS_VDD1_3P3V output capacitance	C	2.2uF <sup>(1)</sup>
<b>SYS_VDD2_3P3V</b>	DGND	TPS65217C	SYS_VDD2_3P3V output capacitance	C	2.2uF <sup>(1)</sup>
<b>SYS_VDD3_3P3V</b>	DGND	TPS65217C	SYS_VDD3_3P3V output capacitance	C	10uF <sup>(1)</sup>
<b>SYS_VDD_1P8V</b>	DGND	TPS65217C	SYS_VDD_1P8V output capacitance	C	10uF <sup>(1)</sup>
<b>SYS_RTC_1P8V</b>	DGND	TPS65217C	SYS_RTC_1P8V output capacitance	C	10uF <sup>(1)</sup>
<b>PMIC_PWR_EN</b>	SYS_RTC_1P8V	TPS65217C	PWR_EN pull-up	R	4.7K Ohm
<b>EXT_WAKEUP</b>	SYS_RTC_1P8V	AM335x	EXT_WAKEUP input pull-up	R	4.7K Ohm
<b>EXTINTIN</b>	VDDSHV6	AM335x	nNMI pull-up	R	4.7K Ohm
<b>I2C0_SCL</b>	VDDSHV6	AM335x	I2C0 SCL pull-up	R	4.7K Ohm
<b>I2C0_SDA</b>	VDDSHV6	AM335x	I2C0 SDA pull-up	R	4.7K Ohm
<b>EEPROM_WP</b>	VDDSHV6	EEPROM	EEPROM WP pull-up	R	4.7K Ohm

(1) Values are approximate.

### 3 Product Number Information

Figure 3.1 shows an example of an orderable product number for the OSD335x-SM family. This section explains the different sections of the product number. It will also list the valid entries and their meaning for each designator.

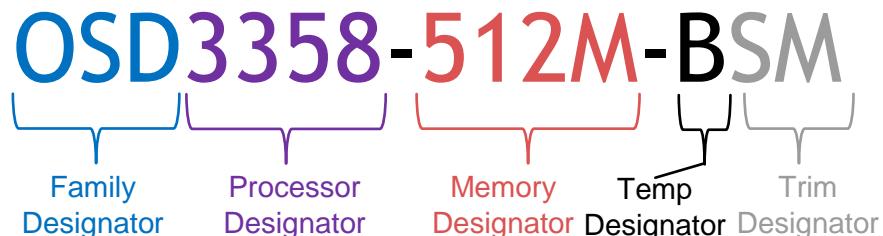


Figure 3.1. Example Product Number

**Family Designator** – Three letters that designate the family of device.

Family Designator	Family
OSD	OSD Family of devices.

**Processor Designator** – A set of letters and numbers that designate the specific processor in the device. Table 3.1 shows the valid values for the Processor Designator.

Table 3.1. Processor Designators

Processor Designator	Processor
3358	Texas Instruments AM3358

**Memory Designator** – A set of letters and numbers that designate the DDR3 memory size in the device. Table 3.2 shows the valid values for the Memory Designator.

Table 3.2. Memory Designator

Memory Designator	DDR Memory Size
1G	1GB DDR3
512M	512 MB DDR3

# OSD335x-SM Family

Rev. 6 2/16/2018



**Temp Designator** – A letter or number that designates the temperature range of the device. Table 3.3 shows the valid values for the Temp Designator.

*Table 3.3. Temp Designator*

Temp Designator	Temperature Range
B	Commercial: 0 to 85°C
I	Industrial: -40 to 85°C

**Trim Designator** – A set of letters and numbers that designate the set of features in the device. Table 3.4 shows the valid values for the Trim Designator.

*Table 3.4. Trim Designator*

Trim Designator	Device Options
SM	Base Model containing the Processor, DDR Memory, PMIC, LDO and 4KB EEPROM in 21mm x 21mm 256 Ball BGA

## 4 Reference Documents

### 4.1 Data Sheets

Below are links to the data sheets for the key devices used in the OSD335x-SM. Please refer to them for specifics on that device. The remainder of this document will describe how the devices are used in the OSD335x-SM system. It will also highlight any differences between the performance stated in the device specific datasheet and what should be expected from its operation in the OSD335x-SM.

- Processor AM335X <http://www.ti.com/product/am3358/datasheet>
- PMIC TPS62517C <http://www.ti.com/product/TPS65217/datasheet>
- LDO TL509 <http://www.ti.com/product/TL5209/datasheet>
- EEPROM 24LC32A <http://www.microchip.com/wwwproducts/en/24LC32A>

### 4.2 Other References

This section contains links to other reference documents that could be helpful when using the OSD335x-SM device. Some are referenced in this document.

- TI AN-2029 – Handling & Process recommendations  
<http://www.ti.com/lit/snoa550>
- OSD335x-SM Pin Assignments and Application Differences from TI AM3358  
[https://octavosystems.com/app\\_notes/osd335x-family-pin-assignments/](https://octavosystems.com/app_notes/osd335x-family-pin-assignments/)
- OSD335x-SM Layout Guide  
[https://octavosystems.com/app\\_notes/osd335x-sm-layout-guide/](https://octavosystems.com/app_notes/osd335x-sm-layout-guide/)
- AM335x DR PHY register configuration for DDR3 using Software Leveling  
[http://processors.wiki.ti.com/index.php/AM335x\\_DDR\\_PHY\\_register\\_configuration\\_for\\_DDR3\\_using\\_Software\\_Leveling](http://processors.wiki.ti.com/index.php/AM335x_DDR_PHY_register_configuration_for_DDR3_using_Software_Leveling)
- AM335x Power Estimation Tool  
[http://processors.wiki.ti.com/index.php/AM335x\\_Power\\_Estimation\\_Tool](http://processors.wiki.ti.com/index.php/AM335x_Power_Estimation_Tool)
- Powering the AM335x with the TPS62517x  
<http://www.ti.com/lit/slvu551>
- OSD3358-SM Reference, Evaluation and Development Platform  
[https://octavosystems.com/octavo\\_products/osd3358-sm-red/](https://octavosystems.com/octavo_products/osd3358-sm-red/)

# OSD335x-SM Family

Rev. 6 2/16/2018



## 5 Ball Map

The pins on the OSD335x-SM belong to 4 distinct categories, AM335x Signals, TPS65217C signals, Oscillators and Power Domains. The signal names for the AM335x and the TPS65217C have been named so they can be easily cross-referenced to the corresponding pin in the TI Datasheet.

All AM335x signals on the OSD335x-SM Ball Map match the signal names of the default functions in the AM335x datasheet.

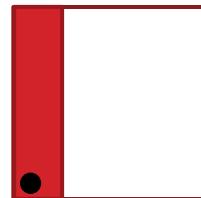
All the TPS65217C signals have the prefix PMIC\_ then the TPS65217C signal name from the TI Datasheet.

***NOTE: This is true except for the signal PMIC\_POWER\_EN which is an AM335x signal.***

The arrangement of the signals has been optimized for easy escape of the BGA. Table 5.1 through Table 5.4 show the ball map for the OSD335x-SM.

Table 5.1. OSD335x-SM Ball Map Top View (Columns A-D)

	<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>
<b>16</b>	MMC0_DAT0	MMC0_CMD	MMC0_DAT2	MII1_RXD1
<b>15</b>	MMC0_DAT1	MMC0_CLK	MMC0_DAT3	MII1_RXD2
<b>14</b>	SPI0_CS0	SPI0_D1	SPI0_CS1	MII1_RXD3
<b>13</b>	SPI0_SCLK	SPI0_D0	UART0_RTSN	MDC
<b>12</b>	UART0_RXD	UART0_TXD	UART0_CTSN	NC
<b>11</b>	UART1_RXD	UART1_TXD	I2C0_SDA	PMIC_SDA
<b>10</b>	UART1_RTSN	UART1_CTSN	I2C0_SCL	PMIC_SCL
<b>9</b>	AGND_ADC	VREFN	AIN6	DGND
<b>8</b>	AIN0	AIN1	AIN5	DGND
<b>7</b>	SYS_ADC_1P8V	VREFP	AIN4	AIN7
<b>6</b>	OSC1_IN	AIN2	AIN3	PMIC_MUX_OUT
<b>5</b>	OSC1_OUT	OSC1_GND	ECAP0_IN_PWM0_OUT	CAP_VDD_RTC
<b>4</b>	XDMA_EVENT_INTR0	XDMA_EVENT_INTR1	MCASP0_AHCLKX	EXTINTN
<b>3</b>	MCASP0_ACLKR	MCASP0_FSR	MCASP0_AXR1	TRSTN
<b>2</b>	MCASP0_FSX	MCASP0_AXR0	TDO	TMS
<b>1</b>	MCASP0_ACLKX	MCASP0_AHCLKR	TDI	TCK



# OSD335x-SM Family

Rev. 6 2/16/2018

Table 5.2. OSD335x-SM Ball Map Top View (Columns E-H)

	<b>E</b>	<b>F</b>	<b>G</b>	<b>H</b>
<b>16</b>	MII1_RX_CLK	MII1_RX_DV	MII1_TXD2	MII1_TX_CLK
<b>15</b>	MII1_RX_ER	MII1_COL	MII1_TXD3	MII1_TXD0
<b>14</b>	MII1_RXD0	MII1_CRS	MII1_TX_EN	MII1_TXD1
<b>13</b>	MDIO	VDD_MPU	VDDS_PLL	DGND
<b>12</b>	DGND	DGND	DGND	DGND
<b>11</b>	DGND	SYS_VDD2_3P3V	SYS_VDD2_3P3V	SYS_VDD_1P8V
<b>10</b>	DGND	SYS_VDD_1P8V	SYS_VDD_1P8V	SYS_VDD_1P8V
<b>9</b>	DGND	VDDSHV4	VDDSHV5	VDDSHV6
<b>8</b>	DGND	SYS_VDD3_3P3V	SYS_VDD3_3P3V	SYS_VDD3_3P3V
<b>7</b>	DGND	SYS_VDD1_3P3V	SYS_VDD1_3P3V	SYS_VDD3_3P3V
<b>6</b>	DGND	SYS_VDD1_3P3V	SYS_VDD1_3P3V	VPP
<b>5</b>	DGND	DGND	DGND	DGND
<b>4</b>	PMIC_NINT	VDDS_DDR	VDD_CORE	DGND
<b>3</b>	EMU1	LCD_VSYNC	LCD_DATA0	LCD_DATA3
<b>2</b>	EMU0	LCD_HSYNC	LCD_DATA1	LCD_DATA4
<b>1</b>	LCD_AC_BIAS_EN	LCD_PCLK	LCD_DATA2	LCD_DATA5

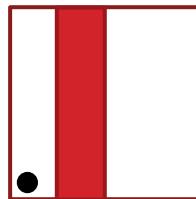
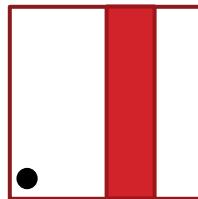


Table 5.3. OSD335x-SM Ball Map Top View (Columns J-M)

	<b>J</b>	<b>K</b>	<b>L</b>	<b>M</b>
<b>16</b>	USB0_VBUS	USB0_DM	USB1_DM	RTC_KALDO_ENN
<b>15</b>	USB0_DRVVBUS	USB0_DP	USB1_DP	USB1_VBUS
<b>14</b>	RMII1_REF_CLK	USB0_ID	USB1_ID	USB1_DRVVBUS
<b>13</b>	DGND	USB0_CE	USB1_CE	PMIC_NRESET
<b>12</b>	DGND	DGND	DGND	DGND
<b>11</b>	SYS_VDD_1P8V	SYS_RTC_1P8V	SYS_RTC_1P8V	DGND
<b>10</b>	SYS_VDD_1P8V	SYS_VDD_1P8V	SYS_VDD_1P8V	DGND
<b>9</b>	VDDSHV1	VDDSHV2	VDDSHV3	DGND
<b>8</b>	SYS_VDD3_3P3V	SYS_VDD3_3P3V	SYS_VDD3_3P3V	DGND
<b>7</b>	SYS_VDD3_3P3V	SYS_VOUT	SYS_VOUT	DGND
<b>6</b>	NC	SYS_VOUT	SYS_VOUT	DGND
<b>5</b>	DGND	DGND	DGND	DGND
<b>4</b>	DGND	NC	PMIC_NWAKEUP	EXT_WAKEUP
<b>3</b>	LCD_DATA6	LCD_DATA9	LCD_DATA12	LCD_DATA15
<b>2</b>	LCD_DATA7	LCD_DATA10	LCD_DATA13	EEPROM_WP
<b>1</b>	LCD_DATA8	LCD_DATA11	LCD_DATA14	GPMC_ADVN_ALE



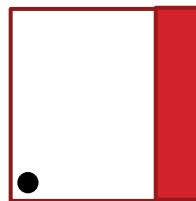
## OSD335x-SM Family

Rev. 6 2/16/2018



Table 5.4. OSD335x-SM Ball Map Top View (Columns N-T)

	<b>N</b>	<b>P</b>	<b>R</b>	<b>T</b>
<b>16</b>	OSC0_OUT	OSC0_IN	GPMC_WPN	GPMC_A11
<b>15</b>	OSC0_GND	GPMC_WAIT0	GPMC_A10	GPMC_A9
<b>14</b>	GPMC_BEN1	GPMC_A8	GPMC_A7	GPMC_A6
<b>13</b>	PMIC_MUX_IN	GPMC_A5	GPMC_A4	GPMC_A3
<b>12</b>	PMIC_PGOOD	GPMC_A2	GPMC_A1	GPMC_A0
<b>11</b>	PMIC_PWR_EN	PWRONRSTN	WARMRSTN	PMIC_PB_IN
<b>10</b>	PMIC_POWER_EN	VIN_AC	VIN_AC	VIN_AC
<b>9</b>	DGND	VIN_USB	VIN_USB	VIN_USB
<b>8</b>	DGND	VIN_BAT	VIN_BAT	VIN_BAT
<b>7</b>	PMIC_BAT_SENSE	GPMC_AD15	GPMC_CSN3	GPMC_CLK
<b>6</b>	PMIC_TS	GPMC_AD12	GPMC_AD13	GPMC_AD14
<b>5</b>	RTC_PWRONRSTN	GPMC_AD9	GPMC_AD10	GPMC_AD11
<b>4</b>	PMIC_LDO_PGOOD	GPMC_AD6	GPMC_AD7	GPMC_AD8
<b>3</b>	GPMC_BEN0_CLE	GPMC_CSN0	GPMC_AD0	GPMC_AD3
<b>2</b>	GPMC_WEN	GPMC_CSN1	GPMC_AD1	GPMC_AD4
<b>1</b>	GPMC_OEN_REN	GPMC_CSN2	GPMC_AD2	GPMC_AD5



## 5.1 Ball Description

Table 5.5 lists all the unique balls of the OSD335x-SM and gives a brief explanation of their function. The table also lists the equivalent pin number for the signal on the OSD335x package and the AM335x ZCZ package. For more detail please refer to the datasheet in section 4.1 for the individual device that ball is associated with.

Table 5.5 OSD335x-SM Ball Descriptions

Pin Name	Description	Pin Number	
		OSD335x-SM	AM335x (ZCZ)
<b>AGND_ADC</b>	Analog Ground (VSSA_ADC in AM335x)	A9	E8
<b>AIN0</b>	Analog Input / Output	A8	B6
<b>AIN1</b>	Analog Input / Output	B8	C7
<b>AIN2</b>	Analog Input / Output	B6	B7
<b>AIN3</b>	Analog Input / Output	C6	A7
<b>AIN4</b>	Analog Input / Output	C7	C8
<b>AIN5</b>	Analog Input	C8	B8
<b>AIN6</b>	Analog Input	C9	A8
<b>AIN7</b>	Analog Input	D7	C9
<b>CAP_VDD_RTC</b>	RTC Supply Voltage Input	D5	D6
<b>DGND</b>	Digital Ground (VSS in AM335x)	D8, D9, E5, E6, E7, E8, E9, E10, E11, E12, F5, F12, G5, G12, H4, H5, H12, H13, J4, J5, J12, J13, K5, K12, L5, L12, M5, M6, M7, M8, M9, M10, M11, M12, N8, N9	See VSS pin in AM335x datasheet.
<b>ECAP0_IN_PWM0_OUT</b>	Enhanced Capture 0 Input or PWM0 Output	C5	C18
<b>EEPROM_WP</b>	EEPROM Write Protect Pin	M2	N/A
<b>EMU0</b>	Miscellaneous Emulation Pin	E2	C14
<b>EMU1</b>	Miscellaneous Emulation Pin	E3	B14
<b>EXTINTN</b>	AM335x External Interrupt to ARM Cortex-A8	D4	B18
<b>EXT_WAKEUP</b>	AM335x EXT_WAKEUP Input	M4	C5
<b>GPMC_A0</b>	GPMC Address	T12	R13
<b>GPMC_A1</b>	GPMC Address	R12	V14
<b>GPMC_A2</b>	GPMC Address	P12	U14
<b>GPMC_A3</b>	GPMC Address	T13	T14
<b>GPMC_A4</b>	GPMC Address	R13	R14
<b>GPMC_A5</b>	GPMC Address	P13	V15
<b>GPMC_A6</b>	GPMC Address	T14	U15
<b>GPMC_A7</b>	GPMC Address	R14	T15
<b>GPMC_A8</b>	GPMC Address	P14	V16
<b>GPMC_A9</b>	GPMC Address	T15	U16
<b>GPMC_A10</b>	GPMC Address	R15	T16
<b>GPMC_A11</b>	GPMC Address	T16	V17
<b>GPMC_AD0</b>	GPMC Address and Data	R3	U7
<b>GPMC_AD1</b>	GPMC Address and Data	R2	V7
<b>GPMC_AD2</b>	GPMC Address and Data	R1	R8
<b>GPMC_AD3</b>	GPMC Address and Data	T3	T8
<b>GPMC_AD4</b>	GPMC Address and Data	T2	U8
<b>GPMC_AD5</b>	GPMC Address and Data	T1	V8
<b>GPMC_AD6</b>	GPMC Address and Data	P4	R9
<b>GPMC_AD7</b>	GPMC Address and Data	R4	T9
<b>GPMC_AD8</b>	GPMC Address and Data	T4	U10
<b>GPMC_AD9</b>	GPMC Address and Data	P5	T10
<b>GPMC_AD10</b>	GPMC Address and Data	R5	T11
<b>GPMC_AD11</b>	GPMC Address and Data	T5	U12
<b>GPMC_AD12</b>	GPMC Address and Data	P6	T12
<b>GPMC_AD13</b>	GPMC Address and Data	R6	R12
<b>GPMC_AD14</b>	GPMC Address and Data	T6	V13

# OSD335x-SM Family

Rev. 6 2/16/2018

<b>GPMC_AD15</b>	GPMC Address and Data	P7	U13
<b>GPMC_ADVN_ALE</b>	GPMC Address Valid / Address Latch Enable	M1	R7
<b>GPMC_BEN0_CLE</b>	GPMC Byte Enable 0 / Command Latch Enable	N3	T6
<b>GPMC_BEN1</b>	GPMC Byte Enable 1	N14	U18
<b>GPMC_CLK</b>	GPMC Clock	T7	V12
<b>GPMC_CSN0</b>	GPMC Chip Select	P3	V6
<b>GPMC_CSN1</b>	GPMC Chip Select	P2	U9
<b>GPMC_CSN2</b>	GPMC Chip Select	P1	V9
<b>GPMC_CSN3</b>	GPMC Chip Select	R7	T13
<b>GPMC_OEN_REN</b>	GPMC Output Enable / Read Enable	N1	T7
<b>GPMC_WAIT0</b>	GPMC Wait 0	P15	T17
<b>GPMC_WEN</b>	GPMC Write Enable	N2	U6
<b>GPMC_WPN</b>	GPMC Write Protect	R16	U17
<b>I2C0_SCL</b>	I2C Clock	C10	C16
<b>I2C0_SDA</b>	I2C Data	C11	C17
<b>LCD_AC_BIAS_EN</b>	LCD AC Bias Enable Chip Select	E1	R6
<b>LCD_DATA0</b>	LCD Data Bus	G3	R1
<b>LCD_DATA1</b>	LCD Data Bus	G2	R2
<b>LCD_DATA2</b>	LCD Data Bus	G1	R3
<b>LCD_DATA3</b>	LCD Data Bus	H3	R4
<b>LCD_DATA4</b>	LCD Data Bus	H2	T1
<b>LCD_DATA5</b>	LCD Data Bus	H1	T2
<b>LCD_DATA6</b>	LCD Data Bus	J3	T3
<b>LCD_DATA7</b>	LCD Data Bus	J2	T4
<b>LCD_DATA8</b>	LCD Data Bus	J1	U1
<b>LCD_DATA9</b>	LCD Data Bus	K3	U2
<b>LCD_DATA10</b>	LCD Data Bus	K2	U3
<b>LCD_DATA11</b>	LCD Data Bus	K1	U4
<b>LCD_DATA12</b>	LCD Data Bus	L3	V2
<b>LCD_DATA13</b>	LCD Data Bus	L2	V3
<b>LCD_DATA14</b>	LCD Data Bus	L1	V4
<b>LCD_DATA15</b>	LCD Data Bus	M3	T5
<b>LCD_HSYNC</b>	LCD Horizontal Sync	F2	R5
<b>LCD_PCLK</b>	LCD Pixel Clock	F1	V5
<b>LCD_VSYNC</b>	LCD Vertical Sync	F3	U5
<b>MCASP0_ACLKR</b>	McASP0 Receive Bit Clock	A3	B12
<b>MCASP0_ACLKX</b>	McASP0 Transmit Bit Clock	A1	A13
<b>MCASP0_AHCLKR</b>	McASP0 Receive Master Clock	B1	C12
<b>MCASP0_AHCLKX</b>	McASP0 Transmit Master Clock	C4	A14
<b>MCASP0_AXR0</b>	McASP0 Serial Data	B2	D12
<b>MCASP0_AXR1</b>	McASP0 Serial Data	C3	D13
<b>MCASP0_FSR</b>	McASP0 Receive Frame Sync	B3	C13
<b>MCASP0_FSX</b>	McASP0 Transmit Frame Sync	A2	B13
<b>MDC</b>	MDIO Clock	D13	M18
<b>MDIO</b>	MDIO Data	E13	M17
<b>MII1_COL</b>	MII Collision	F15	H16
<b>MII1_CRS</b>	MII Carrier Sense	F14	H17
<b>MII1_RX_CLK</b>	MII Receive Clock	E16	L18
<b>MII1_RX_DV</b>	MII Receive Data Valid	F16	J17
<b>MII1_RX_ER</b>	MII Receive Data Error	E15	J15
<b>MII1_RXD0</b>	MII Receive Data	E14	M16
<b>MII1_RXD1</b>	MII Receive Data	D16	L15
<b>MII1_RXD2</b>	MII Receive Data	D15	L16
<b>MII1_RXD3</b>	MII Receive Data	D14	L17
<b>MII1_TX_CLK</b>	MII Transmit Clock	H16	K18
<b>MII1_TX_EN</b>	MII Transmit Enable	G14	J16
<b>MII1_TXD0</b>	MII Transmit Data	H15	K17
<b>MII1_TXD1</b>	MII Transmit Data	H14	K16
<b>MII1_TXD2</b>	MII Transmit Data	G16	K15
<b>MII1_TXD3</b>	MII Transmit Data	G15	J18
<b>MMC0_CLK</b>	MMC/SD/SDIO Clock	B15	G17
<b>MMC0_CMD</b>	MMC/SD/SDIO Command	B16	G18
<b>MMC0_DAT0</b>	MMC/SD/SDIO Data	A16	G16

<b>MMC0_DAT1</b>	MMC/SD/SDIO Data	A15	G15
<b>MMC0_DAT2</b>	MMC/SD/SDIO Data	C16	F18
<b>MMC0_DAT3</b>	MMC/SD/SDIO Data	C15	F17
<b>NC</b>	No Connect	D12, J6, K4	N/A
<b>OSC0_GND</b>	High Frequency Oscillator Ground (VSS_OSC)	N15	V11
<b>OSC0_IN</b>	High Frequency Oscillator Input (XTALIN)	P16	V10
<b>OSC0_OUT</b>	High Frequency Oscillator Output (XTALOUT)	N16	U11
<b>OSC1_GND</b>	Real Time Clock Oscillator Ground (VSS_RTC)	B5	A5
<b>OSC1_IN</b>	Real Time Clock Oscillator Input (RTC_XTALIN)	A6	A6
<b>OSC1_OUT</b>	Real Time Clock Oscillator Output (RTC_XTALOUT)	A5	A4
<b>PMIC_BAT_SENSE</b>	TPS65217C BAT_SENSE Input	N7	N/A
<b>PMIC_LDO_PGOOD</b>	TPS65217C LDO_PGOOD Output	N4	N/A
<b>PMIC_MUX_IN</b>	TPS65217C MUX_IN Input	N13	N/A
<b>PMIC_MUX_OUT</b>	TPS65217C MUX_OUT Output	D6	N/A
<b>PMIC_NINT</b>	TPS65217C NINT Output	E4	N/A
<b>PMIC_NRESET</b>	TPS65217C NRESET Input	M13	N/A
<b>PMIC_NWAKEUP</b>	TPS65217C NWAKEUP Output	L4	N/A
<b>PMIC_PB_IN</b>	TPS65217C PB_IN Input	T11	N/A
<b>PMIC_PGOOD</b>	TPS65217C PGOOD Output	N12	N/A
<b>PMIC_POWER_EN</b>	AM335x PMIC_POWER_EN Output	N10	C6
<b>PMIC_PWR_EN</b>	TPS65217C PWR_EN Input	N11	N/A
<b>PMIC_SCL</b>	TPS65217C SCL Input	D10	N/A
<b>PMIC_SDA</b>	TPS65217C SDA Input / Output	D11	N/A
<b>PMIC_TS</b>	TPS65217C TS Input	N6	N/A
<b>PWRONRSTN</b>	Power On Reset Input (Active Low)	P11	B15
<b>RMII1_REF_CLK</b>	RMII Reference Clock	J14	H18
<b>RTC_KALDO_ENN</b>	Enable input for internal CAP_VDD_RTC voltage regulator (Active Low)	M16	B4
<b>RTC_PWRONRSTN</b>	RTC Reset Input (Active Low)	N5	B5
<b>SPI0_CS0</b>	SPI Chip Select	A14	A16
<b>SPI0_CS1</b>	SPI Chip Select	C14	C15
<b>SPI0_D0</b>	SPI Data	B13	B17
<b>SPI0_D1</b>	SPI Data	B14	B16
<b>SPI0_SCLK</b>	SPI Clock	A13	A17
<b>SYS_ADC_1P8V</b>	Output Power Supply, Analog, 1.8VDC	A7	N/A
<b>SYS_RTC_1P8V</b>	Output Power Supply, RTC, 1.8VDC	K11, L11	N/A
<b>SYS_VDD_1P8V</b>	Output Power Supply, Digital, 1.8VDC	F10, G10, H10, H11, J10, J11, K10, L10	N/A
<b>SYS_VDD1_3P3V</b>	Output Power Supply, Primary, 3.3VDC	F6, F7, G6, G7	N/A
<b>SYS_VDD2_3P3V</b>	Output Power Supply, Secondary, 3.3VDC	F11, G11	N/A
<b>SYS_VDD3_3P3V</b>	Output Power Supply, I/O, 3.3VDC	F8, G8, H7, H8, J7, J8, K8, L8	N/A
<b>SYS_VOUT</b>	TPS65217C SYS Output	K6, K7, L6, L7	N/A
<b>TCK</b>	JTAG Test Clock	D1	A12
<b>TDI</b>	JTAG Test Data Input	C1	B11
<b>TDO</b>	JTAG Test Data Output	C2	A11
<b>TMS</b>	JTAG Test Mode Select	D2	C11
<b>TRSTN</b>	JTAG Test Reset	D3	B10
<b>UART0_CTSN</b>	UART Clear to Send	C12	E18
<b>UART0_RTSN</b>	UART Request to Send	C13	E17
<b>UART0_RXD</b>	UART Receive Data	A12	E15
<b>UART0_TXD</b>	UART Transmit Data	B12	E16
<b>UART1_CTSN</b>	UART Clear to Send	B10	D18
<b>UART1_RTSN</b>	UART Request to Send	A10	D17
<b>UART1_RXD</b>	UART Receive Data	A11	D16
<b>UART1_TXD</b>	UART Transmit Data	B11	D15
<b>USB0_CE</b>	USB0 Charger Enable Output	K13	M15
<b>USB0_DM</b>	USB0 Data (-)	K16	N18
<b>USB0_DP</b>	USB0 Data (+)	K15	N17
<b>USB0_DRVVBUS</b>	USB0 VBUS Control Output	J15	F16
<b>USB0_ID</b>	USB0 OTG ID	K14	P16
<b>USB0_VBUS</b>	USB0 VBUS	J16	P15

# OSD335x-SM Family

Rev. 6 2/16/2018

<b>USB1_CE</b>	USB1 Charger Enable Output	L13	P18
<b>USB1_DM</b>	USB1 Data (-)	L16	R18
<b>USB1_DP</b>	USB1 Data (+)	L15	R17
<b>USB1_DRVVBUS</b>	USB1 VBUS Control Output	M14	F15
<b>USB1_ID</b>	USB1 OTG ID	L14	P17
<b>USB1_VBUS</b>	USB1 VBUS	M15	T18
<b>VDD_CORE</b>	Internal Power Supply Test Point	G4	N/A
<b>VDD_MPU</b>	Internal Power Supply Test Point	F13	N/A
<b>VDDS_DDR</b>	Internal Power Supply Test Point	F4	N/A
<b>VDDS_PLL</b>	Internal Power Supply Test Point	G13	N/A
<b>VDDSHV1</b>	Supply voltage for the dual-voltage IO domain	J9	P7, P8
<b>VDDSHV2</b>	Supply voltage for the dual-voltage IO domain	K9	P10, P11
<b>VDDSHV3</b>	Supply voltage for the dual-voltage IO domain	L9	P12, P13
<b>VDDSHV4</b>	Supply voltage for the dual-voltage IO domain	F9	H14, J14
<b>VDDSHV5</b>	Supply voltage for the dual-voltage IO domain	G9	K14, L14
<b>VDDSHV6</b>	Supply voltage for the dual-voltage IO domain	H9	E10, E11, E12, E13, F14, G14, N5, P5, P6
<b>VIN_AC</b>	TPS65217C AC Input	P10, R10, T10	N/A
<b>VIN_BAT</b>	TPS65217C BAT Input / Output	P8, R8, T8	N/A
<b>VIN_USB</b>	TPS65217C USB Input	P9, R9, T9	N/A
<b>VPP</b>	RESERVED	H6	M5
<b>VREFN</b>	Analog Negative Reference Input	B9	A9
<b>VREFP</b>	Analog Positive Reference Input	B7	B9
<b>WARMRSTN</b>	Warm Reset (Active Low)	R11	A10
<b>XDMA_EVENT_INTR0</b>	External DMA Event or Interrupt 0	A4	A15
<b>XDMA_EVENT_INTR1</b>	External DMA Event or Interrupt 1	B4	D14

## 5.2 Not Connected Balls

The OSD335x-SM ball map contains balls which are marked NC (No Connect). These balls must remain unconnected on the system PCB since they may be used for other purposes in future versions of the OSD335x-SM.

## 5.3 Reserved Signals

There is a subset of signals that are available on the OSD335x-SM ball map but **should not be** used externally to the device. These signals are used internally to the OSD335x-SM and using them could significantly affect the performance of the device. They are provided for test purposes only. The list of signals that should not be used can be found in Table 5.6.



Table 5.6. Reserved Signals

Reserved Signals
VPP
VDD_CORE
VDD_MPU
VDDS_DDR
VDDS_PLL

## 6 OSD335x-SM Components

The OSD335x-SM integrates the Texas Instruments ARM® Cortex®-A8 Sitara™ AM335x processor along with the TI TPS65217C PMIC, the TI TL5209 LDO, up to 1 GB of DDR3 Memory, a 4KB EEPROM for non-volatile configuration storage and the resistors, capacitors, and inductors into a single design-in-ready package. The following section contains any specific device information needed for the integrated components to design your system with the OSD335x-SM.

### 6.1 AM335x Processor

The heart of the OSD335x-SM is the Texas Instruments ARM® Cortex®-A8 Sitara™ AM335x processor. The processor in the OSD335x-SM is configured to perform identically to a standalone device. Please refer to the data sheet in the Reference Documents section for details on using the AM335x processor.

#### 6.1.1 I/O Voltages

The OSD335x-SM allows the I/O voltage domains (VDDSHVx) of the AM335x to be set to either 1.8V or 3.3V. The VDDSHVx pins of the OSD335x-SM (ie VDDSHV1 thru VDDSHV6), which can be found in Table 5.5, must be connected to either a 1.8V or 3.3V power source in order to provide power to the I/Os. Recommendations on how to connect the I/O voltage domain pins is in the OSD335x-SM Layout Guide in the Reference Documents section.



See the AM335x datasheet in the Reference Documents section for more information on the pins associated with each I/O voltage domain.

### 6.2 DDR3 Memory

The OSD335x-SM integrates a DDR3 memory into the device and handles all the connections needed between the AM335x and the DDR3. You will still have to set the proper registers to configure the AM335x DDR PHY to work correctly with the memory included in the OSD335x-SM. Typically, this would require you to run through the procedure outlined in the AM335x DDR PHY register configuration for DDR3 using Software Leveling referred to in the Reference Documents section of this document. This procedure has been run for the OSD335x-SM and a list of the recommended values for the registers is provided in Table 6.1. It is recommended that you use this set of values for optimal performance.

# OSD335x-SM Family

Rev. 6 2/16/2018



Table 6.1 AM335x DDR EMIF, PHY and Control Module Register Settings

Register Name	Peripheral	Recommended Value
DDR_CMDx_ICTRL <sup>(1)</sup>	Control Module	0x0000018B
DDR_DATAx_ICTRL <sup>(2)</sup>	Control Module	0x0000018B
SDRAM_CONFIG	EMIF	0x61C05332
SDRAM_CONFIG_2	EMIF	0x00000000
SDRAM_REF_CTRL	EMIF	0x00000C30
SDRAM_TIM_1	EMIF	0x0AAD4DB
SDRAM_TIM_2	EMIF	0x266B7FDA
SDRAM_TIM_3	EMIF	0x501F867F
ZQ_CONFIG	EMIF	0x50074BE4
DDR_PHY_CTRL_1	EMIF	0x00100007
CMDx_REG_PHY_CTRL_SLAVE_RATIO_0 <sup>(1)</sup>	DDR PHY	0x00000080
CMDx_REG_PHY_INVERT_CLKOUT_0 <sup>(1)</sup>	DDR PHY	0x00000000
DATAx_REG_PHY_RD_DQS_SLAVE_RATIO_0 <sup>(2)</sup>	DDR PHY	0x0000003A
DATAx_REG_PHY_WR_DQS_SLAVE_RATIO_0 <sup>(2)</sup>	DDR PHY	0x00000045
DATAx_REG_PHY_FIFO_WE_SLAVE_RATIO_0 <sup>(2)</sup>	DDR PHY	0x00000095
DATAx_REG_PHY_WR_DATA_SLAVE_RATIO_0 <sup>(2)</sup>	DDR PHY	0x0000007F

<sup>(1)</sup> "CMDx" refers to registers where x is in [0, 1, 2]

<sup>(2)</sup> "DATAx" refers to registers where x is in [0, 1]

Settings in Table 6.1 are recommended and supported. Other values may work but are not guaranteed. If you want to rerun the calibration yourself the seed values provided in Table 6.2 should be used.

Table 6.2 AM335x DDR PHY Calibration Seed Values

DATAx_PHY_RD_DQS_SLAVE_RATIO	40
DATAx_PHY_FIFO_WE_SLAVE_RATIO	64
DATAx_PHY_WR_DQS_SLAVE_RATIO	0

## 6.3 EEPROM

The OSD335x-SM contains a 4KB EEPROM for non-volatile storage of configuration information. The EEPROM is connected to I2C0 at the 7-bit I2C address 0x50 (0b1010000). Please refer to the data sheet in the Reference Documents section for details on using the EEPROM.

### 6.3.1 EEPROM Contents

EEPROM address space 0x000 to 0xEFF is empty and can be used for board specific information during system boot. The final 256 bytes of the EEPROM (0xF00 to 0xFFFF) are reserved for device specific information. The reserved space contents of the EEPROM can be found in Table 6.3

Table 6.3 EEPROM Contents Programmed by Octavo Systems

Name	Description	Size (bytes)	Start address	End address	Contents
RSVD	Reserved for Future Use	256	0xF00	0xFFFF	All 0xFF

### 6.3.2 EEPROM Write Protection

By default, the EEPROM is write protected (ie. the EEPROM\_WP pin is pulled high as seen in Table 2.1). To program values into the EEPROM, it is required to drive the EEPROM\_WP pin to a logic low. See the OSD335x-SM Layout Guide in the Reference Documents section for layout / manufacturing recommendations for the EEPROM\_WP pin.



# OSD335x-SM Family

Rev. 6 2/16/2018

## 7 Power Management

The power management portion of the OSD335x-SM consists of two devices, the TPS65217C (PMIC) and the TL5209 (LDO). The PMIC provides the necessary power rails to the AM335x and the DDR3 while the LDO is not used inside the SiP. Both devices provide power supply outputs that may be used to power circuitry external to the OSD335x-SM. This section describes how to power the OSD335x-SM in a system and the outputs that can be used.

### 7.1 Input Power

The OSD335x-SM may be powered by any combination of the following input power supplies. Please refer to the TPS65217C datasheet for details.

The maximum risetime for input rails VIN\_AC and VIN\_USB (defined as time for the input voltage to rise from 100 mV to 4.5 V) is 50 ms. The device may fail to power up properly if this requirement is not met.



#### 7.1.1 VIN\_AC

The OSD335x-SM may be powered by an external AC Adaptor at 5.0 VDC.

#### 7.1.2 VIN\_USB

The OSD335x-SM may be powered by a USB port at 5.0 VDC.

#### 7.1.3 VIN\_BAT

The OSD335x-SM may be powered by a single cell (1S) Li-Ion or Li-Polymer Battery nominally at 3.7 VDC.



Due to the dropout behavior of the LDO TL5209, its output voltage rail SYS\_VDD1\_3P3V should not be used when the OSD335x is being powered through VIN\_BAT. Please refer to the TL5209 datasheet for details.

## 7.2 Output Power

The OSD335x-SM produces the following output power supplies.

### 7.2.1 SYS\_VOUT: Switched VIN\_AC, VIN\_USB, or VIN\_BAT

The OSD335x-SM contains a shared supply to power the AM335x, DDR3, and TL5209 which is also used to power external circuitry. This is supplied by the TPS65217C SYS output. The SYS output is a switched connection to one of the input power supplies selected by the TPS65217C as described in the datasheet for that device.

### 7.2.2 SYS\_VDD1\_3P3V

The OSD335x-SM contains a dedicated 3.4 VDC supply<sup>1</sup> to power external circuitry. This is supplied by the TL5209, powered by the TPS65217C SYS output, and enabled by the TPS65217C LDO4.

 Due to the dropout behavior of the LDO TL5209, the SYS\_VDD1\_3P3V rail should not be used when the OSD335x is being powered through VIN\_BAT. Please refer to the TL5209 datasheet for details.

### 7.2.3 SYS\_VDD2\_3P3V

The OSD335x-SM contains a dedicated 3.3 VDC supply to power external circuitry. This is supplied by the TPS65217C LDO2.

### 7.2.4 SYS\_VDD3\_3P3V

The OSD335x-SM contains a shared 3.3 VDC supply that can be used to power the AM335x I/O domains (VDDSHVx). This is supplied by the TPS65217C LDO4.

### 7.2.5 SYS\_RTC\_1P8V

The OSD335x-SM contains a shared 1.8 VDC supply to power the AM335x RTC which may also be used to power external circuitry. This is supplied by the TPS65217C LDO1.

 Please note that the AM335x in the OSD335x is powered by TPS65217 PMIC **version C** which does not support RTC only mode.

### 7.2.6 SYS\_VDD\_1P8V

The OSD335x-SM contains a shared 1.8 VDC supply that may be used to power the AM335x I/O domains (VDDSHVx) and external circuitry. It also supplies power to the AM335x SRAM, PLLs and USB. This is supplied by the TPS65217C LDO3.

### 7.2.7 SYS\_ADC\_1P8V

The OSD335x-SM contains a shared 1.8 VDC supply to power the AM335x ADC which may also be used to power external analog circuitry. This is supplied by the TPS65217C LDO3 and filtered for analog applications.

## 7.3 Internal Power

 The OSD335x-SM has internal power supplies that are not available to power external circuitry. To do so will prevent the OSD335x from functioning properly. The power supplies are accessible externally for monitoring purposes only.

### 7.3.1 VDDS\_DDR

The OSD335x-SM contains a dedicated 1.5 VDC supply to power the AM335x DDR3 interface and the DDR3 device. This is supplied by the TPS65217C DCDC1.

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<sup>1</sup> The LDO has an accuracy of 1 – 2% depending on the ambient temperature which will also affect the nominal voltage. See the TL5209 datasheet for more information.

### 7.3.2 VDD\_MPUs

The OSD335x-SM contains a dedicated 1.1 VDC supply to power the AM335x MPU domain. This is supplied by the TPS65217C DCDC2.

### 7.3.3 VDD\_CORE

The OSD335x-SM contains a dedicated 1.1 VDC supply to power the AM335x CORE domain. This is supplied by the TPS65217C DCDC3.

### 7.3.4 VDDPLL\_PLL

The OSD335x-SM contains a filtered 1.8 VDC supply to power the AM335x PLLs and oscillators. This is supplied by the TPS65217C LDO3.

## 7.4 Total Current Consideration



The total current consumption of all power rails must not exceed the recommended input currents described in Table 8.2. This includes power consumption within the SiP from the AM335x and the DDR3, as well as all external loads on the output power rails from Section 7.2.

The power consumed by the AM335x can be estimated using the *AM335x Power Estimation Tool* found in the Reference Documents section of this document. When estimating power consumption, the efficiencies and types of the OSD335x-SM internal power supplies must be considered. Refer to the “*Connections Diagram for TPS65217C and AM335x*” section of *Powering the AM335x with the TPS65217x* found in the Reference Documents section of this document for more information on the power supplies providing power to the AM335x.

## 7.5 Control and Status

The control and status connections for Processor-PMIC interface and RTC subsystem required to power the device are described in this section.

### 7.5.1 Minimum Processor-PMIC interface Connections

Table 7.1 lists the signals required to coordinate the operation of the AM335x and TPS65217C. Figure 7.1 and Figure 7.2 illustrate the required connections between the AM335x and the TPS65217C with RTC subsystem enabled and disabled respectively. These connections are the minimum required to operate the device in corresponding mode. The accessibility of these signals enables other uses of reset, power control, power status, interrupt, wakeup, and serial communication signals.

The figures 7.1 and 7.2 only illustrate the interface between the AM335x and TPS65217C.

Table 7.1. AM335x and TPS65217C Signal Descriptions

Signal	Description	Notes
<b>PMIC_POWER_EN</b>	PMIC Power Enable from AM335x	
<b>PMIC_PWR_EN</b>	PMIC Power Enable to TPS65217C	1
<b>I2C0_SCL</b>	I2C0 SCL from AM335x	1
<b>PMIC_SCL</b>	I2C SCL to TPS65217C	
<b>I2C0_SDA</b>	I2C0 SDA from AM335x	1
<b>PMIC_SDA</b>	I2C SDA to TPS65217C	
<b>PMIC_PGOOD</b>	PGOOD from TPS65217C	
<b>PWRONRSTN</b>	PWRONRSTN to AM335x	
<b>PMIC_LDO_PGOOD</b>	LDO_PGOOD from TPS65217C	
<b>RTC_PWRONRSTN</b>	RTC_PWRONRSTN to AM335x	
<b>PMIC_NINT</b>	NINT from TPS65217C	
<b>EXTINTN</b>	EXTINTN to AM335x	1
<b>PMIC_NWAKEUP</b>	NWAKEUP from TPS65217C	
<b>EXT_WAKEUP</b>	EXT_WAKEUP to AM335x	1

1. See Table 2.1 for pull up on this signal

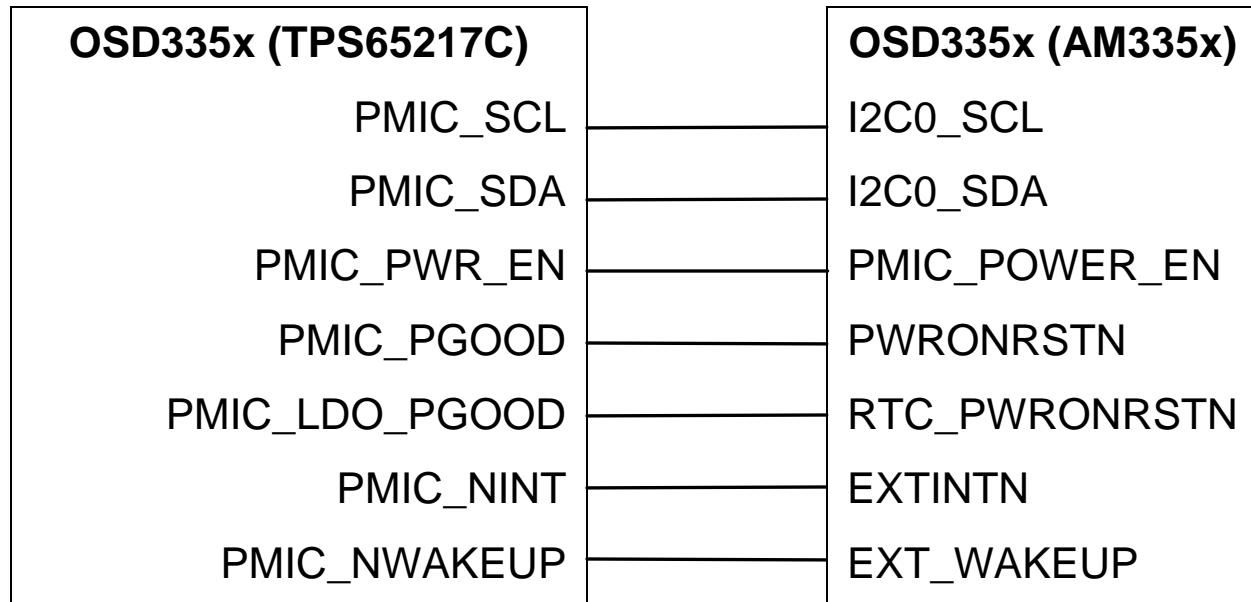


Figure 7.1. OSD335x-SM Minimum Signal Connections with RTC enabled

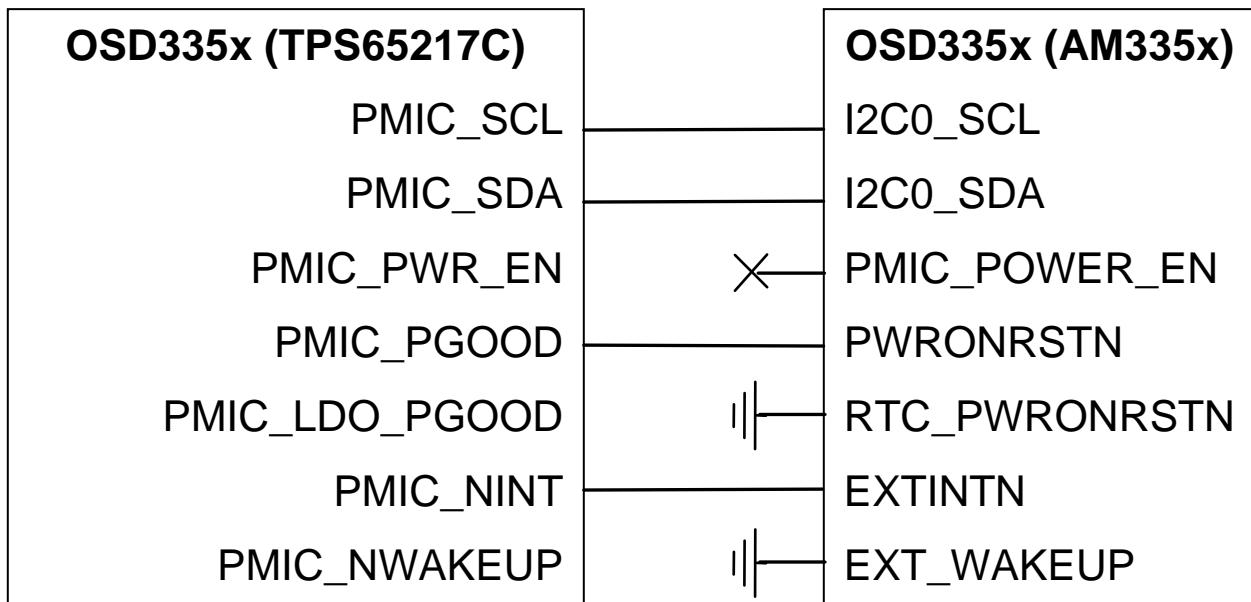


Figure 7.2. OSD335x-SM Minimum Signal Connections with RTC disabled

### 7.5.2 Minimum RTC Power Connections

Table 7.2 lists RTC domain signals required to operate the OSD335x-SM. In addition to the required connections described in Section 7.5.1, Figure 7.3 and Figure 7.4 illustrate additional connections with RTC subsystem enabled and disabled respectively. These connections are also included in the minimum required circuitry to operate the device.

Table 7.2. OSD335x-SM RTC Signal Descriptions

Signal	Description	Notes
CAP_VDD_RTC	Supply voltage for the RTC core domain	
RTC_KALDO_ENN	Active low enable input for internal CAP_VDD_RTC voltage regulator	
RTC_PWRONRSTN	RTC_PWRONRSTN to AM335x	
PMIC_POWER_EN	PMIC Power Enable from AM335x	
EXT_WAKEUP	EXT_WAKEUP to AM335x	1

1. See Table 2.1 for pull up on this signal

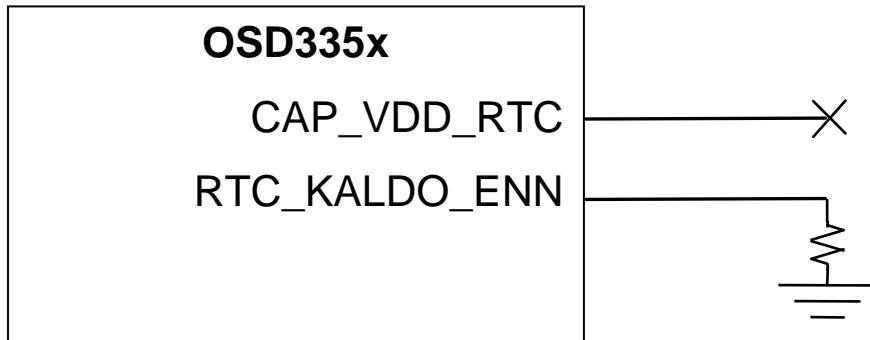


Figure 7.3. Additional connections for OSD335x-SM with RTC enabled

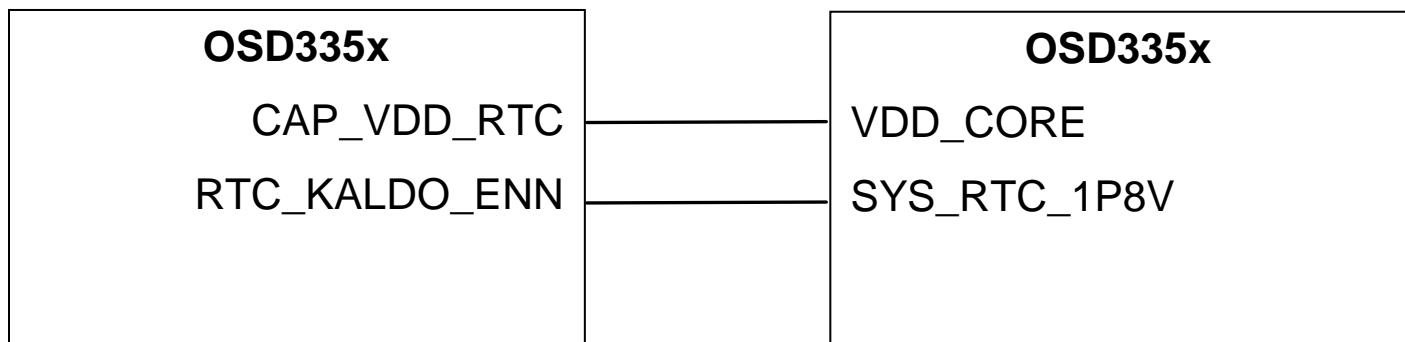


Figure 7.4. Additional connections for OSD335x-SM with RTC disabled

# OSD335x-SM Family

Rev. 6 2/16/2018

## 8 Electrical & Thermal Characteristics

Table 8.1 lists electrical and thermal characteristic parameters of OSD335x-SM.

Table 8.1. OSD335x-SM Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup>

		Value	Unit
<b>Supply voltage range (with respect to VSS)</b>	VIN_BAT	-0.3 to 7	V
	VIN_USB, VIN_AC	-0.3 to 7	
<b>Input/Output voltage range (with respect to VSS)</b>	All pins unless specified separately	-0.3 to 3.6	V
<b>Terminal current</b>	SYS_VOUT, VIN_USB, VIN_BAT	3000	mA
<b>T<sub>c</sub> Operating case temperature</b>	Commercial (B)	0 to 85	°C
	Industrial (I)	-40 to 85	°C
<b>T<sub>stg</sub> Storage temperature</b>		-40 to 125	°C
<b>ESD rating</b>	(HBM) Human body model	±2000	V
	(CDM) Charged device model	±500	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

Table 8.2. Recommended Operating Conditions over operating free-air temperature range (unless otherwise noted)

	Min	Nom	Max	Unit
<b>Supply voltage, VIN_USB, VIN_AC</b>	4.3		5.8	V
<b>Supply voltage, VIN_BAT</b>	2.75		5.5	V
<b>Input current from VIN_AC</b>			2.0	A
<b>Input current from VIN_USB</b>			1.3	A
<b>VIN_BAT current</b>			2.0	A
<b>Output voltage range for SYS_VDD1_3P3V</b>	3.4			V
<b>Output voltage range for SYS_VDD2_3P3V</b>	3.3			V
<b>Output voltage range for SYS_VDD3_3P3V</b>	3.3			V
<b>Output voltage range for SYS_RTC_1P8V</b>	1.8			V
<b>Output voltage range for SYS_VDD_1P8V</b>	1.8			V
<b>Output voltage range for SYS_ADC_1P8V</b>	1.8			V
<b>Output voltage range for VDDS_DDR<sup>1</sup></b>	1.5			V
<b>Output voltage range for VDD_MPU<sup>1</sup></b>	1.1			V
<b>Output voltage range for VDD_CORE<sup>1</sup></b>	1.1			V
<b>Output voltage range for VDDS_PLL<sup>1</sup></b>	1.8			V
<b>Output current for SYS_VOUT<sup>2</sup></b>	0		500	mA
<b>Output current for SYS_VDD1_3P3V<sup>2</sup></b>	0		500	mA
<b>Output current for SYS_VDD2_3P3V<sup>2</sup></b>	0		100	mA
<b>Output current for SYS_VDD3_3P3V<sup>2</sup></b>	0		50	mA
<b>Output current for SYS_RTC_1P8V<sup>2</sup></b>	0		100	mA
<b>Output current for SYS_VDD_1P8V<sup>2</sup></b>	0		250	mA
<b>Output current for SYS_ADC_1P8V<sup>2</sup></b>	0		25	mA

(1) These voltage rails are for reference only and should not be used to power anything on the PCB.

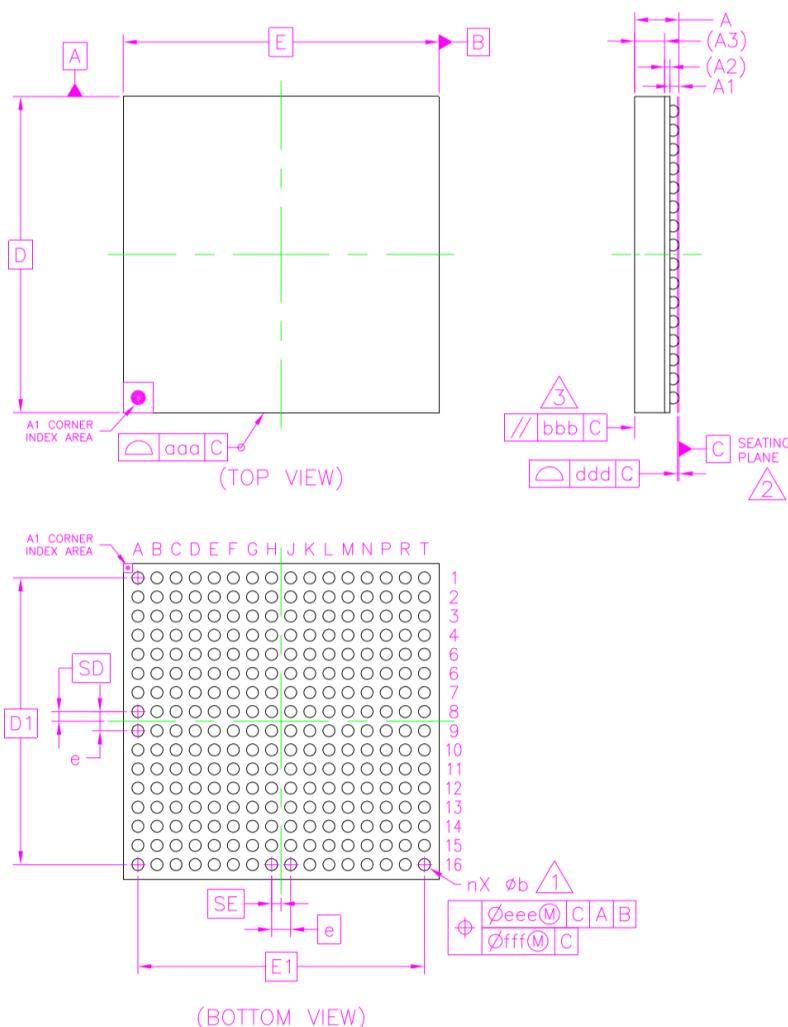
(2) Please note that the total input current on VIN\_AC, VIN\_USB or VIN\_BAT must not exceed the recommended maximum value even if individual currents drawn from these power supply outputs are less than or equal to the maximum recommended operating output currents. See section 7.4 for more details.

## 9 Packaging Information

The OSD335x-SM is packaged in a 256 ball, Ball Grid Array (BGA). The package size is 21 X 21 millimeters with a ball pitch of 1.27 millimeters. This section will give you the specifics on the package.

## 9.1 Mechanical Dimensions

The mechanical drawings of the OSD335x-SM show pin A1 in the lower left-hand corner when looking at the top view of the device. Pin A1 is in the upper left-hand corner if looking at the balls from the bottom view of the package.



**NOTES:**

△ DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.

⚠ DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

# OSD335x-SM Family

Rev. 6 2/16/2018



## 9.2 Reflow Instructions

The reflow profile for this package should be in accordance with the Lead-free process for BGA. A peak reflow temperature is recommended to be 245°C.

Texas Instruments provides a good overview of Handling & Process Recommendations in AN-2029 for this type of device. A link to the document can be found in the Reference Documents section of this document.

## 9.3 Storage Recommendations

The OSD335x-SM Family of devices are sensitive to moisture and need to be handled in specific ways to make sure they function properly during and after the manufacturing process. The OSD335x-SM Family of devices are rated with a Moisture Sensitivity Level (MSL) of 4. This means that they are typically stored in a sealed Dry Pack.



Once the sealed Dry Pack is opened the OSD335x-SM needs to be used within 72 hours to avoid further processing. If the OSD335x-SM has been exposed for more than 72 hours, then it is required that you bake the device for 48 hours at 125°C before using.

Alternatively, the devices could be stored in a dry cabinet with humidity <10% to avoid the baking requirement.

For more information, please refer to the Texas Instruments AN-2029 which can be found in the Reference Documents section of this document.