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QN908x Hardware Design Considerations

Rev. 1.1 — July 2017

Document information

Info	Content
Keywords	QN908x, BLE, clock, power supply, PCB layout, DCDC
Abstract	This application note describes the board design considerations for QN9080 and QN9083.

Revision history

Rev	Date	Description
0.1	20160823	Initial version.
0.2	20160902	Updated the clock source name.
1.0	20170614	Public release.
1.1	20170724	Updated Table 7.

Contact information

For additional information, please visit: http://www.nxp.com

1. Introduction

QN9080 is an ultra-low power, high-performance, and highly-integrated Bluetooth v5.0 Low Energy (BLE) solution for Bluetooth Smart applications. It integrates a BLE radio, controller, protocol stack, and profile software on a single chip, providing a flexible and easy-to-use BLE SoC solution. It also includes a high-performance MCU (32-bit ARM® Cortex®-M4F), on-chip memory, and peripherals to develop a truly single-chip wireless MCU solution.

2. System block diagram

The 9080 SOC includes the ARM Cortex-M4F core and the BLE 4.2 IP stack and abundant peripherals.

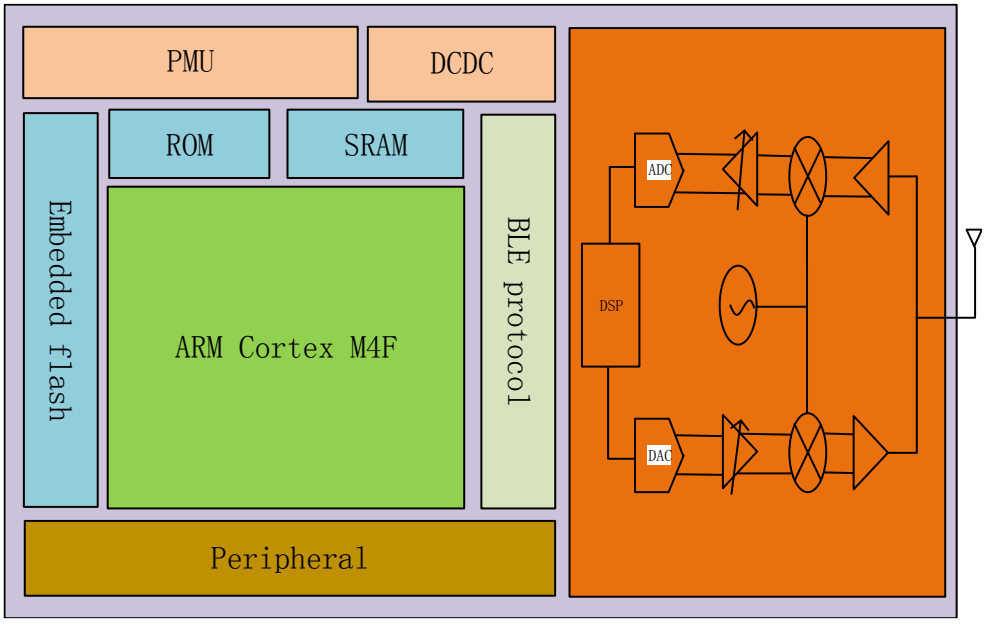


Fig 1. QN908x blocks

3. Pin diagram and pin mux

QN908x offers two packages, while QN9080 has the HVQFN48 6x6 mm package and QN9083 has the WLCSP 3.2x3.2 mm package.

3.1 QN9080 HVQFN48 pin diagram

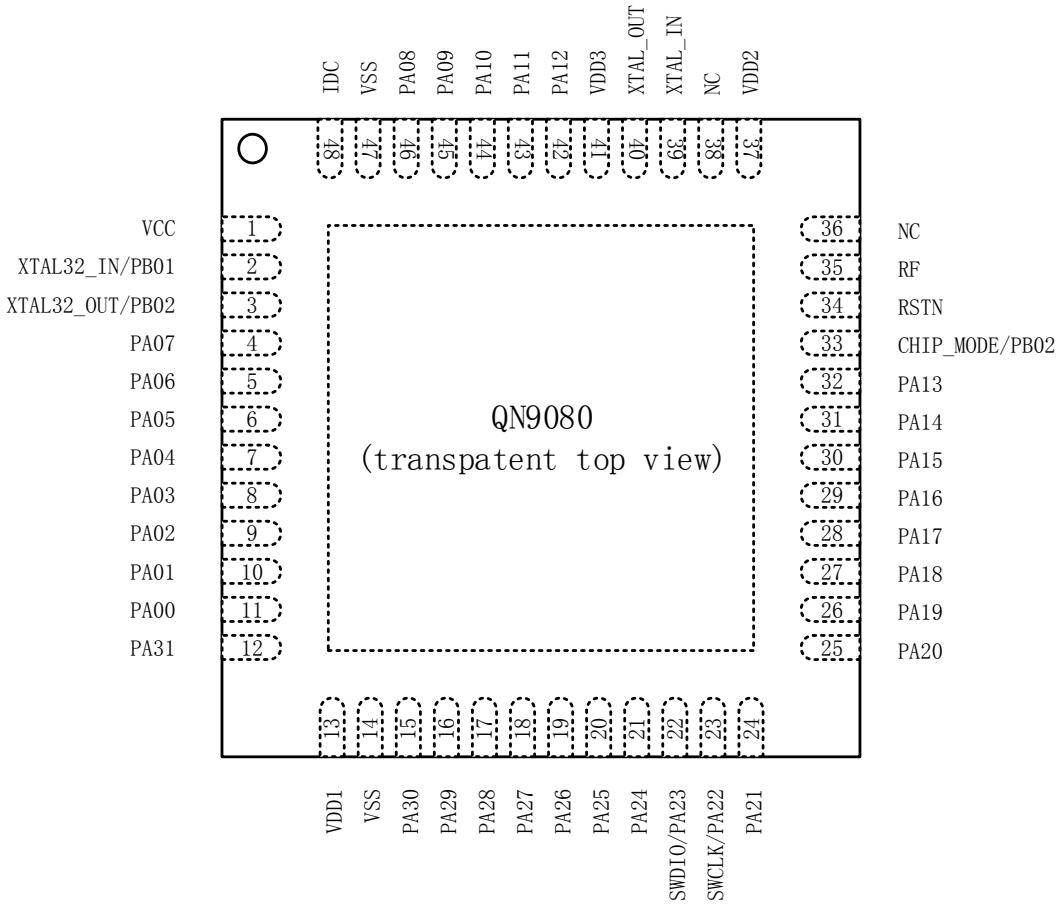


Fig 2. QN9080 pin diagram

3.2 QN9080 QFN48 pin mux

Table 1. QN9080 pin mux

PIN_CTRL	Name	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
[2-0]	PA00	GPIOA0(I/O)	ADC0(A)	PWM_OUT0(O)	TIM0_CAP0(I)	FC0_RTS_SCL_SSEL1(I/O)	FC2_SSEL3(I/O)	WLAN_TX(I)
[5-3]	PA01	GPIOA1(I/O)	ADC1(A)	PWM_OUT1(O)	TIM0_CAP1(I)	FC0_CTS_SDA_SSEL0(I/O)	FC2_SSEL2(I/O)	WLAN_RX(I)
[8-6]	PA02	GPIOA2(I/O)	QDEC0_A(I)	PWM_OUT2(O)	TIM0_OUT0(O)	CHRG_SDA(I/O)	FC2_RTS_SCL_SSEL1(I/O)	RX_EN(O)
[11-9]	PA03	GPIOA3(I/O)	QDEC0_B(I)	PWM_OUT3(O)	TIM0_OUT1(O)	CHRG_SCL(O)	FC2_CTS_SDA_SSEL0(I/O)	TX_EN(O)
[14-12]	PA04	GPIOA4(I/O)	ADC2(A)	PWM_OUT4(O)	TIM0_OUT0(O)	FC0_TXD_SCL_MISO(I/O)	FC2_RXD_SDA_MOSI(I/O)	QSPI_DAT0(I/O)
[17-15]	PA05	GPIOA5(I/O)	ADC3(A)	PWM_OUT5(O)	TIM0_OUT1(O)	FC0_RXD_SDA_MOSI(I/O)	FC2_TXD_SCL_MISO(I/O)	QSPI_DAT1(I/O)
[20-18]	PA06	GPIOA6(I/O)	VBG_EXCAP(A)	PWM_OUT3(O)	TIM0_OUT2(O)	FC1_RTS_SCL_SSEL1(I/O)	BLE_PTI0(O)	QSPI_SCK(O)
[23-21]	PA07	GPIOA7(I/O)	VREF_EXT(A)	PWM_OUT2(O)	TIM1_CAP0(I)	FC1_CTS_SDA_SSEL0(I/O)	BLE_PTI1(O)	QSPI_nCS(O)
[26-24]	PA08	GPIOA8(I/O)	ADC4(A)	PWM_IN0(I)	TIM1_CAP1(I)	FC1_TXD_SCL_MISO(I/O)	BLE_PTI2(O)	QSPI_DAT2(I/O)
[29-27]	PA09	GPIOA9(I/O)	ADC5(A)	PWM_IN1(I)	TIM1_OUT0(O)	FC1_RXD_SDA_MOSI(I/O)	BLE_PTI3(O)	QSPI_DAT3(I/O)
[32-30]	PA10	GPIOA10(I/O)	ADC6(A)	PWM_IN2(I)	TIM1_OUT1(O)	FC1_SCK(I/O)	ACMP0_OUT(O)	BLE_TX(O)
[35-33]	PA11	GPIOA11(I/O)	ADC7(A)	PWM_IN3(I)	TIM1_OUT2(O)	FC2_SSEL2(I/O)	ACMP1_OUT(O)	BLE_RX(O)
[38-36]	PA12	GPIOA12(I/O)	CHRG_SCL(O)	PWM_OUT5(O)	ACMP0_OUT(O)	FC1_TXD_SCL_MISO(I/O)	DAC0(O)	ANTENA(O)
[41-39]	PA13	GPIOA13(I/O)	CHRG_SDA(I/O)	PWM_OUT4(O)	ACMP1_OUT(O)	FC1_RXD_SDA_MOSI(I/O)	FC3_RTS_SCL_SSEL1(I/O)	EXPA(O)
[44-42]	PA14	GPIOA14(I/O)	CS0/ANA_TP0(A)	ANTENA(O)	TIM2_CAP0(I)	FC0_RTS_SCL_SSEL1(I/O)	FC3_CTS_SDA_SSEL0(I/O)	QDEC1_A(I)
[47-45]	PA15	GPIOA15(I/O)	CS1/ANA_TP1(A)	PWM_OUT0(O)	TIM2_CAP1(I)	FC0_CTS_SDA_SSEL0(I/O)	FC3_SCK(I/O)	QDEC1_B(I)
[50-48]	PA16	GPIOA16(I/O)	CS2/ANA_TP2(A)	PWM_OUT1(O)	TIM2_OUT0(O)	FC0_TXD_SCL_MISO(I/O)	FC3_RXD_SDA_MOSI(I/O)	QDEC0_A(I)
[53-51]	PA17	GPIOA17(I/O)	CS3/ANA_TP3(A)	DAC0(O)	TIM2_OUT1(O)	FC0_RXD_SDA_MOSI(I/O)	FC3_TXD_SCL_MISO(I/O)	QDEC0_B(I)
[56-54]	PA18	GPIOA18(I/O)	CS4(A)	PWM_OUT3(O)	TIM2_OUT2(O)	FC0_SCK(I/O)	FC3_SSEL2(I/O)	BLE_SYNC(O)
[59-57]	PA19	GPIOA19(I/O)	CS5(A)	PWM_OUT2(O)	EXPA(O)	FC0_SCK(I/O)	FC3_SSEL3(I/O)	BLE_IN_PROC(O)
[62-60]	PA20	GPIOA20(I/O)	QDEC1_A(I)	PWM_OUT1(O)	TIM2_OUT0(O)	SWO(O)	FC1_RTS_SCL_SSEL1(I/O)	QSPI_SCK(O)
[65-63]	PA21	GPIOA21(I/O)	QDEC1_B(I)	PWM_OUT0(O)	TIM2_OUT1(O)	FC2_SSEL3(I/O)	FC1_CTS_SDA_SSEL0(I/O)	QSPI_nCS(O)
[68-66]	PA22	SWCLK(I)	GPIOA22(I/O)	PWM_IN2(I)	TIM3_OUT0(O)	FC2_CTS_SDA_SSEL0(I/O)	FC3_SSEL3(I/O)	QDEC1_A(I)
[71-69]	PA23	SWDAT(I/O)	GPIOA23(I/O)	PWM_IN3(I)	TIM3_OUT1(O)	FC2_RTS_SCL_SSEL1(I/O)	FC3_SSEL2(I/O)	QDEC1_B(I)
[74-72]	PA24	GPIOA24(I/O)	ACMP0N/CS6(A)	SWD_TRACEDAT0(O	TIM3_CAP0(I)	RX_EN(O)	FC3_RTS_SCL_SSEL1(I/O)	QSPI_DAT0(I/O)
[77-75]	PA25	GPIOA25(I/O)	ACMP0P/CS7(A)	SWD_TRACEDAT1(O	TIM3_CAP1(I)	TX_EN(O)	FC3_CTS_SDA_SSEL0(I/O)	QSPI_DAT1(I/O)
[80-78]	PA26	GPIOA26(I/O)	USB_DP(A)	PWM_IN0(I)	TIM1_OUT0(O)	FC2_RXD_SDA_MOSI(I/O)	QDEC0_A(I)	BLE_SYNC(O)
[83-81]	PA27	GPIOA27(I/O)	USB_DM(A)	PWM_IN1(I)	TIM1_OUT2(O)	FC2_TXD_SCL_MISO(I/O)	QDEC0_B(I)	BLE_IN_PROC(O)
[86-84]	PA28	GPIOA28(I/O)	CLK_AHB(O)	SWD_TRACECLK(O)	RTC_CAP(I)	FC1_SCK(I/O)	DAC0(O)	QSPI_nCS(O)
[89-87]	PA29	GPIOA29(I/O)	ACMP1N(A)	SWD_TRACEDAT2(O	TIM3_OUT0(O)	FC2_SCK(I/O)	FC3_TXD_SCL_MISO(I/O)	QSPI_DAT2(I/O)
[92-90]	PA30	GPIOA30(I/O)	ACMP1P(A)	SWD_TRACEDAT3(O	TIM3_OUT1(O)	FC2_SCK(I/O)	FC3_RXD_SDA_MOSI(I/O)	QSPI_DAT3(I/O)
[95-93]	PA31	GPIOA31(I/O)	DAC(A)	RTC_CAP(I)	TIM3_OUT2(O)	SWO(O)	FC3_SCK(I/O)	QSPI_SCK(O)
	PB00	GPIOB0(I/O)	XTAL32_OUT					
	PB01	GPIOB1(I/O)	XTAL32_IN					
	BOOT_mode	GPIOB2(I/O)	ANTENA(O)					

3.3 QN9083 WLCSP pin diagram

Fig 3. QN9083 pin diagram

3.4 QN9083 WLCSP pin mux

Table 2. QN9083 pin mux

PIN_CTRL	Name	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
[2-0]	**PA00**	GPIOA0(I/O)	ADC0(A)	PWM_OUT0(O)	TIM0_CAP0(I)	FC0_RTS_SCL_SSEL1(I/O)	FC2_SSEL3(I/O)	WLAN_TX(I)
[5-3]	**PA01**	GPIOA1(I/O)	ADC1(A)	PWM_OUT1(O)	TIM0_CAP1(I)	FC0_CTS_SDA_SSEL0(I/O)	FC2_SSEL2(I/O)	WLAN_RX(I)
[14-12]	**PA04**	GPIOA4(I/O)	ADC2(A)	PWM_OUT4(O)	TIM0_OUT0(O)	FC0_TXD_SCL_MISO(I/O)	FC2_RXD_SDA_MOSI(I/O)	QSPI_DAT0(I/O)
[17-15]	**PA05**	GPIOA5(I/O)	ADC3(A)	PWM_OUT5(O)	TIM0_OUT1(O)	FC0_RXD_SDA_MOSI(I/O)	FC2_TXD_SCL_MISO(I/O)	QSPI_DAT1(I/O)
[20-18]	**PA06**	GPIOA6(I/O)	VBG_EXCAP(A)	PWM_OUT3(O)	TIM0_OUT2(O)	FC1_RTS_SCL_SSEL1(I/O)	BLE_PTI0(O)	QSPI_SCK(O)
[23-21]	**PA07**	GPIOA7(I/O)	VREF_EXT(A)	PWM_OUT2(O)	TIM1_CAP0(I)	FC1_CTS_SDA_SSEL0(I/O)	BLE_PTI1(O)	QSPI_nCS(O)
[26-24]	**PA08**	GPIOA8(I/O)	ADC4(A)	PWM_IN0(I)	TIM1_CAP1(I)	FC1_TXD_SCL_MISO(I/O)	BLE_PTI2(O)	QSPI_DAT2(I/O)
[29-27]	**PA09**	GPIOA9(I/O)	ADC5(A)	PWM_IN1(I)	TIM1_OUT0(O)	FC1_RXD_SDA_MOSI(I/O)	BLE_PTI3(O)	QSPI_DAT3(I/O)
[32-30]	**PA10**	GPIOA10(I/O)	ADC6(A)	PWM_IN2(I)	TIM1_OUT1(O)	FC1_SCK(I/O)	ACMP0_OUT(O)	BLE_TX(O)
[35-33]	**PA11**	GPIOA11(I/O)	ADC7(A)	PWM_IN3(I)	TIM1_OUT2(O)	FC2_SSEL2(I/O)	ACMP1_OUT(O)	BLE_RX(O)
[44-42]	**PA14**	GPIOA14(I/O)	CS0/ANA_TP0(A)	ANTENA(O)	TIM2_CAP0(I)	FC0_RTS_SCL_SSEL1(I/O)	FC3_CTS_SDA_SSEL0(I/O)	QDEC1_A(I)
[47-45]	**PA15**	GPIOA15(I/O)	CS1/ANA_TP1(A)	PWM_OUT0(O)	TIM2_CAP1(I)	FC0_CTS_SDA_SSEL0(I/O)	FC3_SCK(I/O)	QDEC1_B(I)
[50-48]	**PA16**	GPIOA16(I/O)	CS2/ANA_TP2(A)	PWM_OUT1(O)	TIM2_OUT0(O)	FC0_TXD_SCL_MISO(I/O)	FC3_RXD_SDA_MOSI(I/O)	QDEC0_A(I)
[53-51]	**PA17**	GPIOA17(I/O)	CS3/ANA_TP3(A)	DAC0(O)	TIM2_OUT1(O)	FC0_RXD_SDA_MOSI(I/O)	FC3_TXD_SCL_MISO(I/O)	QDEC0_B(I)
[56-54]	**PA18**	GPIOA18(I/O)	CS4(A)	PWM_OUT3(O)	TIM2_OUT2(O)	FC0_SCK(I/O)	FC3_SSEL2(I/O)	BLE_SYNC(O)
[59-57]	**PA19**	GPIOA19(I/O)	CS5(A)	PWM_OUT2(O)	EXPA(O)	FC0_SCK(I/O)	FC3_SSEL3(I/O)	BLE_IN_PROC(O)
[68-66]	**PA22**	SWCLK(I)	GPIOA22(I/O)	PWM_IN2(I)	TIM3_OUT0(O)	FC2_CTS_SDA_SSEL0(I/O)	FC3_SSEL3(I/O)	QDEC1_A(I)
[71-69]	**PA23**	SWDAT(I/O)	GPIOA23(I/O)	PWM_IN3(I)	TIM3_OUT1(O)	FC2_RTS_SCL_SSEL1(I/O)	FC3_SSEL2(I/O)	QDEC1_B(I)
[74-72]	**PA24**	GPIOA24(I/O)	ACMP0N/CS6(A)	SWD_TRACEDAT0((	TIM3_CAP0(I)	RX_EN(O)	FC3_RTS_SCL_SSEL1(I/O)	QSPI_DAT0(I/O)
[77-75]	**PA25**	GPIOA25(I/O)	ACMP0P/CS7(A)	SWD_TRACEDAT1((	TIM3_CAP1(I)	TX_EN(O)	FC3_CTS_SDA_SSEL0(I/O)	QSPI_DAT1(I/O)
[80-78]	**PA26**	GPIOA26(I/O)	USB_DP(A)	PWM_IN0(I)	TIM1_OUT0(O)	FC2_RXD_SDA_MOSI(I/O)	QDEC0_A(I)	BLE_SYNC(O)
[83-81]	**PA27**	GPIOA27(I/O)	USB_DM(A)	PWM_IN1(I)	TIM1_OUT2(O)	FC2_TXD_SCL_MISO(I/O)	QDEC0_B(I)	BLE_IN_PROC(O)
[89-87]	**PA29**	GPIOA29(I/O)	ACMP1N(A)	SWD_TRACEDAT2((	TIM3_OUT0(O)	FC2_SCK(I/O)	FC3_TXD_SCL_MISO(I/O)	QSPI_DAT2(I/O)
[92-90]	**PA30**	GPIOA30(I/O)	ACMP1P(A)	SWD_TRACEDAT3((	TIM3_OUT1(O)	FC2_SCK(I/O)	FC3_RXD_SDA_MOSI(I/O)	QSPI_DAT3(I/O)
[95-93]	**PA31**	GPIOA31(I/O)	DAC(A)	RTC_CAP(I)	TIM3_OUT2(O)	SWO(O)	FC3_SCK(I/O)	QSPI_SCK(O)
	PB00	GPIOB0(I/O)	XTAL32_OUT					
	PB01	GPIOB1(I/O)	XTAL32_IN					
	BOOT_mode	GPIOB2(I/O)	ANTENA(O)					

4. Chip power supply

4.1 Power supply pins description

QN908x has four pins for the power supply input.

Table 3. Power descriptions

Pin name	Description
VCC	Chip power supply for the PMU (power management unit) and IOs
VDD1	Chip power supply for the digital core
VDD2	Chip power supply for the RF blocks
VDD3	Chip power supply for the analog blocks

For the power supply,

- **VCC** is the basic power supply for the PMU and the IOs. Its voltage can range from 1.8 V to 3.6 V.
- **VDD1** is the power supply for the internal core and digital blocks. Its voltage can range from 1.3 V to 3.6 V.
- **VDD2** is the power supply for the internal RF blocks. Its voltage can range from 1.3 V to 3.6 V.
- **VDD3** is the power supply for the internal analog blocks. Its voltage can range from 1.3 V to 3.6 V.

To improve power stability, the VCC pin should have a 4.7-μF capacitor connected in parallel with a 0.1-μF capacitor. The VDD1, VDD2, and VDD3 pins should have a 0.1-μF capacitor connected.

4.2 Integrated DCDC

To reduce power consumption, QN908x has an integrated DCDC block, which can transform the voltage from VCC to 1.3 V and supply it to VDD1, VDD2, and VDD3. The DCDC block outputs at the IDC pin and needs a 10-μH inductor together with a 10-nH inductor in series, as well as a 1-μF capacitor.

To disable the DCDC function easily, there is an integrated switch which can connect VCC to IDC directly and is controlled by a software register.

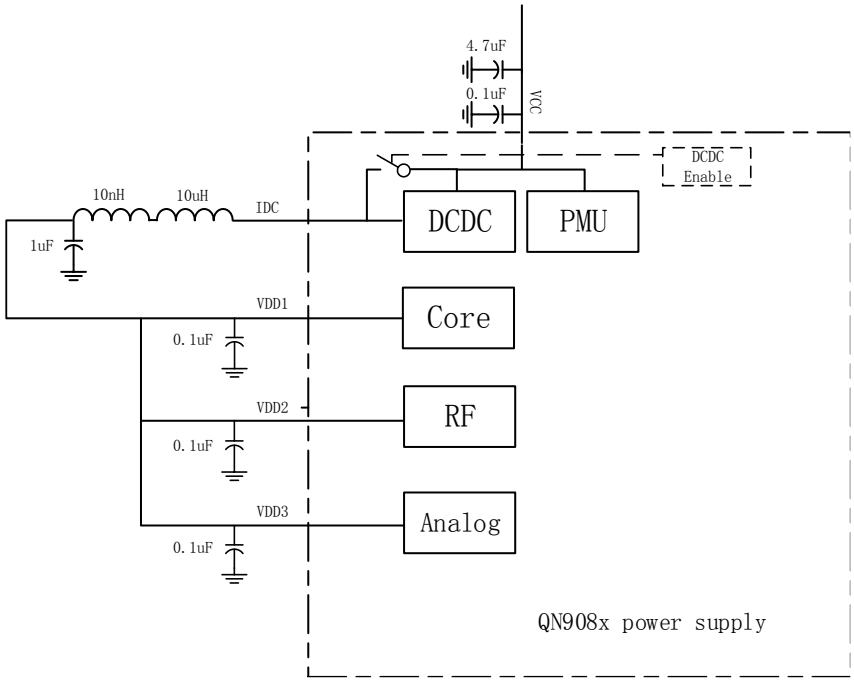


Fig 4. Power supply with an integrated DCDC

If you decide to save the inductors by disabling the internal DCDC, the VDD1, VDD2, and VDD3 can connect to VCC directly and the IDC pin should be floating.

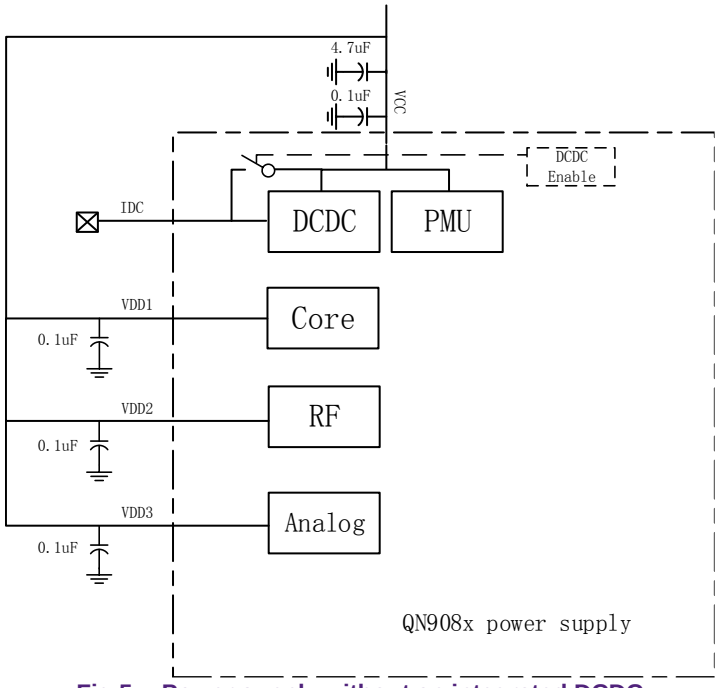


Fig 5. Power supply without an integrated DCDC

4.3 DCDC circuit

The DCDC circuit needs external inductors and an output capacitor. Both the inductors and the output capacitor should be low-ESR. The inductors and the capacitor affect the DCDC oscillating frequency. A 10-μH inductor and a 1-μF output capacitor result in a better efficiency of the DCDC.

The inductor's actual value may change with the current, especially when the current starts to saturate the inductor with magnetic. Select an inductor with a sufficient current limitation. Table 4 lists the verified components and their part numbers.

Table 4. Verified DCDC inductor part number

Vendor	Part number	Inductor value
Murata	LQH2MCN100M52L	10 μH
Murata	LQM21FN100M70L	10 μH
TDK	MLZ2012M100W	10 μH

5. Clock

QN908x needs two clocks to run. The high-frequency clock serves the MCU and peripherals. The BLE block and IP clocks are derived from the high-frequency clock. The low-frequency clock is the sleep clock which is used as the RTC timer source during the MCU power-down period.

5.1 XTAL and RCO32M

There are two high-frequency sources available for QN908x. The first one is the external crystal (called XTAL) and the second is derived from the internal RC oscillator (called RCO32M). XTAL accepts only 16-MHz and 32-MHz crystals. QN908x integrates the load capacitor inside. Its adjust range is 5 pF ~ 27.05 pF with a 0.35-pF pre-step. This integrated capacitor is controlled by a 6-bit register. If you enable the extra addition load capacitor option, the load capacitor adjusting range is 10 pF ~ 32.05 pF. The equivalent capacitor adjusting range is 2.5 pF ~ 13.525 pF and 5 pF ~ 16.025 pF.

Table 5. XTAL integrated load capacitors' parameters

Extra addition capacitor option	Capacitor range for the crystal	Capacitor pre-step for each	Equivalent load capacitor
NO	5 pF ~ 27.05 pF	0.35 pF	2.5 pF ~ 13.525 pF
YES	10 pF ~ 32.05 pF	0.35 pF	5 pF ~ 16.025 pF

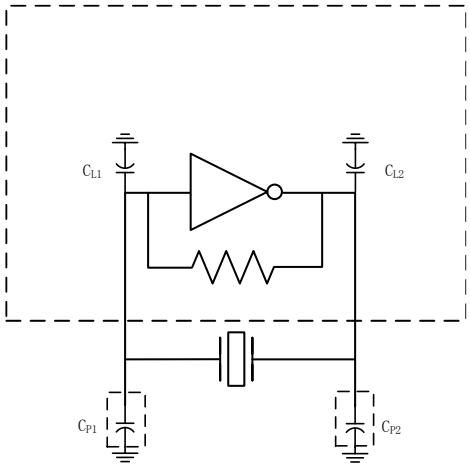


Fig 6. Crystal oscillator block

The load capacitors affect the frequency of the crystal oscillator.

In Fig 6, C_{L1} and C_{L2} are the integrated load capacitors. C_{P1} and C_{P2} are the parasitic capacitors which form the packages' pads and the PCB layout.

$$\text{Equivalent load capacitor} = \frac{(CL1 + CP1) \times (CL2 + CP2)}{CL1 + CP1 + CL2 + CP2}$$

Assuming that $C_{L1} = C_{L2}$ and $C_{P1} = C_{P2}$, the equivalent load capacitor is $\frac{CL}{2} + \frac{CP}{2}$.

Choosing a crystal with a lower-load capacitor results in lower current consumption and shorter startup time. The suggested crystal parameters are shown in Table 6.

Table 6. XTAL parameter

Crystal frequency	ESR	Load capacitor	Tolerance
32 MHz	<100 Ω	<= 10 pF	<= 20 ppm
16 MHz	<200 Ω	<= 10 pF	<= 20 ppm

Table 7. Verified XTAL part number

Vendor	Part number	Frequency	Accuracy	Load cap
MURATA	XRCGB32M000F2N13R0	32 MHz	10 PPM	8 pF
YOKE	S2016A-032000-T08-BDD-YNA	32 MHz	10 PPM	8 pF

5.2 XTAL32K

There are two low-frequency sources available for QN908x. The first is the external crystal (called XTAL32K). XTAL32K is clocked from the external crystal with a frequency of 32.768 kHz. QN908x has also integrated load capacitors for XTAL32K and they are controlled by a 6-bit register. The load capacitors affect the frequency of XTAL32K.

The range of the adjustable load capacitors is shown in Table 8.

Table 8. XTAL32K integrated load capacitors parameters

Extra addition capacitor option	Capacitor for the crystal	Capacitor pre-step for each	Equivalent load capacitor
NO	5 pF ~ 27.05 pF	0.35 pF	2.5 pF ~ 13.525 pF
YES	10 pF ~ 32.05 pF	0.35 pF	5 pF ~ 16.025 pF

The tolerance of the XTAL32K crystal affects the window size of the receiver, which impacts the power consumption.

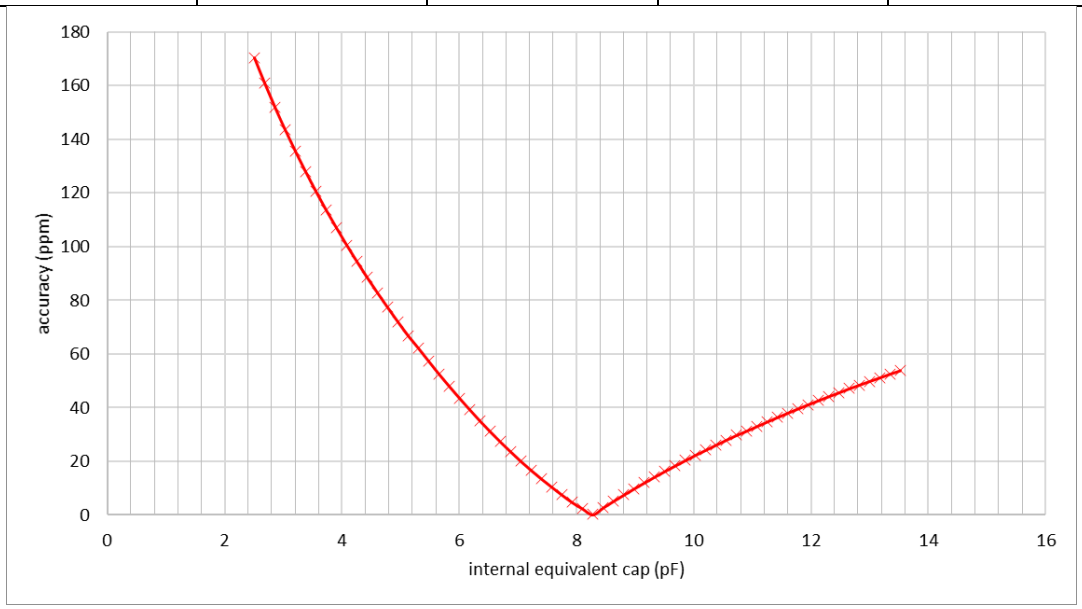
The suggested XTAL32K crystal parameters are shown in Table 9.

Table 9. XTAL32K parameters

Crystal frequency	ESR	Load capacitor	Tolerance
32.768 kHz	< 80 kΩ	<= 10 pF	<= 50 ppm

Table 10. Verified XTAL32K part number

Vendor	Part number	Frequency	Accuracy	Load cap
EPSON	FC-12M	32.768 kHz	20 ppm	12.5 pF



5.3 RCO32K

RCO32K is another clock source for the low-frequency clock. RCO32K uses the internal RC oscillator circuit to generate the clock. The frequency of RCO32K is 32 kHz. To keep the RCO32K frequency around 32 kHz, calibration is enabled when the chip powers up. To calibrate the clock, the software correcting process is started. After the calibration and compensation, RCO32K's tolerance is lower than 500 ppm.

RCO can also perform hardware calibration when the chip powers up and sets the clock close to 32 kHz. The chip is designed with a 22-bit counter to correct little deviations and make the RCO running around 32 kHz. Normally, RCO can offer a clock with a jitter of 150 ppm, but, in a long term, the RCO frequency drifts due to the temperature, voltage, and noise. It is necessary to perform the software calibration periodically to keep the RCO running in the range of 500 ppm.

Considering the temperature as the only factor, the RCO has the change rate of 160 ppm/°C.

5.4 Clock injection

Besides the internal oscillator, QN908x can also get the clock source using clock injection. For the high-frequency clock, the acceptable injection clock frequencies are 16 MHz and 32 MHz. Either a square wave or a sine wave can be injected to the chip. For the low-frequency clock, the chip accepts the 32.768-kHz clock in a square wave or a sine wave.

5.4.1 Square wave

If using the square-wave clock injection, the register of the clock source selection must be set for the square-wave clock injection.

With the square-wave clock, QN908x treats it as a digital signal and the clock must be injected from the XTAL_IN pin of QN908x, while the XTAL_OUT pin must be floating.

The square-wave clock must have a voltage range from 0 to VCC.

For a high frequency, the clock must be 16 MHz or 32 MHz.

For a low frequency, the clock must be 32.768 kHz.

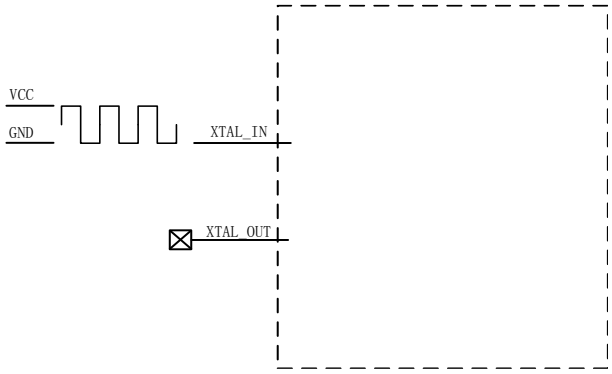


Fig 7. Square wave clock injection

5.4.2 Sine wave

If using the sine-wave clock injection, the register of the clock source selection must be set to the sine-wave clock injection and the QN908x treats it as an analog signal. While injecting the sine wave to the clock, a 1-nF capacitor must be used for AC coupling. The XTAL_OUT pin must connect to the GND with an AC coupling capacitor.

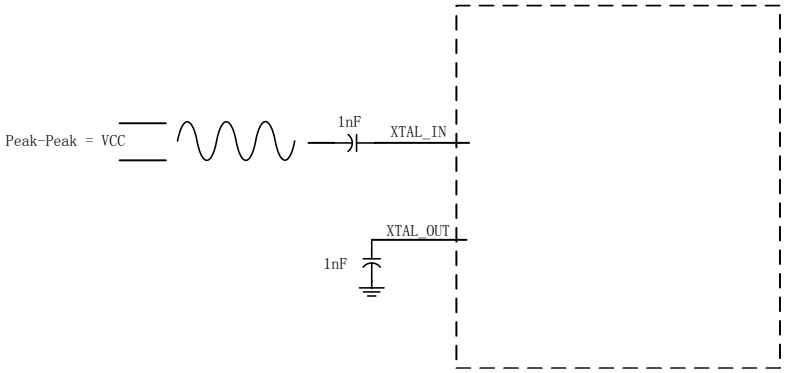


Fig 8. Sine wave clock injection

The voltage of the sine wave must have the peak to peak equal to the voltage of MIN {2.5 V, VCC}.

The high-frequency clock must be either 16 MHz or 32 MHz.

The low-frequency clock must be 32.768 kHz.

5.5 Clock output

QN908x supports the feature of outputting the XTAL and XTAL32K to the IO pins directly with the buffer and divider.

XTAL outputs at pins PA05, PA11, PA19, and PA25.

XTAL32K outputs at pins PA04, PA10, PA18, and PA24.

The GPIO pins and the divider are configurable using registers.

6. IOs

QN908x has a total of 35 IOs in the HVQFN package and 28 IOs in the WLCSP package.

The PB00 and PB01 of both the HVQFN package and the WLCSP package are the clock input pins of the XTAL32K by default.

The PB02 of both the HVQFN and WLCSP packages works in the CHIP_MODE function by default.

PA00 ~ PA31 are general IOs with seven alternate functions. By default, all general IOs are defined as GPIOs except for the SWDIO and SWCLK pins.

All QN908x's IOs have integrated pull-up and pull-down resistors, the IOs can be configured as pull-up, pull-down, or high-Z.

6.1 Pull-up and pull-down resistors

All GPIOs are set to the input function with the pull-up enabled by default after the power-up or reset. The integrated pull-up resistors have a value of roughly 100 kΩ and the pull-down resistors have a value of roughly 200 kΩ.

The pull-up and pull-down resistors values may change a bit with different VCC voltages.

6.2 IOs drive strength

There are four levels of drive strength supported by the GPIOs. An ordinary pin has the first two levels of drive strength, while PA6, PA11, PA19, PA26, and PA27 have four levels of drive strength. See Table 11 for details.

Table 11. IOs drive strength

Current (mA)	DRV_CTRL[x]	DRV_EXTRA
1.6	0	0
6.4	1	0
14.6	0	1
19.4	1	1

6.2.1 Normal drive ability

The normal drive ability setting lets the IO to have roughly 3.5 mA of the source current and 2.5 mA of the sink current.

6.2.2 High drive ability

The high drive ability setting lets the IO to have roughly 13 mA of the source current and 7 mA of the sink current.

6.2.3 Extra-high drive ability

Five of the IOs have the extra-high source current setting.

PA06, PA11, PA19, PA26, and PA27 have extra-high source current. With the extra-high drive ability setting, these five IOs add an extra 26 mA of source current.

7. Debug and program

7.1 Debug port

7.1.1 SWD

QN908x supports the SWD debugging port which uses the GPIO PA22 as the SWDCLK and the GPIO PA23 as the SWDIO. The two pins should be configured as the SWD functions. Not sharing them with other functions is recommended for the system design.

7.1.2 ETM

QN908x has an integrated ETM (Embedded Trace Macro cell) interface, which enables the capturing of instructions while the MCU is running.

The ETM signals are at pins PA24, PA25, PA28, PA29, and PA30. However, PA28 is not available in the WLCSP package, so the ETM function is only supported in the HVQFN package.

7.2 Programing port

7.2.1 ISP

QN908x supports the ISP function via the Flexcomm0 UART, Flexcomm3 SPI, or USB interface. The pads are from PA14 to PA17 when using the UART/SPI for ISP. To enable the ISP mode, pull down the CHIP_MODE pin while the chip is reset. The chip is always in the ISP mode until the CHIP_MODE pin is pulled high. The ISP function starts when a valid handshake is received, and it starts to receive the binary file and program the flash with a new binary file.

The CHIP_MODE pin is pull-up-enabled by default. It is recommended to keep it floating when the ISP process is finished to avoid the IO current leakage.

8. RF

QN908x has a 2.4-GHz RF port which is shared by the receiver and the transmitter. The RF port is designed with a 50-Ω impedance and the RF trace impedance connected to the Radio should be 50 Ω.

8.1 Harmonic rejection

The RF port can have some RF leakage at the harmonic frequency and may cause failure when passing certifications. Even the harmonic signal is rejected by the antenna that only has the resonance frequency of roughly 2.4 GHz (the carrier frequency). However, to make sure that the harmonic signal does not transmit to the open space, it is suggested to have a Pi circuit in front of the RF port which works as the filter to reject the undesired RF leakage.

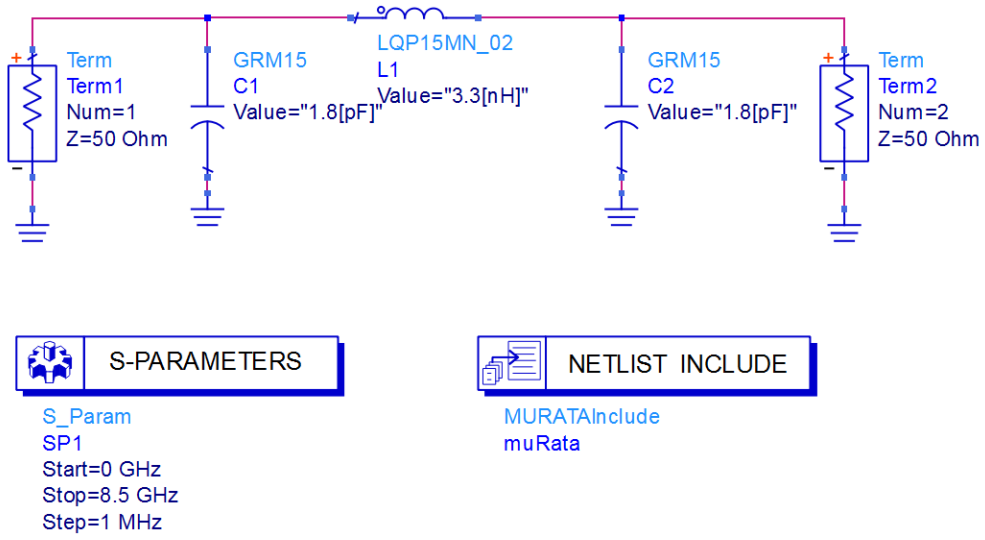


Fig 9. Harmonic frequency rejection filter

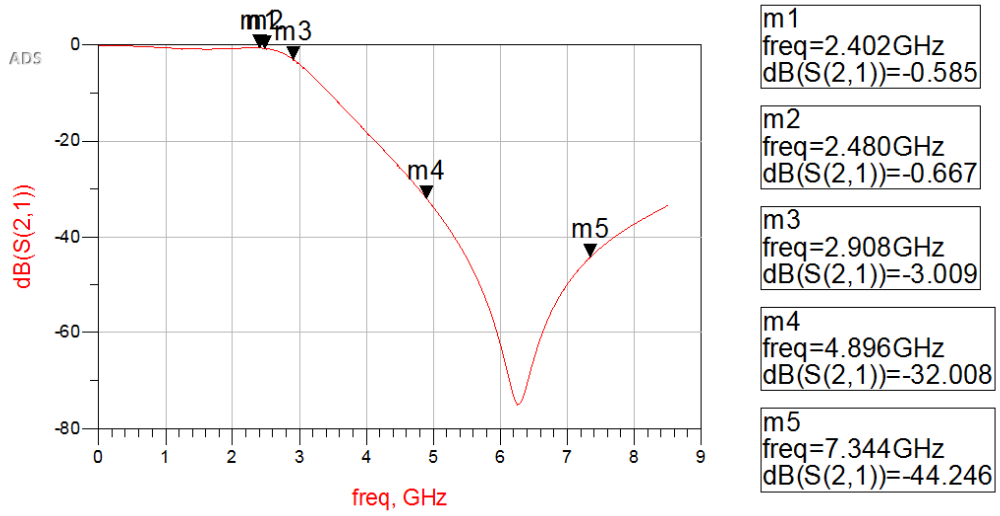


Fig 10. Harmonic frequency rejection filter parameter

As shown in Fig 10, the filter uses two capacitors connected to the ground in parallel and one inductor in series.

The filter's 3-dB corner is at the frequency of 2908 MHz and has a 0.7-dB loss in the range from 2.4 GHz to 2.48 GHz. It has a 32-dB rejection at the second harmonic and a 44-dB rejection at the third harmonic frequency. With a filter with such parameters, the RF performance can pass the RF authentication easily.

8.2 Placement and layout

The component placement and the RF trace layout affect the RF performance.

For the best RF performance, the components must be placed as close as possible to the RF port and the RF trace must be shorted between the RF port and the feed point of the antenna or the SMA connector.

The RF trace must keep a 50-Ω impedance.

The ground at the bottom of the RF components and the RF trace must be complete and solid. No signal trace can go under the RF components and the RF trace.

All the RF components and the RF trace must be on the same layer; no vias are allowed on the RF trace.

The DCDC components must be placed close to the IDC pin and far away from the RF components and the RF trace.

If using QN9083 in the WLCSP package, make the analog ground separated from the digital ground. It is better to separate the analog ground from the digital ground so that the digital noise does not interfere with the analog parts.

For the WLCSP package, 3G, 1F, 3E, 3F, and 3D are the analog ground pins.

4D, 4C, 5C, 5E, and 5D are the digital pins.

9. Reference design

9.1 QN9080 reference design

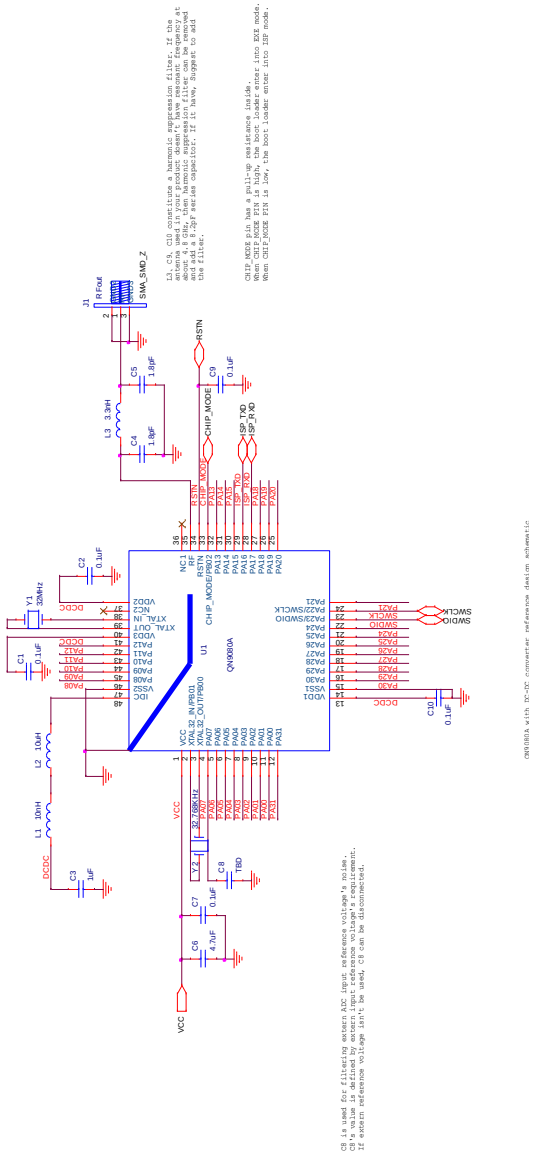


Fig 11. QN9080 with the DC-DC converter reference design schematic

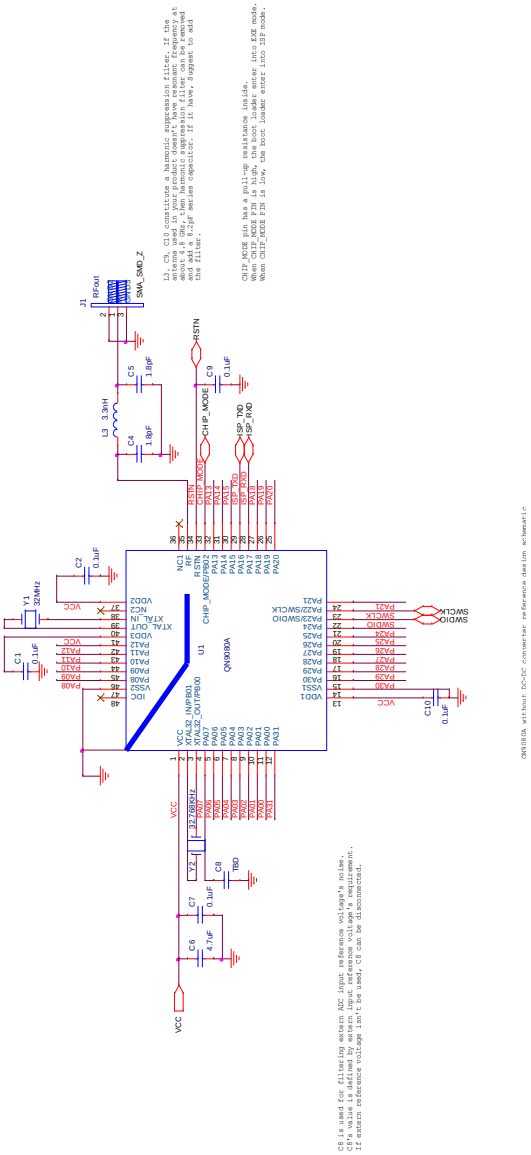


Fig 12. QN9080 without the DC-DC converter reference design schematic

9.2 QN9083 reference design

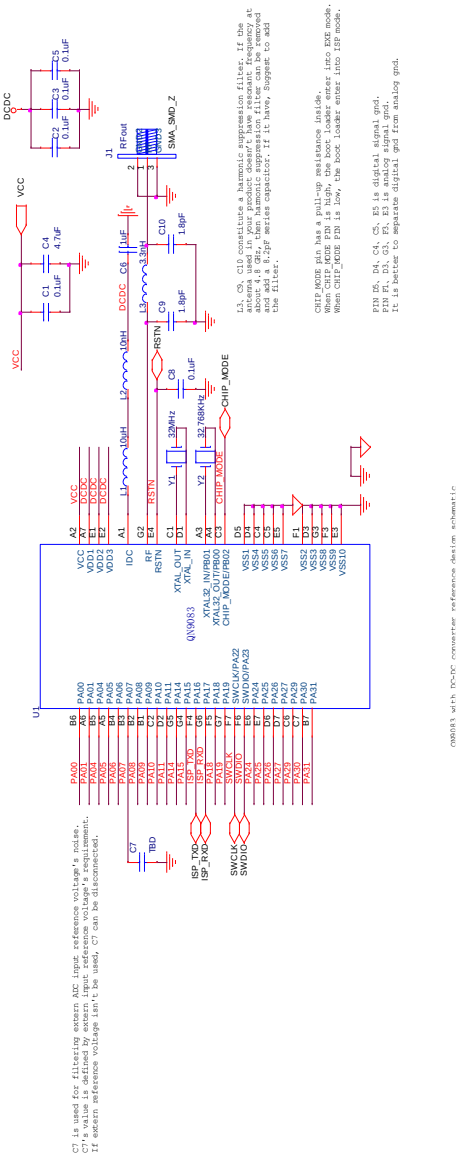


Fig 13. QN9083 with the DC-DC converter reference design schematic

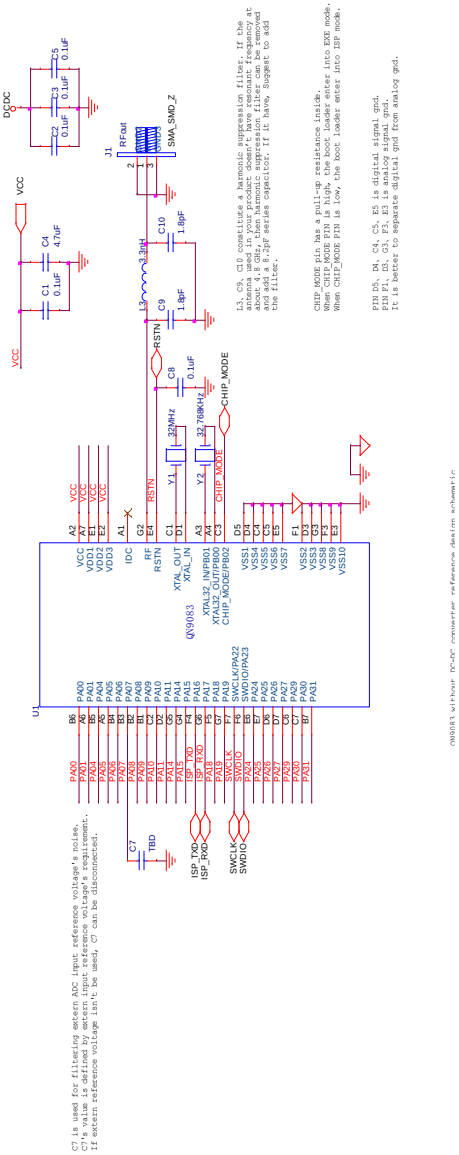


Fig 14. QN9083 without the DC-DC converter reference design schematic

10. PCB layout

10.1 PCB stack-up

The recommended PCB stack-up for a QN9080 application is shown in Fig 15.

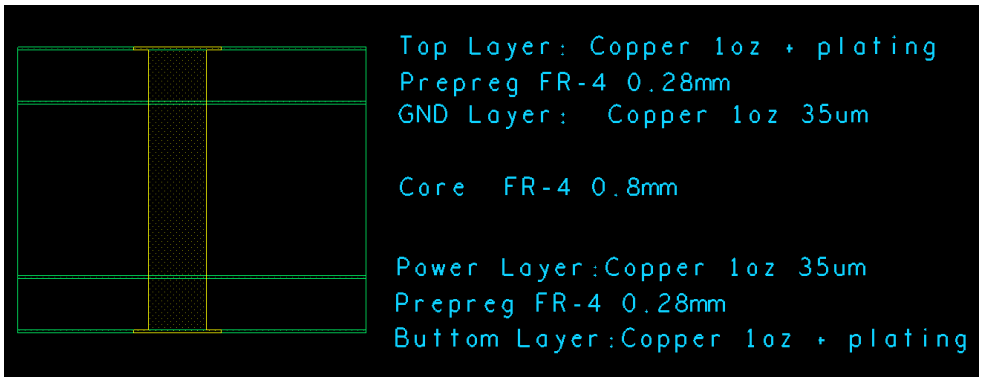


Fig 15. PCB stack-up

The PCB board is 1.6 mm thick and based on the standard flame retardant (FR4) material.

10.2 QN9080 PCB layout reference

Top layer

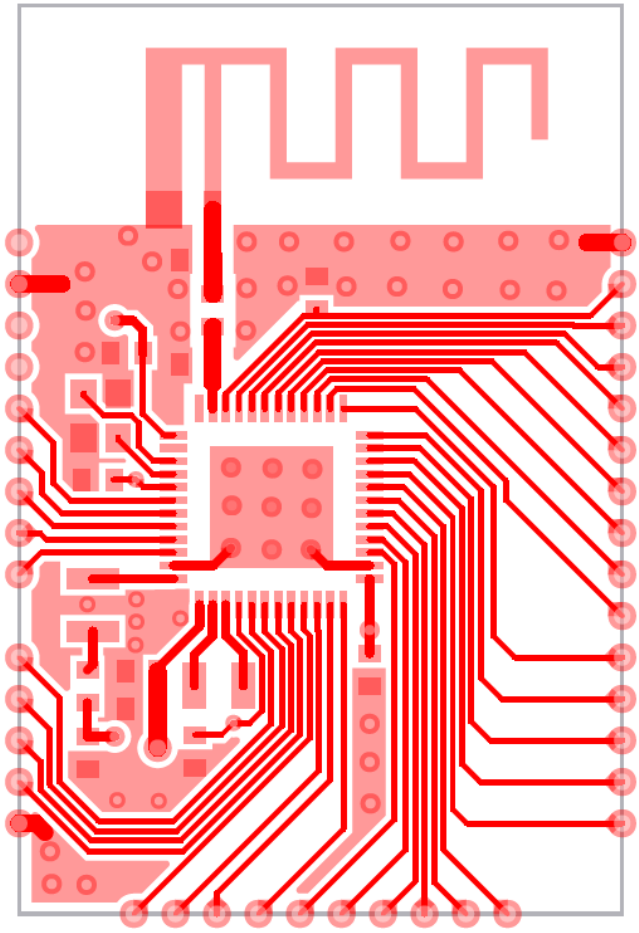


Fig 16. Top layer of the QN9080 PCB layout reference design

GND layer

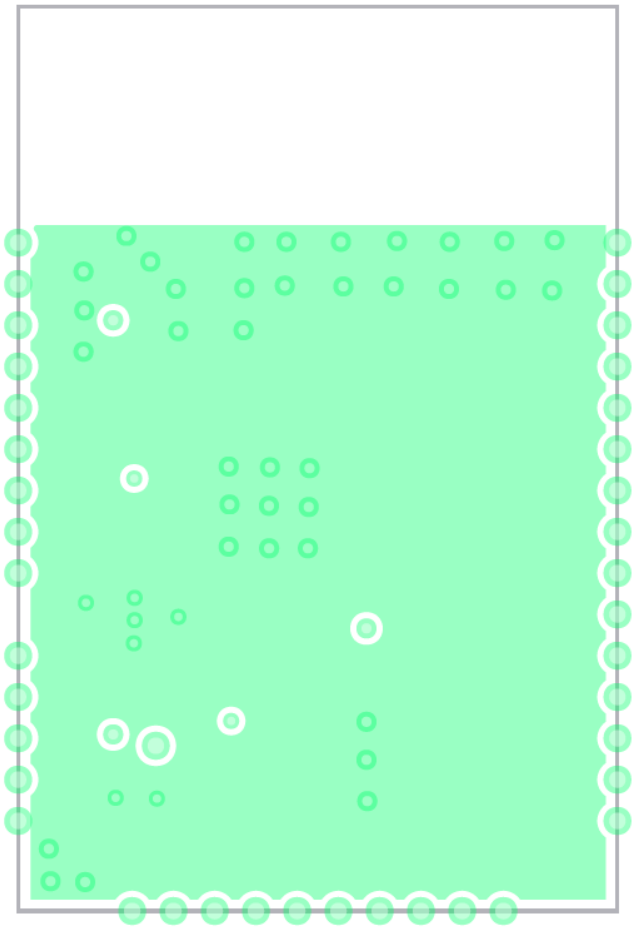


Fig 17. GND layer of the QN9080 PCB layout reference design

Power layer

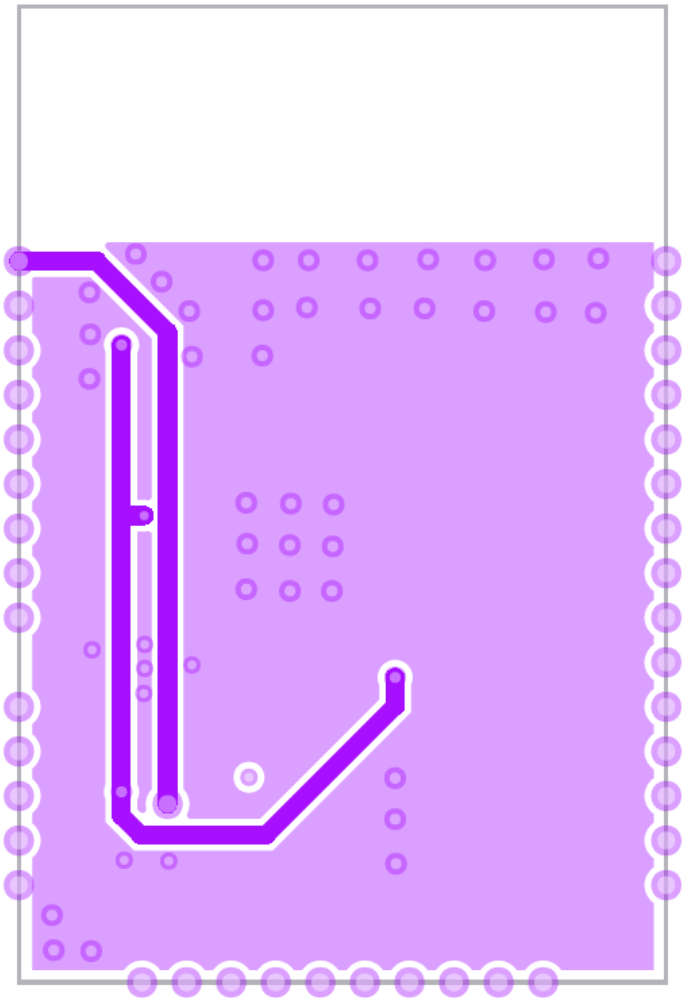


Fig 18. Power layer of the QN9080 PCB layout reference design

Bottom layer

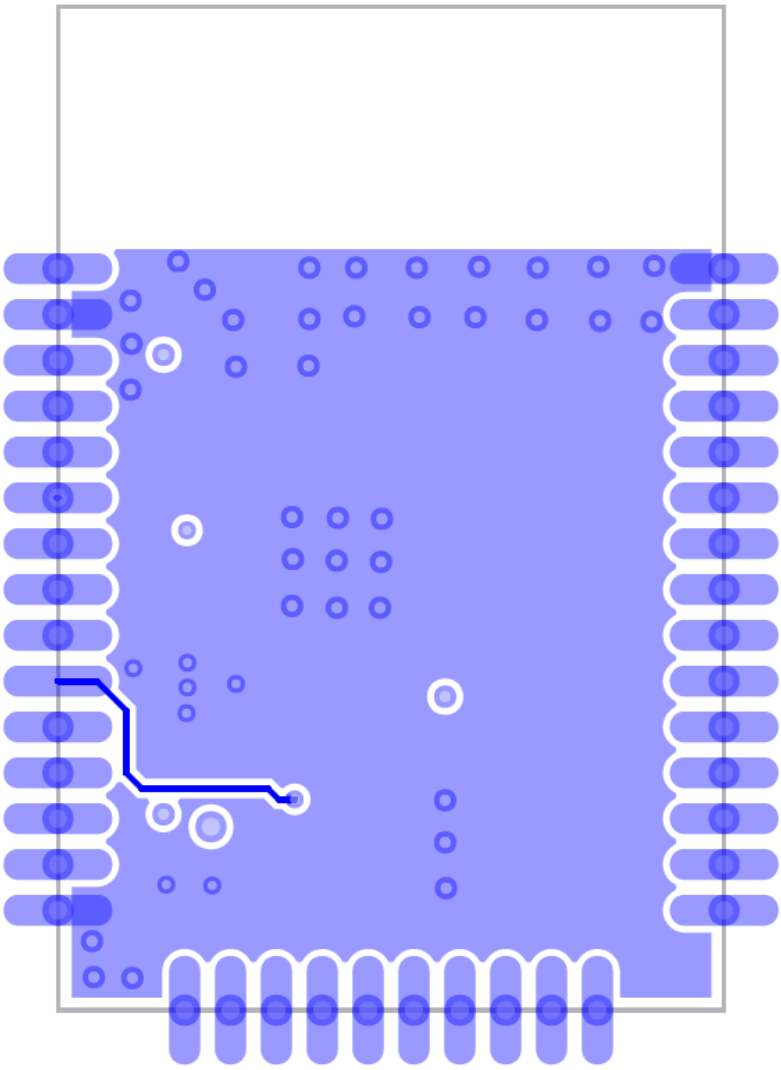


Fig 19. Bottom layer of the QN9080 PCB layout reference design

10.3 QN9083 PCB layout reference

Top layer

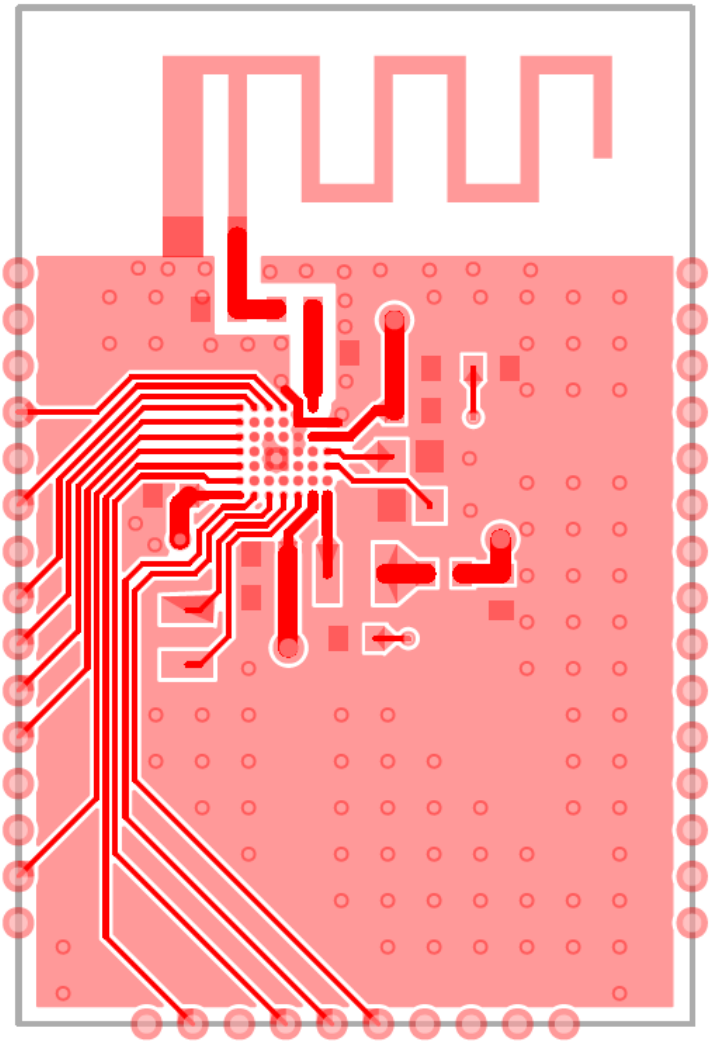


Fig 20. Top layer of the QN9083 PCB layout reference design

GND layer

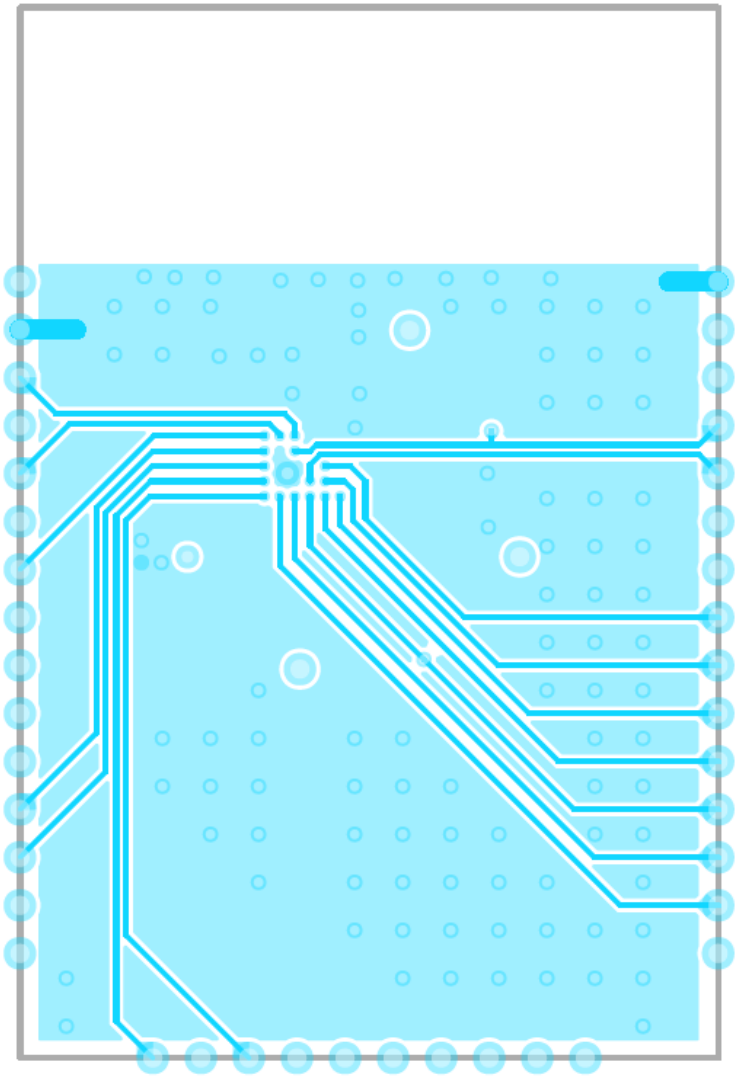


Fig 21. GND layer of the QN9083 PCB layout reference design

Power layer

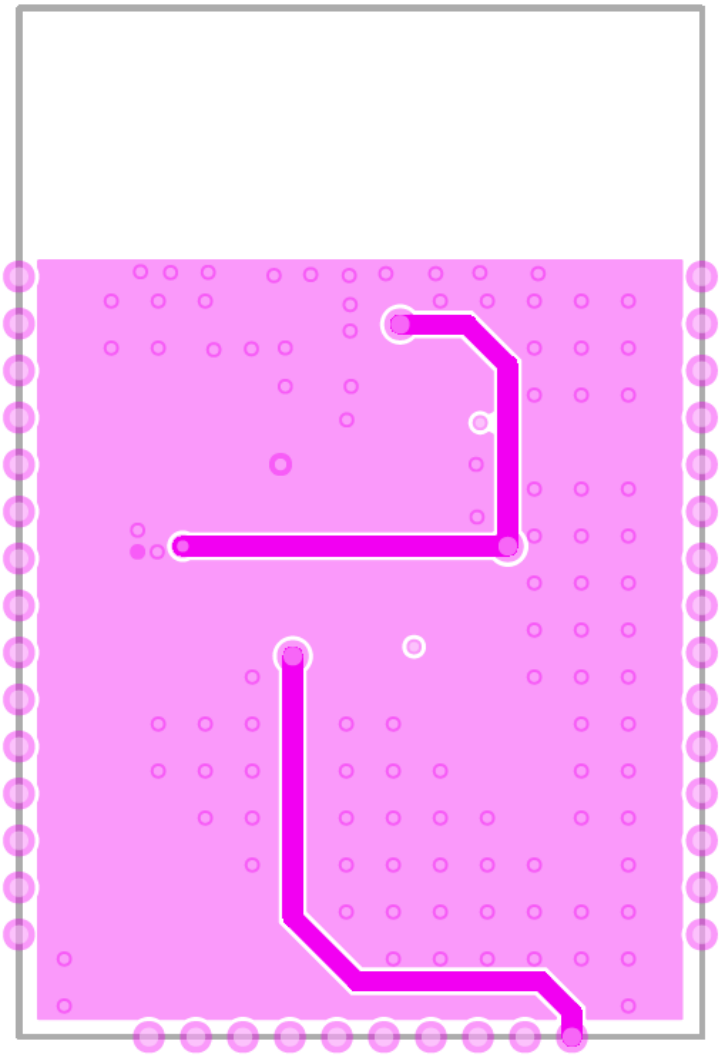


Fig 22. Power layer of the QN9083 PCB layout reference design

Bottom layer

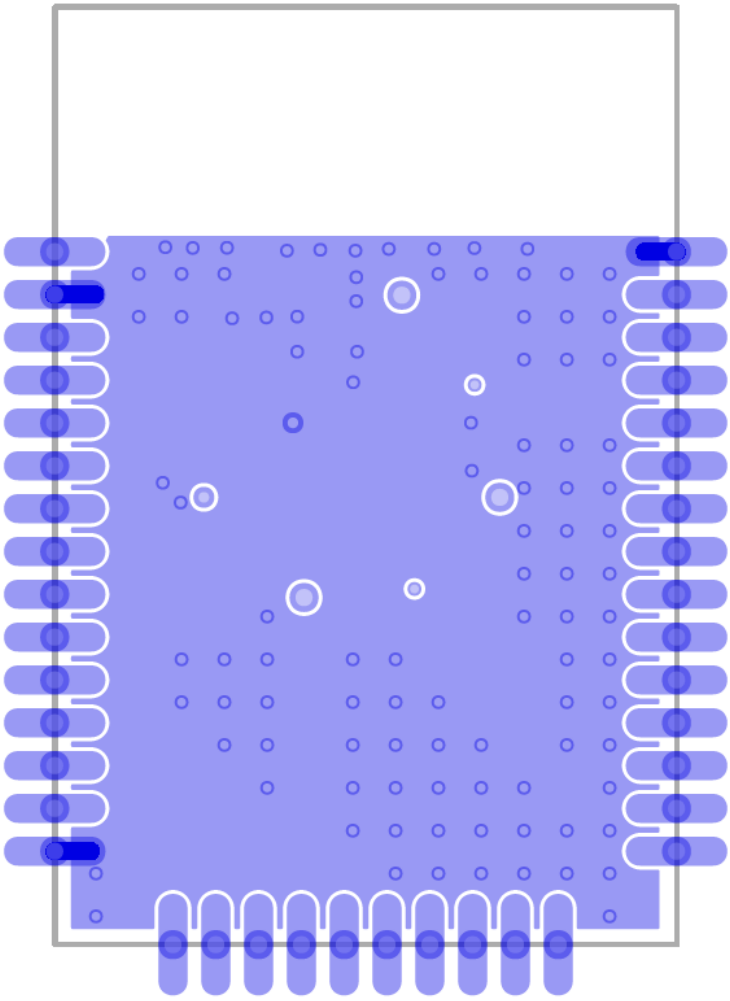


Fig 23. Bottom layer of the QN9083 PCB layout reference design

Contents

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