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KITFS6522LAEEVM, KITFS6523CAEEVM, and KITFS4503CAEEVM evaluation boards

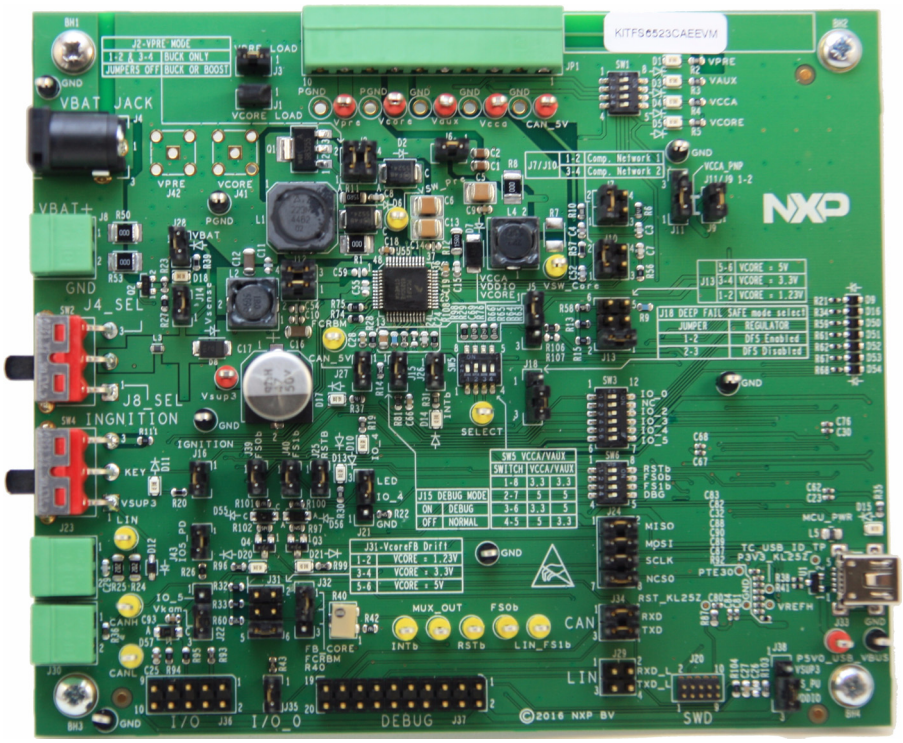

Figure 1. FS45xx/FS65xx evaluation board

Contents

1 Getting started

1.1 Kit contents/packing list

The KITFS6522LAEEVM, KITFS6523CAEEVM, and KITFS4503CAEEVM kit contents include:

- Assembled and tested evaluation boards/modules in anti-static bag
- Connector, terminal block plug, 2 pos., str. 3.81 mm
- Connector, terminal block plug, 10 pos., str. 3.81 mm
- Cable, assy, USB-STD A to USB-B-mini 3.0 ft.
- Quick start guide

1.2 Jump start

NXP's analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal and power solutions. They incorporate monolithic ICs and system-in-package devices that use proven high-volume SMARTMOS technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost and improved performance in powering state of the art systems.

1. Go to the tool summary page:
   www.nxp.com/KITFS6522LAEEVM
   www.nxp.com/KITFS6523CAEEVM
   www.nxp.com/KITFS4503CAEEVM
2. Review the tool summary page
3. Look for

   
   Jump Start Your Design
4. Download the documents, software, and other information
5. Once the files are downloaded, review the user guide in the bundle. The user guide includes setup instructions, BOM, and schematics. Jump start bundles are available on each tool summary page with the most relevant and current information. The information includes everything needed for design.

1.3 Required equipment and software

This kit requires the following items:

- Power supply with a range of 8.0 V to 40 V and a current limit set initially to 2.0 A
- Standard A plug to Mini-B plug USB cable
- FlexGUI graphical user interface
- FlexGUI register definition XML file

2 Getting to know the hardware

2.1 Board overview

The KITFS6522LAEEVM, KITFS6523CAEEVM, and KITFS4503CAEEVM are hardware evaluation tools supporting system designs based on NXP's FS4500 and FS6500 product families. The kits allow testing the devices as an integral part of the overall system being developed. They provide access to all FS45xx and FS65xx functions (SPI, IOs) and support functional modes such as debug, normal, buck, and boost.

Table 1. Kits supporting the FS45xx/FS65xx family

KIT name	Supported silicon	Options
KITFS6522LAEEVM (1)	MC33FS6522LAE	CAN, LIN, No FS1b, V_{CORE} DC/DC 2.2 A
KITFS6523CAEEVM	MC33FS6523CAE	CAN, FS1b, No LIN, V_{CORE} DC/DC 2.2 A
KITFS4503CAEEVM (1)	MC33FS4503CAE	CAN, FS1b, No LIN, V_{CORE} LDO 500 mA

Notes
1. Prototype only. Contact sales for availability.

2.2 Board features

The main features of the KITFS6522LAEEVM, KITFS6523CAEEVM, and KITFS4503CAEEVM evaluation boards are:

- VBAT power supply either through power jack (2.0 mm) or phoenix connector
- VCORE configuration:1.23 V, 3.3 V, and 5.0 V
- VCCA configuration:
  - 3.3 V or 5.0 V
  - Internal transistor or external PNP
- VAUX configuration: 3.3 V or 5.0 V
- Buck or boost setting
- DFS configuration
- Ignition key switch
- LIN bus (optional)
- CAN bus
- FS0B
- FS1B (Option)
- IO connector (IO_0 to IO_5)
- Debug connector (SPI bus, CAN digital, LIN digital, RSTB, FS0B, INTB, Debug, MUX_OUT)
- Signalling LED to give state of signals or regulators
- KL25Z MCU installed on board for easy connection to host computer on USB link

2.3 Block diagram

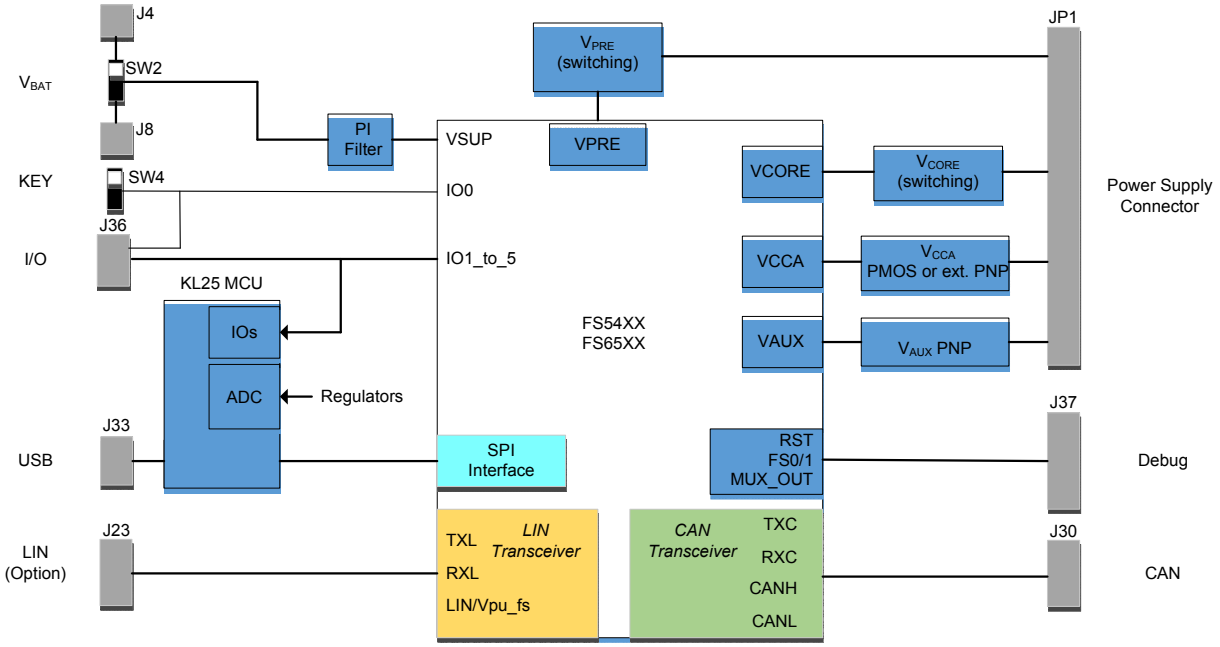

Figure 2. Block diagram

2.4 Device features

The FS65xx/FS45xx are multi-output power-regulating SMARTMOS devices aimed at the automotive market. They include CAN flexible data (FD) and/or LIN transceivers.

Multiple switching and linear voltage regulators—including low-power mode (32 μA) — provide a variety of wake-up capabilities. An advanced power management scheme maintains high efficiency over a wide range of input voltages (down to 2.7 V) and output current ranges (up to 2.2 A).

The FS45xx/FS65xx family includes enhanced safety features with multiple fail-safe outputs. The devices are capable of fully supporting safety-oriented system partitioning with a high integrity safety level (up to ASIL D).

The built-in CAN FD (flexible data-rate) interface meets all ISO11898-2 and -5 standards. The LIN interface is compliant with LIN protocol specifications 2.0, 2.1, 2.2, and SAEJ2602-2.

Table 2. FS45xx/FS65xx features

Device	Description	Features
FS4500/ FS6500	**Automotive control devices**	• Battery voltage sensing and MUX output pin • Highly flexible SMPS pre-regulator, allowing two topologies: non-inverting buck-boost and standard buck • Switching mode power supply (SMPS) dedicated to MCU core supply, from 1.0 V to 5.0 V, delivering up to 2.2 A • Linear voltage regulator dedicated to auxiliary functions, or to sensor supply (V_{CCA} tracker or independent), 5.0 V or 3.3 V • Linear voltage regulator dedicated to MCU A/D reference voltage or I/Os supply (V_{CCA}), 5.0 V or 3.3 V • 3.3 V keep alive memory supply available in low-power mode • Long duration timer available in low-power mode (1.0 s resolution) • Multiple wake-up sources in low-power mode: CAN, LIN, IOs, LDT • Five configurable I/Os
MKL25Z	**Kinetis L 32-bit MCU USB controller**	• Regulator voltage read back (via ADC) • SPI command and control • IO checking • CAN and LIN TX signal support • MCU disconnect capability

2.5 Board overview

The primary components of the evaluation boards are the onboard MCUs. The boards include an FS45xx or FS65xx and provide full access to all the device's features. An MKL25Z MCU USB controller enables access to the FS45xx/FS65xx through a USB connection.

In normal operation, configuration and monitoring applies to the on-board FS45xx/FS65xx device. However, the board can be totally isolated from the on-board MCU. This allows connection to an off-board MCU without interference from the on-board device functions.

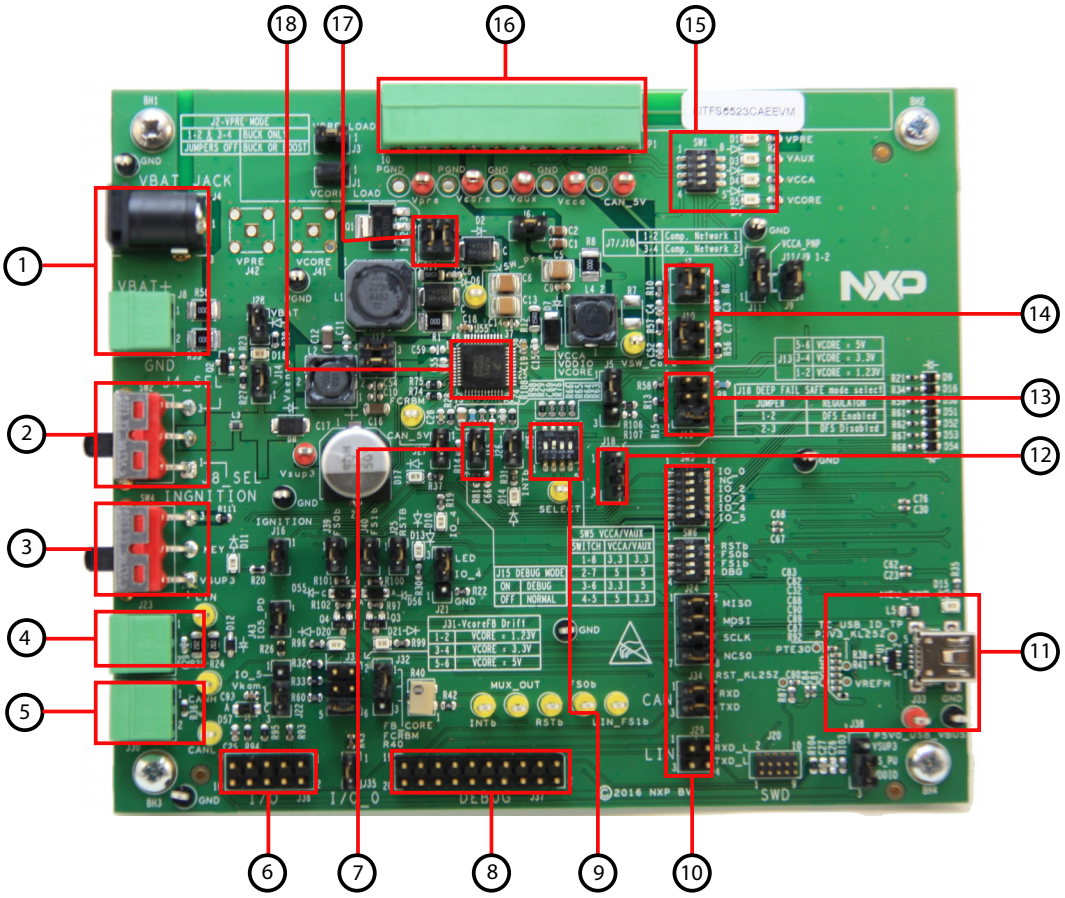

Figure 3. Board description

Table 3. Board description

Number	Description
1	V_{BAT} connectors — Use either jack connector or Phoenix connector to supply board
2	V_{BAT} switch — Select V_{BAT} from jack or from Phoenix connector
3	Ignition key — Ignition key from car
4	LIN bus — LIN bus connector
5	CAN bus — CAN bus connector
6	I/Os — Input and Output from FS45XX/FS65XX (IO0, IO2, IO3, IO4, IO5, GND, V_{KAM}, VDDIO, V_{BAT})
7	DBG mode select
8	Debug connector — Could be used for debug purpose (CAN TX/RX, LIN TX/RX, SPI, Debug, FS0B, FS1B, INTB)
9	V_{CCA} & V_{AUX} selection — Select 3.3 V/5.5 V configuration for V_{CCA} & V_{AUX}
10	MCU to FS65/FS45 connection — Connects part or totality of signals between the KL25Z MCU and FS65XX/FS45XX.
11	KL25 MCU — Location of MCU and USB connector for control through FlexGUI
12	DFS mode select — Enables or disables the deep fail-safe function

Table 3. Board description (continued)

Number	Description
13	V_{CORE} selection — Selects either 1.23, 3.3, or 5.0 V on V_{CORE} DC/DC
14	Compensation network — Selects either Network 1 or 2
15	Power supplies LED — Visualizes regulator state (on or off). The switches can disconnect LEDs
16	Power supplies — Connector for power supplies (CAN_5V/V_{PRE}/V_{CORE}/V_{CCA}/V_{AUX})
17	Buck/buck or boost selection — These jumpers select V_{PRE} mode as a buck or buck or boost.
18	FS45xx/FS65xx

2.6 LEDs

The LEDs are located on the board as shown in Figure 4.

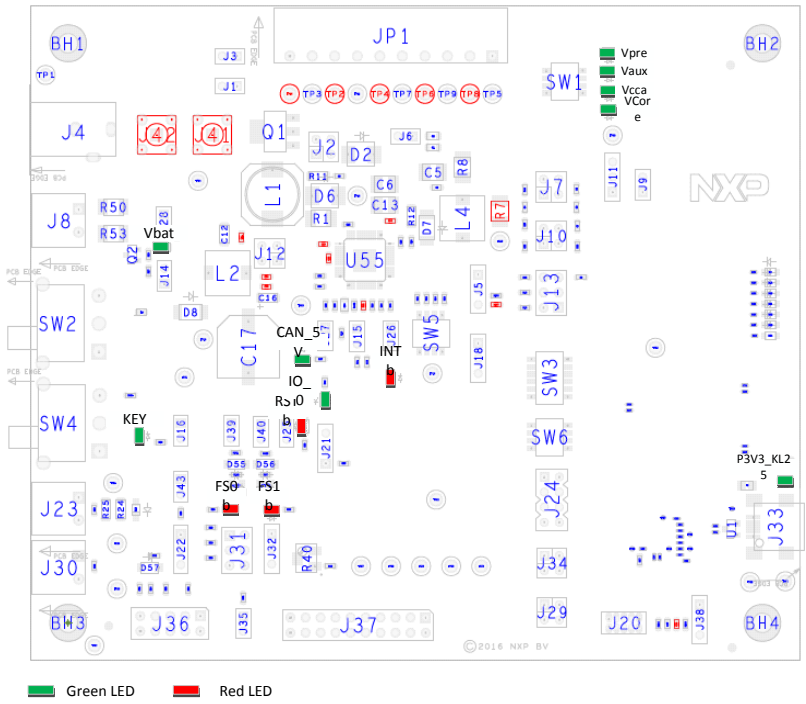

Figure 4. LEDs

The LEDs can be switched on or off through jumpers or switches. Table 4 shows the function of all LEDs.

Table 4. LEDs

Schematic label	Name	Color	LED activation	Description
D1	V_{PRE}	Green	D1/SW1-1	V_{PRE} on
D3	V_{AUX}	Green	D3/SW1-2	V_{AUX} on
D4	V_{CCA}	Green	D4/SW1-3	V_{CCA} on
D5	V_{CORE}	Green	D5/SW1-4	V_{CORE} on
D10	IO_4	Green	D10/J21-2/3	IO_4 high level
D11	KEY	Green	D11/J16	Ignition key switch to V_{SUP3} (tied to IO_0)
D13	RSTB	Red	D13/J25	RSTB asserted (logic level = 0)
D14	INTB	Red	D14/J28	INTB asserted (logic level = 0)
D15	P3V3_KL25	Green	D15/NA	MCU KL25 power supply ON
D17	CAN_5V	Green	D17/J27	CAN_5V ON
D18	V_{BAT}	Green	D18/J28	V_{BAT} ON
D20	FS0B	Red	D20/J39	FS0B asserted (logic level = 0)
D21	FS1B	Red	D21/J40	FS1B asserted (logic level = 0)

2.7 Jumper settings

Figure 5 shows the location of all jumpers on the board. Table 5 provides the name and function of each jumper.

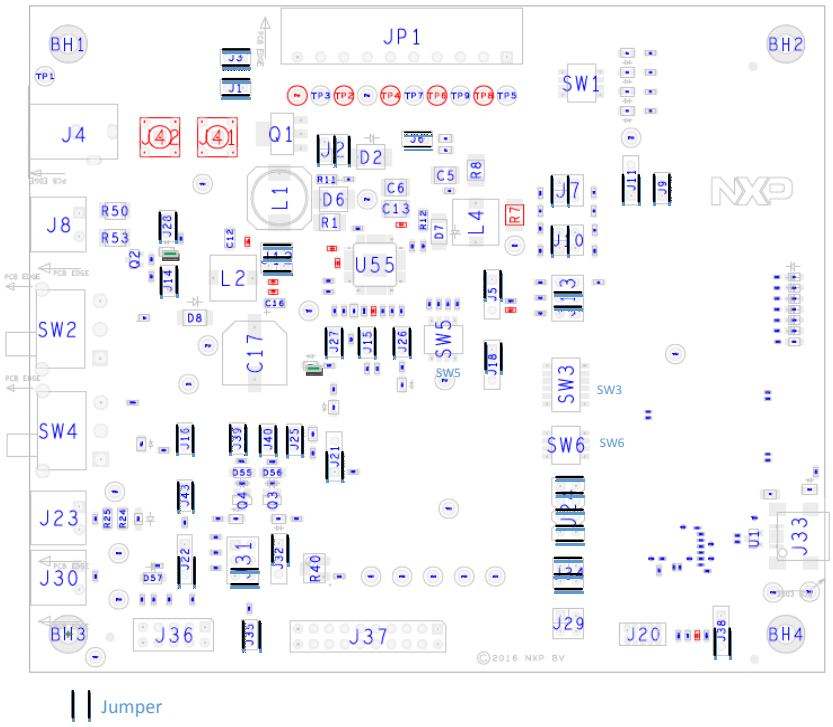

Figure 5. Jumpers

Table 5. Jumper settings

Schematic label	Function	Pin Number	Jumper/pin function
JI	V_{CORE} load	1-2	Connect 30 Ω resistor load on V_{CORE}
J2	V_{PRE} mode	1-2	Both jumper plugged: V_{PRE} Buck configuration Both jumper unplugged: V_{PRE} Boost configuration
		3-4	
J3	V_{PRE} load	1-2	Connect 60 Ω resistor load on V_{PRE}
J5	VDDIO selection	1-2	VDDIO referenced to V_{CCA}
		2-3	VDDIO referenced to V_{CORE} or P3V3_KL25Z. Configuration is selected with R106 or R107, respectively V_{CORE} or P3V3_KL25Z
J6	V_{CORE} output capacitor	1-2	V_{CORE} output capacitance. When set, adds 20 µF on V_{CORE}.
J7	Comp. network1	1-2	Select compensation network1. Used in conjunction with J10:1-2
	Comp. network2	3-4	Select compensation network2. Used in conjunction with J10:3-4
J9	V_{CCA} PNP		External PNP used Used in conjunction with J11:1-2
	V_{CCA} MOS	1-2	Internal MOS used Used in conjunction with J11:2-3
J10	Comp. network1	1-2	Select compensation network1. Used in conjunction with J7:1-2
	Comp. network2	3-4	Select compensation network2. Used in conjunction with J7:3-4
J11	V_{CCA} PNP	1-2	External PNP used in conjunction with J11:1-2
	V_{CCA} MOS	2-3	Internal MOS used in conjunction with J11:2-3
J12	V_{SUP}1-2	1-2	Connect V_{SUP1} and V_{SUP2} to the power supply on the output of PI filter
	V_{SUP}3	3-4	Connect V_{SUP3} to the power supply (before PI filter)

Table 5. Jumper settings (continued)

Schematic label	Function	Pin Number	Jumper/pin function
J13	V_{CORE} setting	1-2	V_{CORE} = 1.23 V
		3-4	V_{CORE} = 3.3 V
		5-6	V_{CORE} = 5.0 V
J14	V_{SENSE}	1-2	Connect V_{SENSE} to V_{BAT}
J15	Debug mode	1-2	ON: Debug mode off: normal mode
J16	KEY LED	1-2	Enable KEY signaling LED
J18	DFS	1-2	DFS enabled
		2-3	DFS disabled
J21	IO_4	1-2	IO_4 tied to GND through 510 k
		2-3	IO_4wired on LED signaling works in conjunction with J19:1-2
J22	IO_5	1-2	Connect IO_5 to KL25Z and I/O connector (J36-5)
	V_{KAM}	2-3	Connect V_{KAM} to I/O connector(J36-8) and 220 nF capacitor.
J25	RSTB	1-2	Enable RSTB signaling LED
J26	INTB	1-2	Enable INTB signaling LED
J27	CAN_5V	1-2	Enable CAN_5V signaling LED
J28	V_{BAT}	1-2	Enable V_{BAT} signaling LED
J31	V_{CORE} drift	1-2	V_{CORE} = 1.23 V
		3-4	V_{CORE} = 3.3 V
		5-6	V_{CORE} = 5.0 V
J32	FCRBM	1-2	Connect FB_Core to FCRBM
		2-3	Connect potentiometer R40 to FCRBM
J35	IO-0	1-2	Connect IO_0 to ground through 510 k
J38	FS0B Pull-up	1-2	FS0b pull-up connected to VSUP3
		2-3	FS0b pull-up connected to VDDIO
J39	FS0B LED	1-2	Enable FS0B signaling LED
J40	FS1B LED	1-2	Enable V_{PU} FS signaling LED (FS1B)
J41	V_{CORE}	1	SMB connector on V_{CORE}
J42	V_{PRE}	1	SMB connector on V_{PRE}
J43	IO_5	1-2	Connect IO_5 to ground through 5.1 k

2.8 Test point definitions

Figure 6 shows the location of the test points on the board.

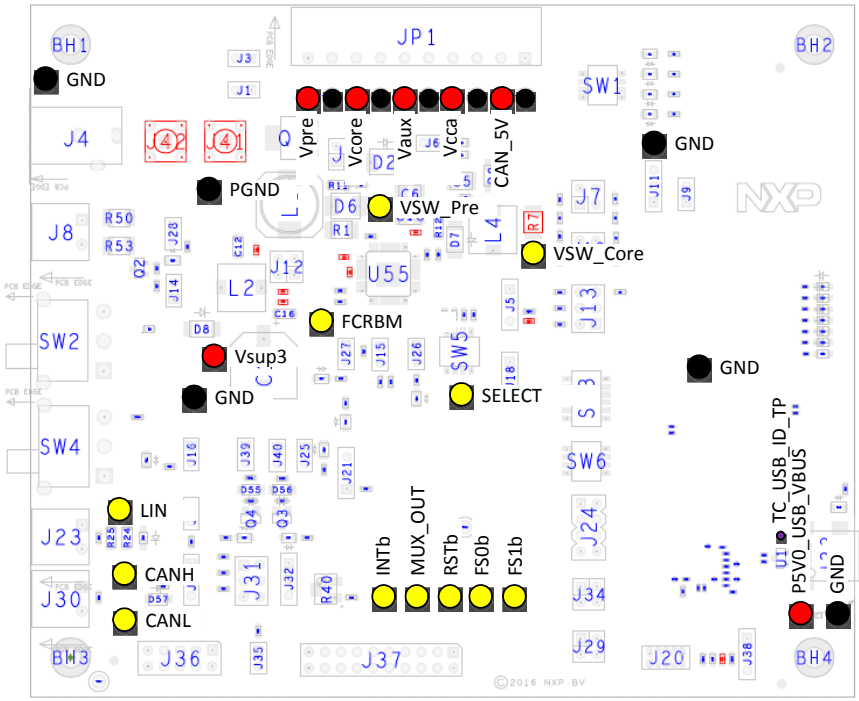

Figure 6. Test points

The following test points provide access to various signals to and from the board.

Table 6. Test points

Schematic label	Signal name	Schematic label/description
TP1	GND	Ground
TP2	GND	Ground
TP3	V_{PRE}	TP3/V_{PRE} regulator output voltage
TP4	GND	Ground
TP5	CAN_5V	TP5/CAN power supply
TP6	GND	Ground
TP7	V_{AUX}	TP7/V_{AUX} output voltage
TP8	GND	Ground
TP9	V_{CCA}	TP9/V_{CCA} output voltage
TP10	PGND	TP10/power ground
TP11	V_{CORE}	TP11/V_{CORE} output voltage
TP12	GND	Ground
TP13	GND	Ground
TP14	PGND	Power ground
TP15	VSW_PRE	TP15/V_{PRE} switcher signal
TP16	V_{SUP3}	TP16/V_{SUP3} voltage
TP17	GND	Ground

Table 6. Test points (continued)

Schematic label	Signal name	Schematic label/description
TP18	VSW_Core	TP18/V_{core} switcher
TP19	SELECT	TP19/SELECT pin voltage
TP20	TC_USB_ID_TP	TP20/USB Identification pin
TP21	LIN	TP21/LIN bus signal
TP22	GND	Ground
TP23	FCRBM	TP23/feedback core resistor bridge monitoring
TP24	CANH	TP24/CAN high
TP25	CANL	TP25/CAN low
TP26	MUX_OUT	TP26/MUX_OUT signal
TP27	INTB	TP27/INTB/interrupt pin level. Active low
TP28	RSTB	TP28/Reset. Active low
TP29	FS1B	TP29/fail-safe 1 signal. Active low
TP30	FS0B	TP30/fail-safe 0 signal. Active low
TP31	GND	Ground
TP32	P5V_USB_CONN_VBUS	TP32/USB power supply level
TP33	GND	Ground

2.9 Connectors

Figure 7 shows the location of connectors on the board. Table 7 and Table 8 list the pin-outs for each connector.

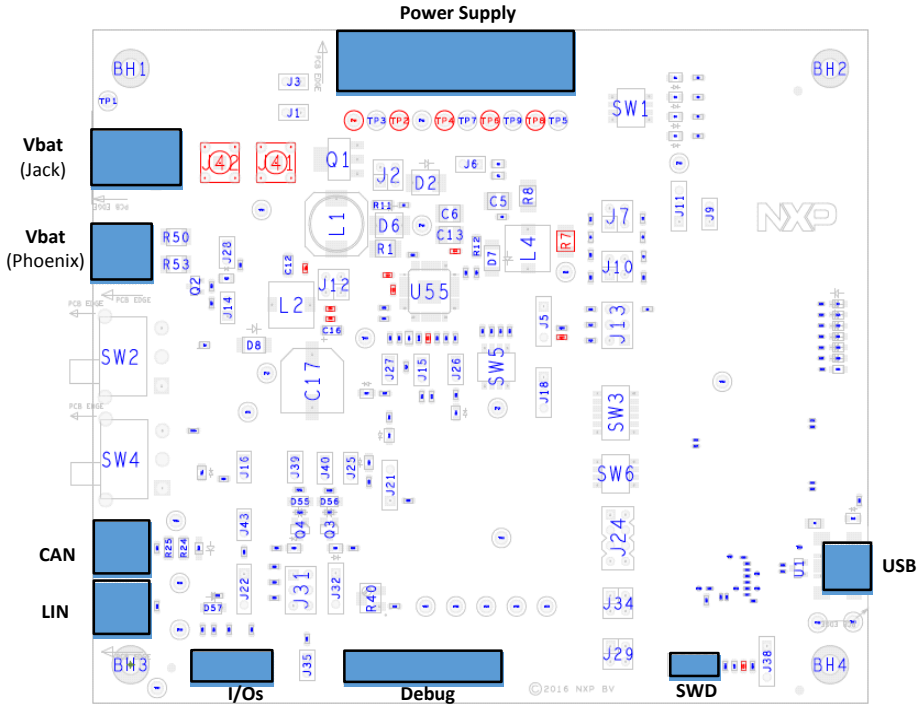

Figure 7. Connectors

2.9.1 V_{BAT} connectors (J4 and J8)

V_{BAT} connects to the board either through jack connector (J4) or Phoenix connector (J8) at the user's discretion. Switch SW2 switches from one source to the other.

Table 7. V_{BAT} jack connector (J4)

Pin number	Connection	Description
1	V_{BAT}	Connects to V_{BAT} when switch SW2 is set to V_{BAT}
2	Ground	Connects to ground when switch SW2 is set to ground

Table 8. V_{BAT} Phoenix connector (J8)

Pin number	Connection	Description
1	V_{BAT}	Connects to V_{BAT} when switch SW2 is set to V_{BAT}
2	Ground	Connects to ground when switch SW2 is set to ground

2.9.2 Debug connector (J37)

The Debug connector (J37) gives access to the FS65xx main signal for debug or experimentation purposes.

Table 9. Debug connector (J37)

Pin number	Connection	Description
1	FSOB	Fail-safe 0.
2	VDDIO	Reference voltage for IOs.
3	MISO	SPI, Master Input Slave Output
4	RSTB	Reset, active low
5	MOSI	SPI Master Output Slave Input
6	GND	Ground
7	SCLK	SPI serial clock
8	GND	Ground
9	NCSB	SPI chip select, active low.
10	GND	Ground
11	MUX_OUT	Multiplexer output
12	INTB	Interrupt output. Active low.
13	RXD_L	LIN receiver data. Logic level.
14	TXD_L	LIN transmit data. Logic level.
15	GND	Ground
16	FS1B	Fail-safe 1
17	RXD	CAN receiver data. Logic level
18	TXD	CAN transmit data. Logic Level
19	DBG	Debug pin selection
20	GND	Ground

2.9.3 LIN connector (J23)

The LIN connector is mounted on all three kits, but LIN is supported only on the KITFS6522LAEEVM.

Table 10. LIN connector (J23)

Pin number	Connection	Description
1	LIN	Connects to the LIN bus
2	GND	Connects to ground.

2.9.4 CAN connector (J30)

Table 11. CAN connector (J30)

Pin number	Connection	Description
1	CANH	Connects to the CANH bus line
2	CANL	Connects to CANL bus line

2.9.5 USB connector (J33)

The USB connector provides a communication link between the evaluation board's MKL25Z device and a PC running the FlexGUI software.

Table 12. USB connector (J33)

Pin number	Connection	Description
1	P5V0_USB_CONN_VBUS	+5.0 V DC supply
2	USB_CONN_DN	Data–
3	USB_CONN_DP	Data+
4	TC_USB_ID_TP	USB OTG ID
5	GND	Ground

2.9.6 I/O connector (J36)

The I/O connector accesses the device under test (DUT) IO and V_{KAM} signals.

Table 13. I/O connector (J36)

Pin number	Connection	Description
1	Not connected	Not connected
2	IO_0	Input/Output 0
3	IO_3	Input/Output 3
4	IO_2	Input/Output 2
5	IO_5	Input/Output 5
6	IO_4	Input/Output 4
7	VDDIO	Reference voltage for IOs.
8	V_{KAM}	Keep alive memory voltage
9	V_{BAT}	Battery voltage
10	GND	Ground

2.9.7 Power supply connector (JP1)

The power supply connector (JP1) connects any of the SBC regulators to an external load or board for evaluation purposes.

Table 14. Power supply connector (JP1)

Pin number	Connection	Description
1	CAN_5V	CAN voltage regulator
2	GND	Ground
3	V_{CCA}	V_{CCA} output voltage
4	GND	Ground
5	V_{AUX}	V_{AUX} auxiliary voltage regulator
6	GND	Ground
7	V_{CORE}	V_{CORE} voltage output
8	GND	Ground
9	V_{PRE}	V_{PRE} regulator output regulator
10	GND	Ground

2.10 Switches

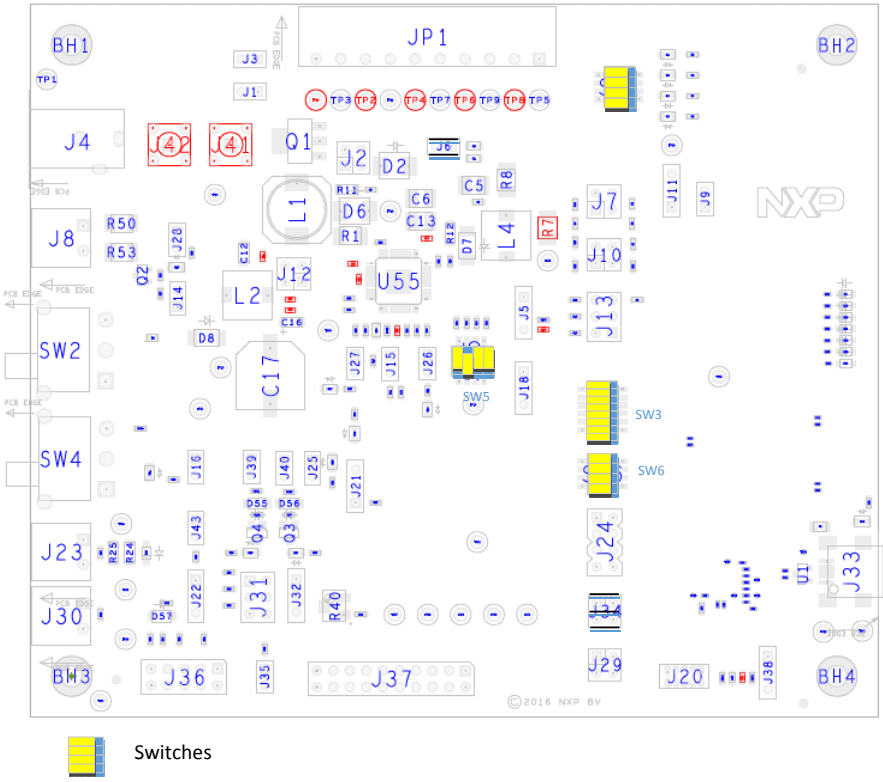

Figure 8. Switches

2.10.1 SW3

Table 15. SW3

Position	Function	Description
1	IO_O	Connection between IO_O from product to MCU
2	NA	Not used
3	IO_2	Connection between IO_2 from product to MCU
4	IO_3	Connection between IO_3 from product to MCU
5	IO_4	Connection between IO_4 from product to MCU
6	IO_5	Connection between IO_5 from product to MCU

2.10.2 SW5

Table 16. SW5

Switch	V_{CCA}	V_{AUX}
1 – 8	3.3 V	3.3 V
2 – 7	5.0 V	5.0 V
3 – 6	3.3 V	5.0 V
4 – 5	5.0 V	3.3 V

2.10.3 SW6

Table 17. SW6

Position	Function	Description
1	RSTB	Connection between RSTB from product to MCU
2	FS0B	Connection between FS0B from product to MCU
3	FS1B	Connection between FS1B from product to MCU
4	DBG	Connection between DBG from product to MCU

3 Configuring the hardware

3.1 Connecting the hardware

The KITFS6522LAEEVM/KITFS6523CAEEVM/KITFS4503CAEEVM must be connected to a PC through the USB port on the board. A 13.5 V power supply connects either to a jack connector (J4) or a Phoenix connector (J8). The evaluation board connects to an external load or another board through connector JP1.

Caution:

To avoid damaging the board, the V_{BAT} voltage must not exceed 40 V.

1. With the power switched off, attach the DC power supply to either the Jack connector (J4) or the Phoenix connector (J8) on the evaluation board. (There is no difference between the two connectors other than plug compatibility.)
2. Attach a load or an external board through connector JP1.
3. Connect a USB cable from the evaluation board USB port (J33) to the USB port on a PC with the FlexGUI installed.
4. Turn on the DC power supply.

Figure 9 illustrates the hardware configuration.

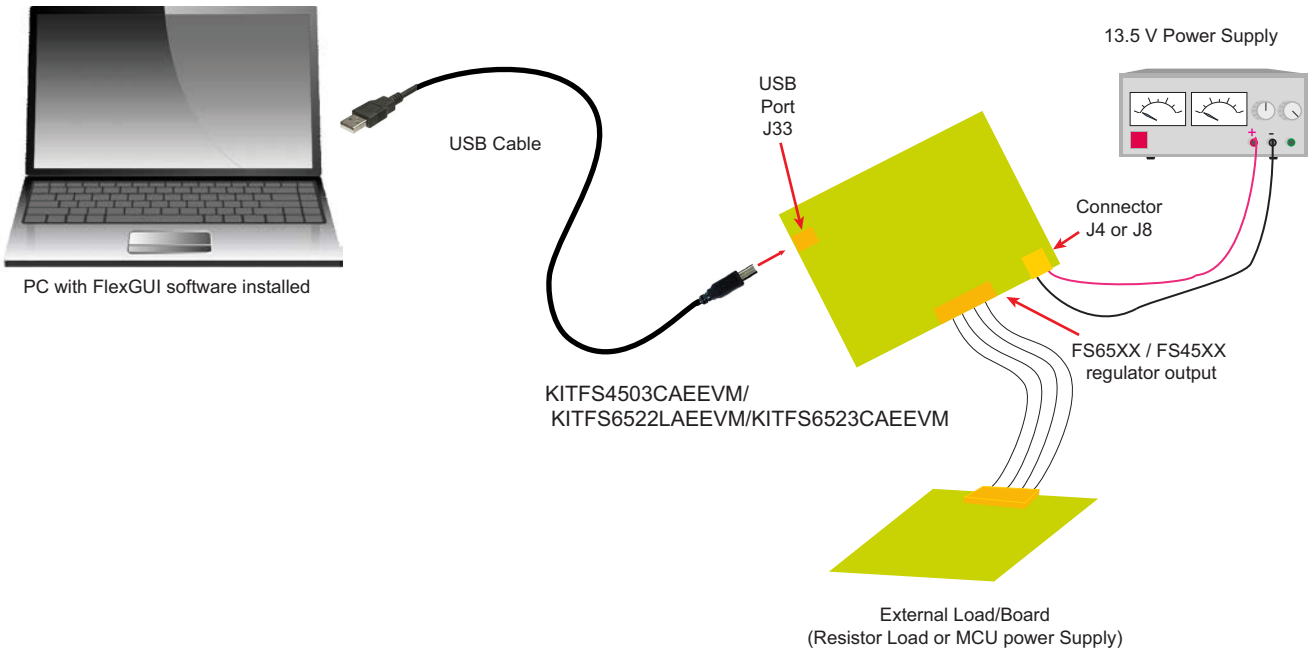

Figure 9. Evaluation board hardware configuration

4 Evaluation board settings

4.1 V_{CCA} and V_{AUX} setting

To select various voltage levels on V_{CCA} and V_{AUX}, set the switch SW5 as shown in Table 18 and Figure 10 below:

Table 18. SW5 V_{CCA}/V_{AUX} voltage configurations

Switch	V_{CCA}	V_{AUX}
1 – 8	3.3 V	3.3 V
2 – 7	5.0 V	5.0 V
3 – 6	3.3 V	5.0 V
4 – 5	5.0 V	3.3 V

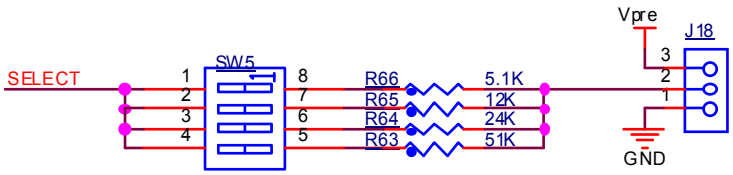

Figure 10. V_{CCA} and V_{AUX} voltage settings

V_{CCA} regulator can be configured to use the internal PMOS transistor at current levels up to 100 mA. To achieve higher current levels (up to 300 mA), use a PNP external transistor. Table 19 and Figure 11 show the jumper settings for both configurations.

Table 19. J9/J11 V_{CCA} PNP configurations

Jumper	J9	J11
Internal MOS	OFF	2 – 3
External PNP	ON	1 – 2

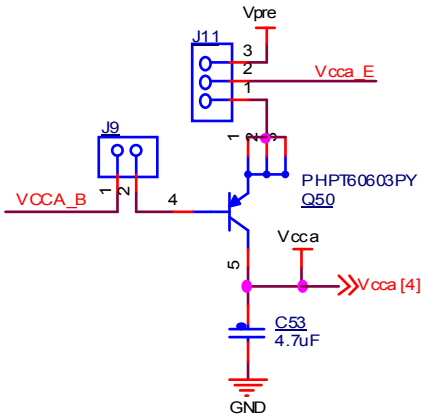

Figure 11. V_{CCA} transistor setting

The V_{CCA} regulator is always tied to the external PNP transistor. Resistors R105 and R10 limit the power dissipation in the PNP transistor.

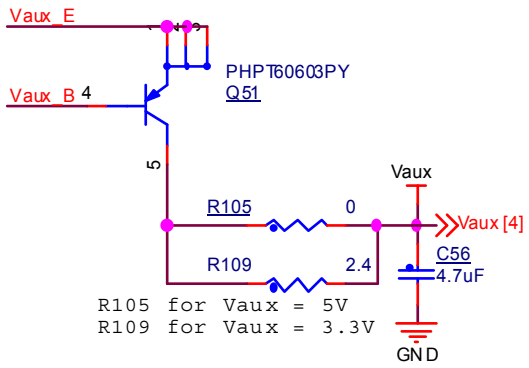

Figure 12. V_{AUX} external transistor

4.2 V_{CORE} settings and related configurations

4.2.1 V_{CORE} and F45xx versus FS65xx

The FS45xx family of devices only support V_{CORE} LDO (low dropout) voltage regulators. The FS65xx family only supports V_{CORE} DC/DC voltage regulators. The evaluation board circuitry accommodates this discrepancy by implementing a separate circuit network for each of the two device families. Populating or not populating resistors R7 and R8 depend on which device family is in use and determines which network is enabled.

For the FS45xx family, R7 is populated and R8 is not populated. For the FS65xx family, R8 is populated and R7 is not populated. Because resistor R8 is not populated for FS45xx devices, the compensation network is also disabled for those devices. See Figure 13.

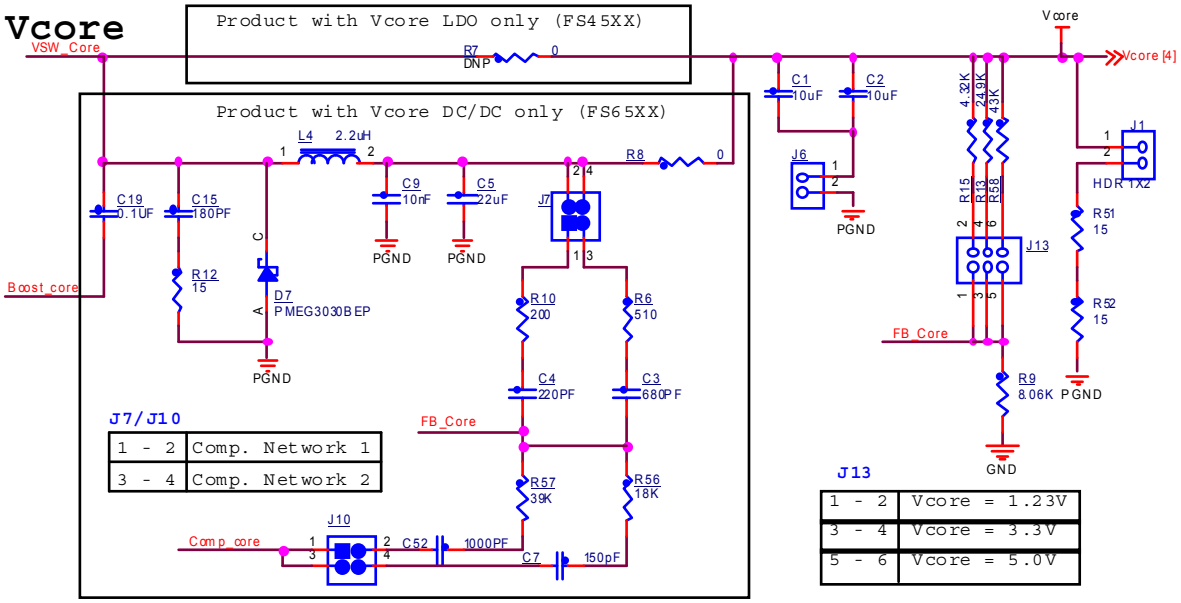

Figure 13. V_{CORE} configuration

4.2.2 Compensation network

Both LDO and DC/DC voltage regulators use V_{CORE} voltage feedback to control the output voltage. For this reason, two separate external bridges enable feedback support for either FS45xx or FS65xx devices (see Figure 13).

For FS45xx devices using static (steady-state) LDO regulators, a simple resistor bridge (resistors R15/R13/R58 and R9) in conjunction with jumper settings on jumper J13 determines the feedback voltage.

For FS65xx devices using DC/DC voltage regulators, a selectable pair of RC voltage dividers control the dynamic behavior of the regulator. One RC divider --compensation network 1-- consists of the resistor-capacitor series R10/C4/R57/C52. The other RC divider --compensation network 2-- consists of the resistor-capacitor series R6/C3/R56/C7. Jumpers J7 and J10 select which of the two compensation networks is enabled.

The default value for compensation network 1 is 1.23 V. For compensation network 2, the default value is 3.3 V. These values can be changed for other configurations. The compensation network tool referenced in Table 26 is useful in calculating the appropriate values.

Table 20 illustrates the jumper settings for each feedback voltage level.

Table 20. V_{CORE} compensation network settings

V_{CORE}	Jumper setting		
	Static behavior	Dynamic behavior	
	J13	J7	J10
1.23 V	1–2	1–2	1–2
3.3 V	3–4	3–4	3–4
5.0 V	5–6	(2)	(2)

Notes
2. Use compensation network tool to calculate value

4.2.3 FCRBM resistor bridge

The feedback core bridge monitoring (FCRBM) resistor bridge is an evaluation board safety feature.

The bridge generates the same voltage as the bridge connected to the FB_core pin. If the difference between the two voltages is greater than the VCORE_FB_DRIFT value, the FS state machine is impacted (refer to data sheet).

To implement this functionality, use jumper J31 to configure the second resistor bridge as shown in Figure 14. Then, set the potentiometer R40 to match the voltage of the first V_{CORE} bridge.

To disable the FCRBM function, place a jumper on position 1–2 of J32. This connects FB_CORE directly to the FCRBM bridge, causing the drift to be zero.

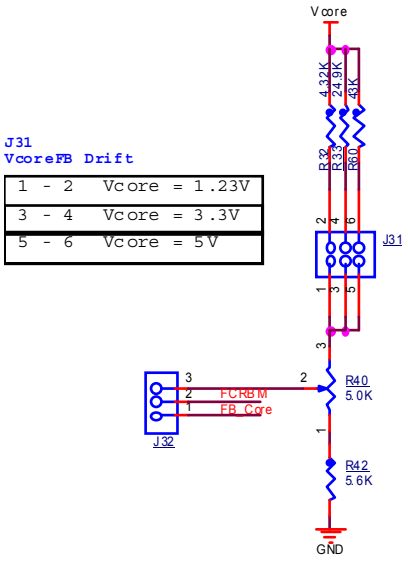

Figure 14. FCRBM bridge resistor

4.3 MCU settings

4.3.1 MCU jumper configuration

Table 21. MCU Jumper configuration

Schematic label	Pin number	Function	Jumper/pin function
J24	1–2	SPI	Connect MISO to KL25Z
	3–4		Connect MOSI to KL25Z
	5–6		Connect MSCLK to KL25Z
	7–8		Connect NCSB to KL25Z
J29	1–2	LIN	Connect RXD_L LIN to KL25Z
	3–4		Connect TXD_L LIN to KL25Z
J34	1–2	CAN	Connect RXD CAN to KL25Z
	3–4		Connect RXD CAN to KL25Z

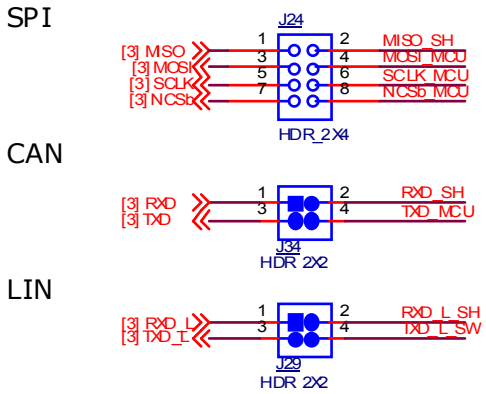

Figure 15. MCU jumper configuration

4.3.2 MCU switch configuration

4.3.2.1 Switch SW3

Table 22. Switch SW3

Position	Function	Description
1	IO_O	Connection between IO_O from product to MCU
2	NA	Not used
3	IO_2	Connection between IO_2 from product to MCU
4	IO_3	Connection between IO_3 from product to MCU
5	IO_4	Connection between IO_4 from product to MCU
6	IO_5	Connection between IO_5 from product to MCU

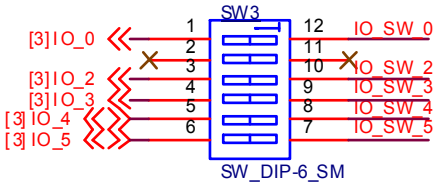

Figure 16. Switch SW3

4.3.2.2 Switch SW6

Table 23. Switch SW6

Position	Function	Description
1	RSTB	Connection between RSTB from product to MCU
2	FS0B	Connection between FS0B from product to MCU
3	FS1B	Connection between FS1B from product to MCU
4	DBG	Connection between DBG from product to MCU

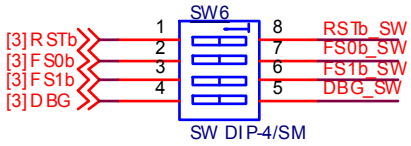

Figure 17. Switch SW6

4.3.3 MCU analog input

To assure the complete isolation of analog signals connected from an external component to the MCU, remove input resistance as applicable for the following:

- V_{PRE} tied to MCU through R82
- V_{CORE} tied to MCU through R89
- V_{AUX} tied to MCU through R90
- V_{CCA} tied to MCU through R82
- CAN_5V tied to MCU through R80
- MUX_OUT tied to MCU through R71
- V_{DDIO} tied to MCU through R70
- V_{KAM} tied to MCU through R79

5 Software

The KITFS6522LAEEVM/KITFS6523CAEEVM/KITFS4503CAEEVM is bundled with software allowing the user to interact directly with the onboard MCU during the development process. The boards contain an MKL25Z Kinetis processor pre-loaded with firmware controlling communication with the FS45xx/FS65xx MCU. A graphical user interface installed on a PC serves as the user interface to the evaluation board. When connecting the evaluation board to a PC through a USB cable, the following data exchanges are available:

- SPI access (read and write) to FS45xx/FS65xx
- ADC readout, connected to regulators
  - V_{PRE}
  - V_{CORE}
  - V_{AUX}
  - V_{CCA}
  - CAN_5V
  - MUX_OUT
  - V_{DDIO}
  - V_{KAM}
- I/O readout, connected to IO_0 to IO_5
- FS0B/FS1B readout
- RSTB readout
- CAN generated TX signal
- LIN generated TX signal with loopback checking

Note that MCU connections to FS45XX/FS65XX can be fully isolated by removing related jumpers and switching off the related switch.

The software bundle also includes an XML file containing register descriptions for the FS45xx or FS65XX (depending on the evaluation board). This file must be installed for the GUI to work properly. In addition, an optional Excel file can be created to facilitate setting several registers at a click.

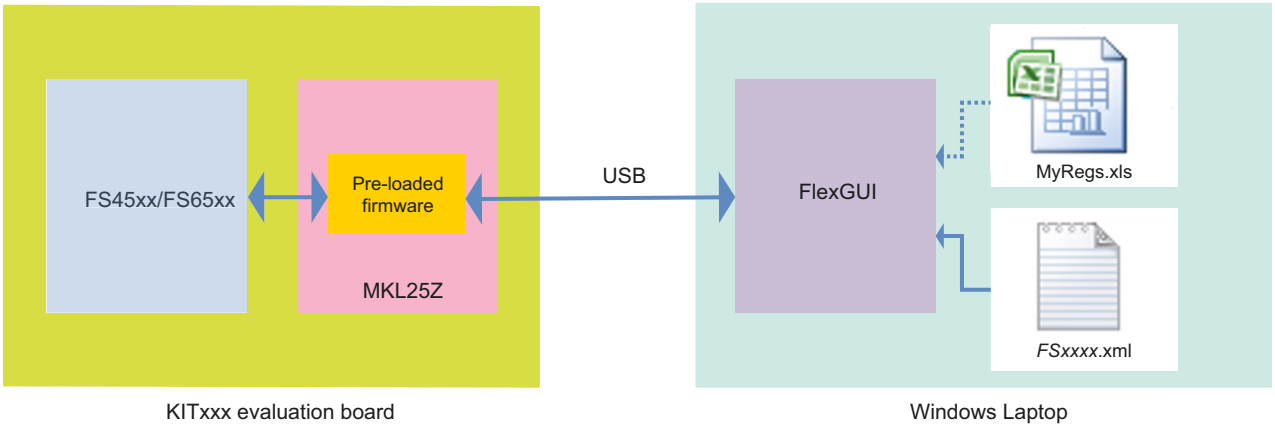

Figure 18. Software overview

5.1 Installing the FlexGUI

The FlexGUI graphical user interface provides a PC-based interface for accessing the evaluation board and exercising FS45xx/FS65xx functions. The GUI runs on any Windows 8, Windows 7, Vista, or XP-based operating system.

To install the FlexGUI software:

1. Go to the evaluation board tool summary page
2. Under **Jump Start Your Design**, click on the **Get Started with the KITFS65xx** link.
3. From the list of files that appear, click on the **FlexGUI** link. The software downloads to the PC and initiates the installation. An installation wizard guides the user through the process. Upon completion, the GUI executable (FlexGUI.exe), and the relevant register description XML file are installed on the system.
4. To simplify launching the FlexGUI, create a .bat file with the following commands:

```
C:\Program Files (x86)\FlexGUI\bin\FlexGUI.exe
C:\Program Files (x86)\FlexGUI\Sequences&Config\FSxxxx.xml
```

5.2 Creating and using a register configuration file

Creating an Excel register configuration file allows the user to initialize the evaluation board MCU with a predefined set of register values. To create a register configuration file, do the following:

1. Open a new Excel spreadsheet file and label the first three columns in row 1 **hex**, **registers** and **comment**. Notice that the first two columns —**hex** and **registers**— are mandatory. The **comment** column is optional.
2. In the **hex** column (column A), enter the data or address to be assigned to each register. The address and data must be contained in two bytes and must be expressed as a hexadecimal value. Enter one row per register.
3. In the **registers** column (column B), enter the register name associated with the value in the **hex** column.
4. In the **comments** column (column C), enter any comments desired. Data in this column is not processed by the FlexGUI.

Figure 19 illustrates a typical register configuration file.

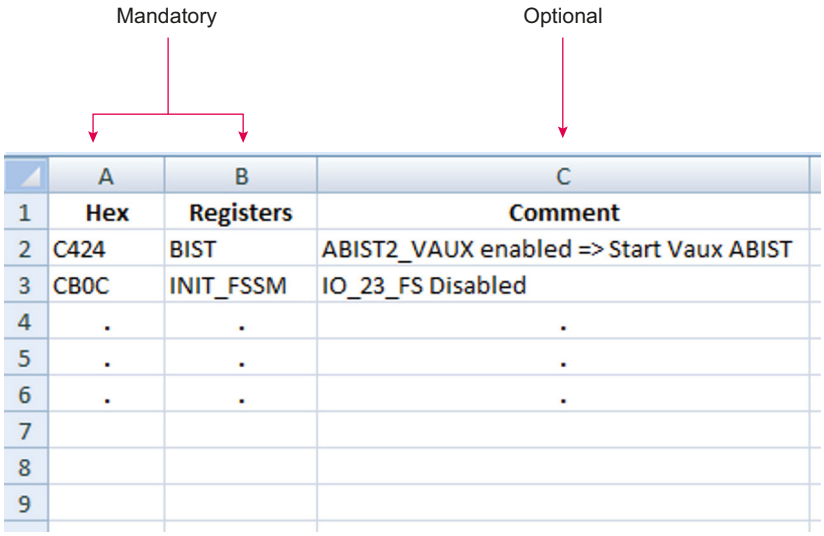

Figure 19. Register configuration Excel file

5. Launch FlexGUI. When FlexGUI opens, click the **load sequence** button to load the register configuration file (see Figure 20).

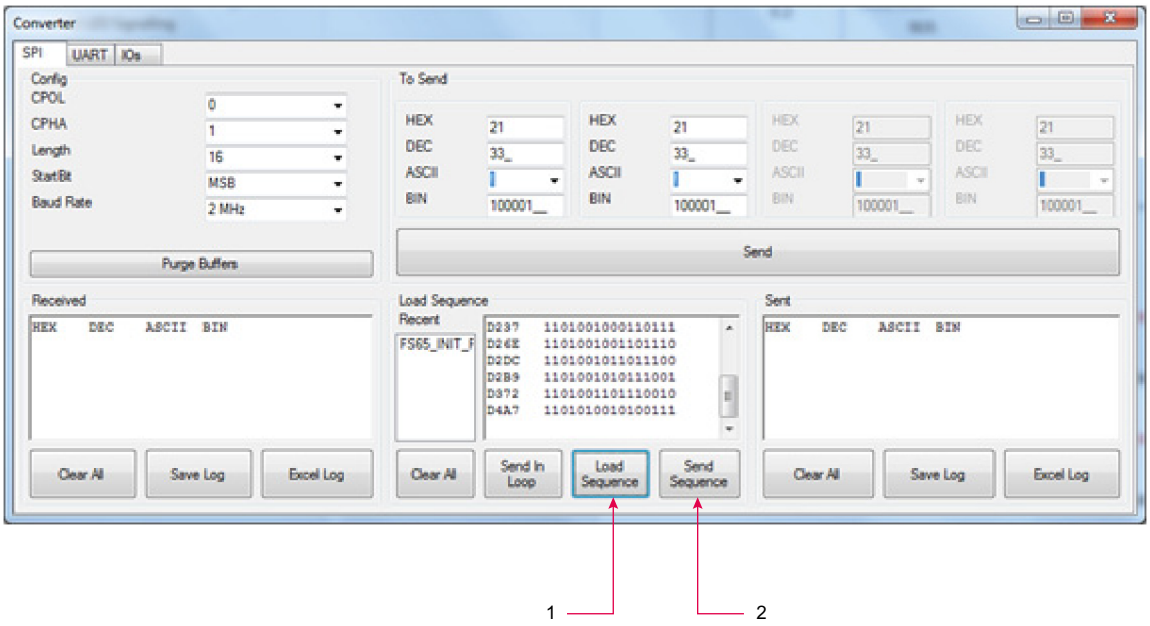

Figure 20. Loading the register configuration example file

6. Send the resister configuration file to the FS45xx/FS65xx by clicking the **send sequence** button (see Figure 20).

5.3 Using the FlexGUI

To start the FlexGUI, do the following:

1. Configure the hardware as described in Section 3.1, Connecting the hardware.
2. To launch the FlexGUI, execute the .bat file created in Section 5.1, Installing the FlexGUI.

5.4 Use case example

This example assumes the user has configured the hardware as shown in Figure 9 and put the evaluation board into debug mode by placing a connector on jumper J15 (see Table 5). After launching the FlexGUI, the example configures registers to disable IO_23_FS safety mode, disable the watchdog and release the FS*x* pins.

1. Create an Excel file configured as shown in Table 24. For details on creating an Excel register configuration file, see Section 5.2, Creating and using a register configuration file.

Table 24. Use case register configuration Excel file example

HEX	Registers	Comment
C424	BIST	ABIST2_VAUX enabled => Start V_{AUX} ABIST
CB0C	INIT_FSSM	IO_23_FS Disabled
8900	INIT_INT	Close main machine initialization sequence
D34D	WD_refresh_0	1st Watchdog refresh answer
D29B	WD_refresh_1	2nd Watchdog refresh answer
D237	WD_refresh_2	3rd Watchdog refresh answer
D26E	WD_refresh_3	4th Watchdog refresh answer
D2DC	WD_refresh_4	5th Watchdog refresh answer
D2B9	WD_refresh_5	6th Watchdog refresh answer
D372	WD_refresh_6	7th Watchdog refresh answer
D4A7	RELEASE_FSxB	Release FS0B & FS1B pins

2. To use the register configuration file, open FlexGUI, then load the register configuration file and send it to the evaluation board (see Figure 20).

Now read or write any bit from the FS45xx/FS65xx on-board MCU as shown in Table 21.

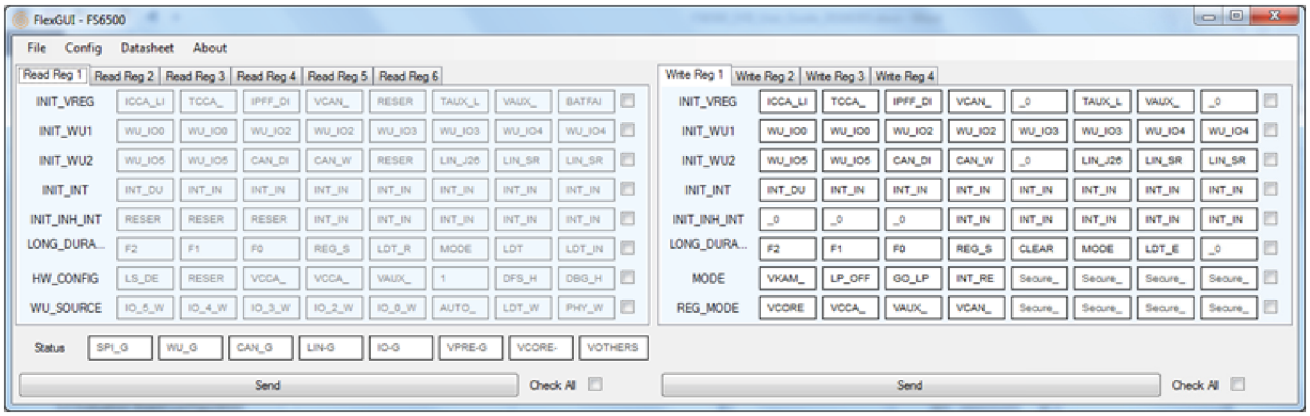

Figure 21. FlexGUI register window

Register values display in the register value window as shown in Figure 22.

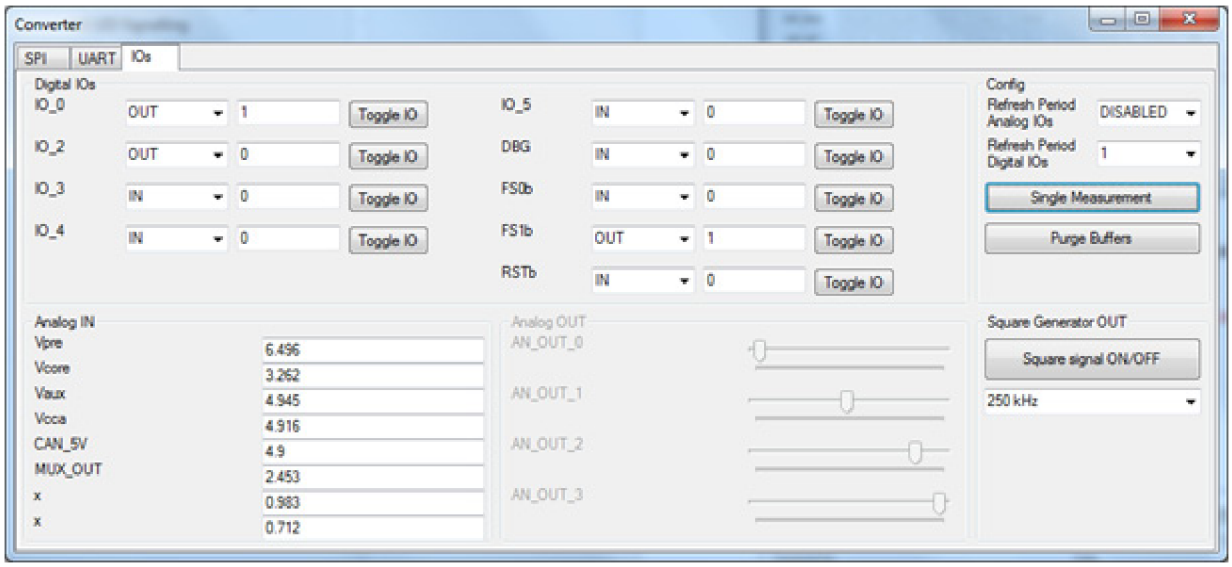

Figure 22. FlexGUI register value window

6 Schematic

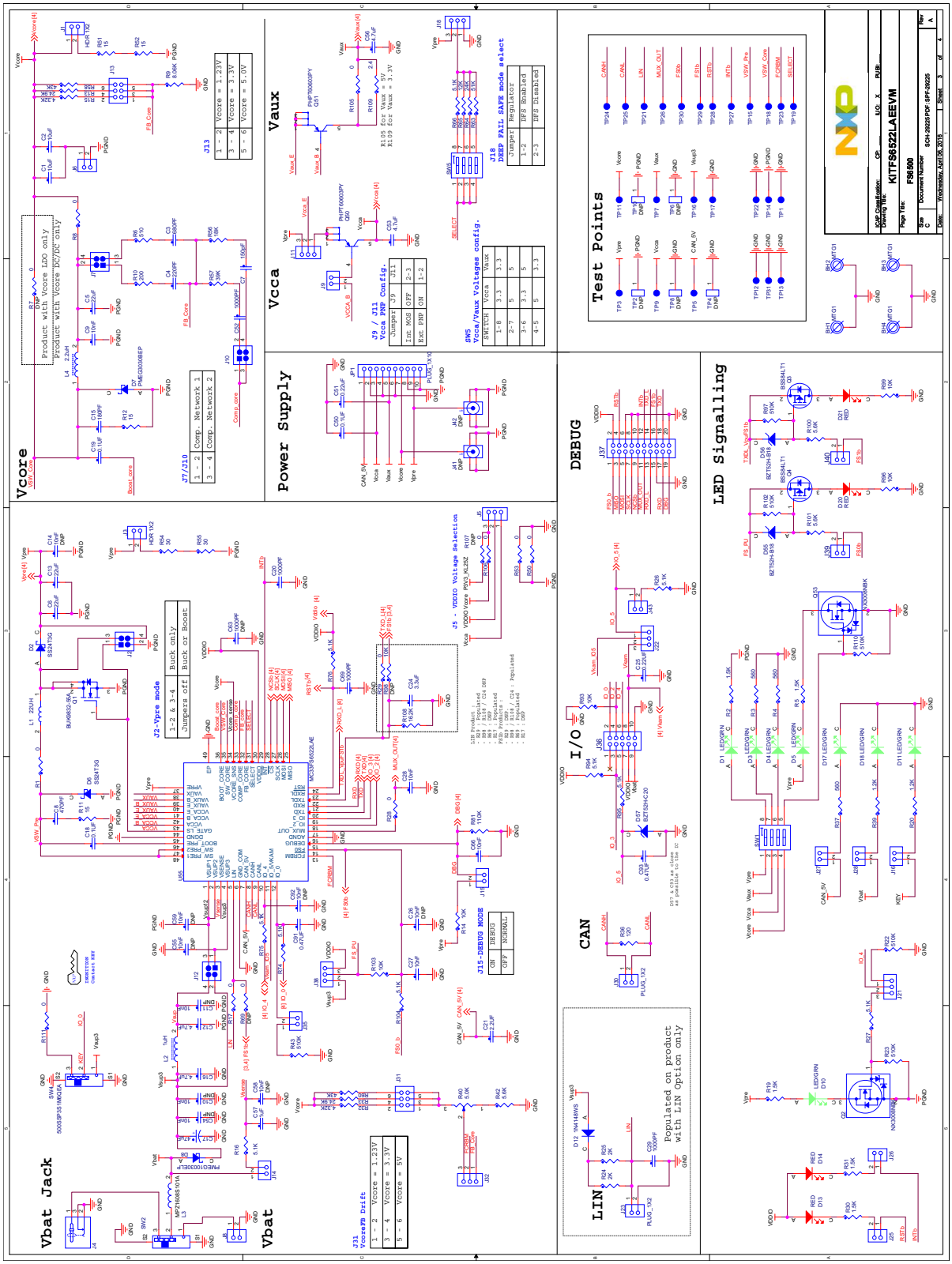

Figure 23. Evaluation board schematic

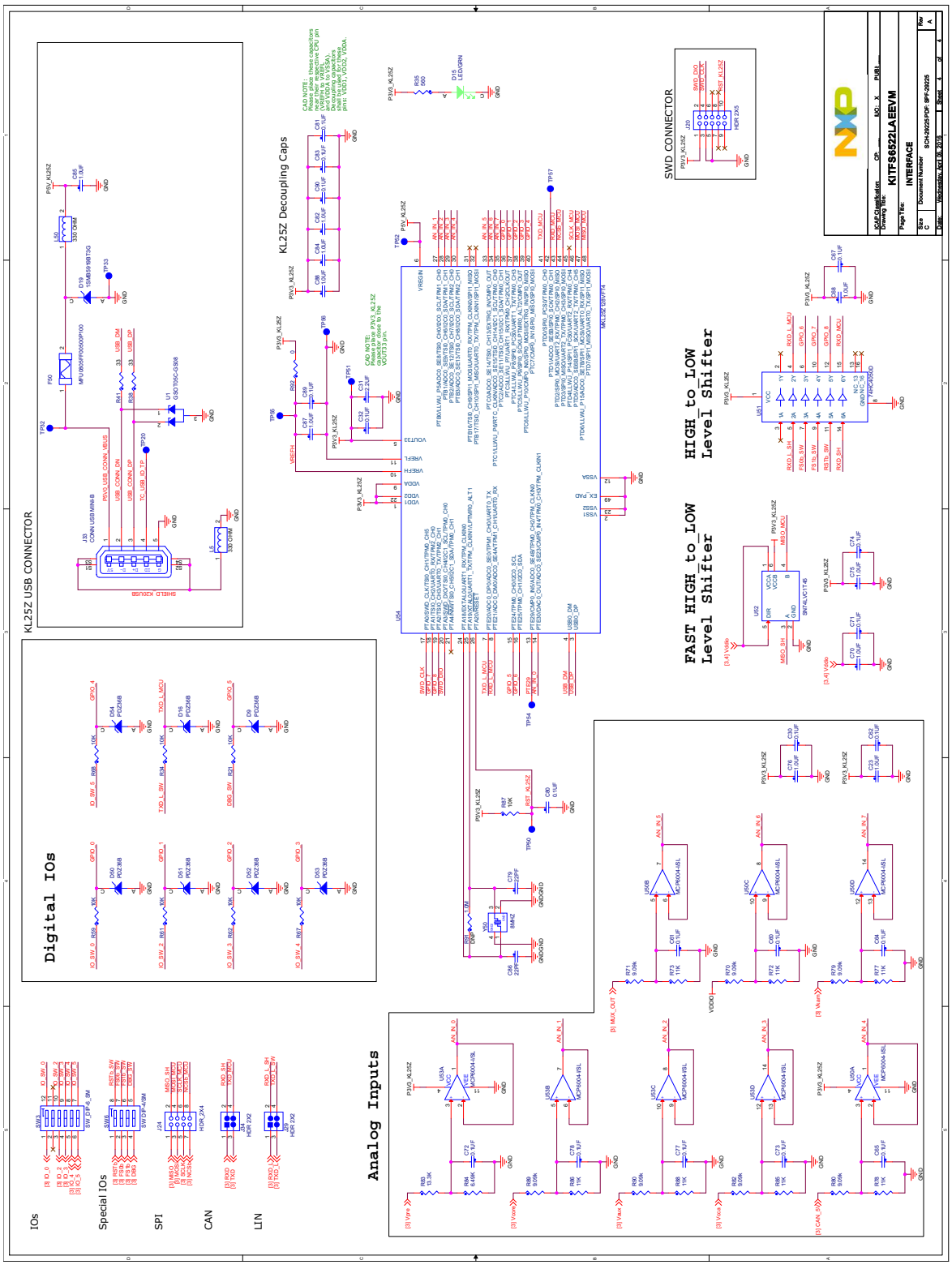

Figure 24. Evaluation board schematic

7 Board layout

7.1 Assembly layer top

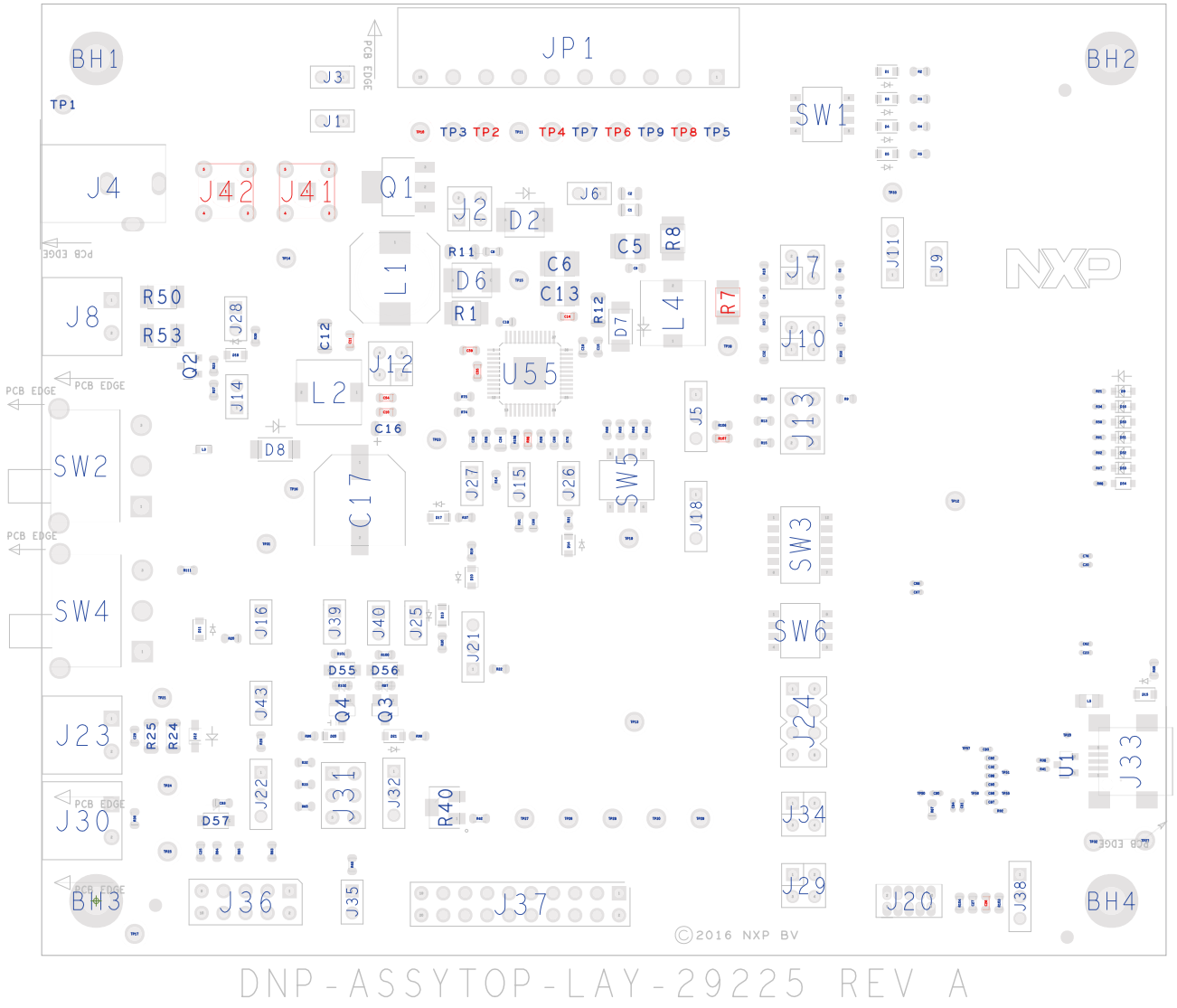

Figure 25. Assembly layer top

7.2 Assembly layer bottom

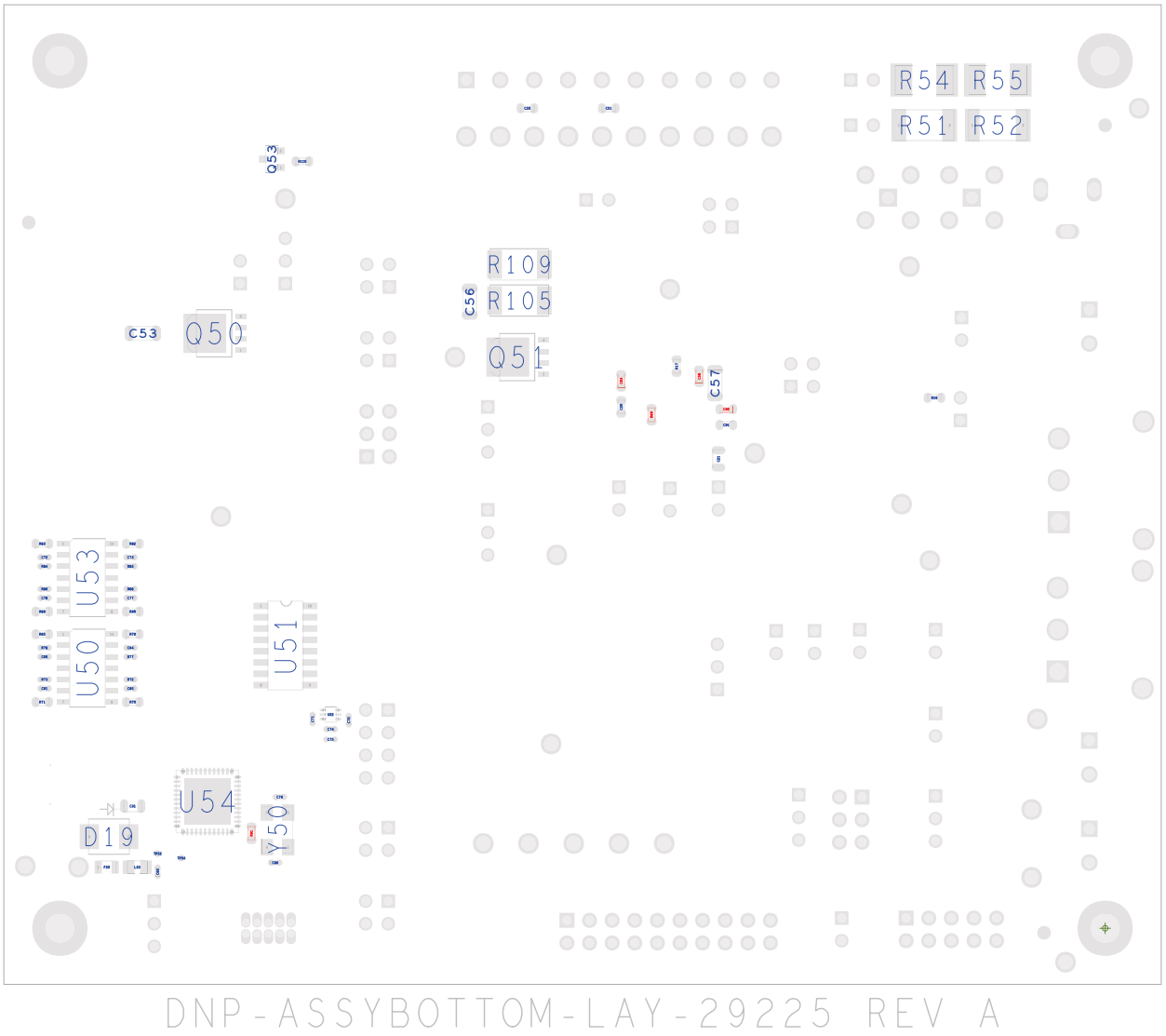

Figure 26. Assembly layer bottom

8 Board bill of materials

Bill of materials for KITFS6522LAEEVM, KITFS6523CAEEVM, and KITFS4503CAEEVM are available in the download section of the Tool Summary page at the following URLs: www.nxp.com/KITFS6522LAEEVM, www.nxp.com/KITFS6523CAEEVM, or www.nxp.com/KITFS4503CAEEVM.

9 Accessory item bill of materials

Table 25. Accessory Bill of Materials [3]

Item	Qty	Part number	Description
1	1	10U2-03103BK	USB cable A plug to USB mini B
2	1	1803659	10 ways PCB screw connector
3	3	1803578	2 ways PCB screw connector

Notes

3. NXP does not assume liability, endorse, or warrant components from external manufacturers are referenced in circuit drawings or tables. While NXP offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

10 References

Table 26. References

NXP.com Support Pages	Description	URL
FS6500-FS4500	Data sheet	TBD
AN4661	Designing the VCORE Compensation Network	http://www.nxp.com/AN4661.pdf
AN4388	Quad Flat Package (QFP)	http://www.nxp.com/files/AN4388.pdf
Power dissipation tool (Excel file)		TBD
VCORE compensation network simulation board (CNC)		upon demand
Non ISO pulses report		upon demand
FMEDA	FS6500/FS4500 FMEDA	upon demand
FS4500-FS6500SMUG	FS4500-FS6500SMUG safety manual – User Guide	TBD
KITFS6522LAEEVM, KITFS6523CAEEVM, KITFS4503CAEEVM	Tool Summary Page	www.nxp.com/KITFS6522LAEEVM www.nxp.com/KITFS6523CAEEVM www.nxp.com/KITFS4503CAEEVM
FS6500 Product summary page		http://www.nxp.com/FS6500
FS4500 Product summary page		http://www.nxp.com/FS4500
Analog home page		http://www.nxp.com/analog

10.1 Support

Visit www.nxp.com/support for a list of phone numbers within your region.

10.2 Warranty

Visit www.nxp.com/warranty to submit a request for tool warranty.

11 Revision history

Revision	Date	Description of Changes
1.0	5/2016	• Initial release

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Document Number: KTFS4500-FS6500UG
Rev. 1.0
5/2016