Frequently Asked Questions

Product Name: System Basis Chips (SBCs) **Date:** September 2014
Application: Automotive ECUs **Datasheet:** TLE9263-3QX rev. 1.1
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Mid-Range SBC

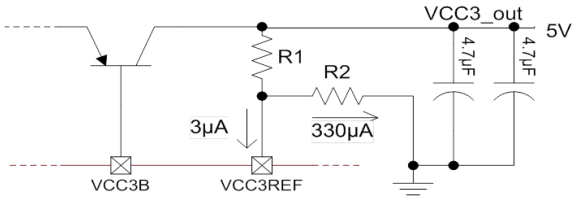
Question 1: Chapter 3	What's the difference between **n.c.** pins and **N.U.** pins?
Answer:	**n.c.** pins means "not connected pins". They are high impedance pins and internally not bonded to the chip. It is recommended to connect to GND to ensure better thermal resistance. **N.U.** pins means not used pin. These pins are electrically connected to the silicon chip via bonding wires; therefore they should be left as electrically open on the PCB, i.e. not connected to any potential on the board. In case N.U. pins are connected on the board an open bridge has to be foreseen to avoid external disturbances.
Question 2: Chapter 3.3	How shall I connect the unused pins?

Answer:	Please refer to the following recommendations:
	• WK1/2/3: connect to GND and disable WK inputs via SPI
	• HSx: leave open
	• LIN, CAN: leave all pins open
	• RO, FOx: leave open
	• INT: leave open
	• TEST:
	  ○ To activate SBC Development Mode, connect to GND during power-up operation. The connection can be removed after power-up
	  ○ For normal operations, leave open
	• VCAN: connect to VCC1
	• VCC2: leave open and keep disabled
	VCC3: Do not enable the VCC3 via SPI if not used because this will lead to an increased current consumption.
	• VCC3SH: Connect to VS or leave open
	• VCC3B, VCC3REF: leave open

Question 3: Chapter 4.1.4	What does it means "VCC2 is short-to-battery protected"?
Answer:	Most discrete regulators have the maximum rating of the 5V output pin at around 5.5V (or slightly higher). In this case, if the 5V output pin is shorted to battery, the device will be damaged. The VCC2 output pin of Mid-Range SBC can withstand a short up to 28V, and up to 40V for load dump, as described in the datasheet. Therefore this SBC will not be damaged even if the output pin is shorted to battery.
Question 4: Chapter 4.4	What is the current consumption adder during cyclic sense in SBC Stop or Sleep Mode?
Answer:	The current consumption adder for cyclic sense (CS) with one high-side switch in SBC Stop Mode can be calculated using following equation: IStop,CS = 18µA + (525µA *ton-time/Tperiod). The same applies for SBC Sleep Mode. A typ. 75µA / max 125µA (Tj= 85°C) adder applies for every additionally activated HSx switch.

Question 5: **Chapter 4.4**	How can we calculate the High-Side Switch (HSS) current consumptions for every additional activated HSx switch in SBC Stop or Sleep Mode?
Answer:	When one of the four HSS is already turned on during SBC Stop Mode, the additional current consumption is typ. 575µA / max 700µA (Tj = 85°C). A typ. 75µA / max 125µA (Tj = 85°C) adder applies for every additionally activated HSx switch in SBC Stop Mode. The current consumption for cyclic sense is reduced by the duty cycle of the configured period and on-time.
Question 6: **Chapter 4.4**	Is “the VCC2 low power mode current consumption in SBC stop mode” the same to the VCC2 current consumption in SBC sleep mode?
Answer:	The VCC2 current is the same for SBC Stop and for SBC Sleep Mode. Please refer to (P_4.4.19) and (P_4.4.20). Note: You do not have to enable VCC2 for SBC Stop or SBC Sleep Mode for the CAN wake capable mode.
Question 7: **Chapter 4.4**	What is the contribution of the watchdog operation to the SBC current consumption during SBC stop mode?
Answer:	Additional 20µA typ. is required at 25°C. For more details, please refer to the datasheet, (P_4.4.30) and (P_4.4.31).
Question 8: **Chapter 4.4**	What is the HSS current consumption value for 1 * HSx in SBC Stop Mode without cyclic sense?
Answer:	The difference on the HS current consumptions with and without cyclic sense is that the current consumption in cyclic sense is reduced by the duty cycle (ton/Tperiod). See also the footnotes of the datasheet parameters (P_4.4.23), (P_4.4.27), (P_4.4.33) and (P_4.4.34).
Question 9: **Chapter 5.1**	Is the transition from SBC Init Mode to SBC Normal Mode automatic, or do we have to send a SPI command?
Answer:	The transition from SBC Init Mode to SBC Normal Mode is NOT automatic, i.e. a SPI command has to be sent by the microcontroller. However, any SPI command will bring the SBC from SBC Init Mode to SBC Normal Mode. A recommendation would be a watchdog trigger command to start with the proper watchdog timing. If no SPI command is sent then a watchdog trigger failure will occur after the long open window (typ. 200ms).
Question 10: **Chapter 5.1.1**	What is the watchdog mode after power-up? Window watchdog or time-out/standard watchdog?
Answer:	The default watchdog mode is time-out watchdog.
Question 11: **Chapter 5.1.1.2**	Do you have some recommendation for the sequence of initial settings?
Answer:	After the Power-On Reset (POR), the SBC is in SBC Init Mode. Then following actions are recommended: • Watchdog trigger and watchdog (WD) settings • Configure VCC3 load sharing if it will be used • Clear the POR bit for proper diagnosis • All other initializations of the SBC peripherals (CAN, LIN, HSx, WKx, etc.)

	The actual sequence and timing of the commands depends on the application and other boundary conditions (e.g. microcontroller, drivers, functional safety requirements, etc.).
Question 12: **Chapter 5.1.4**	SBC Stop Mode will be used for our application in low-power mode of the ECU. There is a concern to accidentally enter SBC Sleep Mode (VCC1 OFF) by single point failure. Is there any suggestion to reduce this risk?
Answer:	One suggestion is to set a wake-flag as “1” and leave it intentionally (just after SBC initialization) because SBC Sleep Mode access is prevented when wake-flags are still set. One possibility would be following configuration after power-up: • Create an internal wake-event (TIMER_WU) from an unused timer (Timer 1 or Timer 2) using cyclic wake • Keep this bit set (do not clear in the register). Only then, set other wake sources before entering SBC Stop Mode. • In case other wake sources are set and the register needs to be cleared then the procedure should be repeated. As explained on Chapter 5.1.4, in order to enter SBC Sleep Mode successfully, all wake source signalization flags from WK_STAT_1 and WK_STAT_2 need to be cleared. A failure to do so will result in an immediate wake-up from SBC Sleep Mode by going via SBC Restart to Normal Mode.
Question 13: **Chapter 8**	What is the current capability and the current limitation of VCC3?
Answer:	Current capability of VCC3: • VCC3 is designed to drive PNP transistors with a base current from VCC3B of up to 80mA. Depending on the current amplification of the respective PNP the collector current could go up to 400mA. For power dissipation and thermal protection reasons, also multiple PNPs can be driven in parallel. • The power dissipation within the PNP is also determining the current capability and needs to be managed to avoid a thermal damage. With 400mA and VS = 16V the power dissipation will be 4.4W for a 5V configuration, which can only be managed for short periods because the heat cannot be dissipated from the PCB itself. Assuming an Rth of 40K/W and an ambient temperature of 85°C, the junction temperature of the PNP would be already ~300°C, which is too high for the PNP on a steady state level. In addition the overall SBC power dissipation also needs to be considered Current limitation of VCC3: • In stand-alone configuration, the current limitation for the PNP is determined by the shunt resistor between VS and VCC3SH. • In load-sharing configuration, the current limitation is only indirect by the current limitation of VCC1.
Question 14: **Chapter 8**	Is it possible to set VCC1=3.3V, VCC2=5V and VCC3=5V?
Answer:	Yes, it is possible to configure VCC3 to a different voltage higher than VCC1 (e.g. VCC3 at 5V while VCC1 is set to 5V). An external resistor divider must be used, see below. The same mechanism applies when VCC1 is 5V and VCC3 should be higher than 5V.



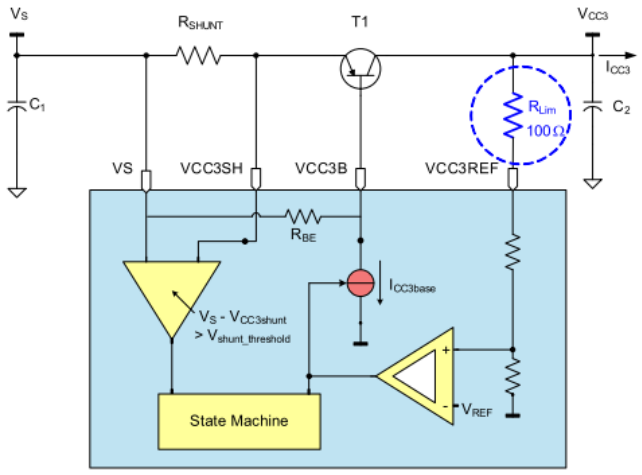
Input current on Vcc3_ref. Typical value form BE@ambient results

The resulting 330uA is an optimum choice between circuit robustness and current consumption (see also next page)

$$R1 = \frac{VCC3_{out} - VCC3_{ref}}{I_{R2} + I_{VCC3\_ref}} = \frac{5 - 3.3}{330E^{-6} + 3E^{-6}} = 5.11k\Omega$$

$$R2 = \frac{VCC3_{ref}}{I_{R2}} = \frac{3.3}{330 \cdot E^{-6}} = 10K\Omega$$

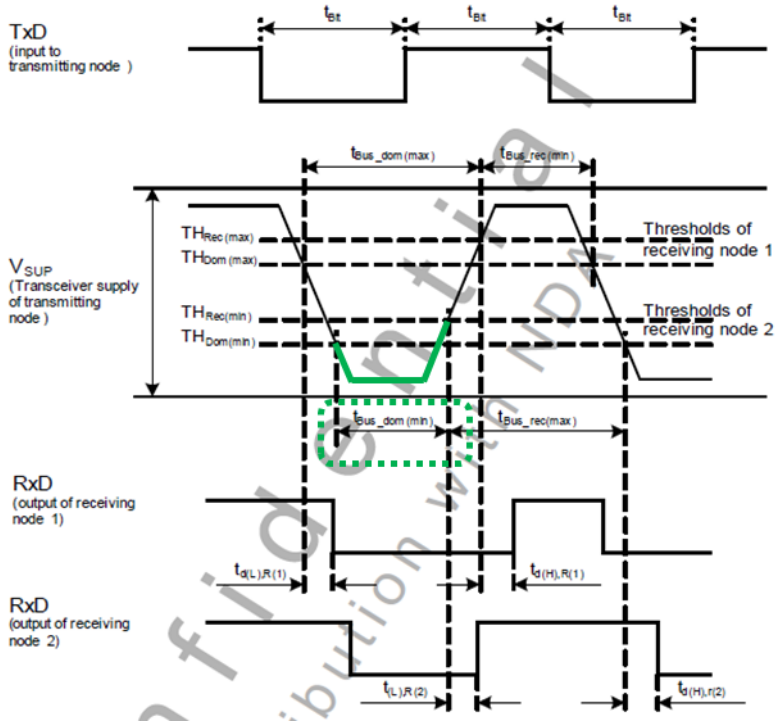
Question 15: **Chapter 8.2.1**	1. What is the function of R_{Lim}? 2. Does it affect Vcc3 output accuracy a lot?
Answer:	1. R_{Lim} will increase the robustness of the VCC3 regulator in case of short circuit to GND in case it is used off-board, e.g. for sensor supply. R_{Lim} is not needed when VCC3 stays on board. It is also not needed if it is ensured that the max ratings are not violated. However, negative pulses could be generated in case of a short circuit to GND at the end of a longer cable (wire harness). This negative pulse would violate the max rating of the VCC3REF pin and could cause disturbances, e.g. resets. R_{Lim} is a simple solution to protect the pin in case of off-board usage. 2. Regarding the VCC3 output voltage accuracy, a 100Ω resistor would add only 1mV offset taking account a worst-case VCC3REF input current of 10µA (P_8.6.2).
Question 16: **Chapter 8.2.2**	1. When we use VCC3 independently, it is possible to turn on and off VCC3? 2. Is it possible to turn ON and OFF VCC3 once configured for load sharing?
Answer:	1. In stand-alone configuration VCC3 can be turned on and off when needed. Once configured then the load sharing cannot be chosen anymore unless the SBC is powered down. 2. When load sharing is chosen (VCC3_LS_= 1), VCC3 can't be turned off by using the VCC3_ON register. Because VCC3_ON register setting will be ignored. VCC3 status will be always synchronized with VCC1 during load sharing. By default VCC3 will be disabled in SBC Stop Mode and for VS < VS_UV. If needed VCC3 can also stay activated in Stop Mode by setting the bit VCC3_LS_ STP_ON (with a slightly increased quiescent current) and below VS_UV by setting the bit VCC3_VS_ UV_OFF



	Note: Setting the bit VCC3_ON before setting the bit VCC3_LS will prevent the load sharing configuration to be activated
Question 17: **Chapter 8.3**	Would you provide the information on the acceptable ESR values for the VCC3 output capacitor, as reference?
Answer:	It is recommended to use a ceramic capacitor with 10mΩ – 150mΩ. Below table is the recommendation for the external devices of VCC3. **Table 12 Bill of Materials for the V_{CC3} Function with and without load sharing configuration** **Device** / **Vendor** / **Reference / Value** C2 / Murata / 10 µF/10 V GCM31CR71AA106K RSHUNT / - / 1 Ω (with LS) / 470 mΩ (without LS) T1 / Infineon / BCP52-16
Question 18: **Chapter 8.4**	Would you provide the information on the load sharing ratio in case of the Mid-Range SBC when the load sharing is used?
Answer:	The load sharing ratio can be selected via the shunt resistor (between VS and VCC3SH) by using the equation from the datasheet. A shunt resistor of 1Ω would result in a load sharing ratio of 1:1 (VCC3:VCC1).
Question 19: **Chapter 8.4**	1. How is the load-sharing function working? 2. How can I calculate the appropriate RSHUNT value?
Answer:	1. VCC1 circuit work as the main feedback loop to control the voltage (voltage controlled voltage source. The shunt resistor determines the load sharing ratio between VCC1 and VCC3. In other words, the VCC3 circuit work as the additional current supply (current controlled current source) and it is similar to a current mirror function. 2. Based on above (i), following calculation approach and method is proposed to determine the proper RSHUNT value: (i) Take the total current needed and determine the Icc1 value (e.g. based on your power dissipation estimation) (ii) Calculate the Icc3 value based on Step 1. (iii) RSHUNT will be calculated by using following equation: $$R_{SHUNT} = \frac{I_{CC1} \cdot 110\ \Omega / 105 - 15\ mV}{I_{CC3}}$$
Question 20: **Chapter 8.6**	Would you provide the information on the output voltage accuracy when operating in load sharing?
Answer:	It is ±2% from the nominal value (5V or 3,3V) in SBC Normal Mode and ±4% in SBC Stop Mode (P_8.6.13).
Question 21: **Chapter 8.6.6**	Why does the datasheet state “up to 400mA with 470mΩ shunt resistor”? Regarding the 400mA, does it come from Vshunt_threshold 180mV min?
Answer:	Yes, it is based on the min shunt threshold voltage of 180mV. When using a 470mΩ shunt then the VCC3 current is ~382mA. It is also a practical achievable max. value. In theory the VCC3 current is limited by the max. base current and the power dissipation within the SBC and the PNP.
Question 22: **Chapter 10.1**	What is the internal link between the CAN transceiver and VCC2?

Answer:	The CAN transceiver and VCC2 are independent. CAN is supplied by the dedicated VCAN supply input pin and any 5V supply could be used, e.g. for the 5V variant from VCC1, VCC2, VCC3 or an external voltage regulator.
Question 23: **Chapter 10.1**	Can we disable VCC2 in SBC Stop Mode while keeping the CAN transceiver in wake capable mode?
Answer:	An internal supply derived from VS is active during CAN wake capable to supply the wake receiver. Therefore, VCC2 must not be active during SBC Stop or Sleep, i.e. it can be switched off during CAN wake capable mode.
Question 24: **Chapter 10.2.4**	How can the microcontroller detect a wake-up on CAN in SBC Stop Mode?
Answer:	There are two signalizations how a CAN wake-up is detected: 1. The INT pin is pulled low for t_{INT}. 2. RXDCAN is pulled low until the CAN mode is changed via SPI. The microcontroller can use either signal as wake-up detection. Please refer to the datasheet Chapter 10.2.4 “CAN wake Capable Mode” for the details. The same applies for a wake-up on LIN but with a signalization on RXDLIN
Question 25: **Chapter 11.1**	Which pin is the power supply for the integrated LIN module?
Answer:	It is supplied via VSHS pin. Please refer to the block diagram in Chapter 11.1.
Question 26: **Chapter 11.3**	What is the LIN dominant voltage level?
Answer:	TLE926x specifications are based on LIN2.2A standard. Therefore it is NOT described as voltage level but it is described as the duty cycle.

Duty Cycle D2 (for worst case at 20 kbit/s) LIN2.1 Normal Slope	D2	–	–	0.581		[4)]THRec(min.) = 0.422 × V_S; THDom(min.) = 0.284 × V_S; VS = 7.6 … 18 V; tbit = 50 µs; D2 = tbus_rec(max)/2 tbit; LIN2.1 Param 28	P_11.3.32
Duty Cycle D4 (for worst case at 10.4 kbit/s) SAE J2602 Low Slope	D4	–	–	0.590		[4)]THRec(min.) = 0.389 × V_S; THDom(min.) = 0.251 × V_S; VS = 7.6 … 18 V; tbit = 96 µs; D4 = tbus_rec(max)/2 tbit; LIN2.1 Param 30	P_11.3.34

	
Question 27: **Chapter 12.3**	1. What max. voltage can be applied to the WKx pins and how big is the current flowing into the pin? 2. Must the current be limited if a pin voltage of >40V is applied?
Answer:	1. Even if the voltage on a WKx input exceed VS+0.3V, the current remains within the limits specified in (P_12.3.5). i.e. no additional current flowing into the pin as long as the absolute max rating of 40V are observed (P_4.1.6). 2. In general, voltages of >40V are not allowed because of the break through voltage of the ESD diode. ESD diodes can withstand a high (>1mA) current only for a very short period. When the pin leaves the control unit, then the protection of ESD / ISO pulses with an external capacitor of 10nF and a 1 k series resistor to limit the current into the pin are necessary (as in the diagram shown application example). *Note: The 500µA maximum rating of (P_4.1.13 and (P_4.1.14) apply for the case when the HV measurement function between WK1 and WK2 is enabled (Chapter 12.2.2) and the current between the two pins must be limited.*
Question 28: **Chapter 14.1**	1. Is there internal pull-up resistor on FO3 /TEST pin? 2. Do we need to add an external pull-up for the productive application?
Answer:	1. Yes, there is an internal pull-up resistor (R_{TEST}) implemented in the FO3/TEST pin, which is active only during the power-up phase of the SBC. It is used to detect if the SBC Development Mode should be activated or not. The SBC Software Development Mode is reached automatically if the FO3/TEST pin is set and kept LOW during SBC Init Mode. The voltage level monitoring is started as soon as VS > $V_{POR,r}$. The SBC Development Mode is configured and maintained if SBC Init Mode is left by sending any SPI command while FO3/TEST is LOW. The Software Development Mode is NOT configured if the FO3/TEST level will be HIGH for longer than t_{TEST} during the monitoring period. 2. After the power-up phase the internal pull-up resistor will be disabled and the pin has by default an open drain output. The external pull-up may be required depending on the used functionality. *Note: FO2 and FO3/TEST can also be reconfigured after power-up as a low-side, high-side or wake-input functionality. The configuration is performed in the register GPIO_CTRL.*
Question 29:	Do VCC1, VCC2 and VCC3 have an under-voltage detection feature?

Chapter 15.6	
Answer:	• VCC1: a pre-warning detection (P_15.6.1), a configurable under-voltage reset (P_15.6.1), a short circuit detection (Chapter 15.7), and an over voltage detection (P_15.6.2) are implemented • VCC2: and under-voltage detection is implemented (P_15.8). A SPI bit will be set but no reset is generated • VCC3: and under-voltage detection is implemented (P_15.7) depending on the configured voltage. A SPI bit will be set but no reset is generated Please refer to the datasheet Section 15.6 – 15.8 for further information
Question 230: **Chapter 15.9.1**	What happens to VCC1 when VCC2 enters thermal shutdown and is turned off?
Answer:	There are independent temperature's sensors on each voltage regulator and also for the other power stages. Therefore VCC1 will continue to operate independently from the VCC2 condition as long as the temperature is below the thermal shutdown threshold for VCC1..
Question 31: **Chapter 15.10**	Would you provide the information on the VS min voltage to release reset (RO is L to H) surely during VS ramp-up?
Answer:	It is 5.45V based on following calculation. (Vrt1,f) + (Vrt, hys) + (Vcc1, d2) = 4.75Vmax + 0.2Vmax + 0.5Vmax = 5.45Vmax
Question 32: **Chapter 15.10.18**	How long is the reset pulse width for the WD time-out?
Answer:	The so called reset delay time is typ. 2ms typ. In case of a watchdog trigger reset the RO pin is pulled low for this time. For other events, e.g. under voltage reset, the RO is pulled down for at least the 2ms but as long as VCC1 is below the reset threshold.
Question 33: **Chapter 16**	Are the SPI registers exactly the same among TLE926x(-3)QX(V33) family? What happen in case of programming a register associated to a non-available function?
Answer:	All members of the MR-SBC family are fully software compatible between each other. The LIN2 (in the TLE9262, TLE9261 and TLE9260 variants), the LIN1 (in the TLE9261 and TLE9260 variants) and VCC3 (in TLE9260 variant) are disabled via internal hardwiring. The respective control bits behave like other reserved bits, i.e. they read as '0' and are also tied to '0'. No control or configuration is possible. No SPI_FAIL bit is set.
Question 34: **Chapter 16.2**	A reserved bit in configuration register has to be written as 0, will it trigger a raise of SPI_FAIL flag if programmed as 1?
Answer:	Nothing will happen, when trying to write a '1' to a reserved bit because there is no real digital registers for reserved bits, The read back value is always '0' for reserved bits. The SPI_FAIL flag will not be set.. *Note: For the details of the invalid SPI Commands leading to SPI_FAIL, please refer to the datasheet Chapter 16.2.*
Question 35: **Chapter 16.7**	Are there any internal pull-ups or pull-downs at SPI pins?
Answer:	• CSN pin: there is a pull-up resistor (40kΩ typ.) • SDI and CLK pin: each pin has a pull down resistor (40kΩ typ.). • SDO pin: there is no pull-up or pull-down resistor. It is usually high impedance (HiZ). Please refer to (P_16.7.6) and (P_16.7.7).

Frequently Asked Questions

Question 36: **Chapter 16.7.23**	What is the transition time for SBC mode changes triggered via SPI?
Answer:	The mode transition time is max. 6µs. Please refer to (P_16.7.23).
Question 37: **Chapter 3**	Which pins have which internal structures?

Please see below table for each pin:

Pin	Name	Pin Configuration / Property	Pin	Name	Pin Configuration / Property
1	GND		25	TXDLIN2	40k pull-up to VCC1
2	n.c.		26	RXDLIN2	Push-pull output stage
3	VCC3REF	Active pull-down (~2.5mA) to GND when VCC3 = OFF	27	CLK	40k pull-down to GND
4	VCC3B	150k pull-up to VS	28	SDI	40k pull-down to GND
5	VCC3SH	5k pull-up to VS	29	SDO	Push-pull output stage
6	n.c.		30	CSN	40k pull-up to VCC1
7	n.c.		31	INT	250k pull-down to GND during reset delay time and Init, push-pull output stage afterwards
8	HS1	High-side switch	32	RO	20k pull-up to VCC1, Open-drain output stage
9	HS2	High-side switch	33	TXDLIN1	40k pull-up to VCC1
10	HS3	High-side switch	34	RXDLIN1	Push-pull output stage
11	HS4	High-side switch	35	TXDCAN	40k pull-up to VCC1
12	n.c.		36	RXDCAN	Push-pull output stage
13	VSHS		37	VCAN	
14	VS		38	GND	
15	VS		39	CANL	Low-side switch
16	n.c.		40	CANH	High-side switch
17	VCC1	Active pull-down to GND when VCC1 = off (~1mA)	41	n.c.	
18	VCC2	Active pull-down to GND when VCC2 = off (~1mA)	42	LIN1	Low-side switch, internal 30k pull-up
19	n.c.		43	GND	
20	GND		44	LIN2	Low-side switch, internal 30k pull-up
21	FO1	Low-side switch	45	n.c.	
22	WK1	High-ohmic after POR, configurable 10uA pull-up/-down to internal 5V/GND	46	n.c.	
23	WK2	High-ohmic after POR, configurable 10uA pull-up/-down to internal 5V/GND	47	FO2	Default is low-side switch, Configurable to high-side switch or to input with 5k pull-up to internal 5V
24	WK3	High-ohmic after POR, configurable 10uA pull-up/-down to internal 5V/GND	48	FO3_ TEST	5k pull-up to internal 5V during POR and Init, Configurable to low-side or high-side switch or to input with 5k pull-up to internal 5V