The ABCs of Interleaved ADCs

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INTRODUCTION

Across many segments of the market today, interleaving ADCs offers several advantages in many applications. In communications infrastructure there is constantly a push for higher sample rate ADCs to allow for multiband, multicarrier radios, in addition to wider bandwidth requirements for linearization techniques like DPD (digital predistortion). In military and aerospace, higher sample rate ADCs allow for multipurpose systems that can be used for communications, electronic surveillance, and radar just to name a few. In yet another segment, industrial instrumentation, the need is always increasing for higher sample rate ADCs so that higher speed signals can be measured adequately and accurately.

It is first important to understand exactly what interleaving ADCs is about. To understand interleaving, it is good to look at what is actually happening and how it is being implemented. With a basic understanding, the benefits of interleaving can then be discussed. Of course, as many know, there is no such thing as a free lunch, so the challenges of interleaving need to be evaluated and assessed.

ABOUT INTERLEAVING

When ADCs are interleaved, two or more ADCs with a defined clocking relationship are used to simultaneously sample an input signal and produce a combined output signal that results in a sampling bandwidth at some multiple of the individual ADCs. Utilizing m number of ADCs allows for the effective sample rate to be increased by a factor of m. For the sake of simplicity and ease of understanding, we'll focus on the case of two ADCs. In this case, if two ADCs with each having a sample rate of fS are interleaved, the resultant sample rate is simply 2fS. These two ADCs must have a clock phase relationship for the interleaving to work properly. The clock phase relationship is governed by Equation 1, where n is the specific ADC and m is the total number of ADCs.

$$\emptyset_n = 2\pi\left(\frac{n-1}{m}\right) \tag{1}$$

As an example, two ADCs each, with a sample rate of 100 MSPS, are interleaved to achieve a sample rate of 200 MSPS. In this case, Equation 1 can be used to derive the clock phase relationship of the two ADCs and is given by Equation 2 and Equation 3.

$$\emptyset_1 = 2\pi\left(\frac{1-1}{2}\right) = 0 \; radians = 0° \tag{2}$$

$$\emptyset_2 = 2\pi\left(\frac{2-1}{2}\right) = \pi \; radians = 180° \tag{3}$$

Now that the clock phase relationship is known, the construction of samples can be examined. Figure 1 gives a visual representation of the clock phase relationship and the sample construction of two 100 MSPS interleaved ADCs. Notice the 180° clock phase relationship and how the samples are interleaved. The input waveform is alternatively sampled by the two ADCs. In this case, the interleaving is implemented by using a 200 MHz clock input that is divided by a factor of two and the required phases of the clock to each ADC.
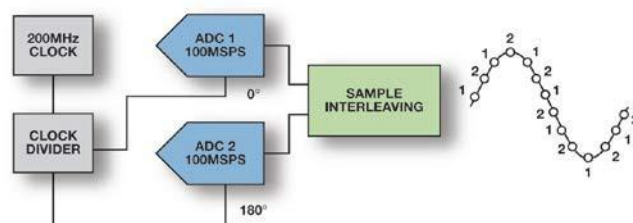

Figure 1. Two Interleaved 100 MSPS ADCs—Basic Diagram

Another representation of this concept is illustrated in Figure 2. By interleaving these two 100 MSPS ADCs, the sample rate is increased to 200 MSPS. This extends each Nyquist zone from 50 MHz to 100 MHz, doubling the available bandwidth in which to operate. The increased operational bandwidth brings many advantages to applications across many market segments. Radio systems can increase the number of supported bands; radar systems can improve spatial resolution, and measurement equipment can achieve greater analog input bandwidth.
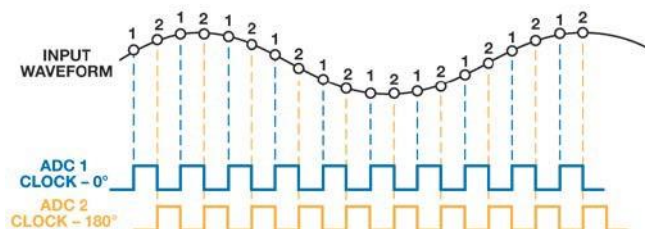

Figure 2. Two Interleaved 100 MSPS ADCs—Clocking and Samples

BENEFITS OF INTERLEAVING

The benefits of interleaving span across multiple segments of the market. The most desired benefit of interleaving is the increased bandwidth made possible by the wider Nyquist zone of the interleaved ADCs. Once again, taking the example of two 100 MSPS ADCs interleaved to create a sample rate of 200 MSPS, Figure 3 gives a representation of the much wider bandwidth allowed by interleaving the two ADCs. This creates advantages for many different applications. As cellular standards increase channel bandwidth and the number of operating bands, there are increased demands on the available bandwidth in the ADC. In addition, in military applications, the requirements for better spatial recognition, as well as increased channel bandwidths in backend communications require higher bandwidths from the ADC. Due to the increased demands for bandwidth in these areas, there is a need created to measure these signals accurately. Therefore, measurement equipment has increased needs for higher bandwidths in order to properly acquire and measure these signals that have higher bandwidth. The system requirements in many designs inherently stay ahead of commercial ADC technology. Interleaving allows for some of this gap to be closed.
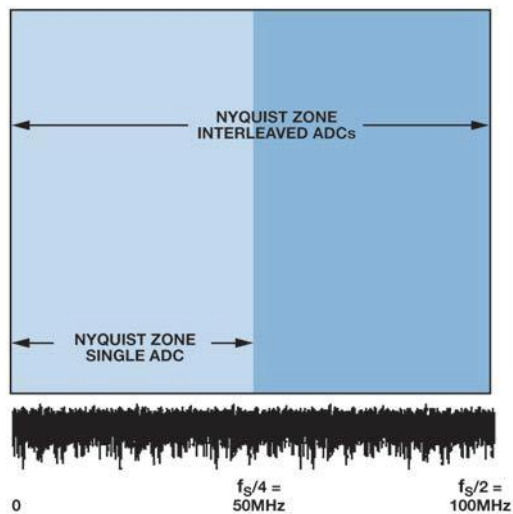

Figure 3. Two Interleaved ADCs—Nyquist Zone

The increased sample rate provides more bandwidth for these applications but also allows for easier frequency planning and reduction in the complexity and cost of the anti-aliasing filter that is typically used at the ADC inputs. With all these great benefits, one has to wonder what the price is to pay. As with most things, there is no such thing as a free lunch. Interleaved ADCs offer increased bandwidth and other nice benefits, but there are some challenges that arise when dealing with interleaved ADCs.

CHALLENGES WITH INTERLEAVING

There are some challenges and things to look out for when interleaving ADCs. There are spurs that appear in the output spectrum that result from the imperfections associated with interleaving ADCs. These imperfections are basically mismatches between the two ADCs that are being interleaved. There are four basic mismatches that result in spurs in the output spectrum. These are offset mismatch, gain mismatch, timing mismatch, and bandwidth mismatch.

The easiest of these to understand is probably the offset mismatch between the two ADCs. Each ADC will have an associated dc offset value. When the two ADCs are interleaved and samples are acquired alternatively back and forth between the two ADCs, the dc offset of each successive sample is changing. Figure 4 gives an example of how each ADC has its own dc offset and how the interleaved output will effectively switch back and forth between these two dc offset values. The output switches between these offset values at a rate of $f_S/2$ which will result in a spur in the output spectrum located at $f_S/2$. Since the mismatch itself does not have a frequency component and is only at dc, the frequency of the spur that appears in the output spectrum only depends on the sampling frequency and will always appear at a frequency of $f_S/2$. The magnitude of the spur is dependent upon the magnitude of the offset mismatch between the ADCs. The greater the mismatch, the larger the spur will be. In order to minimize the spur caused by the offset mismatch, it is not necessary to completely null the dc offset in each ADC. Doing this would filter out any DC content in the signal and would not work for systems using a ZIF (zero IF) architecture where the signal content is real and complex and includes data at DC. Instead, a more appropriate technique would be to match the offset of one of the ADCs to the other ADC. The offset of one ADC is chosen as the reference, and the offset of the other ADC is set to match that value as closely as possible. The better matched the offset values are, the lower the resulting spur is at $f_S/2$.

The second mismatch to look at when interleaving is the gain mismatch between the ADCs. Figure 5 gives a representation of the gain mismatch between two interleaved converters. In this case, there is a frequency component to the mismatch. In order to observe this mismatch, there has to be a signal applied to the ADCs. In the case of the offset mismatch, no signal is necessary to see the inherent dc offset of the two ADCs. In the case of the gain mismatch, there is no way to see the gain mismatch unless a signal is present and the gain mismatch can be measured. The gain mismatch will result in a spur in the output spectrum that is related to the input frequency, as well as the sampling rate, and will appear at $f_S/2 \pm f_{IN}$. In order to minimize the spur caused by

the gain mismatch, a similar strategy as what is used for the offset mismatch is employed. The gain of one of the ADCs is chosen as the reference, and the gain of the other ADC is set to match that gain value as closely as possible. The better the gain values of each ADC are matched to each other, the less the resulting spur will be in the output spectrum.

Next, we must examine the timing mismatch between the two ADCs. The timing mismatch has two components, group delay in the analog section of the ADC and clock skew. The analog circuitry within the ADC has an associated group delay and the value can be different between the two ADCs. In addition, there is clock skew that has an aperture uncertainty component in each of the ADCs and has a component related to the accuracy of the clock phases that are input to each converter. Figure 6 gives a visual representation of the mechanism and effects of the timing mismatches in the ADCs. Similar to the gain mismatch spur, the timing mismatch spur is also a function of the input frequency and the sample rate and appears at $f_S/2 \pm f_{IN}$. In order to minimize the resulting spur, the group delay through the analog section of each converter needs to be properly matched with good circuit design techniques. In addition, the clock path designs need to be closely matched to minimize aperture uncertainty differences. And lastly, the

clock phase relationships need to be precisely controlled such that the two input clocks are as close to 180° apart as possible. As with the other mismatches, the goal is to attempt to minimize the mechanisms that cause the timing mismatch.

The last mismatch to look at is probably the most difficult to comprehend and handle; it is the bandwidth mismatch. As shown in Figure 7, the bandwidth mismatch has a gain and a phase/frequency component. This makes bandwidth mismatch more difficult because it contains components from two of the other mismatch parameters. In the bandwidth mismatch, however, we see different gain values at different frequencies. In addition, the bandwidth has a timing component which causes signals at different frequencies to have different delays through each converter. The best way to minimize the bandwidth mismatch is to have very good circuit design and layout practices that work to minimize the bandwidth mismatches between the ADCs. The better matched each ADC is, the less the resulting spur will be. Just as the gain and timing mismatches caused spurs in the output spectrum at $f_S/2 \pm f_{IN}$, the bandwidth mismatch also results in a spur at the same frequency.
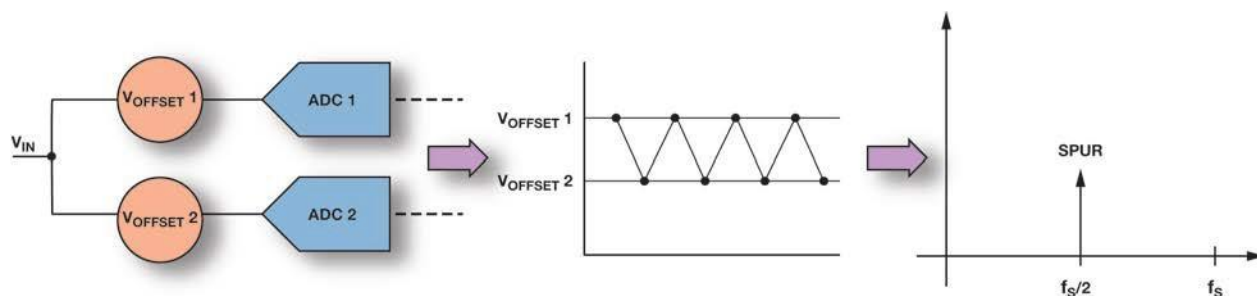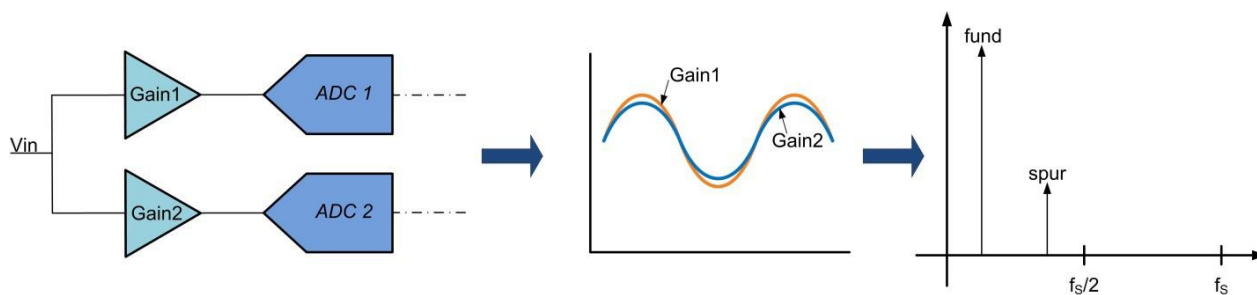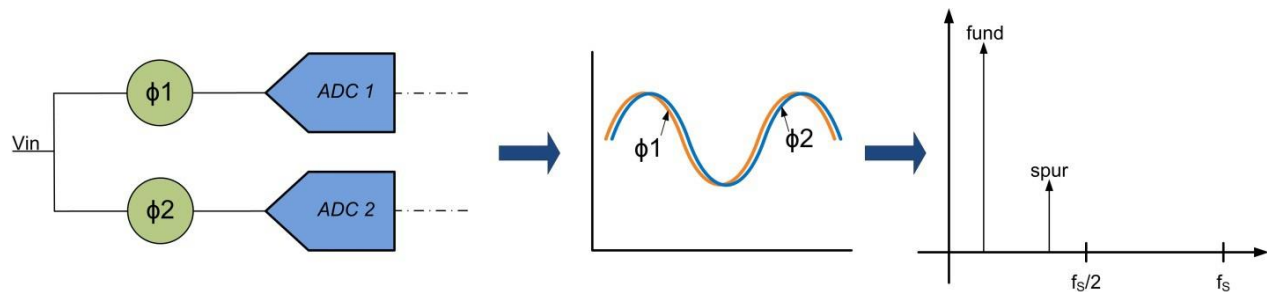

Figure 4. Offset Mismatch

Figure 5. Gain Mismatch

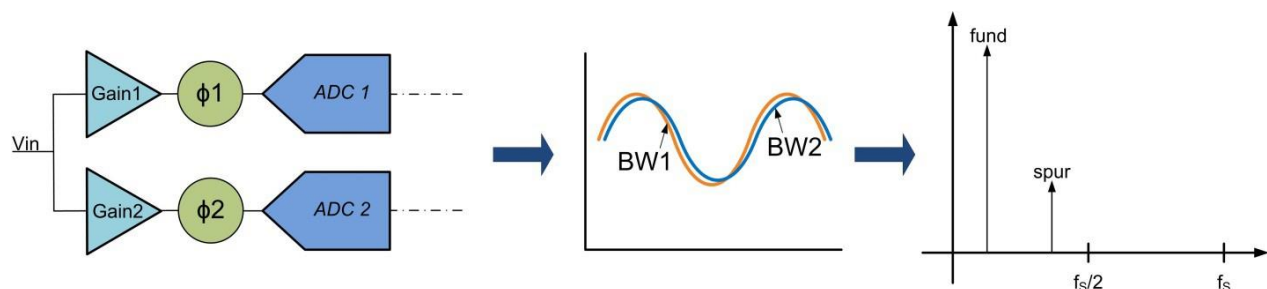*Figure 6. Timing Mismatch*

Figure 7. Bandwidth Mismatch

Now that we've discussed four different mismatches that cause issues when interleaving ADCs, it is apparent that a commonality has emerged. Three of the four mismatches produce a spur in the output spectrum at $f_S/2 \pm f_{IN}$. The offset mismatch spur can be easily identified since it alone resides at $f_S/2$ and can be compensated fairly easily. The gain, timing, and bandwidth mismatches all produce a spur at $f_S/2 \pm f_{IN}$ in the output spectrum so the question is how to identify the contribution of each. Figure 8 gives a quick visual guide to the process of identifying the sources of the spurs from the different mismatches of interleaved ADCs.
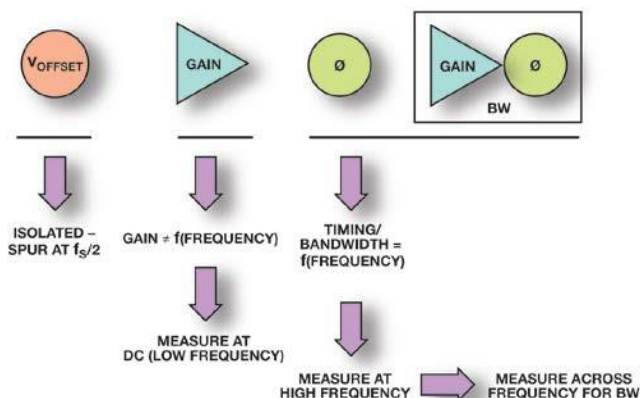

Figure 8. Interrelated Nature of Interleaving Mismatches

If looking purely at gain mismatch alone, it is a low frequency, or dc, type of mismatch. The gain component of the bandwidth mismatch can be separated from the gain mismatch by performing a gain measurement at low

frequency near dc and then performing gain measurements at higher frequencies. The gain mismatch is not a function of frequency like the gain component of the bandwidth mismatch. A similar approach is used for the timing mismatch. A measurement is performed at low frequency near dc and then subsequent measurements are performed at higher frequencies to separate the timing component of bandwidth mismatch from the timing mismatch.

CONCLUSION

The newest communication system designs, cutting edge radar technologies, and ultrahigh bandwidth measurement equipment seem to constantly outpace the available ADC technology. These requirements push both users and manufacturers of ADCs to develop methods to keep pace with these demands. Interleaving ADCs allows for greater bandwidths to be achieved at a faster pace than the traditional path of increasing the conversion rate of a typical ADC. By taking two or more ADCs and interleaving them together, the available bandwidth is increased, and system design requirements can be met at a faster pace. Interleaving ADCs does not come for free, however, and mismatches between the ADCs cannot be ignored. Even though the mismatches do exist, knowing about them and how to appropriately deal with them can enable designers to use these interleaved ADCs more intelligently and meet the ever increasing demands of their latest system designs.

REFERENCES

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