MAX77813 High-Efficiency Buck-Boost Converter

General Description

The MAX77813 is a high-efficiency buck-boost converter targeted for single-cell Li-ion battery powered applications. The device supports an input voltage range from 2.30V to 5.5V with an output voltage range from 2.60V to 5.14V. The device can support up to 2A and 3A of output current in boost and buck modes respectively. The peak efficiency of 97% allows longer operating time.

The device is designed to support seamless transitions between buck and boost modes. A unique control algorithm allows high-efficiency and outstanding performances in line/load transient responses. The I^2C-compatible serial interface provides design flexibility to optimize performance along with protection features. The output voltage can be dynamically adjusted for finer control of system power consumption. The device supports two input current limits selected by ILIM logic input.

The MAX77813 is available in a 1.827mm x 2.127mm, 20-bump wafer-level package (WLP).

Applications

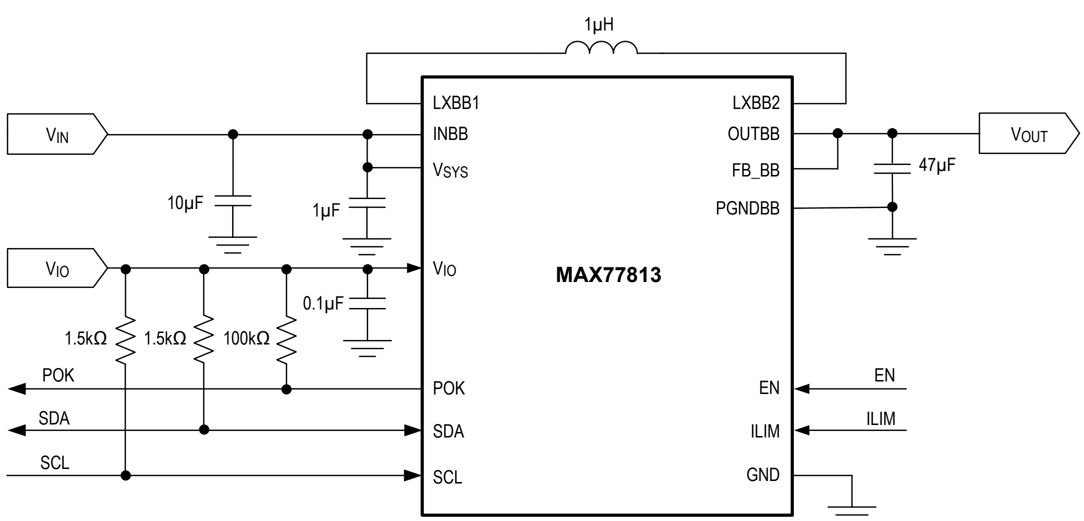
- Single-Cell Li-ion Powered Applications
- Handheld Scanners, Mobile Payment Terminals, Security Cameras
- AR/VR Headsets

Features and Benefits

- V_{IN} Range: 2.30V to 5.5V
- V_{OUT} Range: 2.60V to 5.14V (I^2C Programmable in 20mV Step)
- Up to 2A Output Current in Boost Mode (V_{IN} = 3.0V, V_{OUT} = 3.4V, ILIM = High)
- Up to 3A Output Current in Buck Mode (ILIM = High)
- Up to 97% Peak Efficiency
- SKIP Mode for Optimal Light Load Efficiency
- 55μA (Typ) Low Quiescent Current
- 3.4MHz High Speed I^2C Serial Interface
- Input Current Limit Selection Pin
- Power-OK Output
- 2.5MHz Switching Frequency
- Protection Features
  - Soft-Start
  - Thermal Shutdown
  - Overvoltage Protection
  - Short Circuit Protection
- 1.827mm x 2.127mm, 20-Bump WLP

***Ordering Information** appears at end of data sheet.*

Typical Application Circuit



Absolute Maximum Ratings

SYS, V_{IO} to GND ....-0.3V to +6.0V
INBB, OUTBB to PGNDBB ....-0.3V to +6.0V
PGNDBB to GND ....-0.3V to +0.3V
SCL, SDA to GND .... -0.3V to (V_{VIO} + 0.3V)
EN, ILIM, POK to GND.......................... -0.3V to (V_{SYS} + 0.3V)
FB_BB to GND ....-0.3V to (V_{OUTBB} + 0.3V)
LXBB1 to PGNDBB .... -0.3V to (V_{INBB} + 0.3V)
LXBB2 to PGNDBB...........................-0.3V to (V_{OUTBB} + 0.3V)
LXBB1/LXBB2 Continuous RMS Current (Note 1) 3.2A
Operating Junction Temperature Range .... -40°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range .... -65°C to +150°C
Soldering Temperature (Reflow)....................................+260°C

Note 1: LXBB1/LXBB2 node has internal clamp diodes to PGNDBB and INBB. Applications that give forward bias to these diodes should ensure that the total power loss does not exceed the power dissipation limit of the IC package.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	W201F2+1
Outline Number	21-0771
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction to Ambient Thermal Resistance (θ_{JA})	55.49°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Buck-Boost Electrical Characteristics

(V_{SYS} = V_{INBB} = +3.8V, V_{FB_BB} = V_{OUTBB} = +3.3V, T_J = -40°C to +125°C, typical values are at $T_A \approx T_J$ = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Input Voltage Range	V_{INBB}		2.30		5.50	V
Shutdown Supply Current	I_{SHDN_25C}	EN = low, T_J = +25°C		0.1		µA
	I_{SHDN_125C}	EN = low, T_J = +125°C		1		
Input Supply Current	I_{Q_SKIP}	SKIP mode, no switching, T_J = -40° to +85°C		55	70	µA
	I_{Q_PWM}	FPWM mode, no load		6		mA
Active Discharge Resistance	R_{DISCHG}			100		Ω
Thermal Shutdown Threshold	T_{SHDN}	Rising, +20°C hysteresis		+165		°C
H-BRIDGE						
Output Voltage Range	V_{OUT}	I²C programmable (20mV Step)	2.60		5.14	V
Output Voltage Accuracy	V_{OUT_ACC1}	FPWM mode, VOUT[6:0] = 0x28, no load, T_J = +25°C	-1.0		+1.0	%
	V_{OUT_ACC2}	SKIP mode, VOUT[6:0] = 0x28, no load, T_J = +25°C	-1.0		+4.5	
Line Regulation		V_{INBB} = 2.63V to 5.5V		0.200		%/V
Load Regulation		(Note 5)		0.125		%/A
Line Transient Response	V_{OS1} V_{US1}	I_{OUT} = 1.0A, V_{INBB} changes from 3.4V to 2.9V in 25µs (20mV/µs), L = 1µH, C_{OUT_NOM} = 47µF (Note 5)		50		mV
Load Transient Response	V_{OS2} V_{US2}	V_{INBB} = 3.4V, I_{OUT} changes from 10mA to 1.5A in 15µs, L = 1µH, C_{OUT_NOM} = 47µF (Note 5)		50		mV
Output Voltage Ramp-Up Slew Rate		BB_RU_SR = 0		20		mV/µs
		BB_RU_SR = 1		40		
Output Voltage Ramp-Down Slew Rate		BB_RD_SR = 0		5		mV/µs
		BB_RD_SR = 1		10		
Typical Condition Efficiency	η_{TYP}	I_{OUT} = 100mA (Note 5)		95		%
Peak Efficiency	η_{PK}	(Note 5)		97		%
LXBB1/2 Current Limit	I_{LIM_LXBB}	ILIM = high	3.70	4.50	5.70	A
		ILIM = low (OTP: 1.8A, 2.2A, 2.7A, 3.1A)	1.2	1.80	2.65	
High-Side PMOS ON Resistance	$R_{DSON(PMOS)}$	I_{LXBB} = 100mA per switch		40		mΩ
Low-Side NMOS ON Resistance	$R_{DSON(NMOS)}$	I_{LXBB} = 100mA per switch		55		mΩ
Switching Frequency	f_{SW}	PWM mode, T_J = +25°C	2.25	2.50	2.75	MHz

Buck-Boost Electrical Characteristics (continued)

(V_{SYS} = V_{INBB} = +3.8V, V_{FB_BB} = V_{OUTBB} = +3.3V, T_J = -40°C to +125°C, typical values are at $T_A \approx T_J$ = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Turn-On Delay Time	t_{ON_DLY}	From EN asserting to LXBB switching with bias ON		100		µs
Soft-Start Time	t_{SS}	I_{OUT} = 10mA, ILIM = high		120		µs
		I_{OUT} = 10mA, ILIM = low		800		
Minimum Effective Output Capacitance	$C_{EFF(MIN)}$	0A < I_{OUT} < 2000mA		16		µF
LXBB1, LXBB2 Leakage Current	I_{LK_25C}	$V_{LXBB1/2}$ = 0V or 5.5V, V_{OUTBB} = 5.5V, V_{SYS} = V_{INBB} = 5.5V, T_J = +25°C		0.1	1	µA
	I_{LK_125C}	$V_{LXBB1/2}$ = 0V or 5.5V, V_{OUTBB} = 5.5V, V_{SYS} = V_{INBB} = 5.5V, T_J = +125°C		0.2		
POWER-OK COMPARATOR						
Output POK Trip Level		Rising threshold		80		%
		Falling threshold		75		
V_{SYS} UNDERVOLTAGE LOCKOUT						
V_{SYS} Undervoltage Lockout Threshold	V_{UVLO_R}	V_{SYS} rising	2.375	2.50	2.625	V
	V_{UVLO_F}	V_{SYS} falling		2.05		
LOGIC AND CONTROL INPUTS						
Input Low Level	V_{IL}	EN, ILIM, V_{SYS} = 3.8V, T_J = +125°C			0.4	V
Input High Level	V_{IH}	EN, ILIM, V_{SYS} = 3.8V, T_J = -40°C	1.2			V
POK Output Low Voltage	V_{OL}	I_{SINK} = 1mA			0.4	V
POK Output High Leakage	I_{OZH_25C}	T_J = +25°C	-1		+1	µA
	I_{OZH_125C}	T_J = +125°C		0.1		
INTERNAL PULLDOWN RESISTANCE						
EN	R_{PD}	Pulldown resistance to GND	400	800	1600	kΩ

Note 2: Limits are 100% production tested at T_J = +25°C. The device is tested under pulsed load conditions such that $T_J \approx T_A$. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Note 3: Guaranteed by design. Not production tested.

I²C Electrical Characteristics

(V_{SYS} = 3.8V, V_{VIO} = 1.8V, T_J = -40°C to +125°C, typical values are at $T_A \approx T_J$ = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{IO} Voltage Range	V_{VIO}		1.7		3.6	V
SDA AND SCL I/O STAGES						
SCL, SDA Input High Voltage	V_{IH}		0.7 x V_{VIO}			V
SCL, SDA Input Low Voltage	V_{IL}				0.3 x V_{VIO}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{VIO}		V
SCL, SDA Input Current	I_I	V_{VIO} = 3.8V	-10		+10	µA
SDA Output Low Voltage	V_{OL}	I_{SINK} = 20mA			0.4	V
SCL, SDA Input Capacitance	C_I			10		pF
Output Fall Time from V_{VIO} to 0.3 x V_{VIO}	t_{OF}				120	ns
I²C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST, AND FAST-MODE PLUS) (Note 5)						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (REPEATED) START Condition	$t_{HD;STA}$		0.26			µs
SCL Low Period	t_{LOW}		0.5			µs
SCL High Period	t_{HIGH}		0.26			µs
Setup Time REPEATED START Condition	t_{SU_STA}		0.26			µs
DATA Hold Time	t_{HD_DAT}		0			µs
DATA Setup Time	t_{SU_DAT}		50			ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Bus-Free Time Between STOP and START	t_{BUF}		0.5			µs
Capacitive Load for Each Bus Line	C_B				550	pF
Maximum Pulse Width of Spikes that must be suppressed by the input filter				50		ns

I^2C Electrical Characteristics (continued)

(V_{SYS} = 3.8V, V_{VIO} = 1.8V, T_J = -40°C to +125°C, typical values are at $T_A \approx T_J$ = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I^2C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, C_B = 100pF) (Note 5)						
Clock Frequency	f_{SCL}				3.4	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
CLK Low Period	t_{LOW}		160			ns
CLK High Period	t_{HIGH}		60			ns
DATA Setup Time	t_{SU_DAT}		10			ns
DATA Hold Time	t_{HD_DAT}			35		ns
SCL Rise Time (Note 3)	t_{RCL}	T_J = +25°C	10		40	ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit	t_{RCL1}	T_J = +25°C	10		80	ns
SCL Fall Time	t_{FCL}	T_J = +25°C	10		40	ns
SDA Rise Time	t_{RDA}	T_J = +25°C			80	ns
SDA Fall Time	t_{FDA}	T_J = +25°C			80	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				100	pF
Maximum Pulse Width of Spikes that must be suppressed by the input filter				10		ns
I^2C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, C_B = 400pF) (Note 5)						
Clock Frequency	f_{SCL}				1.7	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
SCL Low Period	t_{LOW}		320			ns
SCL High Period	t_{HIGH}		120			ns
DATA Setup Time	t_{SU_DAT}		10			ns
DATA Hold Time	t_{HD_DAT}			75		ns

I^2C Electrical Characteristics (continued)

(V_{SYS} = 3.8V, V_{VIO} = 1.8V, T_J = -40°C to +125°C, typical values are at $T_A \approx T_J$ = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Rise Time	t_{RCL}	T_J = +25°C	20		80	ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit	t_{RCL1}	T_J = +25°C	20		160	ns
SCL Fall Time	t_{FCL}	T_J = +25°C	20		80	ns
SDA Rise Time	t_{RDA}	T_J = +25°C			160	ns
SDA Fall Time	t_{FDA}	T_J = +25°C			160	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				400	pF
Maximum Pulse Width of Spikes that Must be Suppressed by the Input Filter	t_{SP}			10		ns

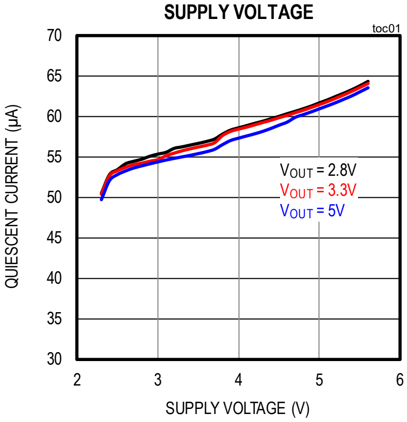
Note 4: Limits are 100% production tested at T_J = +25°C. The device is tested under pulsed load conditions such that $T_J \approx T_A$. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Note 5: Guaranteed by design. Not production tested.

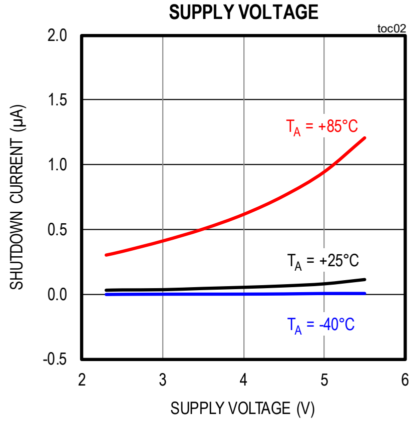
Typical Operating Characteristics

(V_{SYS} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 0A, FPWM = 0, T_A = +25°C, unless otherwise noted.)

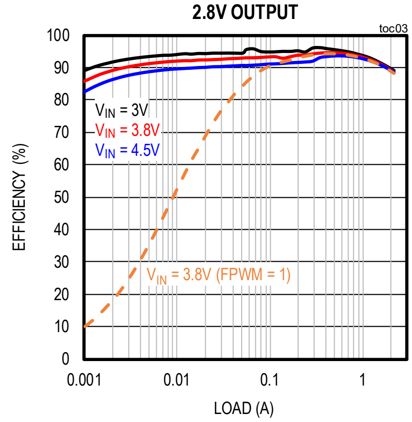
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



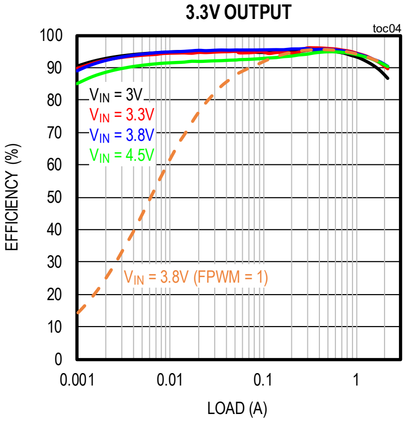
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



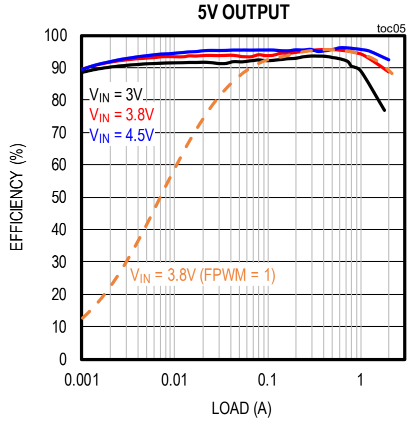
EFFICIENCY vs. LOAD 2.8V OUTPUT



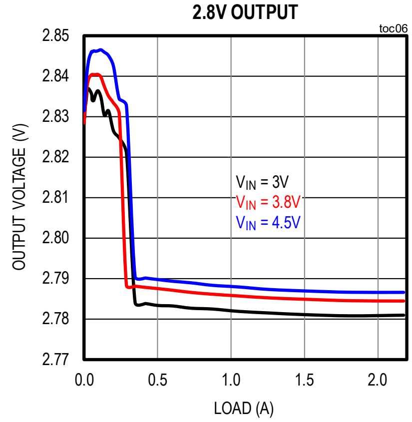
EFFICIENCY vs. LOAD 3.3V OUTPUT



EFFICIENCY vs. LOAD 5V OUTPUT



LOAD REGULATION 2.8V OUTPUT



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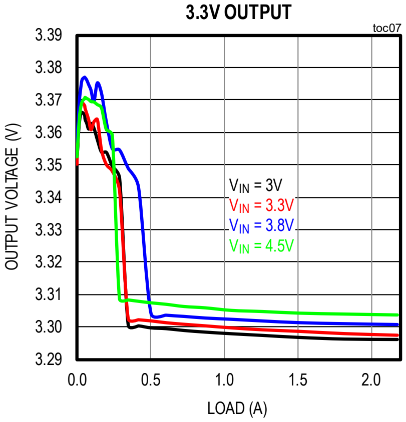
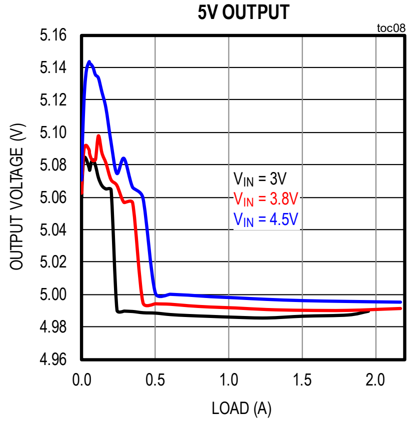
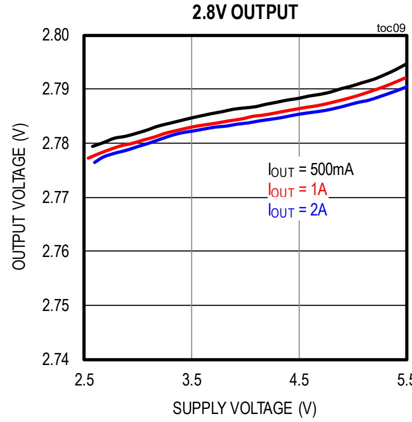


LOAD REGULATION 5V OUTPUT



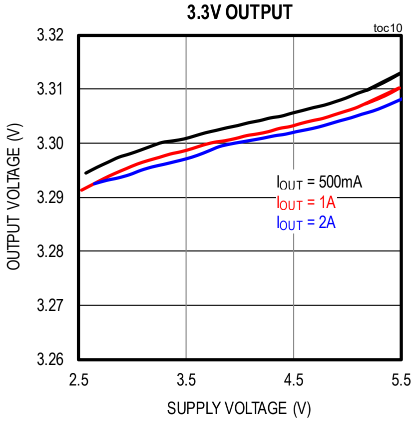
LINE REGULATION 2.8V OUTPUT



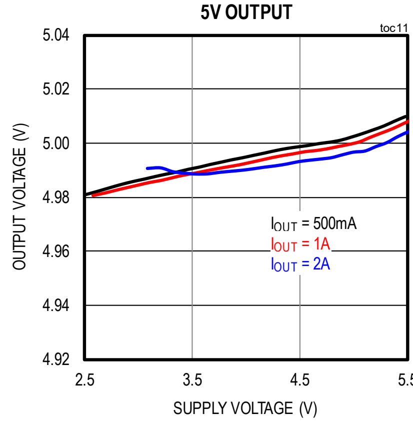
Typical Operating Characteristics (continued)

(V_{SYS} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 0A, FPWM = 0, T_A = +25°C, unless otherwise noted.)

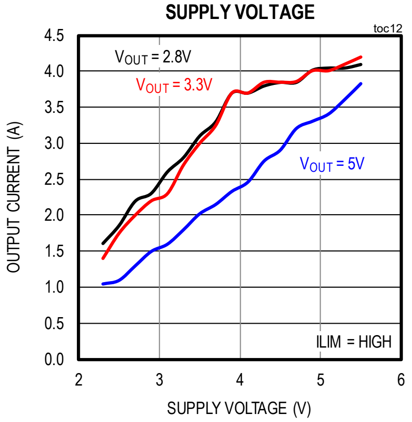
LINE REGULATION
3.3V OUTPUT



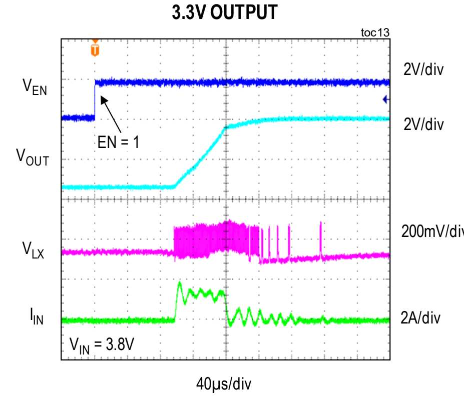
LINE REGULATION
5V OUTPUT



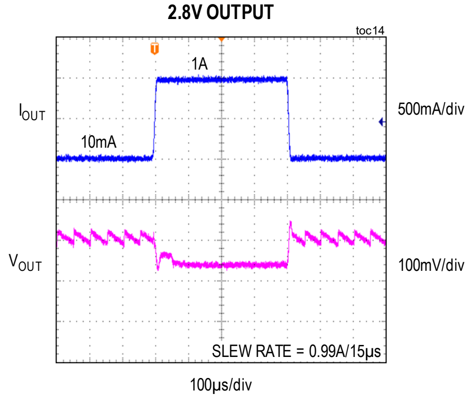
MAXIMUM OUTPUT CURRENT vs.
SUPPLY VOLTAGE



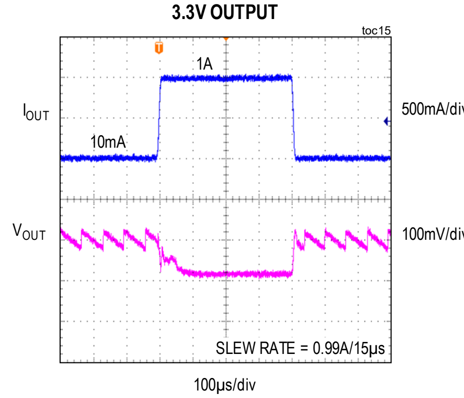
ENABLE STARTUP WAVEFORM
3.3V OUTPUT



LOAD TRANSIENT RESPONSE
2.8V OUTPUT



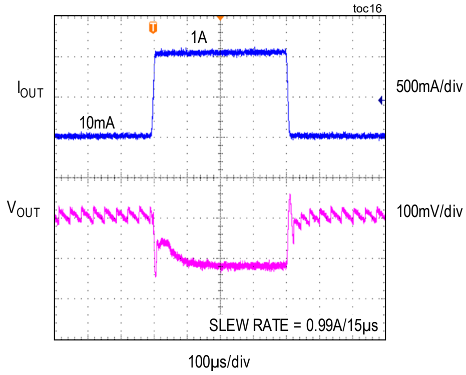
LOAD TRANSIENT RESPONSE
3.3V OUTPUT



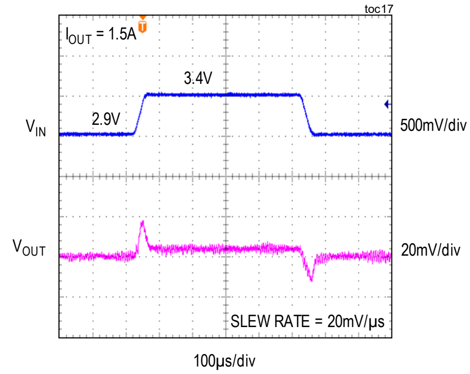
Typical Operating Characteristics (continued)

(V_{SYS} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 0A, FPWM = 0, T_A = +25°C, unless otherwise noted.)

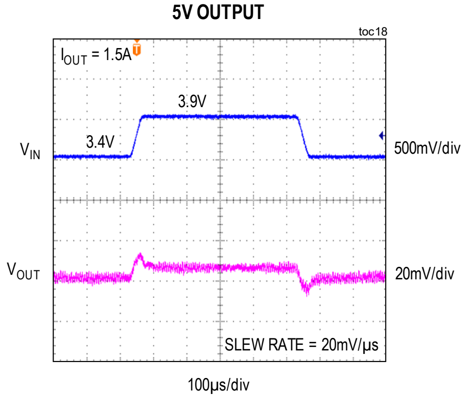
LOAD TRANSIENT RESPONSE
5V OUTPUT



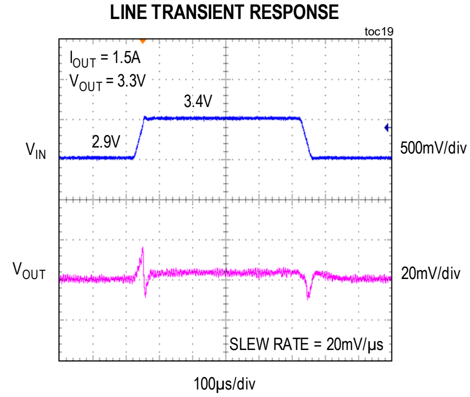
LINE TRANSIENT RESPONSE
2.8V OUTPUT



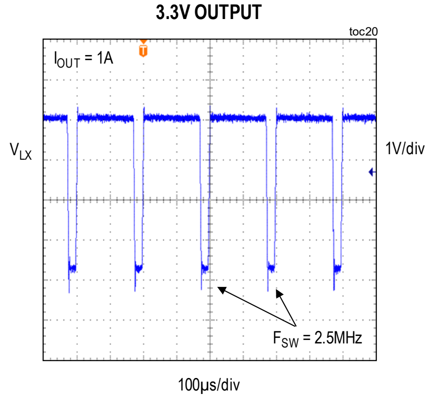
LINE TRANSIENT RESPONSE
5V OUTPUT



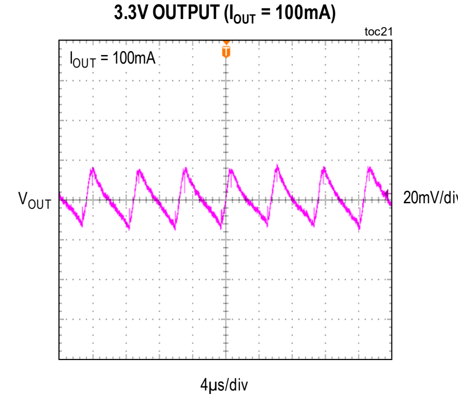
BOOST TO BUCK
LINE TRANSIENT RESPONSE



SWITCHING WAVEFORM
3.3V OUTPUT

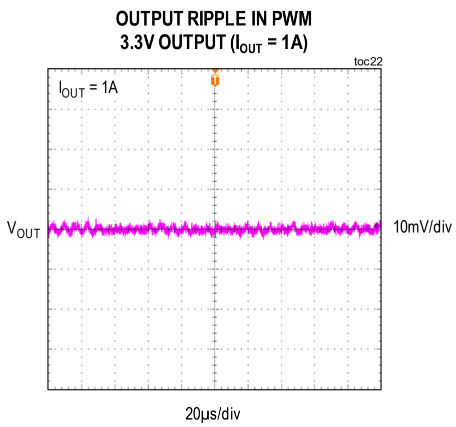


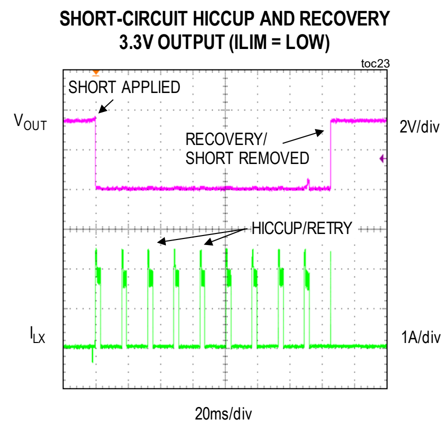
OUTPUT RIPPLE IN SKIP MODE
3.3V OUTPUT (I_{OUT} = 100mA)

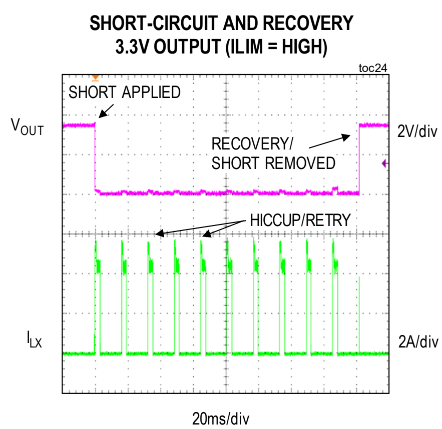


Typical Operating Characteristics (continued)

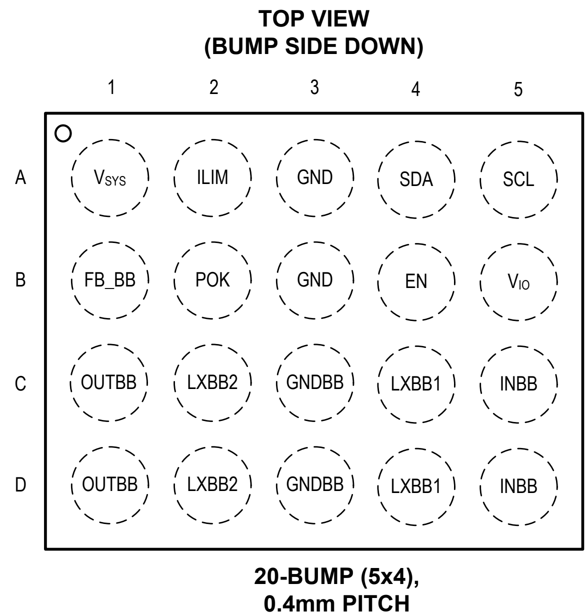
(V_{SYS} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 0A, FPWM = 0, T_A = +25°C, unless otherwise noted.)







Bump Configuration



Bump Description

PIN	NAME	FUNCTION
A1	V_{SYS}	System (Battery) Voltage Input. Bypass to GND with a 1μF capacitor.
A2	ILIM	Current Limit Selection Input. It must not be left open.
A3, B3	GND	Ground. “Star-Ground” connection to system GND.
A4	SDA	I^2C Data I/O (Hi-Z in OFF State). A 1.5kΩ to 2.2kΩ of pullup resistor to V_{IO} is required.
A5	SCL	I^2C Clock Input (Hi-Z in OFF State). A 1.5kΩ to 2.2kΩ of pullup resistor to V_{IO} is required.
B1	FB_BB	Buck-Boost Output Voltage Feedback
B2	POK	Power-OK. Open drain output asserted after buck-boost output reaches 80% of output voltage. Polarity of POK output is selectable through I^2C (active-high by default).
B4	EN	Chip Enable Input (Active-high). An 800kΩ internal pulldown resistance to GND.
B5	V_{IO}	I^2C Supply Voltage Input. Bypass to GND with a 0.1μF capacitor. If not in use, connect to GND.
C1, D1	OUTBB	Buck-Boost Output
C2, D2	LXBB2	Buck-Boost Switching Node2
C3, D3	PGNDBB	Buck-Boost Power Ground. “Star-Ground” connection to system GND.
C4, D4	LXBB1	Buck-Boost Switching Node1
C5, D5	INBB	Buck-Boost Input. Bypass to PGNDBB with a 10μF capacitor.

Detailed Description

Chip Enable (EN)

When the EN pin goes high, the MAX77813 turns on the internal bias circuitry which takes typically 85μs to be settled. As soon as the bias is ready, the buck-boost regulator is enabled. Once V_{IO} is supplied, then all user registers are accessible through I^2C. When the EN pin is pulled low, the device goes into shutdown mode. This event also resets all Type-O registers to their POR default values.

Immediate Turn-Off Events

The following events initiate “Immediate Turn-Off”:

- Thermal Shutdown (T_J > 165°C)
- V_{SYS} < V_{SYS} UVLO Falling Threshold (V_{UVLO_F})
- Overcurrent Protection

The events in this category disable buck-boost until the hazardous condition comes back to normal conditions.

Regulator Enable Control

The buck-boost has a chip enable pin (EN) as well as an I^2C enable bit. As shown in Table 1, the EN pin of MAX77813 should be in logic high to allow I^2C to enable/disable the device.

Current Limit Selection Input (ILIM)

The device provides two different current limit levels selectable by ILIM pin logic set up. When ILIM is logic high, the switching current limit level is set to 4.5A (typ) and capable of handling higher load current. When ILIM is logic low, the switching current limit level is set to 1.8A (typ) for default OTP options to allow for smaller inductors. The device supports three other OTP programmable switching current limit levels for ILIM logic low option.

Table 1. Enable Control Logic Truth Table

EN	BB_EN BIT	OPERATING MODE
Low	x	Device OFF
High	0	Disable Output
High	1 (default)	Enable Output

Contact sales representatives to get different options other than the default value.

During soft-start, the device lowers the switching current limit level than the values set by the ILIM pin and it comes back to the normal level after soft-start is finished.

Programmable Ramp-Up/Down Rate Through I^2C Interface

The device allows selectable slew rate for output voltage change through the I^2C interface. The ramp-up slew rate can be set as either 20mV/μs or 40mV/μs through the BB_RU_SR bit, also the ramp-down slew rate can be set as either 5mV/μs or 10mV/μs through the BB_RD_SR bit.

Power-OK (POK) Indicator

The buck-boost has an open-drain output which is asserted after output voltage reaches 80% of output voltage. The polarity of the POK output is selectable by the POK_POL register bit (active-high by default).

H-Bridge Controller

The H-Bridge architecture operates at 2.5MHz fixed frequency with a pulse width modulated (PWM) current-mode control scheme. This topology is in a cascade of a boost regulator and a buck regulator using a single inductor and output capacitor.

There are three phases implemented with the H-bridge switch topology, as shown in Figure 2:

- Φ1 switch period (Phase-1: HS1 = ON, LS2 = ON) stores energy in the inductor, ramping up the inductor current at a rate proportional to the input voltage divided by inductance; V_{INBB} / L.
- Φ2 switch period (Phase-2: HS1 = ON, HS2 = ON) ramps the inductor current up or down, depending on the differential voltage across the inductor, divided by inductance; $\pm(V_{INBB} - V_{OUTBB})$ / L.
- Φ3 switch period (Phase-3: LS1 = ON, HS2 = ON) ramps down the inductor current at a rate proportional to the output voltage divided by inductance, $-V_{OUTBB}$ / L.

Buck-Boost Regulator

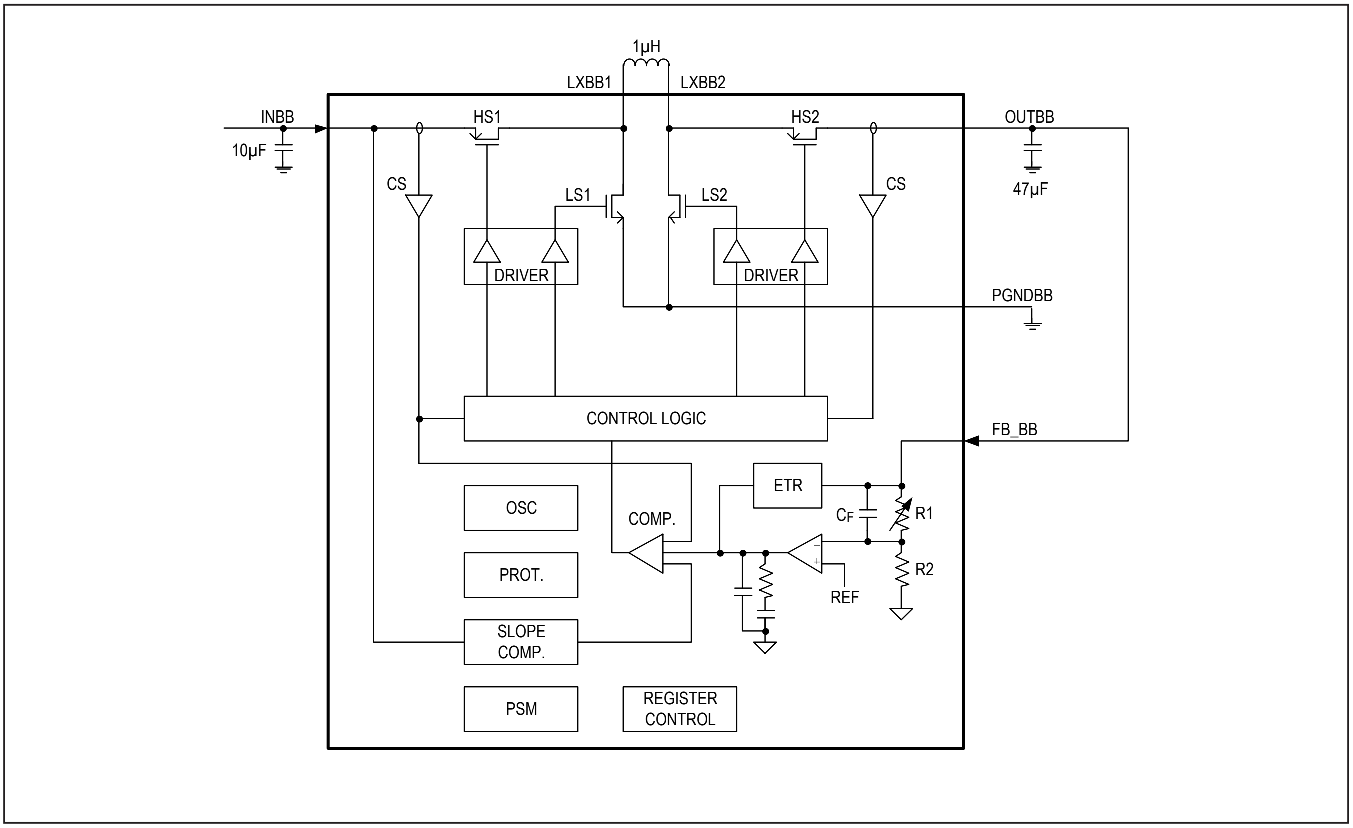


Figure 1. Buck-Boost Block Diagram

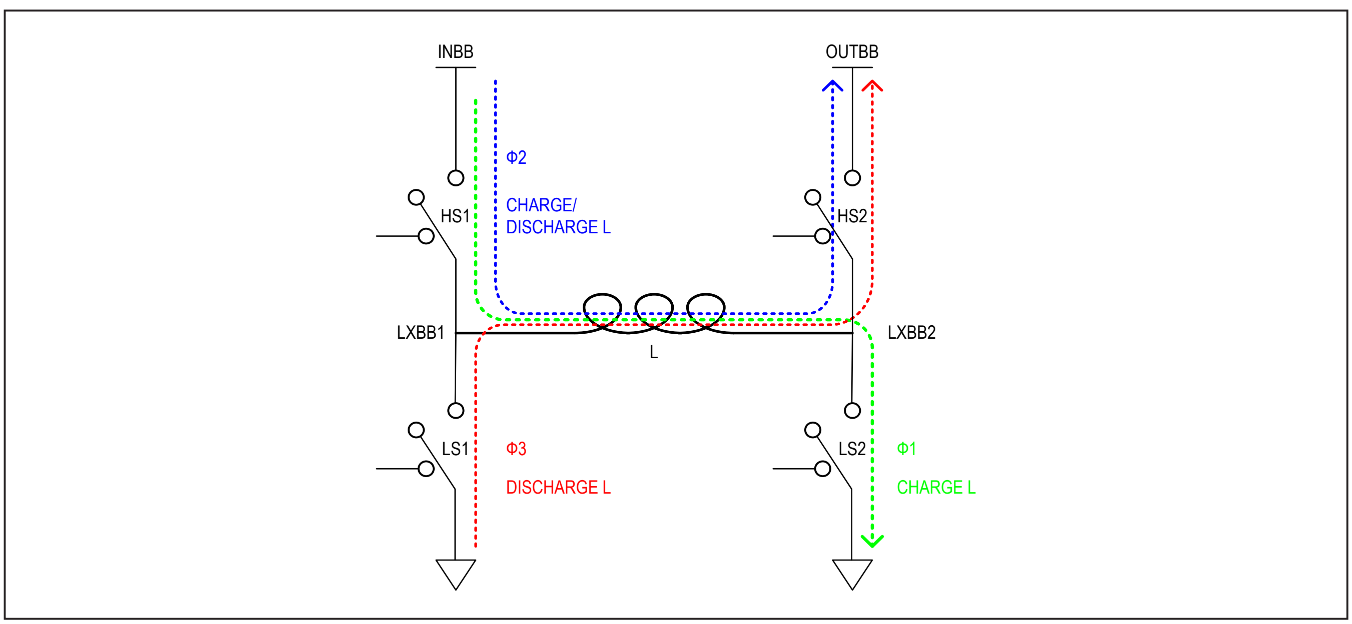


Figure 2. Buck-Boost Switching Intervals

2-Phase buck topology is utilized when $V_{INBB} > V_{OUTBB}$. A switching cycle is completed in one clock period. Switch period Φ2 is followed by switch period Φ3, resulting in an inductor current waveform similar to Figure 3.

2-Phase boost topology is utilized when $V_{INBB} < V_{OUTBB}$. A switching cycle is completed in one clock period. Switch period Φ1 is followed by switch period Φ2, resulting in an inductor current waveform similar to Figure 4 below.

Output Voltage Slew-Rate Control

The device allows selectable slew rates for output voltage change. The ramp-up slew-rate can be set to 12.5mV/μs or 25mV/μs through the BB_RU_SR bit, while the ramp-down slew-rate is programmable to 3.125mV/μs or 6.25mV/μs through the BB_RD_SR bit.

Inductor Selection

Buck-boost is optimized for a 1μH inductor. The lower the inductor DCR, the higher the buck-boost efficiency is expected. The saturation current of an inductor should be higher than the switching current limit level of the MAX77813. Table 2 shows examples of inductors for each current limit setting.

Input Capacitor Selection

The input capacitor, C_{IN}, reduces the current peaks drawn from the battery or input power source and reduces switching noise in the device. The impedance of C_{IN} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. For most applications, a 10μF capacitor is sufficient.

Output Capacitor Selection

The output capacitor, C_{OUT}, is required to keep the output voltage ripple small and to ensure regulation loop stability. C_{OUT} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. For stable operation, buck-boost requires 16μF of minimum effective output capacitance. Considering the DC bias characteristic of ceramic capacitors, a 47μF 6.3V capacitor is recommended for most applications.

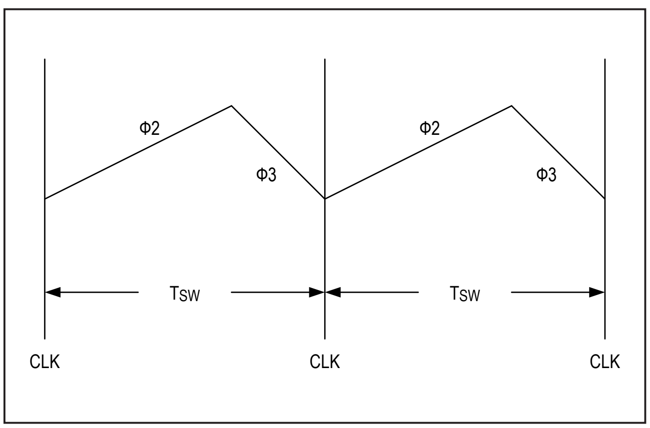


Figure 3. 2-Phase Buck Mode Switching Current Waveforms

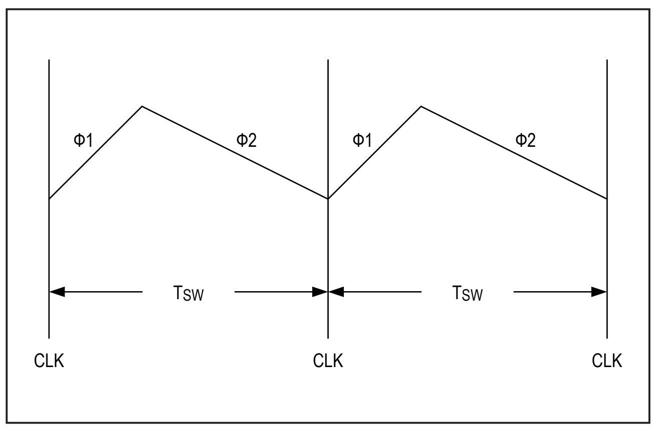


Figure 4. 2-Phase Boost Mode Switching Current Waveforms

Table 2. Suggested Inductors for Buck-Boost

MFGR.	SERIES	NOMINAL INDUCTANCE [μH]	TYPICAL DC RESISTANCE [mΩ]	CURRENT RATING [A] -30% (ΔL/L)	CURRENT RATING [A] ΔT = +40°C RISE	DIMENSIONS L x W x H [mm]	ILIM SETTING
TDK	TFM201610GHM - 1R0MTAA	1.0	50	3.8	3.0	2.0 x 1.6 x 1.0	Low
TOKO	DFE322512C	1.0	34	4.6	3.7	3.2 x 2.5 x 1.2	Low
Coilcraft	XAL4020-102MEB	1.0	13	8.7	9.6	4.0 x 4.0 x 2.1	High

Serial Interface

The I^2C-compatible 2-wire serial interface is used for regulator on/off control, setting output voltages, and other functions. See the complete register map.

The I^2C serial bus consists of a bidirectional serial-data line (SDA) and a serial clock (SCL). I^2C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional 24Ω resistors in series with SDA and SCL help to protect the device inputs from high voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

System Configuration

The I^2C bus is a multi-master bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

Figure 5 shows an example of a typical I^2C system. A device on I^2C bus that sends data to the bus in called a "Transmitter". A device that receives data from the bus is called a "Receiver". The device that initiates a data transfer and generates SCL clock signals to control the data transfer is a "Master". Any device that is being addressed by the master is considered a "Slave". When the MAX77813 I^2C-compatible interface is operating, it is a slave on the I^2C bus and it can be both a transmitter and a receiver.

Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on SDA must remain stable during the high portion of SCL clock pulse. Changes in SDA while SCL is high are control signals (START and STOP conditions).

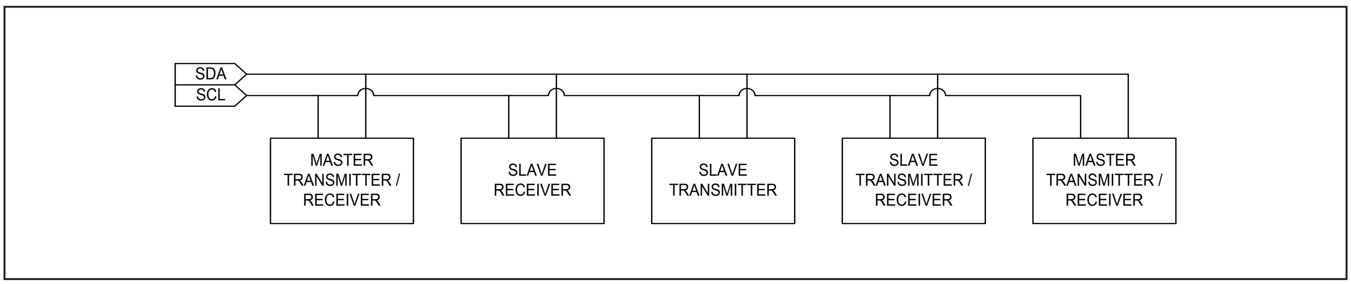


Figure 5. Functional Logic Diagram for Communications Controller

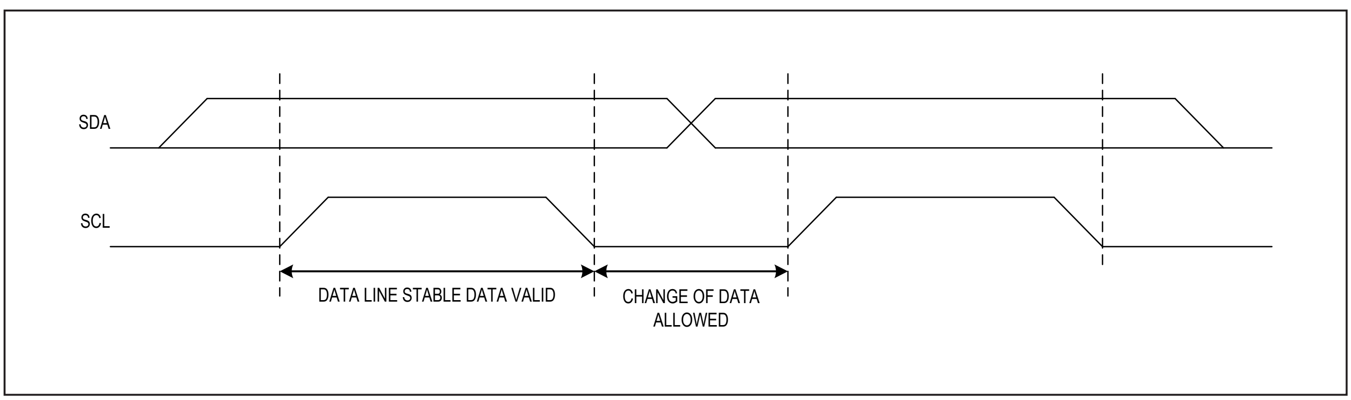


Figure 6. I^2C Bit Transfer

START and STOP Conditions

When I2C serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high.

A START condition from the master signals the beginning of a transmission to the device. The master terminates transmission by issuing a NOT-ACKNOWLEDGE followed by a STOP condition.

A STOP condition frees the bus. To issue a series of commands to the slave, the master may issue REPEATED START (Sr) commands instead of a STOP command in order to maintain control of the bus. In general, a REPEATED START command is functionally equivalent to a regular START command.

When a STOP condition or incorrect address is detected, the device internally disconnects SCL from the I2C serial interface until the next START condition, minimizing digital noise and feed-through.

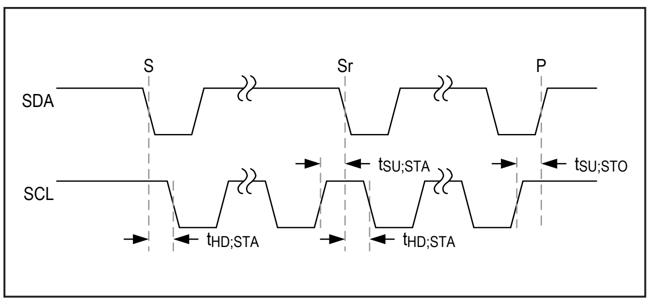


Figure 7. START and STOP Conditions

Acknowledged

Both the I2C bus master and the device (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine-bit data packet. To generate an ACKNOWLEDGE (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. To generate a NOT-ACKNOWLEDGE (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Slave Address

The I2C slave address of the device is shown in Table 3.

Table 3. I2C Slave Address

SLAVEADDRESS (7 BIT)	SLAVEADDRESS (WRITE)	SLAVEADDRESS (READ)
001 1000	0x30 (0011 0000)	0x31 (0011 0001)

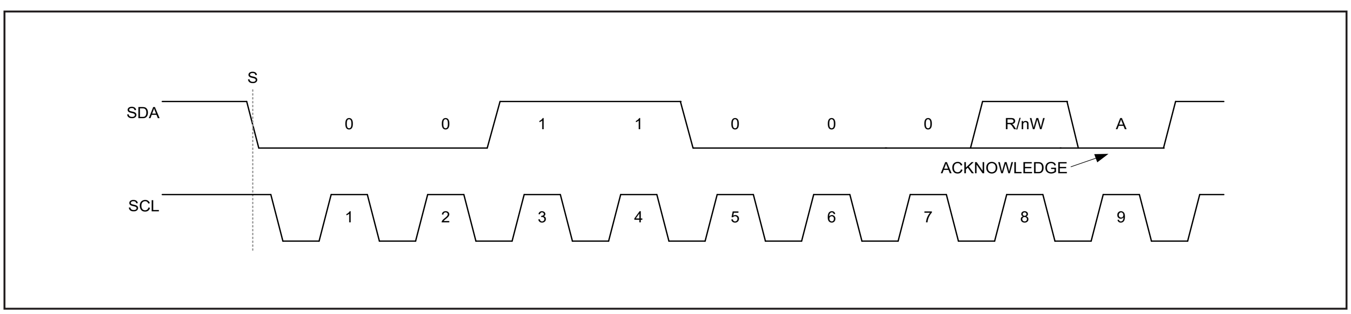


Figure 8. Slave Address Byte Example

Clock Stretching

In general, the clock signal generation for the I2C bus is the responsibility of the master device. I2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The device does not use any form of clock stretching to hold down the clock line.

General Call Address

The device does not implement I2C specification “General Call Address.” If the device sees “General Call Address (00000000b)” it does not issue an ACKNOWLEDGE (A).

Communication Speed

The device provides I2C 3.0-compatible (3.4MHz) serial interface.

- I2C Revision 3 Compatible Serial Communications Channel
  - 0Hz to 100kHz (Standard mode)
  - 0Hz to 400kHz (Fast mode)
  - 0Hz to 1MHz (Fast-mode plus)
  - 0Hz to 3.4MHz (High-speed mode)
- Does not utilize I2C Clock Stretching

Operating in standard mode, fast mode, and fast-mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. See the *Pullup Resistor Sizing* section of the I2C revision 3.0 specification for detailed guidance on the pullup resistor selection. In general, for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that the pullup resistor is dissipating power when the open-drain bus is low. The lower the value of the pullup resistor, the higher the power dissipation (V^2/R).

Operating in high-speed mode requires some special considerations. For the full list of considerations, see the I2C 3.0 specification. The major considerations with respect to the MAX77813 are:

- I2C bus master use current source pullups to shorten the signal rise times.
- I2C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each STOP condition, the device input filters are set for standard mode, fast mode, or fast-mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the *Communication Protocols* section.

Communication Protocols

The device supports both writing and reading from its registers. The following sections show the I2C communication protocols for each functional block. The power block uses the same communication protocols.

Writing to a Single Register

Figure 9 shows the protocol for the I2C master device to write one byte of data to the device. This protocol is the same as SMBus specification's "Write Byte" protocol.

The "Write Byte" protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. At the rising edge of SCL, the data byte loads into its target register and the data becomes active.
8) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

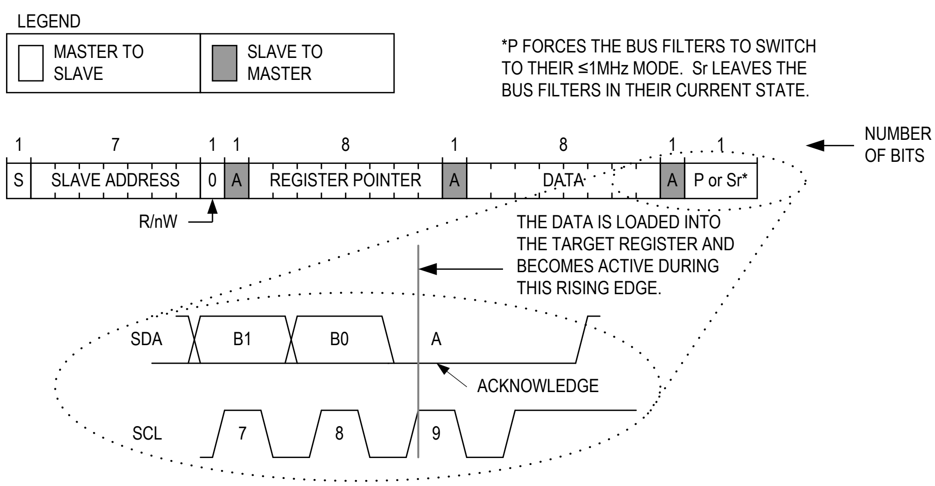


Figure 9. Writing to a Single Register with "Write Byte" Protocol

Writing to Sequential Registers

Figure 10 shows the protocol for writing to sequential registers. This protocol is similar to the "Write Byte" protocol, except the master continues to write after it receives the first byte of data. When the master is done writing, it issues a STOP or REPEATED START.

The "Writing to Sequential Registers" protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. At the rising edge of SCL, the data byte loads into its target register and the data becomes active.
8) Steps 6 to 7 are repeated as many times as the master requires.
9) During the last acknowledge related clock pulse, the slave issues an ACKNOWLEDGE (A).
10) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

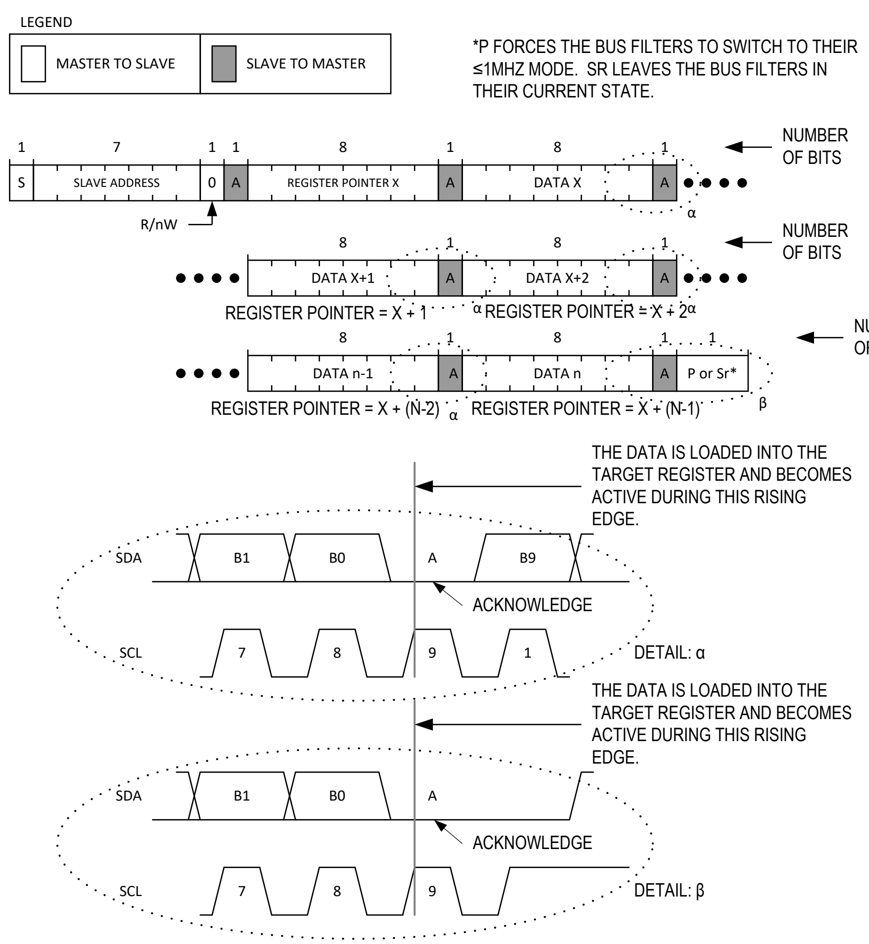


Figure 10. Writing to Sequential Registers

Reading from a Single Register

The I2C master device reads one byte of data to the device. This protocol is the same as SMBus specification's "Read Byte" protocol.

The "Read Byte" protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START command (Sr).
7) The master sends the 7-bit slave address followed by a read bit (R/nW = 1).
8) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9) The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10) The master issues a NOT-ACKNOWLEDGE (nA).
11) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

Reading from Sequential Registers

Figure 11 shows the protocol for reading from sequential registers. This protocol is similar to the "Read Byte" protocol except the master issues an ACKNOWLEDGE (A) to signal the slave that it wants more data – when the master has all the data it requires, it issues a NOT-ACKNOWLEDGE (nA) and a STOP (P) to end the transmission.

The "Continuous Read from Sequential Registers" protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START command (Sr).
7) The master sends the 7-bit slave address followed by a read bit (R/nW = 1).
8) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9) The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10) The master issues an ACKNOWLEDGE (A) signaling the slave that it wishes to receive more data.
11) Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a NOT-ACKNOWLEDGE (nA) to signal that it wishes to stop receiving data.
12) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

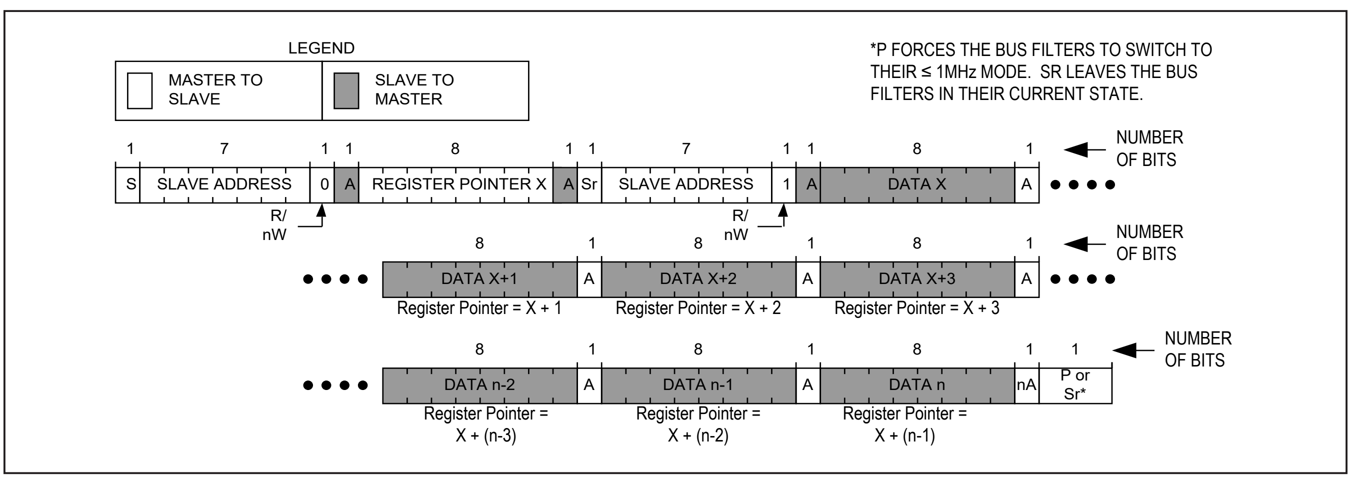


Figure 11. Reading Continuously from Sequential Registers

Engaging HS-Mode for Operation up to 3.4MHz

Figure 12 shows the protocol for engaging HS-mode operation. HS-mode operation allows for a bus operating speed up to 3.4MHz.

The “Engaging HS-Mode” protocol is as follows:

1) Begin the protocol while operating at a bus speed of 1MHz or lower.
2) The master sends a START command (S).
3) The master sends the 8-bit master code of 00001xxxb where xxxb are *don’t care* bits.
4) The addressed slave issues a NOT-ACKNOWLEDGE (nA).
5) The master may now increase its bus speed up to 3.4MHz and issue any read/write operation.

The master may continue to issue high-speed read/write operations until a STOP (P) is issued. Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation.

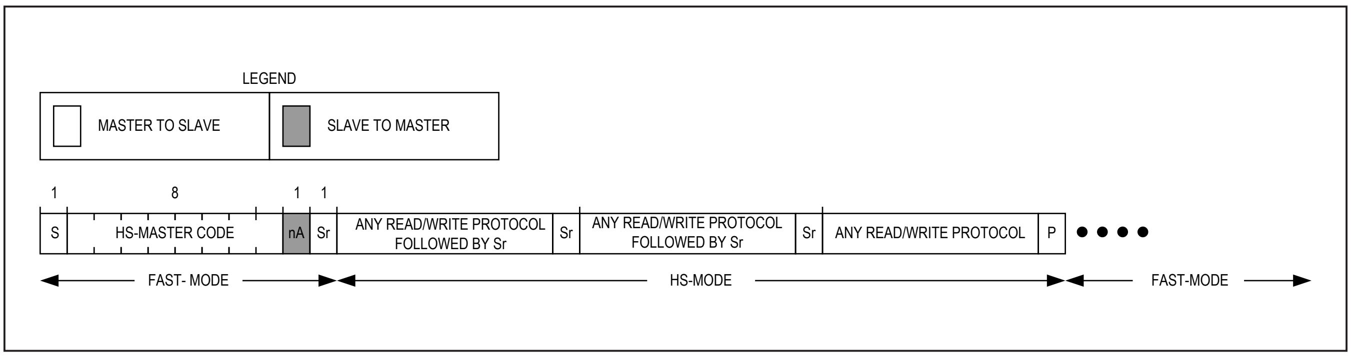


Figure 12. Engaging HS-Mode

Registers

Register Reset Conditions

- Type-O: Registers are reset when $V_{SYS} < V_{UVLO\_F}$ OR EN = Low

Register Map

I²C Slave Address (7-bit): 0x18

ADDR	REGISTER NAME	RESET TYPE	R/W	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET VALUE
0x00	DEVICE_ID	Type-O	R	RESERVED	VERSION[3:0]				CHIP_REV[2:0]			–
0x01	STATUS	Type-O	R	RESERVED	RESERVED	RESERVED	RESERVED	TSHDN	BB_POKn	BB_OVP	BB_OCP	–
0x02	CONFIG1	Type-O	R/W	RESERVED	RESERVED	BB_RU_SR	BB_RD_SR	BB_OVP_TH[1:0]		BB_AD	BB_FPWM	0x0E
0x03	CONFIG2	Type-O	R/W	RESERVED	BB_EN	EN_PD	POK_POL	RESERVED	RESERVED	RESERVED	RESERVED	0x70
0x04	VOUT	Type-O	R/W	RESERVED	VOUT[6:0]							0x28/ 0x23
0x05 – 0xFF	RESERVED											

DEVICE_ID

Device ID Register

ADDRESS	MODE		TYPE: O	RESET VALUE: NA
0x00	R			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7	RESERVED	0		
6:3	VERSION[3:0]	–	Version 0000b: Plain 0001b: -1Z 0010b: -2Z	
2:0	CHIP_REV[2:0]	–	Chip Revision History 001b: PASS1 010b: PASS2 011b: PASS3 and so on	

STATUS

Status Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x00
0x01	R			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:4	RESERVED	–		
3	TSHDN	–	0: Junction Temperature (T_J) ≤ 165°C 1: Junction Temperature (T_J) > 165°C	
2	BB_POKn	–	Buck-Boost POKn Status	
1	BB_OVP	–	Buck-Boost OVP Status	
0	BB_OCP	–	Buck-Boost OCP Status	

CONFIG1

Configuration Register1

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x0E
0x02	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7:6	RESERVED	00		
5	BB_RU_SR	0	Rising Ramp Rate Control **0: 20mV/µs** 1: 40mV/µs	
4	BB_RD_SR	0	Ramp-Down Slew-Rate Control **0: 5mV/µs** 1: 10mV/µs	
3:2	BB_OVP_TH [1:0]	11	Output OVP Threshold 00b: No OVP 01b: 110% of V_{OUT} 10b: 115% of V_{OUT} **11b: 120% of V_{OUT}**	
1	BB_AD	1	Output Active Discharge 0: Disable active discharge **1: Enable active discharge**	
0	BB_FPWM	0	Forced PWM Enable **0: SKIP mode** 1: Forced PWM	

CONFIG2

Configuration Register2

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x70
0x03	R/W			
BIT	**NAME**	**POR**	**DESCRIPTION**	
7	RESERVED	0		
6	BB_EN	1	0: Disable buck-boost output **1: Enable buck-boost output**	
5	EN_PD	1	EN Input Pulldown Resistor Enable Setting 0: Disable **1: Enable**	
4	POK_POL	1	0: Active low **1: Active high**	
3:0	RESERVED	0000		

V_{OUT}

Output Voltage Setting Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x23/0x28		
0x04	R/W					
BIT	**NAME**	**POR**	**DESCRIPTION**			
7	RESERVED	0				
6:0	VOUT [6:0]	010 0011/ 010 1000	Buck-Boost Output Voltage Table			
			0x00 = 2.60V	0x20 = 3.24V	0x40 = 3.88V	0x60 = 4.52V
			0x01 = 2.62V	0x21 = 3.26V	0x41 = 3.90V	0x61 = 4.54V
			0x02 = 2.64V	0x22 = 3.28V	0x42 = 3.92V	0x62 = 4.56V
			0x03 = 2.66V	**0x23 = 3.30V**	0x43 = 3.94V	0x63 = 4.58V
			0x04 = 2.68V	0x24 = 3.32V	0x44 = 3.96V	0x64 = 4.60V
			0x05 = 2.70V	0x25 = 3.34V	0x45 = 3.98V	0x65 = 4.62V
			0x06 = 2.72V	0x26 = 3.36V	0x46 = 4.00V	0x66 = 4.64V
			0x07 = 2.74V	0x27 = 3.38V	0x47 = 4.02V	0x67 = 4.66V
			0x08 = 2.76V	**0x28 = 3.40V**	0x48 = 4.04V	0x68 = 4.68V
			0x09 = 2.78V	0x29 = 3.42V	0x49 = 4.06V	0x69 = 4.70V
			0x0A = 2.80V	0x2A = 3.44V	0x4A = 4.08V	0x6A = 4.72V
			0x0B = 2.82V	0x2B = 3.46V	0x4B = 4.10V	0x6B = 4.74V
			0x0C = 2.84V	0x2C = 3.48V	0x4C = 4.12V	0x6C = 4.76V
			0x0D = 2.86V	0x2D = 3.50V	0x4D = 4.14V	0x6D = 4.78V
			0x0E = 2.88V	0x2E = 3.52V	0x4E = 4.16V	0x6E = 4.80V
			0x0F = 2.90V	0x2F = 3.54V	0x4F = 4.18V	0x6F = 4.82V
			0x10 = 2.92V	0x30 = 3.56V	0x50 = 4.20V	0x70 = 4.84V
			0x11 = 2.94V	0x31 = 3.58V	0x51 = 4.22V	0x71 = 4.86V
			0x12 = 2.96V	0x32 = 3.60V	0x52 = 4.24V	0x72 = 4.88V
			0x13 = 2.98V	0x33 = 3.62V	0x53 = 4.26V	0x73 = 4.90V
			0x14 = 3.00V	0x34 = 3.64V	0x54 = 4.28V	0x74 = 4.92V
			0x15 = 3.02V	0x35 = 3.66V	0x55 = 4.30V	0x75 = 4.94V
			0x16 = 3.04V	0x36 = 3.68V	0x56 = 4.32V	0x76 = 4.96V
			0x17 = 3.06V	0x37 = 3.70V	0x57 = 4.34V	0x77 = 4.98V
			0x18 = 3.08V	0x38 = 3.72V	0x58 = 4.36V	0x78 = 5.00V
			0x19 = 3.10V	0x39 = 3.74V	0x59 = 4.38V	0x79 = 5.02V
			0x1A = 3.12V	0x3A = 3.76V	0x5A = 4.40V	0x7A = 5.04V
			0x1B = 3.14V	0x3B = 3.78V	0x5B = 4.42V	0x7B = 5.06V
			0x1C = 3.16V	0x3C = 3.80V	0x5C = 4.44V	0x7C = 5.08V
			0x1D = 3.18V	0x3D = 3.82V	0x5D = 4.46V	0x7D = 5.10V
			0x1E = 3.20V	0x3E = 3.84V	0x5E = 4.48V	0x7E = 5.12V
			0x1F = 3.22V	0x3F = 3.86V	0x5F = 4.50V	0x7F = 5.14V

Ordering Information

PART	DEFAULT V_{OUT}	PIN-PACKAGE
MAX77813EWP33+T	3.3V	20-Bump (5 x 4) 0.4mm Pitch
MAX77813EWP+T	3.4V	20-Bump (5 x 4) 0.4mm Pitch

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/18	Initial release	—

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