MAX14746/MAX14747

USB Detection with Smart Power Selector Li+ Chargers

General Description

The MAX14746/MAX14747 are a series of USB charger detectors with an integrated Smart Power Selector™ linear charger solutions that provide a single-chip solution for charging and charger detection.

The MAX14746/MAX14747 charger detectors are compliant to USB Battery Charger Detection Rev 1.2* and capable of detecting multiple USB battery-charging methods, including Standard Downstream Ports (SDP), Charging Downstream Ports (CDP), and Dedicated Charger Ports (DCP). The devices also detect common proprietary charge adapters, including those from Apple.

The MAX14746/MAX14747 battery chargers feature Smart Power Selector operation, allowing operation with dead or no battery present. The devices limit USB V_{BUS} current based on the detect charger source type. If the charger power source is unable to supply the entire system load, the smart-power control circuit supplements the system load with current from the battery.

The devices protect against overvoltage faults up to 28V.

This series of USB charger detectors are available with several options, with slight variations in, for example, power-up states. These variations are noted throughout this data sheet.

There are five options available, with slight variations in, for example, power-up states (see Ordering Information). The devices are available in a 25-ball, 0.4mm pitch wafer-level package (WLP), and are specified over the -40°C to +85°C extended temperature range.

Applications

- Portable Consumer Devices
- Portable Digital Cameras
- Portable Digital Video Cameras
- Portable Industrial Devices

**Except DCD timeout extended from 900ms to 2s for the MAX14746/MAX14747.*

Smart Power Selector™ is a trademark of Maxim Integrated Products, Inc.

Benefits and Features

- Flexible System Design to Operate with Any USB Charger Source
  - Compliant to USB Battery Charger Rev 1.2 Specification*
  - Supports Proprietary USB Charging Sources, Including Apple
  - D+/D- Bias Voltage Supported
- Easy to Implement Li+ Battery Charging
  - Smart Power Selector
  - Fully Compliant with Dead Battery/Weak Battery Charging According to USB 2.0 Specification
  - JEITA Charge Protection
  - Thermal Protection
  - Internal USB D+/D- Switch to Manage Connection
- Integrates High Level of Protection
  - 28V Tolerant Input on VB
  - ±15kV Human Body Model ESD Protection on CDP and CDN

***Ordering Information* appears at end of data sheet.**

19-8036; Rev 1; 1/17

maxim integrated™

Absolute Maximum Ratings

(All voltages referenced to GND.)
BAT, $\overline{INT}$, THM, LED, UOK1, $\overline{CTYP}$, IDEF, FSUS, TDN, TDP, CDN, CDP, SYS, SCL, SDA.....-0.3V to +6V
UOK2/EXT.....V_{SYS} + 0.3V
SFOUT, CAP .....-0.3V to min ((V_{VB} + 0.3V), +6V)
VB.....-0.3V to +30V
NVP .....-0.3V to (V_{VB} + 0.3V)
Continuous Current into VB, BAT, SYS.....±3A
Continuous Current into any Other Terminal.....±100mA
Continuous Power Dissipation (T_A = +70°C)
WLP (derate 19.2mW/°C above +70°C) 1536mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Reflow Temperature .....+260°C

Package Thermal Characteristics (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....52°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{VB} = 5.0V, V_{BAT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.6V, V_{VB} = 5.0V, V_{SYS} = V_{SYS_REG}, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CHARACTERISTICS						
VB Input Voltage Range	V_{VB}		0		28	V
V_{BAT} Input Voltage Range	V_{BAT}		0		5.5	V
VB Detection Threshold	V_{VBDET}	V_{VB} rising	3.8	3.9	4.1	V
		V_{VB} falling	3.0	3.1	3.2	
VB Overvoltage Threshold	V_{VBOV}	V_{VB} rising	7.2	7.5	7.8	V
VB Overvoltage Hysteresis	V_{VBOV_HYS}			200		mV
VB Valid Trip Point	V_{VB_TRIP}		30	145	290	mV
VB Valid Trip Point Hysteresis	$V_{VB\_TP\_HYS}$			275		mV
VB Charger-Detection-Active Supply Current	I_{B_CDETON}	V_{BAT} = 0V, I_{SYS} = 0mA charger detection active, analog switch open			2.5	mA
VB Charger-Detection-Idle Supply Current	$I_{B\_CDCIDLE}$	V_{BAT} = 0V, I_{SYS} = 0mA charger detection idle, analog switch closed			2	mA
V_{CCINT} UVLO Threshold	V_{UVLO}	V_{CCINT} rising (Note 3)	1.6	2.2	2.6	V
V_{CCINT} UVLO Hysteresis	V_{UVLO_HYS}	(Note 3)		50		mV
BAT Overvoltage Threshold	V_{BATOV}	V_{BAT} rising, VB not connected	4.8	5.15	5.7	V
BAT Overvoltage Hysteresis	V_{BATOV_HYS}			100		mV
BAT UVLO Threshold	V_{BAT_UVLO}	V_{BAT} rising (Note 4)	1.9	2.05	2.2	V
BAT UVLO Hysteresis	V_{BAT_UVLOH}			50		mV

Electrical Characteristics (continued)

(V_{VB} = 5.0V, V_{BAT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.6V, V_{VB} = 5.0V, V_{SYS} = V_{SYS_REG}, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BAT Supply Current With VB	I_{BAT_NOCHG}	V_{BAT} = 4.2V, VB connected, charger disabled			4	8	µA
BAT Supply Current No VB	I_{BAT_NOVB}	V_{BAT} = 4.2V, VB not connected			6	11	µA
CAP Regulator Voltage	V_{CAP}	V_{VB} = 5V		3.9	4.2	4.7	V
SFOUT Regulator Voltage	V_{SFOUT}	V_{VB} = 6.0V, I_{SFOUT} = 0mA		5.0	5.25	5.5	V
		V_{VB} = 5.0V, I_{SFOUT} = 15mA			4.9		
SFOUT Overvoltage Protection Voltage	V_{SFOUT_OVP}	(Note 5)			17		V
NVP Clamp Voltage	V_{NVP}	Measured between VB and NVP, V_{VB} > 10V		5	7	10	V
NVP Resistance	R_{NVP}	V_{VB} < 5V		120	200	300	Ω
THERMAL PROTECTION							
Thermal Shutdown Threshold	T_{SHDN_LIM}	(Note 6)			150		°C
Current Reduce Thermal Threshold	T_{CHG_LIM}	(Note 7)			120		°C
VB-TO-SYS PATH							
SYS Regulation Voltage	V_{SYS_REG}	I_{SYS} = 5mA	MAX14746	V_{BAT_REG} + 0.14	V_{BAT_REG} + 0.2	V_{BAT_REG} + 0.26	V
			MAX14747		4.8		
VB-to-SYS Voltage Drop	V_{VB_SYS}				40		mV
VB-to-SYS On-Resistance	R_{VB_SYS}	V_{VB} = 4.4V, I_{SYS} = 400mA			160	350	mΩ
Soft-Start Input Current Time	$t_{SS\_VB\_SYS}$				1		ms
USB Input Current Limit	I_{LIMIT}	FSUS = 1			0		mA
		IDEF = 0, IBusLim = 1, IBusDetSw[1:0] = 11, ILimSet[2:0] = 000			96.5		
		IDEF = 0, IBusLim = 1, IBusDetSw[1:0] = 11, ILimSet[2:0] = 001			475	500	
		IDEF = 0, IBusLim = 1, IBusDetSw[1:0] = 11, ILimSet[2:0] = 010			633		
		IDEF = 0, IBusLim = 1, IBusDetSw[1:0] = 11, ILimSet[2:0] = 011			737		
		IDEF = 0, IBusLim = 1, IBusDetSw[1:0] = 11, ILimSet[2:0] = 100			944		
		IDEF = 0, IBusLim = 1, IBusDetSw[1:0] = 11, ILimSet[2:0] = 101			1048		
		IDEF = 0, IBusLim = 1, IBusDetSw[1:0] = 11, ILimSet[2:0] = 110			1570		
		IDEF = 0, IBusLim = 1, IBusDetSw[1:0] = 11, ILimSet[2:0] = 111			1885		

Electrical Characteristics (continued)

(V_{VB} = 5.0V, V_{BAT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.6V, V_{VB} = 5.0V, V_{SYS} = V_{SYS_REG}, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGER PATH						
BAT to SYS On-Resistance	R_{BAT_SYS}	V_{BAT} = 5V, I_{BAT} = 400mA		40	80	mΩ
		V_{BAT} = 1.9V, I_{BAT} = 100mA		83		
BAT to SYS Switch-On Threshold	$V_{BAT\_SYS\_ON}$	V_{SYS} falling	10	22	35	mV
BAT to SYS Switch-Off Threshold	$V_{BAT\_SYS\_OFF}$	V_{SYS} rising	-3	-1.5	0	mV
SYS Charger Current-Limiting Threshold Voltage	V_{SYS_LIM}	SysMin[2:0] = 000, V_{BAT} > 3.6V		V_{BAT} + 0.1		
		SysMin[2:0] = 000, V_{BAT} < 3.4V		3.6		
		SysMin[2:0] = 001, V_{BAT} < 3.4V		3.7		
		SysMin[2:0] = 010, V_{BAT} < 3.4V		3.8		
		SysMin[2:0] = 011, V_{BAT} < 3.4V		3.9		
		SysMin[2:0] =100, V_{BAT} < 3.4V	3.86	4	4.14	
		SysMin[2:0] =101, V_{BAT} < 3.4V		4.1		
		SysMin[2:0] =110, V_{BAT} < 3.4V		4.2		
		SysMin[2:0] =111, V_{BAT} < 3.4V		4.3		
Charger Current Soft-Start Time				1		ms
BATTERY CHARGER LEVELS						
Precharge Current	I_{PCHG}	IPChg[1:0] = 00		30		mA
		IPChg[1:0] = 01		50		
		IPChg[1:0] = 10		70		
		PChg[1:0] = 11		100		
Prequalification Threshold	V_{BAT_PCHG}	VPChg = 0, VPChgLow[1:0] = 00, V_{BAT} rising		2.15		V
		VPChg = 0, VPChgLow[1:0] = 01, V_{BAT} rising	2.15	2.25	2.35	
		VPChg = 0, VPChgLow[1:0] = 10, V_{BAT} rising		2.35		
		VPChg = 0, VPChgLow[1:0] = 11, V_{BAT} rising		2.45		
		VPChg = 1, VPChgHigh[1:0] = 00, V_{BAT} rising		2.7		
		VPChg = 1, VPChgHigh[1:0] = 01, V_{BAT} rising	2.70	2.80	2.90	
		VPChg = 1, VPChgHigh[1:0] = 10, V_{BAT} rising		2.9		
		VPChg = 1, VPChgHigh[1:0] = 11, V_{BAT} rising		3		
Prequalification Threshold Hysteresis	$V_{BAT\_PCHG\_HYS}$			100		mV

Electrical Characteristics (continued)

(V_{VB} = 5.0V, V_{BAT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.6V, V_{VB} = 5.0V, V_{SYS} = V_{SYS_REG}, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BAT Charge Current Set Range	I_{FCHG}	IFChg[2:0] = 000		700		mA
		IFChg[2:0] = 001		300		
		IFChg[2:0] = 010	180	200	220	
		IFChg[2:0] = 011		600		
		IFChg[2:0] = 100		800		
		IFChg[2:0] = 101		900		
		IFChg[2:0] = 110		350		
		IFChg[2:0] = 111		450		
Charge Done Qualification	I_{CHG_DONE}	ChgDone[2:0] = 000		10		mA
		ChgDone[2:0] = 001		20		
		ChgDone[2:0] = 010		40		
		ChgDone[2:0] = 010, TA = 0°C to +60°C	30		50	
		ChgDone[2:0] = 011		50		
		ChgDone[2:0] = 100		60		
		ChgDone[2:0] = 101		80		
		ChgDone[2:0] = 110		100		
		ChgDone[2:0] = 111		120		
BAT Regulation Voltage	V_{BAT_REG}	BatRegSel = 0, BatRegLow[1:0] = “00”		4.05		V
		BatRegSel = 0, BatRegLow[1:0] = “01”		4.1		
		BatRegSel = 0, BatRegLow[1:0] = “10”		4.15		
		BatRegSel = 0, BatRegLow[1:0] = “11”, T_A=+25°C	4.179	4.2	4.221	
		BatRegSel = 0, BatRegLow[1:0] = “11”, T_A=-40°C to +85°C	4.158	4.2	4.242	
		BatRegSel = 1, BatRegHi[2:0] = “000”		4.25		
		BatRegSel = 1, BatRegHi[2:0] = “001”		4.3		
		BatRegSel = 1, BatRegHi[2:0] = “010”		4.35		
		BatRegSel = 1, BatRegHi[2:0] = “011”		4.4		
		BatRegSel = 1, BatRegHi[2:0] = “100”		4.45		
		BatRegSel = 1, BatRegHi[2:0] = “101”		4.5		
		BatRegSel = 1, BatRegHi[2:0] = “110”		4.55		
		BatRegSel = 1, BatRegHi[2:0] = “111”		4.6		

Electrical Characteristics (continued)

(V_{VB} = 5.0V, V_{BAT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.6V, V_{VB} = 5.0V, V_{SYS} = V_{SYS_REG}, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BAT Recharge Threshold	V_{BAT_RECHG}	BatReChg[1:0] = 00		50		mV
		BatReChg[1:0] = 01		100		
		BatReChg[1:0] = 10		150		
		BatReChg[1:0] = 11		200		
BATTERY CHARGER TIMING						
Maximum Prequalification Time	t_{PCHG}	PChgTmr[1:0] = 00		30		Minutes
		PChgTmr[1:0] = 01		60		
		PChgTmr[1:0] = 10		120		
		PChgTmr[1:0] = 11		240		
Maximum Fast-Charge Time	t_{FCHG}	FChgTmr[1:0] = 00		75		Minutes
		FChgTmr[1:0] = 01		150		
		FChgTmr[1:0] = 10		300		
		FChgTmr[1:0] = 11		600		
Maintain-Charge Time	t_{TOCHG}	MtChgTmr[1:0] = 00		30		Minutes
		MtChgTmr[1:0] = 01		15		
		MtChgTmr[1:0] = 10		0		
		MtChgTmr[1:0] = 11		60		
Charge-Timer Accuracy	OSC		-10		+10	%
Charge-Timer Extend Threshold	I_{FC_HALF}	Charge current reduced due to overcurrent or overtemperature condition (Note 10)		50		$\%I_{FCHG}$
Charge-Timer Suspend Threshold	I_{FC_FIFTH}	Charge current reduced due to overcurrent or overtemperature condition (Note 10)		20		$\%I_{FCHG}$
BATTERY DETECTION						
V_{VB} Rising to Battery Detection Valid Delay	t_{BUS_BATDET}	BatDetCntl = 0, $V_{BAT} > V_{BAT\_UVLO}$		61		ms
		BatDetCntl = 0, $V_{BAT} < V_{BAT\_UVLO}$		1.031		s
		BatDetCntl = 1		46		ms
V_{BAT} Falling to BatDet Update Delay	t_{BATDET_F}	BatDetCntl = 0		1.015		s
		BatDetCntl = 1		15		ms
V_{BAT} Rising to BatDet Update Delay	t_{BATDET_R}	BatDetCntl = 0, $V_{BAT} > V_{BAT\_UVLO}$		1.03		s
		BatDetCntl = 0, $V_{BAT} < V_{BAT\_UVLO}$		1.015		
		BatDetCntl = 1		15		ms

Electrical Characteristics (continued)

(V_{VB} = 5.0V, V_{BAT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.6V, V_{VB} = 5.0V, V_{SYS} = V_{SYS_REG}, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
JEITA BATTERY PACK MONITOR AND NTC DETECTION							
THM Hot Threshold	T_4	V_{THM} falling	MAX14746		23.8		$\%V_{CAP}$
			MAX14747		19		
THM Warm Threshold	T_3	V_{THM} falling	MAX14746		33.7		$\%V_{CAP}$
			MAX14747		30		
THM Cool Threshold	T_2	V_{THM} rising	MAX14746		63.3		$\%V_{CAP}$
			MAX14747		66.75		
THM Cold Threshold	T_1	V_{THM} rising	MAX14746		72.3		$\%V_{CAP}$
			MAX14747		77.2		
THM Disable Threshold	T_{HMDIS}	V_{THM} rising			96.6		$\%V_{CAP}$
THM Threshold Hysteresis	T_{HMHYS}				60		mV
THM Input Leakage Current	I_{LTHM}			-1		+1	µA
THM Detection Time	t_{THM}				15		ms
CHARGER STATUS OUTPUT (LED)							
Output Logic-Low Voltage	V_{OLED}	I_{SINK} = 10mA			35	100	mV
Temperature Suspend Mode Blink Period	t_{TSUS}	Blinking with 50% duty cycle			1.5		s
Timeout Mode Blink Period	t_{TIMOUT}	Blinking with 50% duty cycle			0.15		s
Pulse Time for Fresh Battery Insertion					1		s
IMPEDANCE-MODE BATTERY DETECTION							
Discharge Current	I_{DIS}	V_{BAT} = 3.6V		6	10	14	mA
Replace Current	I_{RPL}	V_{BAT} = 3.6V, V_{SYS} > 4.0V		6	10	14	mA
Test Current Mismatch	I_{DR_MIS}			-15		+15	%
Discharge Replace Time	t_{DIS_RPL}	V_{BAT} = 3.6V			15		ms

Electrical Characteristics (continued)

(V_{VB} = 5.0V, V_{BAT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.6V, V_{VB} = 5.0V, V_{SYS} = V_{SYS_REG}, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGER DETECTION						
V_{DP_SRC} Voltage	V_{DP_SRC}	I_{LOAD} = 0 to 200µA	0.5	0.6	0.7	V
V_{DAT_REF} Voltage	V_{DAT_REF}		0.25	0.3	0.35	V
V_{LGC} Voltage	V_{LGC}		1.15	1.24	1.5	V
I_{DM_SINK} Current	I_{DM_SINK}	V_{OUT} = 0.15V to 3.6V	50	80	110	µA
I_{DP_SRC} Current	I_{DP_SRC}	V_{OUT} = 0V to 2.5V	5.5	8.4	10	µA
R_{DM_DWN}	R_{DM_DWN}		14.25	20	24.8	kΩ
I_{WEAK} Current	I_{WEAK}		0.01	0.1	0.3	µA
25% Resistor-Divider Ratio	R_{25}		22.5	25	27.5	%
47% Resistor-Divider Ratio	R_{47}		43.3	47	51.7	%
71% Resistor-Divider Ratio	R_{71}		69.5	71.6	73.5	%
USB Charger Detect Time	t_{DPSRC_ON}		40		60	ms
V_{BUS} Debounce Time	t_{MDEB}		20	30	40	ms
DCD Debounce	t_{DCD_DEB}		36	40	44	ms
DCD Timeout	t_{DCD_TO}			2000		ms
USB ANALOG SWITCH PERFORMANCE (TDN/TDP)						
Analog-Signal Range	V_{TDN} V_{TDP}		0		V_{CCINT}	V
On-Resistance	R_{ONUSB}	V_{BAT} = 3.0V, I_{CDN}, I_{CDP} = 10mA, V_{CDN},V_{CDP} = 0 to 3.0V		3	6	Ω
On-Resistance Match Between Channels	DR_{ONUSB}	V_{BAT} = 3.0V, I_{CDN}, I_{CDP} = 10mA, V_{CDN},V_{CDP} = 400mV			0.5	Ω
On-Resistance Flatness	$R_{FLATUSB}$	V_{BAT} = 3.0V, I_{CDN}, I_{CDP} = 10mA, V_{CDN},V_{CDP} = 0 to 3V		0.3	1	Ω
Off-Leakage Current	I_{LUSB_OFF}	Switch open, V_{TDN}/V_{TDP} = 0.3V/2.5V, V_{CDP}/V_{CDN} = 2.5V/0.3V	-360		+360	nA
On-Leakage Current	I_{LUSB_ON}	Switch closed, V_{TDN}/V_{TDP}/V_{CDN}/V_{CDP} = 0.3V/2.5V	-360		+360	nA
Analog Switch Turn-On Time	t_{ON}	I²C stop to switch on, R_L = 50Ω		0.5	1	ms
Analog Switch Turn-Off Time	t_{OFF}	I²C stop to switch on, R_L = 50Ω		0.1	1	ms
On-Capacitance	C_{ON}	V_{IN} = 0.5V_{P-P} DC = 0V, f = 240MHz		6		pF
Off-Capacitance	C_{OFF}	V_{IN} = 0.5V_{P-P} DC = 0V, f = 240MHz		3.5		pF

Electrical Characteristics (continued)

(V_{VB} = 5.0V, V_{BAT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.6V, V_{VB} = 5.0V, V_{SYS} = V_{SYS_REG}, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Off-Isolation	V_{ISO}	R_S = R_L = 50Ω, f = 20kHz, V_{IN} = 0.5V_{P-P}		-60		dB
DIGITAL INPUTS/OUTPUTS (IDEF, $\overline{CTYP}$, $\overline{INT}$, UOK_, FSUS)						
Input Logic High-Voltage	V_{IH}		1.4			V
Input Logic Low-Voltage	V_{IL}				0.4	V
Leakage Current	I_{LEAK}	$\overline{CTYP}$, $\overline{INT}$, UOK_ only	-250		+250	nA
Open-Drain Output Logic-Low	V_{ODOL}				0.4	V
STARTUP TIMINGS						
VB to SYS Rise		IBusLim = 0, FSUSMsK = 0, IDEF = 0		205		ms
VB to SFOUT Rise		SFoutAsrt = 0		205		ms
VB to $\overline{CTYP}$ Falling Edge				205		ms
$\overline{CTYP}$ to UOK1 Falling Edge	$t_{SYS\_UOK1\_F}$			5.5		ms
UOK1 to UOK2 Falling Edge Delay	t_{UOK1_UOK2}	If UOK2 option enabled		400		ms
I²C TIMING SPECIFICATIONS (FIGURE 1)						
I²C Maximum Clock Frequency	f_{SCL}			400		kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
Repeated Start Condition Setup Time	$t_{SU:STA}$		0.6			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Valid to SCL Rise Time	$t_{SU:DAT}$	Write-setup time	100			ns
Data Hold Time to SCL Fall	$t_{HD:DAT}$	Write-hold time	0			ns
SCL, SDA Spike Suppression	t_{SP}	Duration of spike on SCL and SDA that is not detected as a valid edge		50		ns
PROTECTION SPECIFICATIONS						
ESD Protection, CDP/CDN		Human Body Model		±15		kV
		IEC61000-4-2 Air Gap		±4		
		IEC61000-4-2 Contact		±5		
ESD Protection, All Other Pins		Human Body Model		±2		kV

Electrical Characteristics (continued)

Note 2: All units are production tested at +25°C. Specifications over temperature are guaranteed by design.
Note 3: V_{CCINT} = V_{CAP} (if CAP is present) or V_{BAT} (if CAP is not present).
Note 4: Threshold is valid when V_{VBDET} < V_{VB} < V_{VBOV}. When V_{SYS} < V_{BAT_UVLO}, the BAT-SYS switch opens and BAT is connected to SYS through a diode.
Note 5: When V_{VB} > V_{SFOUT_OVP}, SFOUT LDO turns off.
Note 6: When the die temperature exceeds T_{SFOUT_TLIM}, SFOUT regulator and SYS limiter turns off. V_{SYS} is supplied by V_{BAT}.
Note 7: When the die temperature exceeds T_{CHG_LIM}, charger current starts to reduce.
Note 8: V_{SYS_LIM} is the SYS voltage below which the charger starts to limit the charging current.
Note 9: When V_{SYS} drops below V_{SYS_HLD}, the battery charger does not move to the maintain charge state.
Note 10: The charge timer extend threshold is the charge current level below which the charge timer clock runs at half speed. The charge timer suspend threshold is the charge current level below which the charge timer clock is paused.

Timing Diagram

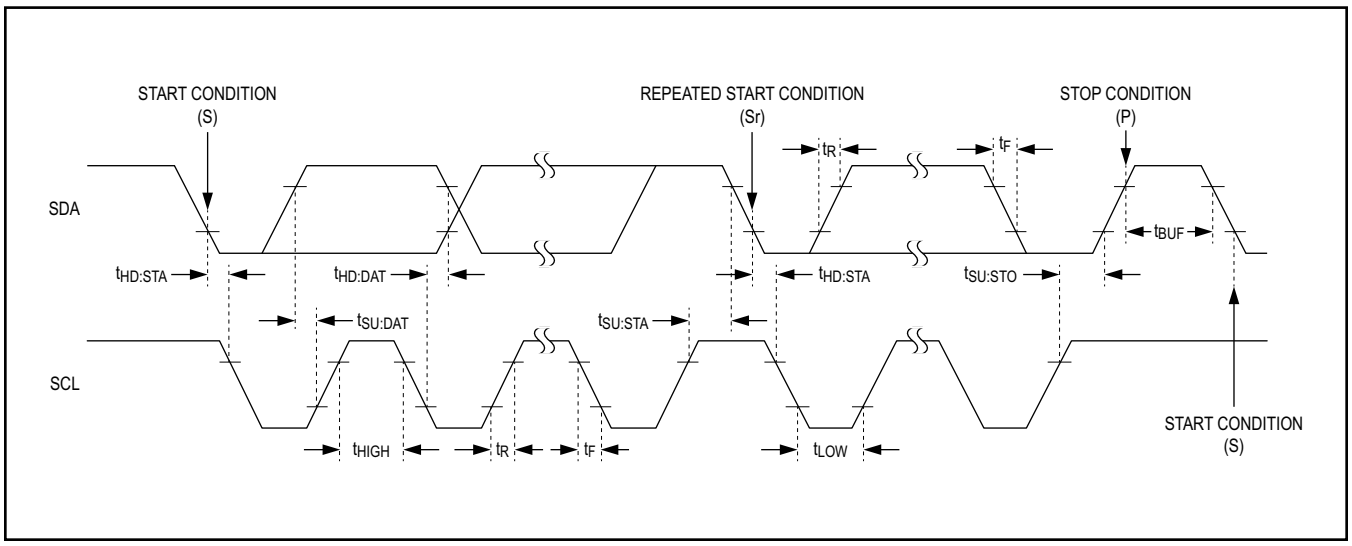
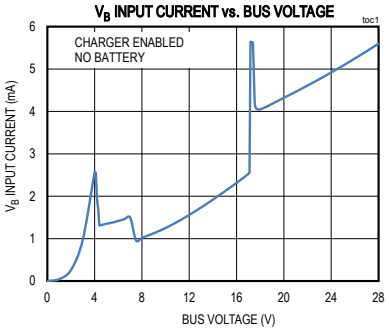
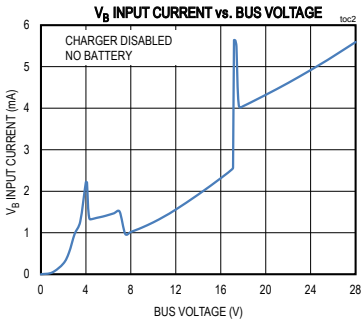


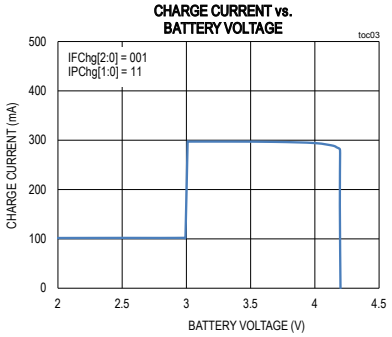
Figure 1. I²C Timing Diagram

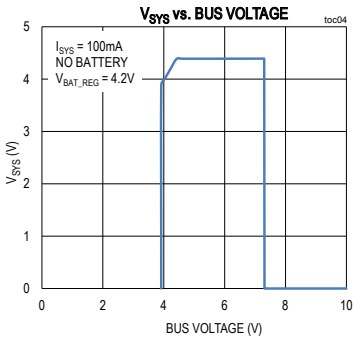
Typical Operating Characteristics

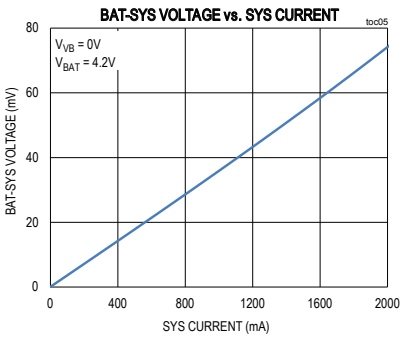
(V_{BAT} = 3.6V, V_{VB} = 5V, T_A = +25°C, unless otherwise noted.)

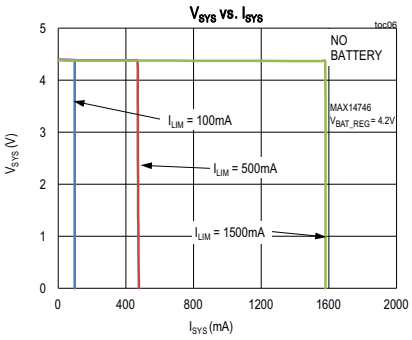


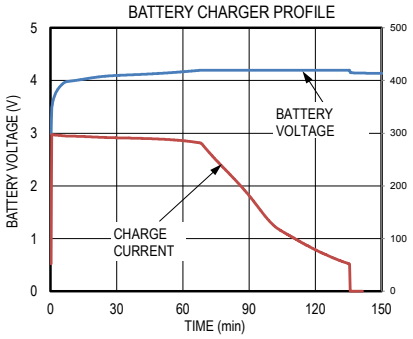


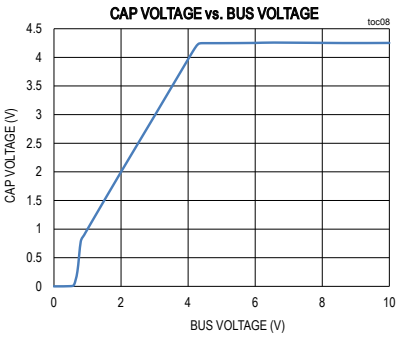






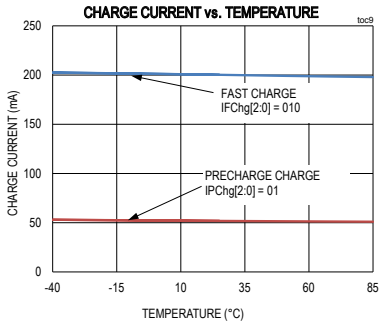


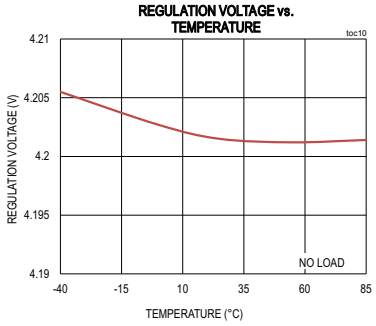


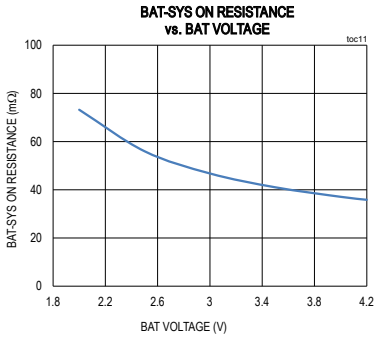


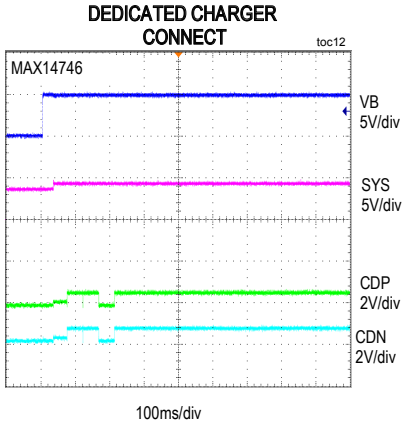
Typical Operating Characteristics (continued)

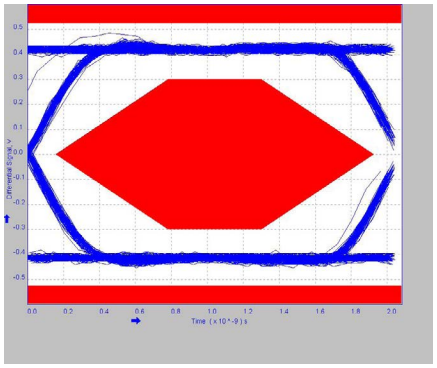
(V_{BAT} = 3.6V, V_{VB} = 5V, T_A = +25°C, unless otherwise noted.)

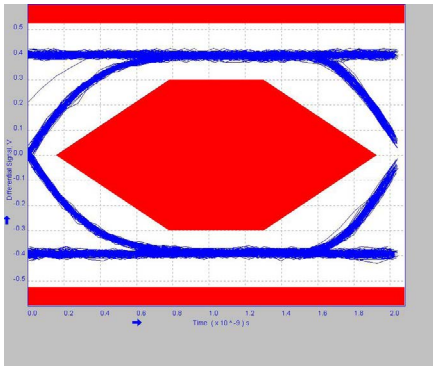


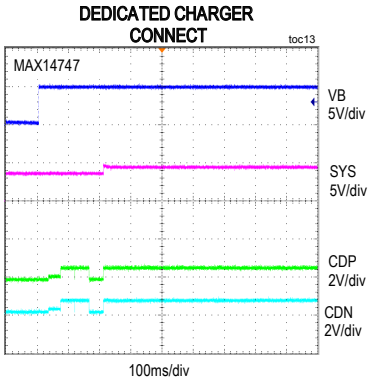


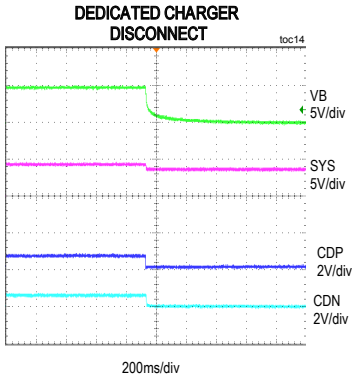








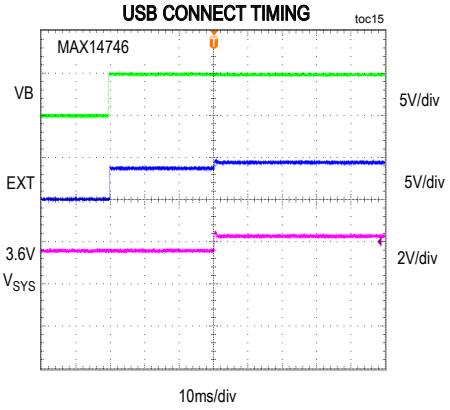




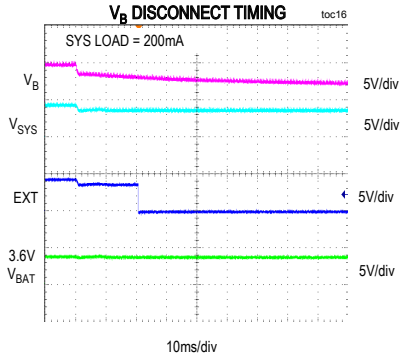
Typical Operating Characteristics (continued)

(V_{BAT} = 3.6V, V_{VB} = 5V, T_A = +25°C, unless otherwise noted.)

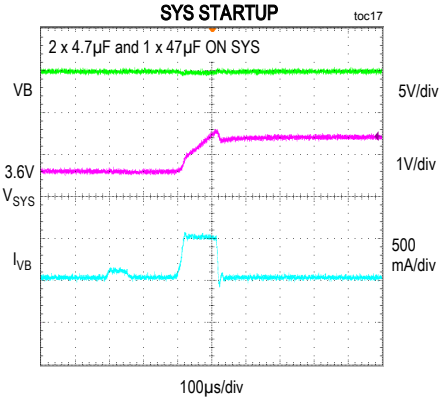
USB CONNECT TIMING



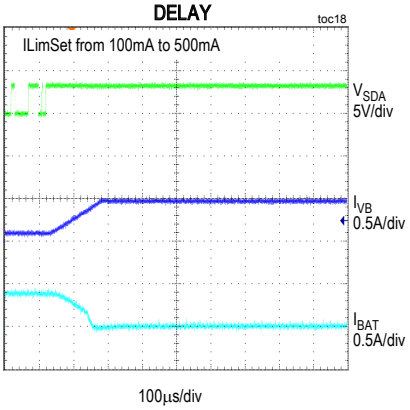
V_B DISCONNECT TIMING



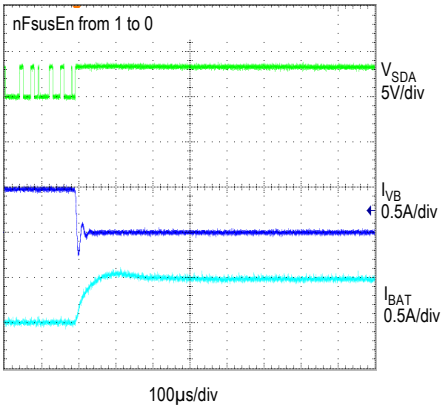
SYS STARTUP



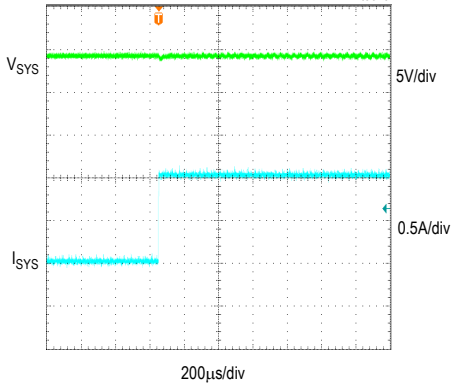
LIMITER TURN-ON DELAY



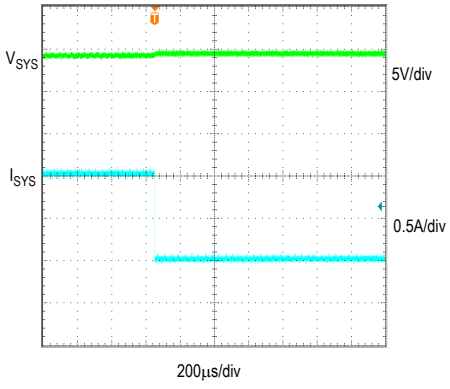
LIMITER TURN-OFF DELAY



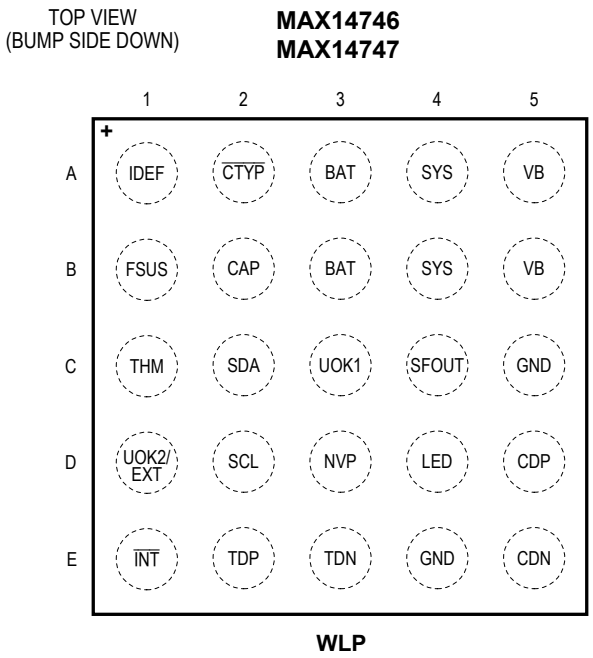
SYS LOAD TRANSIENT RISING



SYS LOAD TRANSIENT FALLING



Bump Configuration



WLP

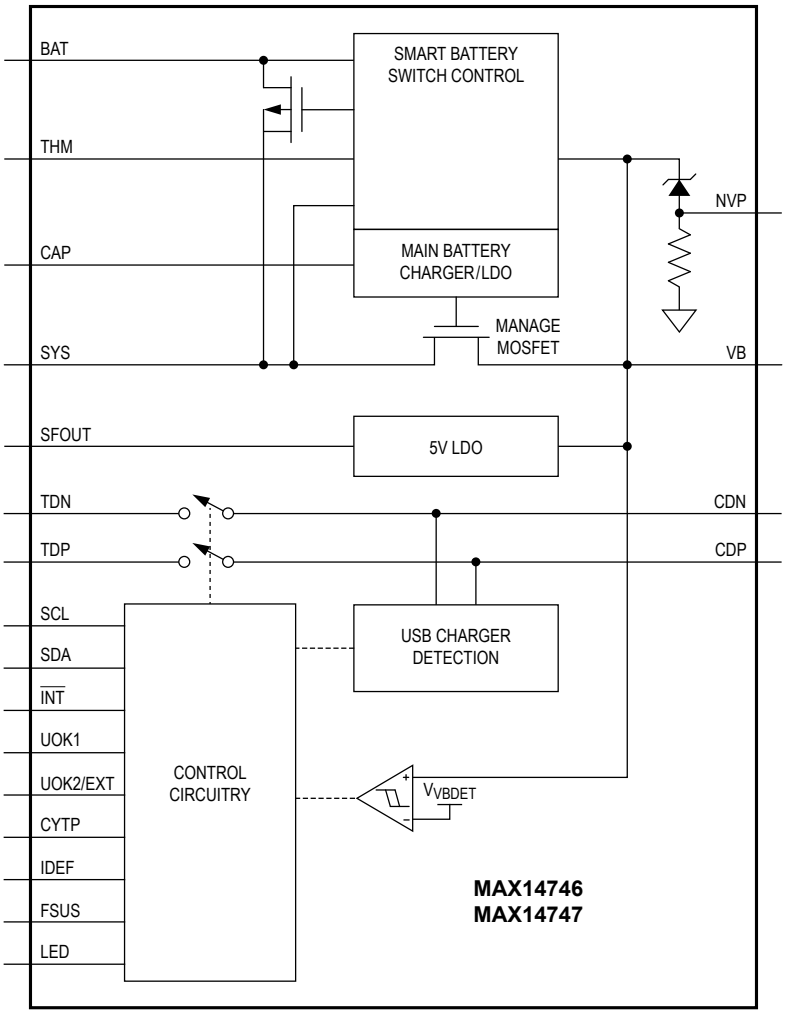
Bump Descriptions

BUMP	NAME	FUNCTION
A1	IDEF	Current-Limit Setting Input. IDEF has an internal 470kΩ pulldown resistor to GND. IDEF is only active if FSUSMsk bit is set to 0 and FSUS is LOW 0 = Input current limit determined by I²C settings (IBusLim, ILimSet, IBusDetSw bits) 1 = Input current limit set to 100mA
A2	$\overline{\text{CTYP}}$	Charger Type Output. $\overline{\text{CTYP}}$ is an open-drain output that asserts when DCP, CDP, or Apple 2A adapter is detected.
A3, B3	BAT	Battery Connection. Connect a single-cell Li+ battery from BAT to GND. Connect a capacitor from BAT to GND with a minimum value of 10µF and a maximum value of 30µF.
A4, B4	SYS	System Load Connection. Connect SYS to the system load. Bypass SYS with a 10µF low-ESR ceramic capacitor to GND as close as possible to the device. Connect 50µF additional capacitance to GND away from the device.
A5, B5	VB	USB V_{BUS} Input. VB is the input for the overvoltage protector. VB is monitored to detect the presence of a USB input power supply. Bypass VB with a 1µF ceramic capacitor to GND as close as possible to the device.
B1	FSUS	Force-Suspend Enable Input. FSUS is only active if the FSUSMsk bit is set to 0. FSUS has a 470kΩ pulldown resistor to GND. 0 = Current limit determined by IDEF/I²C configuration 1 = Input current limit is forced to 0

Bump Description (continued)

BUMP	NAME	FUNCTION
B2	CAP	Internal LDO Bypass Connection. Connect a 1µF ceramic capacitor from CAP to GND as close as possible to the device. Connect the pullup resistor for the battery thermistor output (THM) to CAP. Ensure that the total load current out of CAP is less than 2mA.
C1	THM	Battery Temperature Thermistor Measurement Input
C2	SDA	I²C Serial Data Input/Output. Connect an external pullup resistor on SDA to the logic supply voltage.
C3	UOK1	SYS Voltage Valid and Battery Detect Output. UOK1 is an open-drain output.
C4	SFOUT	Protected LDO Output. SFOUT is powered from VB. Bypass SFOUT with a 1µF ceramic capacitor to GND as close as possible to the device. SFOUT can power the on-board USB 2.0 Hi-Speed host.
C5, E4	GND	Ground
D1	UOK2/EXT	UOK2: Delayed SYS Voltage Valid and Battery-Detect Output. UOK2 is an open-drain output. EXT: Push-Pull Output Control for External SYS-BAT pMOS Switch. Output pulled high to BAT when the charger is not present.
D2	SCL	I²C Serial Clock Input. Connect an external pullup resistor on SCL to the logic supply voltage.
D3	NVP	Gate Bias and Protection for External PFET. NVP protects VB from negative voltages. Leave unconnected if not used.
D4	LED	Charging Fault Indicator. LED is an open-drain output that indicates a battery charging fault. When a JEITA temperature fault is detected, LED is pulsed at 50% duty cycle with a period of 1.5s. When a charge timer fault is detected, or the BAT overvoltage threshold (V_{BATOV}) is exceeded, LED is pulsed at 50% duty cycle with a period of 0.15s. Connect LED to GND if unused.
D5	CDP	USB Connector D+ Input
E1	INT	Interrupt Output. $\overline{INT}$ is an open-drain output that asserts whenever an unmasked interrupt occurs. Connect an external pullup resistor on $\overline{INT}$ to the logic supply voltage.
E2	TDP	USB Transceiver D+ Connection. Connect TDP to device microprocessor USB transceiver D+ line.
E3	TDN	USB Transceiver D- Connection. Connect TDN to device microprocessor USB transceiver D- line.
E5	CDN	USB Connector D- Input

Functional Diagram



Detailed Description

The MAX14746/MAX14747 charger detector solutions integrate a smart-power selector with a linear charger that allows charging a Li+ battery and a powering system to load off the same USB power source. When the USB power source is not present or cannot provide enough power, the Li+ battery helps power the system. The devices protect against voltage faults and transients on VB up to 28V without interrupting operation.

The MAX14746/MAX14747 are compliant to USB Battery Charger Detection Rev 1.2* as well, as special chargers that bias the D+/D- lines. The devices limit VB input current based on the type of charging device that is detected and two digital inputs (IDEF and FSUS).

The devices monitor overcurrent and overtemperature faults and automatically manages the charger. Configurable interrupts and status information allow the system microcontroller to intervene.

Negative Voltage Protection

The MAX14746/MAX14747 feature a gate protection circuit for an external PFET that protects against negative voltages on V_{BUS}. The NVP output has a resistor to GND and a voltage clamp for the gate of the PFET. The voltage clamp limits the gate-to-source voltage to 7.0V (typ) when the V_{BUS} voltage is positive. If a negative voltage is present on V_{BUS}, e.g., by a backwards connector, then the PFET turns off and provides negative voltage protection. This negative voltage protection requires that a device downstream from the MAX14746/MAX14747 provide reverse-current blocking on V_{BUS}. This is required to allow the PFET to turn off. When the drain of the PFET is negative, current flows out of VB. If this reverse current is limited to a small value, V_{VB} drops and the PFET gate-to-source voltage will drop below the threshold voltage.

Supply Voltage Selector

The MAX14746/MAX14747 select their power source themselves by monitoring the voltages at VB and BAT. The devices select V_{VB} when it is present; otherwise, V_{BAT}.

Smart Power Selector

The MAX14746/MAX14747 feature circuitry that seamlessly distributes power between the USB power supply input on VB, the battery on BAT, and system load on SYS when both an external charger adaptor and a battery are connected.

When the system load requirements are less than the input current limit, residual power from the input charges the battery. When the system load requirements exceed the input current limit, the battery supplies supplemental current to the load. When the battery is connected and there is no external power input, the battery powers the system. When an external power input is connected and the battery is discharged or not present, VB powers the system.

USB Charger Detection

The MAX14746/MAX14747 charger detection circuitry support full USB Battery Charger Rev 1.2* detection. The devices detect all charger types, including standard USB ports, charging downstream ports (CDPs), and dedicated chargers. The devices also support Apple power adaptors with resistor dividers on the D+/D- pins at 500mA, 1000mA, and 2000mA current levels. See Charger Detection Timing Diagram.

System Load Switch

The MAX14746/MAX14747 feature an internal MOSFET that connect SYS to BAT for the battery to provide power to the system load. If the USB supply is at the current limit, the devices enable the switch to prevent the system voltage from falling below the battery voltage by supplying extra current from the battery. The battery is not charged if the system load continuously exceeds the input current limit, so this feature is useful for handling loads that are nominally below the input current limit but have high-current peaks exceeding the input current limit. The system uses battery energy during these peaks, but VB charges the battery at all other times.

External System Load Switch

The UOK2/EXT pin can be configured to function as a control signal for an external system load switch.

When the EXT functionality is enabled, the UOK2/EXT pin can drive the gate of an external PMOS connected between SYS and BAT.

When a valid VB voltage is present, EXT is pulled up to V_{SYS}. When VB is disconnected and V_{SYS} is equal to V_{BAT}, the EXT pin is driven to GND. This feature provides an extremely low-impedance SYS-BAT connection.

**Except DCD timeout extended from 900ms to 2s for the MAX14746/MAX14747.*

Input-Current Limiter

The input-current limiter distributes power from the external USB supply to the system load and battery charger. The input current limiter consists of a MOSFET bulk management to optimize the use of available power.

Invalid VB Voltage Protection

The MAX14746/MAX14747 enter overvoltage lockout (OVL) if V_{VB} is above the overvoltage threshold. OVL protects the device and downstream circuitry from high-voltage stress up to 28V. The internal circuit remains powered, the charger turns off, the system load switch closes, and an interrupt triggers during OVL. V_{VB} is also invalid if it is less than V_{BAT} or less than the USB undervoltage threshold. The device takes the same actions as OVL while V_{VB} is invalid.

VB Input Current Limit

The device limits VB input current to prevent input overload. Three methods can set the input current limit:

- a) Set the current limit automatically based on the capabilities of the source as indicated by the ChgTyp [3.0] value read from I²C (register 0x02).
- b) Set the current limit manually over I²C.
- c) Set the current limit manually using the IDEF and/or FSUS inputs.

Thermal Limiting

If the local temperature exceeds 120°C (typ), the MAX14746/MAX14747 attempt to limit temperature increase by reducing the input current from VB. The system load has priority over charger current, so the device lowers the charge current to reduce overall input current. If the temperature continues to rise and reaches 150°C (typ), the device disconnects VB and the battery powers the entire system load.

Adaptive Battery Charging

The battery charger draws power from SYS while VB powers the system. The device reduces charge current to prevent V_{SYS} from falling if the total load exceeds the input current limit.

JEITA Compliant Battery Protection/ Charging

The MAX14746/MAX14747 monitor the temperature of the battery for safe charging of Li+ batteries according to JEITA standards. The devices measure the battery pack temperature by using a resistor divider formed by a pullup resistor connected to CAP and the battery pack thermistor. The external pullup allows matching to different thermistor nominal values. The JEITA circuitry supports thermistors with different β values, but the value must be fixed to choose the CAP pullup resistor. Typical β values are 4250 (MAX14747) and 3380 (MAX14746). The THM input measures the voltage across the resistor divider. There are five temperature zones of operation and the charger termination voltage is controlled based on the pack temperature. The charger is automatically controlled and the active current temperture zone can be read from the JEITAStat[3:0] bits over I²C (register 0x03).

Register Map and Descriptions

REGISTER	ADDR	TYPE	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Chip_Id	0x00	R	Chip_Id[7:0]							
Chip_Rev	0x01	R	Chip_Rev[7:0]							
StatusA	0x02	R	ChgTyp[3:0]				BatDet	ChgStat[2:0]		
StatusB	0x03	R	VLim	ILim	UsbOVP	SysBatV	UsbOk	JeitaStat[2:0]		
StatusC	0x04	R	RFU	RFU	RFU	RFU	ThrmSd	ChgTReg	DCDTmr	ChgTmo
IntA	0x05	CoR	ChgTypInt	UsbOVPInt	SysBatVInt	RFU	BatDetInt	ChgStatInt	ChgTRegInt	ChgTmoInt
IntB	0x06	CoR	VLimInt	DCDTmrInt	ILimInt	ThrmSdInt	UsbOkInt	JeitaStatInt	JeitaHighTInt	JeitaTSdInt
IntMaskA	0x07	R/W	ChgTypIntM	UsbOVPIntM	SysBatVIntM	RFU	BatDetIntM	ChgStatIntM	ChgTRegIntM	ChgTmoIntM
IntMaskB	0x08	R/W	VLimIntM	DCDTmrIntM	ILimIntM	ThrmSdIntM	UsbOkIntM	JeitaStatIntM	JeitaHighTIntM	JeitaTSdIntM
CDetCntlA	0x09	R/W	RFU	RFU	nFsusEn	FSUSMsk	RFU	RFU	DCDEn	RFU
ILimCntl	0x0A	R/W	IBusLim	RFU	RFU	ILimSet[2:0]			IBusDetSw[2:0]	
ChgCntlA	0x0B	R/W	RFU	RFU	RFU	IFChg[2:0]			RFU	RFU
ChgCntlB	0x0C	R/W	JeitaEn	BatUOKMsk	BatDetCntl	ChgEn	RFU	ChgDone[2:0]		
ChgTmr	0x0D	R/W	RFU	RFU	MtChgTmr[1:0]		FChgTmr[1:0]		PChgTmr[1:0]	
ChgVSet	0x0E	R/W	BatReChg[1:0]		BatRegLow[1:0]		BatRegSel	BatRegHi[2:0]		
RFU	0x0F	R/W	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
ChgPCntl	0x10	R/W	VPChg	IPChg[1:0]		VPChgLow[1:0]		VPChgHigh[1:0]		BatDetChgM
CDetCntlB	0x11	R/W	SFOutOrd	SFOutAsrt	AnSwCntl[1:0]		ChgTypMan	ChgAutoStart	BatDetChgEn	UsbCompI
ChgCntlC	0x12	R/W	ChgAutoStp	SFOutData	RFU	RFU	SysMin[2:0]			RFU
ILimMon	0x13	R	ILimMon[7:0]							

RFU = Reserved for future use. Do not change from default value.

*** Register resets to default value on VB rising edge.*

Chip ID Register

ADDRESS:	0x00							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	Chip_Id[7:0]							
RESET	SEE TABLE 4							
Chip_Id[7:0]	The Chip_Id[7:0] bits show information about the version of the MAX14746/MAX14747.							

Chip Revision Register

ADDRESS:	0x01							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	Chip_Rev[7:0]							
RESET	SEE TABLE 4							
Chip_Rev[7:0]	The Chip_Rev[7:0] bits show information about the revision of the MAX14746/MAX14747 silicon.							

Status A Register

ADDRESS:	0x02							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	ChgTyp[3:0]				BatDet	ChgStat[2:0]		
RESET	SEE TABLE 4							

ChgTyp[3:0]	ChgTyp[3:0] identifies what kind of charger is detected on the USB connector. 0000 = Nothing attached. 0001 = SDP. In automatic mode, the current limit is set to 500mA (Or 100mA if UsbCompl = 0). 0010 = CDP. In automatic mode, the current limit is set to 1.5A. 0011 = DCP. In automatic mode, the current limit is set to 1.5A. 0100 = Apple 500mA charger. In automatic mode, the current limit is set to 500mA 0101 = Apple 1A charger. In automatic mode, the current limit is set to 500mA. 0110 = Apple 2A charger. In automatic mode, the current limit is set to 1.5A. 0111 = Non-standard charger (D+/D- > 0.715 x V_{VB}, possibly indicating a PS2 adapter). In automatic mode, the current limit is set to 0mA. 1010 = Other charger (D+/D- = 0.46 x V_{VB} to 0.715 x V_{VB}). In automatic mode, the current limit is set to 500mA. Other = Reserved
BatDet	BatDet indicates the status of the battery detection when VB is present. 0 = No battery detected. 1 = Battery detected.
ChgStat[2:0]	ChgStat[2:0] indicates the current status of the battery charger. 000 = Charger off. 001 = Charging suspended due to overtemperature. 010 = Precharge in progress. 011 = Fast charge in progress using constant-current mode. 100 = Fast charge in progress using constant-voltage mode. 101 = Maintain charge in progress. 110 = Maintain charge timer done. 111 = Charger fault condition.

**POR value depends on external conditions.*

Status B Register

ADDRESS:		0x03						
MODE:		Read Only						
BIT	7	6	5	4	3	2	1	0
NAME	VLim	ILim	UsbOVP	SysBatV	UsbOk	JeitaStat[2:0]		
RESET	SEE TABLE 4							
RFU	Reserved for future use.							
VLim	VLim indicates when the input limiter is in drop-out. 0 = VB input voltage under limit 1 = VB input voltage limited							
ILim	ILim indicates when the VB input current reaches the limit. 0 = VB input current under limit. 1 = VB input current limited.							
UsbOVP	VB Overvoltage Protection Status 0 = VB OVP is not active 1 = VB OVP is active							
SysBatV	SYS-BAT Voltage Minimum. While the system is powered from V_{BUS}, the charger draws power from SYS to charge the battery. If the total load exceeds the input current limit, an adaptive charger control loop reduces charge current to prevent V_{SYS} from collapsing. The regulation of the charge current is done looking for the first valid condition between the following two: a) V_{SYS} - V_{BAT} = 100mV (typ) b) V_{SYS} = V_{SYS_LIM} falling 0 = Charge current is actively reduced 1 = Charge current is NOT actively reduced							
UsbOk	UsbOk indicates when the VB voltage is present and valid. 0 = VB not present or outside of valid range. 1 = VB present and valid.							
JeitaStat[2:0]	JeitaStat[2:0] indicates what temperature the JEITA battery monitor is currently detecting. 000 = T < 0°C or T > 60°C. 001 = 0°C < T < 10°C. 010 = 10°C < T < 45°C. 011 = 45°C < T < 60°C. 100 = No thermistor detected (THM high due to external pullup). 101 = NTC input disabled by JeitaEn. 110 = Detection disabled due to VB not present. 111 = Reserved.							

Status C Register

ADDRESS:	0x04							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	RFU	RFU	RFU	RFU	ThrmSd	ChgTReg	DCDTmr	ChgTmo
RESET	SEE TABLE 4							

RFU	Reserved for future use.
ThrmSd	ThrmSd indicates when the device is in thermal shutdown. 0 = Device not in thermal shutdown. 1 = Device in thermal shutdown.
ChgTReg	ChgTReg indicates when the device is reducing charger current to prevent overheating. 0 = Device not reducing charger current or charger disabled. 1 = Device reducing charger current.
DCDTmr	DCDTmr indicates when a data contact detect time wait exceeds t_{DCD_TO}. 0 = DCD timer not expired or not running. 1 = DCD timer has been running for t_{DCD_TO}.
ChgTmo	ChgTmo indicates when the battery charger reaches a timeout condition. 0 = Charger has not reached a timeout condition or is disabled. 1 = Charger has reached a timeout condition. ChgStat[2:0] in register 0x02 = 111 to indicate this fault condition.

Interrupt A Register

ADDRESS:	0x05							
MODE:	Clear on Read							
BIT	7	6	5	4	3	2	1	0
NAME	ChgTypInt	UsbOVPInt	SysBatVInt	RFU	BatDetInt	ChgStatInt	ChgTRegInt	ChgTmoInt
RESET	SEE TABLE 4							

ChgTypInt	ChgTypInt is set when there is a change in ChgTyp[3:0] in register 0x02.
UsbOVPInt	UsbOVPInt is set when there is a change in UsbOVP in register 0x03.
SysBatVint	SysBatVint is set when there is a change in SysBatV in register 0x03.
BatDetInt	BatDetInt is set when there is a change in BatDet or the first battery detection completes after a POR or a change in battery detection method.
ChgStatInt	ChgStatInt is set when there is a change in ChgStat[2:0] in register 0x02 or the first charger status is entered after a POR.
ChgTRegInt	ChgTRegInt is set when there is a change in ChgTReg in register 0x04.
ChgTmoInt	ChgTmoInt is set when there is a change in ChgTmo in register 0x04.

Interrupt B Register

ADDRESS:	0x06							
MODE:	Clear on Read							
BIT	7	6	5	4	3	2	1	0
NAME	VLimInt	DCDTmrInt	ILimInt	ThrmSdInt	UsbOkInt	JeitaStatInt	JeitaHighTInt	JeitaTSdInt
RESET	SEE TABLE 4							
VLimInt	VLimInt is set when the VB voltage reaches the input voltage limit.							
DCDTmrInt	DCDTmrInt is set when a DCD timeout occurs.							
ILimInt	ILimInt is set when the VB current reaches the input current limit.							
ThrmSdInt	ThrmSdInt is set when there is a change in ThrmSd in register 0x04.							
UsbOkInt	UsbOkInt is set when there is a change in UsbOk in register 0x03.							
JeitaStatInt	JeitaStatInt is set when there is a change in JeitaStat[2:0] in register 0x03.							
JeitaHighTInt	JeitaHighTInt is set when the JEITA monitor enters the high battery temperature range (45°C < T < 60°C).							
JEITATSDINT	JeitaTSdInt is set when the JEITA monitor enters the very low or very high battery temperature range (T < 0°C or T > +60°C).							

Interrupt Mask A Register

ADDRESS:	0x07							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	ChgTypIntM	UsbOVPIntM	SysBatVIntM	RFU	BatDetIntM	ChgStatIntM	ChgTRegIntM	ChgTmoIntM
RESET	SEE TABLE 4							
ChgTypIntM	ChgTypIntM masks the ChgTypInt interrupt in the IntA register (0x05). 0 = Masked. 1 = Not masked.							
UsbOVPIntM	UsbOVPIntM masks the UsbOVPInt interrupt in the IntA register (0x05). 0 = Masked. 1 = Not masked.							
SysBatVIntM	SysBatVintM masks the SysBatVint interrupt in the intA register (0x05).							
BatDetIntM	BatDetIntM masks the BatDetInt interrupt in the IntA register (0x05). 0 = Masked. 1 = Not masked.							
ChgStatIntM	ChgStatIntM masks the ChgStatInt interrupt in the IntA register (0x05). 0 = Masked. 1 = Not masked.							
ChgTRegIntM	ChgTRegIntM masks the ChgTRegInt interrupt in the IntA register (0x05). 0 = Masked. 1 = Not masked.							
ChgTmoIntM	ChgTmoIntM masks the ChgTmoInt interrupt in the IntA register (0x05). 0 = Masked. 1 = Not masked.							

Interrupt Mask B Register

ADDRESS:	0x08							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	VLimIntM	DCDTmrIntM	ILimIntM	ThrmSdIntM	UsbOkIntM	JeitaStatIntM	JeitaHighTIntM	JeitaTSdIntM
RESET	SEE TABLE 4							
VLimIntM	VLimIntM masks the VLimInt interrupt in the IntB register (0x06).							
DCDTmrIntM	DCDTmrIntM masks the DCDTmrInt interrupt in the IntB register (0x06). 0 = Masked. 1 = Not masked.							
ILimIntM	ILimIntM masks the ILimInt interrupt in the IntB register (0x06). 0 = Masked. 1 = Not masked.							
ThrmSdIntM	ThrmSdIntM masks the ThrmSdInt interrupt in the IntB register (0x06). 0 = Masked. 1 = Not masked.							
UsbOkIntM	UsbOkIntM masks the UsbOkInt interrupt in the IntB register (0x06). 0 = Masked. 1 = Not masked.							
JeitaStatIntM	JeitaStatIntM masks the JeitaStatInt interrupt in the IntB register (0x06). 0 = Masked. 1 = Not masked.							
JeitaHighTIntM	JeitaHighTIntM masks the JeitaHighTInt interrupt in the IntB register (0x06). 0 = Masked. 1 = Not masked.							
JeitaSdIntM	JeitaSdIntM masks the JeitaSdInt interrupt in the IntB register (0x06). 0 = Masked. 1 = Not masked.							

Charger Detection Control A Register

ADDRESS:	0x09							
MODE:	Read/Write*							
BIT	7	6	5	4	3	2	1	0
NAME	RFU	RFU	nFsusEn	FSUSMsk	RFU	RFU	DCDEn	RFU
RESET	SEE TABLE 4							
RFU	Reserved for future use.							
nFsusEn	nFsusEn is a software force-suspend control. If FSUSMsk = 0, the FSUS input controls the force suspend current limit. If FSUSMsk = 1, then nFsusEn controls the force suspend current limit. 0 = The device is forced into standby mode and the current limit is reduced to 0mA. 1 = Normal operation.							
FSUSMsk	FSUSMsk masks the function of the FSUS input. 0 = FSUS input controls force-suspend mode. 1 = nFsusEn bit controls force-suspend mode.							
DCDTEn	DCDTEn enables data contact detection. 0 = Not enabled. 1 = Enabled.							

**Register resets to default value on VB rising edge.*

Input-Current Limit Control Register

ADDRESS:	0x0A							
MODE:	Read/Write*							
BIT	7	6	5	4	3	2	1	0
NAME	IBusLim	RFU	RFU	ILimSet[2:0]			IBusDetSw[1:0]	
RESET	SEE TABLE 4							
IBusLim	IBusLim selects the automatic/manual VB input current limit. 0 = Automatic mode. The current limit is determined using adaptor detection status (ChgTyp[3:0] bits in register 0x02). 1 = Manual mode. The current limit is determined by IBusDetSw[1:0] and ILimSet[2:0].							
RFU	Reserved for future use.							
ILimSet[2:0]	ILimSet[2:0] sets the VB current limit in manual mode when IBusDetSw[1:0] = 11. 000 = 100mA 001 = 500mA 010 = 600mA 011 = 700mA 100 = 900mA 101 = 1000mA 110 = 1500mA 111 = 2000mA							
IBusDetSw [1:0]	IBusDetSw[1:0] sets the current limit on VB in manual mode. 00 = 0mA 01 = 100mA 10 = 500mA 11 = set by ILimSet[2:0]							

**Register resets to default value on VB rising edge.*

Charge Control Register A

ADDRESS:		0x0B						
MODE:		Read/Write*						
BIT	7	6	5	4	3	2	1	0
NAME	RFU	RFU	RFU	IFChg[2:0]			RFU	RFU
RESET	SEE TABLE 4							
RFU	Reserved for future use.							
IFChg[2:0]	IFChg[2:0] sets the charger current in fast-charge mode. 000 = 700mA 001 = 300mA 010 = 200mA 011 = 600mA 100 = 800mA 101 = 900mA 110 = 350mA 111 = 450mA							

**POR value depends on external conditions.*

Charger Control B Register

ADDRESS:	0x0C							
MODE:	Read/Write*							
BIT	7	6	5	4	3	2	1	0
NAME	JeitaEn	BatUOKMsk	BatDetCntl	ChgEn	RFU	ChgDone[2:0]		
RESET	SEE TABLE 4							

JeitaEn	JeitaEn enables JEITA battery monitoring. 0 = JEITA monitoring of thermistor disabled. When JeitaEn = 0, JeitaStat[2:0] in register 0x03 always reads 101. 1 = JEITA monitoring of thermistor enabled. JeitaStat[2:0] in register 0x03 reads back the current temperature status of the thermistor at THM.
BatUOKMsk	BatUOKMsk masks the UOK_ signals. 0 = Battery detection signals are generated by the UOK_ outputs. 1 = Battery detection signals are not generated by the UOK_ outputs.
BatDetCntl	BatDetCntl selects which method the MAX14646/MAX14647 uses to detect the battery. 0 = BatDet status bit will indicate battery presence based on the impedance method. 1 = BatDet status bit will indicate battery presence based on presence of the NTC thermistor on THM.
ChgEn	ChgEn enables the battery charger. ChgEn does not affect the SYS node. 0 = Charger disabled. 1 = Charger enabled.
RFU	Reserved for future use.
ChgDone[2:0]	ChgDone[2:0] sets the threshold current when constant-voltage fast charging is done. 000 = 10mA 001 = 20mA 010 = 40mA 011 = 50mA 100 = 60mA 101 = 80mA 110 = 100mA 111 = 120mA

**Register resets to default value on VB rising edge.*

Charger Timer Register

ADDRESS:	0x0D							
MODE:	Read/Write*							
BIT	7	6	5	4	3	2	1	0
NAME	RFU	RFU	MtChgTmr[1:0]		FChgTmr[1:0]		PChgTmr[1:0]	
RESET	SEE TABLE 4							

RFU	Reserved for future use.
MtChgTmr[1:0]	MtChgTmr[1:0] sets the maintain charge timer when ChgAutoStp is register 0x12 is 1. 00 = 30min 01 = 15min 10 = 0min 11 = 60min
FChgTmr[1:0]	FChgTmr[1:0] sets the fast charge timer. 00 = 75min 01 = 150min 10 = 300min 11 = 600min
PChgTmr[1:0]	PChgTmr[1:0] sets the pre charge timer. 00 = 30min 01 = 60min 10 = 120min 11 = 240min

**Register resets to default value on VB rising edge.*

Charger Detection Control A Register

ADDRESS:	0x0E							
MODE:	Read/Write*							
BIT	7	6	5	4	3	2	1	0
NAME	BatReChg[1:0]		BatRegLow[1:0]		BatRegSel	BatRegHi[2:0]		
RESET	SEE TABLE 4							
BatReChg[1:0]	BatReChg[1:0] sets the recharge threshold in relation to V_{BAT}. Once V_{BAT} falls to below the regulation voltage less this amount, the MAX14746/MAX14747 will recharge it. 00 = 50mV 01 = 100mV 10 = 150mV 11 = 200mV							
BatRegLow[1:0]	BatRegLow[1:0] sets the battery regulation voltage when BatRegSel = 0. 00 = 4.05V 01 = 4.10V 10 = 4.15V 11 = 4.20V							
BatRegSel	BatRegSel selects which value to use for the battery regulation voltage setting. V_{SYS} is nominally set at VBAT_REG + 200mV. Note, if V_{BAT_REG} is chosen such that $V_{SYS} < V_{SYS\_LIM}$, the battery charger will not function properly. 0 = Use BatRegLow 1 = Use BatRegHi							
BatRegHi[2:0]	BatRegHi sets the battery regulation voltage when BatRegSel = 1 000 = 4.25V 001 = 4.30V 010 = 4.35V 011 = 4.40V 100 = 4.45V 101 = 4.50V 110 = 4.55V 111 = 4.60V							

**Register resets to default value on VB rising edge.*

Precharge Control Register

ADDRESS:	0x10							
MODE:	Read/Write*							
BIT	7	6	5	4	3	2	1	0
NAME	VPChg	IPChg[1:0]		VPChgLow[1:0]		VPChgHigh[1:0]		BatDetChgM
RESET	SEE TABLE 4							
VPChg	VPChg selects which voltage threshold setting to use for pre-charging. The charger uses precharging until the battery voltage rises above the threshold or the timer expires. 0 = Use VPChgLow[1:0]. 1 = Use VPChgHigh[1:0].							
IPChg[1:0]	IPChg[1:0] sets the precharge current. 00 = 30mA 01 = 50mA 10 = 70mA 11 = 100mA							
VPChgLow [1:0]	VPChgLow[1:0] sets the precharge voltage threshold when VPChg = 0. 00 = 2.15V 01 = 2.25V 10 = 2.35V 11 = 2.45V							
VPChgHigh [1:0]	VPChgHigh[1:0] sets the precharge voltage threshold when VPChg = 1. 00 = 2.70V 01 = 2.80V 10 = 2.90V 11 = 3.00V							
BatDetChgM	BatDetChgM mask for battery detection-charger interaction. 0 = BatDet state affects charger behavior per state diagram. 1 = BatDet state does not affect charger behavior. (i.e., it is possible to turn on charger without a battery present.)							

**Register resets to default value on VB rising edge.*

Charger Detection Control B Register

ADDRESS:	0x11							
MODE:	Read/Write*							
BIT	7	6	5	4	3	2	1	0
NAME	SFOutOrd	SFOutAsrt	AnSwCntl[1:0]		ChgTypMan*	ChgAutoStart	BatDetChgEn	UsbCompl
RESET	SEE TABLE 4							
SFOutOrd	SFOutOrd enables the SFOUT output. 0 = Force SFOUT to off. The internal LDO is disabled and V_{SFOUT} is 0V. 1 = SFOUT is automatically controlled by the VB voltage presence and the SFOutAsrt bit.							
SFOutAsrt	SFOutAsrt controls the period when SFOUT turns on. 0 = SFOUT turns on after a complete charger detection cycle. VB does not pass current until charger detection is complete. 1 = SFOUT turns on immediately after VB is a valid voltage.							
AnSwCntl[1:0]	AnSwCntl[1:0] controls the analog USB data switches. 00 = Automatic mode. The switches are open during adapter detection and closed if an SDP or CDP are detected. 01 = Switches forced open. 10 = Switches forced open. 11 = Switches forced closed.							
ChgTypMan*	Charger-Type Manual Detection Set to 1 to force charger detection. After the detection completes the bit resets to 0. 0 = Disable 1 = Force a charger detection run							
ChgAutoStart	Charger Auto-Restart Control 0 = Charger remains in maintain charge done even when V_{BAT} is less than charge restart threshold. 1 = Charger automatically restarts when V_{BAT} drops below charge restart threshold.							
BatDetChgEn	BatDetChgEn enables running the charger during battery detection. 0 = The charger is not allowed to turn on during battery detection if ChgEn = 0 in register 0x0C. 1 = The charger is allowed to turn on during battery detection even when ChgEn = 0 in register 0x0C.							
UsbCompl	UsbCompl controls whether a USB compliant port is expected for an SDP port. 0 = If an SDP is detected in auto current limit setting mode, the input current limit is set to 500mA. 1 = If an SDP is detected in auto current limit setting mode, the input current limit is set to 100mA.							

**Register resets to default value on VB rising edge.*

Charger Control C Register

ADDRESS:		0x12						
MODE:		Read/Write*						
BIT	7	6	5	4	3	2	1	0
NAME	ChgAutoStp	SFOutData	RFU	RFU	SysMin[2:0]			RFU
RESET	SEE TABLE 4							
ChgAutoStp	ChgAutoStp controls the transition from maintain charge mode to maintain charge done. 0 = Auto stop disabled. 1 = Auto stop enabled.							
SFOutData	SFOutData controls whether SFOUT is turned on for all chargers or only for SDP/CDP. SFOutData is overridden by the SFOutOrd and SFOutAsrt settings in register 0x11. 0 = SFOUT is turned on for all valid charger types (see ChgTyp[3:0] in register 0x02). 1 = SFOUT is turned on only for SDP (ChgTyp[3:0] = 001) or CDP (ChgTyp[3:0] = 010) chargers.							
SysMin[2:0]	SysMin sets System Voltage Minimum Threshold. When V_{SYS} approaches V_{SYS_LIM}, an internal loop will actively reduces the charge current in order to regulate V_{SYS}. Note, if $V_{SYS} < V_{SYS\_LIM}$, the battery charger will not function properly. 000 = 3.6V 001 = 3.7V 010 – 3.8V 011 = 3.9V 100 = 4.0V 101 = 4.1V 110 = 4.2V 111 = 4.3V							
RFU	Reserved for future use. Must be set to 1.							

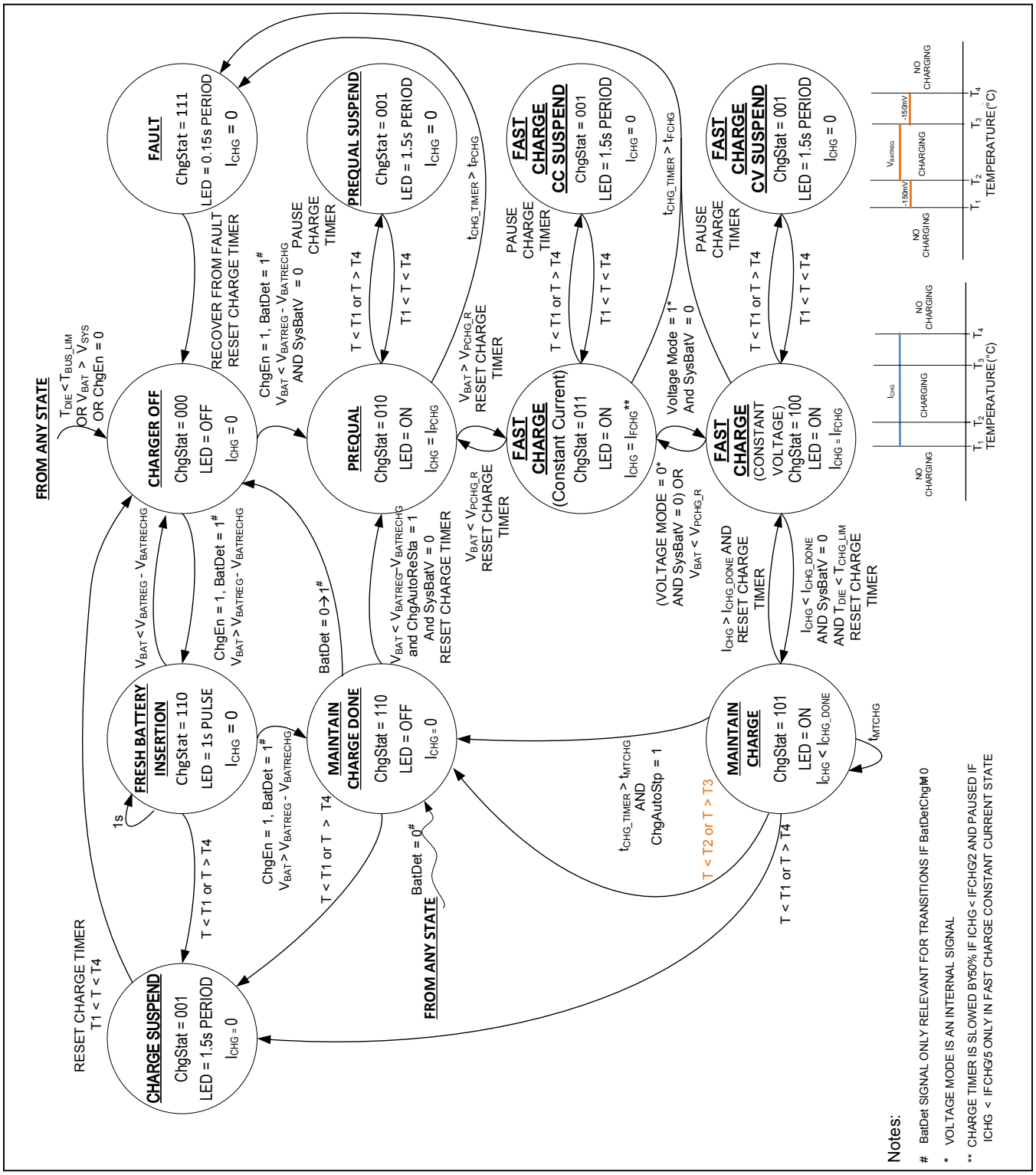
**Register resets to default value on VB rising edge.*

Current-Limit Monitor Register

ADDRESS:	0x13							
MODE:	Read Only*							
BIT	7	6	5	4	3	2	1	0
NAME	ILimMon[7:0]							
RESET	SEE TABLE 4							
ILimMon[7:0]	ILimMon[7:0] reads out the VB input current limit setting that is currently used. 0000 0000 = 0mA 0000 0001 = 100mA 0000 0010 = 500mA 0000 0100 = 600mA 0000 1000 = 700mA 0001 0000 = 900mA 0010 0000 = 1000mA 0100 0000 = 1500mA 1000 0000 = 2000mA							

**Register resets to default value on VB rising edge.*

State Diagram



Applications Information

I²C Interface

The MAX14646/MAX14647 contain an I²C-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

Start, Stop, And Repeated Start Conditions

When writing to the MAX14646/MAX14647 using I²C, the master sends a START condition (S) followed by the MAX14646/MAX14647 I²C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I²C slave. See Figure 2.

Slave Address

Set the Read/$\overline{\text{Write}}$ bit high to configure the MAX14646/MAX14647 to read mode (Table 1). Set the Read/$\overline{\text{Write}}$ bit low to configure the MAX14646/MAX14647 to write mode. The address is the first byte of information sent to the MAX14646/MAX14647 after the START condition.

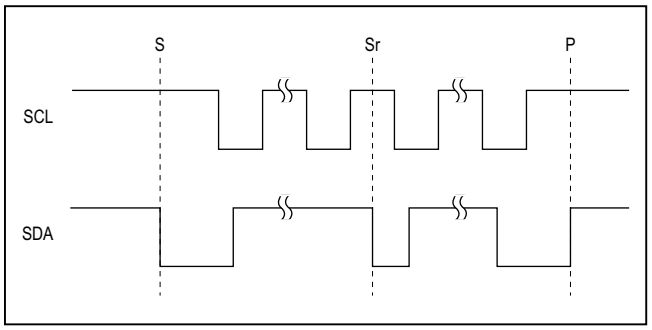


Figure 2. I²C START, STOP and REPEATED START Conditions

Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *Start, Stop, And Repeated Start Conditions* section). Both SDA and SCL remain high when the bus is not active.

Single-Byte Write

In this operation, the master sends an address and two data bytes to the slave device (Figure 3). The following procedure describes the single byte write operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends 8 data bits
- 7) The slave asserts an ACK on the data line
- 8) The master generates a STOP condition

Table 1. I²C Slave Addresses

ADDRESS FORMAT	HEX	BINARY
7-bit slave ID (MAX14746)	0x12	0001 010
Write Address (MAX14746)	0x14	0001 0100
Read Address (MAX14746)	0x15	0001 0101
7-bit slave ID (MAX14747)	0x02	0000 010
Write Address (MAX14747)	0x04	0000 0100
Read Address (MAX14747)	0x05	0000 0101

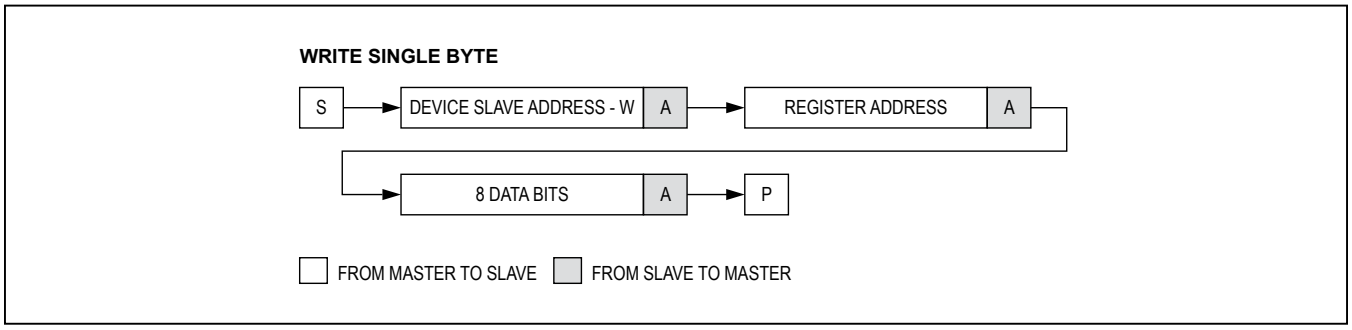


Figure 3. Write Byte Sequence

Burst Write

In this operation, the master sends an address and multiple data bytes to the slave device (Figure 4). The slave device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends eight data bits
- 7) The slave asserts an ACK on the data line
- 8) Repeat 6 and 7 N-1 times
- 9) The master generates a STOP condition

Single Byte Read

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device (Figure 5). The following procedure describes the single byte read operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends a REPEATED START condition
- 7) The master sends the 7-bit slave address plus a read bit (high)
- 8) The addressed slave asserts an ACK on the data line
- 9) The slave sends eight data bits
- 10) The master asserts a NACK on the data line
- 11) The master generates a STOP condition

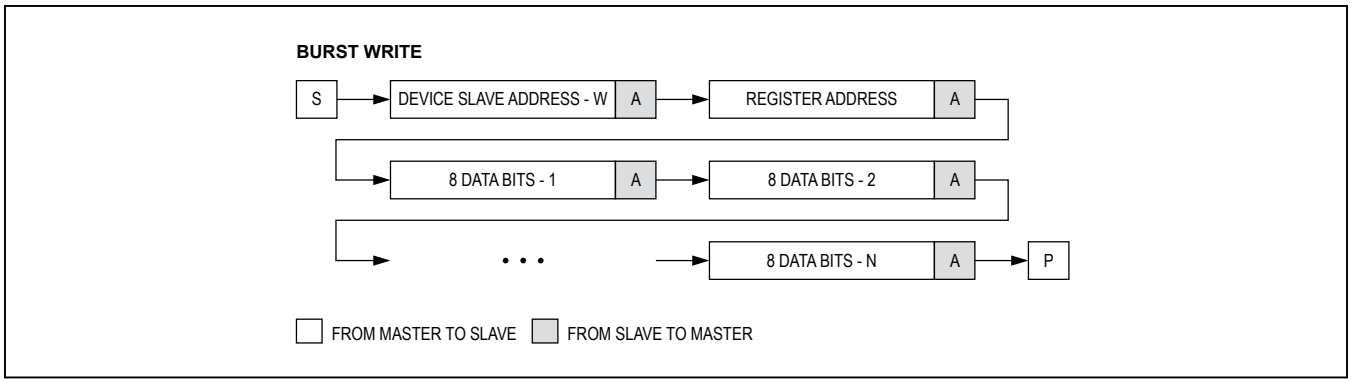


Figure 4. Burst Write Sequence

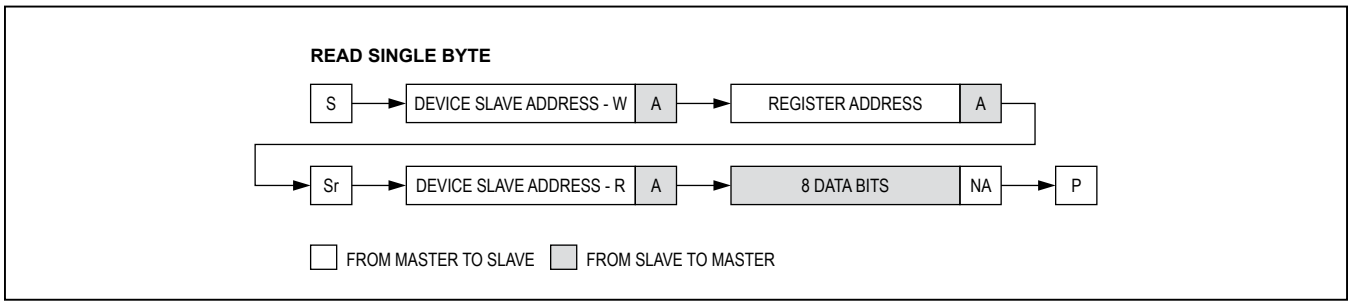


Figure 5. Read Byte Sequence

Burst Read

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device (Figure 6). The following procedure describes the burst byte read operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends a REPEATED START condition
- 7) The master sends the 7-bit slave address plus a read bit (high)
- 8) The slave asserts an ACK on the data line
- 9) The slave sends eight data bits
- 10) The master asserts an ACK on the data line
- 11) Repeat 9 and 10 N-2 times
- 12) The slave sends the last eight data bits
- 13) The master asserts a NACK on the data line
- 14) The master generates a STOP condition

Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX14746 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (see Figure 7). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

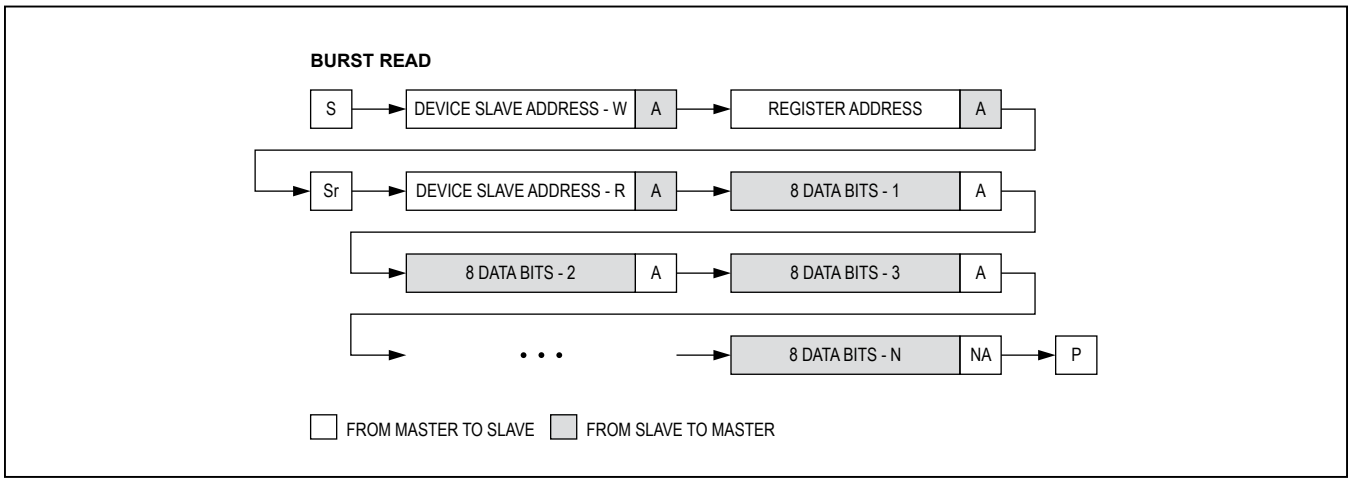


Figure 6. Burst Read Sequence

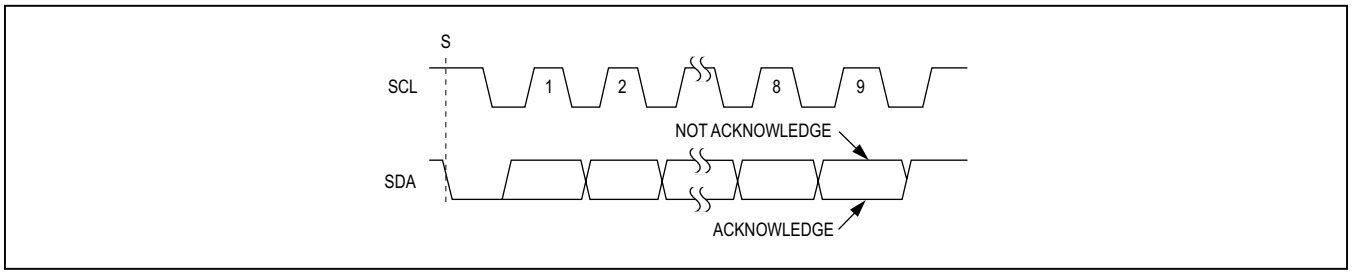


Figure 7. Acknowledge

High-ESD Protection

Electrostatic Discharge (ESD)-protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV Human Body Model (HBM) encountered during handling and assembly. CDP and CDN are further protected against ESD up to ±15kV (HBM) without damage. The ESD structures withstand high ESD in both normal operation and when the device is powered down. After an ESD event, the MAX14746/MAX14747 continues to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 8 shows the Human Body Model. Figure 9 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The MAX14746/MAX14747 are specified for ±4kV Air-Gap and ±5kV Contact Discharge IEC 61000-4-2 on the CDP and CDN pins.

The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 10), the ESD-withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 11 shows the current waveform for the ±6kV IEC 61000-4-2 Level 4 ESD Contact Discharge test. The Contact Discharge method connects the probe to the device before the probe is energized.

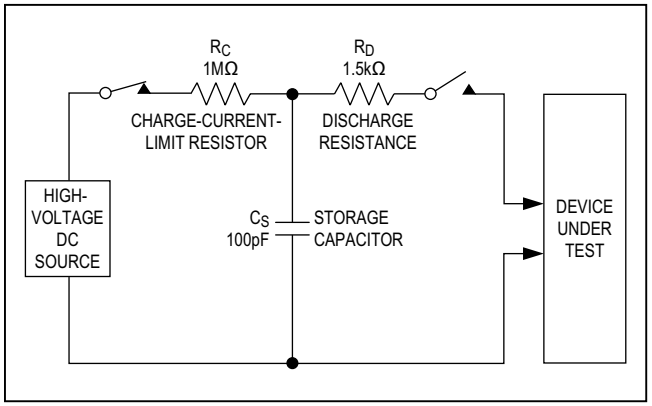


Figure 8. Human Body ESD Test Model

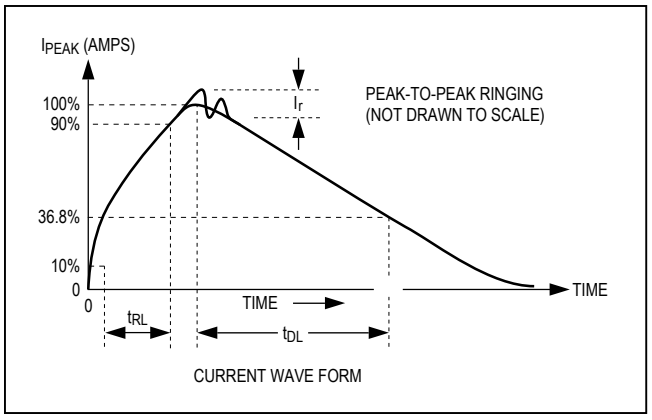


Figure 9. Human Body Current Waveform

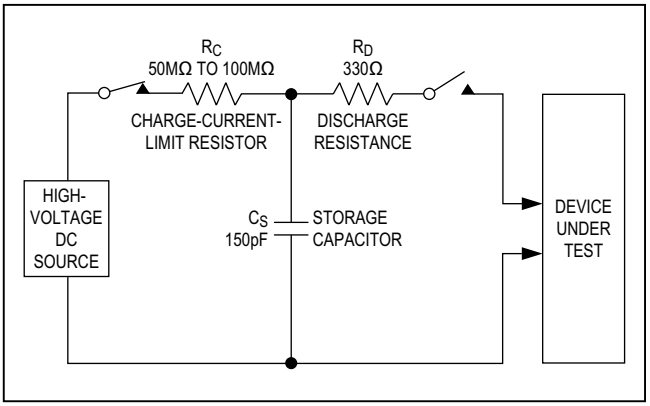


Figure 10. IEC61000-4-2 ESD Test Model

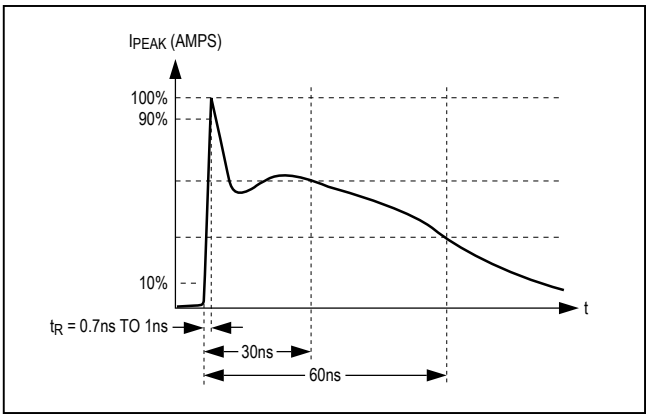


Figure 11. IEC61000-4-2 ESD Generator Current Waveform

Table 2. Part Selection

PART NUMBER	EXT/UOK2 FUNCTION	BATTERY OVP
MAX14746B	EXT	Disabled
MAX14747	EXT	Enabled

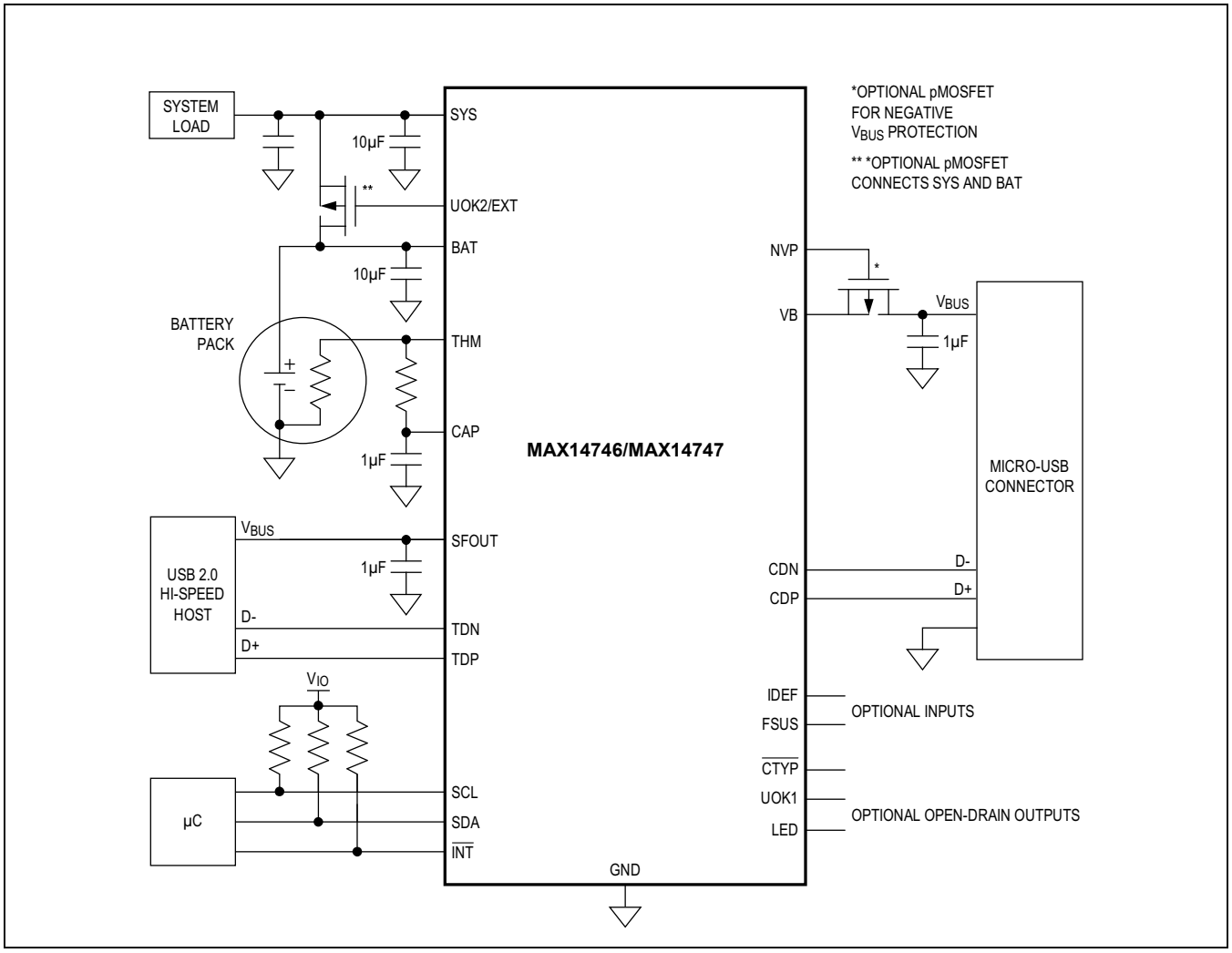
Table 3. Register Bit Default Values

REGISTER BITS	MAX14746B	MAX14747
IBusLim	Manual	Automatic
ILimSet[2:0]	500mA	500mA
IFChg[2:0]	600mA	200mA
ChgEn	Enabled	Disabled
BatReChg[1:0]	100mV	100mV
BatRegLow[1:0]	4.20V	4.20V
BatDetIntM	Masked	Masked
ChgStatIntM	Masked	Masked
VPChg	VPChgHigh	VPChgLow
IPChg[1:0]	100mA	50mA
VPChgLow[1:0]	2.45V	2.25V
VPChgHigh[1:0]	3.00V	2.80V
SFoutAsrt	Immediately	Delayed
FSUSMsk	FSUS	FSUS
BatDetChgM	Not Masked	Not Masked
JeitaEn	Enabled	Enabled
BatDetCntl	Thermistor	Thermistor
ChgDone[2:0]	50mA	60mA
ChgAutoStart	Enabled	Enabled
BatDetChgEn	Enabled	Enabled
UsbCmpl	500mA	500mA
BatRegSel	BatRegLow	BatRegLow
BatRegHi[2:0]	4.35V	4.35V
SFoutData	All Chargers	All Chargers
SysMin[2:0]	4.3V	4.3V
MAX_VSYS_REG	V_{BAT_REG} + 0.2V	4.8V

Table 4. Register Default Values

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUES	
		MAX14746B	MAX14747
0x00	Chip_Id	0x2E	0x30
0x01	Chip_Rev	0x01	0x11
0x02	StatusA	0x00	0x00
0x03	StatusB	0x46	0x46
0x04	StatusC	0x00	0x00
0x05	IntA	0xA0	0xA0
0x06	IntB	0xA4	0xA4
0x07	IntMaskA	0x00	0x00
0x08	IntMaskB	0x00	0x00
0x09	CDetCntlA	0x22	0x22
0x0A	ILimCntl	0x87	0x07
0x0B	ChgCntlA	0x0C	0x08
0x0C	ChgCntlB	0xF3	0xE4
0x0D	ChgTmr	0x2E	0x2E
0x0E	ChgVSet	0x72	0x72
0x0F	JeitaCntl	0x00	0x00
0x10	ChgPCntl	0xFE	0x2A
0x11	CDetCntlB	0xC6	0x86
0x12	ChgCntlC	0x8F	0x81
0x13	ILimMon	0x00	0x00

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE	BUMP-PACKAGE
MAX14746BEWA+	-40°C to +85°C	25 WLP
MAX14747EWA+*	-40°C to +85°C	25 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

**Future product—Contact factory for availability.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
25 WLP	W252J2+1	**21-0453**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/15	Initial release	—
1	1/17	Updated for Pass 2 material	3, 11, 13, 19–33, 39

