Lattice Embedded Vision Development Kit

User Guide

FPGA-UG-02015 Version 1.0

April 2017

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CSI	Camera Serial Interface
GPIO	General Purpose Input/Output
HDMI	High Definition Multimedia Interface
I^2C	Inter-Integrated Circuit
MIPI	Mobile Industry Processing Interface
VIP	Video Interface Protocol
USB	Universal Serial Bus

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1. Introduction

This document describes the design and setup procedure for the Lattice Embedded Vision Development Kit to demonstrate dual CSI-2 camera to High Definition Multimedia Interface (HDMI®) bridging that features the CrossLink™, pASSP, ECP5™ FPGA and SiI1136 transmitter devices.

Figure 2.1 shows the Lattice Embedded Vision Development Kit that is designed as a stackable modular architecture with 80 mm × 80 mm form factor. The Lattice Embedded Vision Development Kit consists of three boards:

- CrossLink Video Interface Protocol (VIP) Input Bridge Board
- ECP5 VIP Processor Board
- HDMI VIP Output Bridge Board

For more information on Embedded Vision Development Kit, visit
www.latticesemi.com/en/Products/DevelopmentBoardsAndKits/EmbeddedVisionDevelopmentKit.aspx

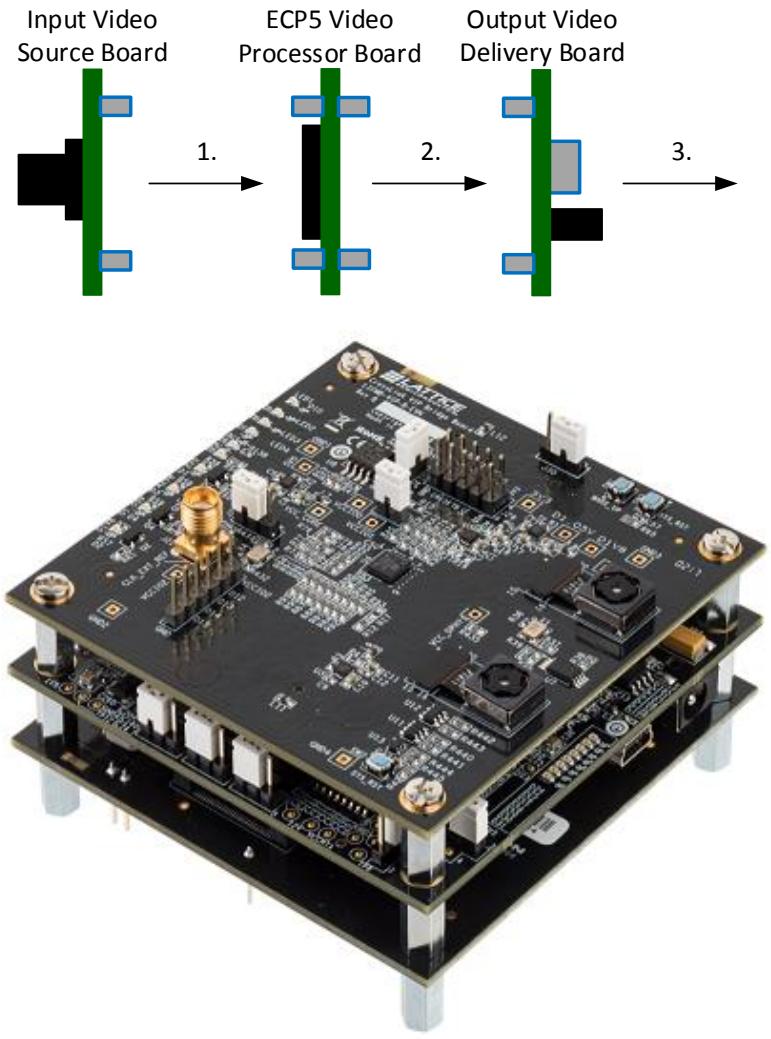

Figure 1.1. 2:1 MIPI CSI-2 to HDMI Bridge

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2. Functional Description

The dual camera Mobile Industry Processing Interface (MIPI®) CSI-2 to HDMI demo uses a Sony IMX214 camera to output 1080p video over four MIPI data lanes, each running at 371.25 Mb/s. CrossLink VIP input bridge board receives the MIPI video stream from onboard camera sensor and extracts the video pixels. These video pixels from two cameras are merged side by side and the combined image data is transmitted to ECP5 in the form of parallel CMOS interface on the ECP5 video processor board through board-to-board connectors.

The ECP5 FPGA processes the image with its pixel correction, white balance, debayer, RGB2RGB, and gamma correction modules, and sends the processed parallel image data to Sil1136 HDMI transmitter on the HDMI VIP output bridge board through board to board connectors. The Sil1136 chip transmits the video data via HDMI to the 1080p display.

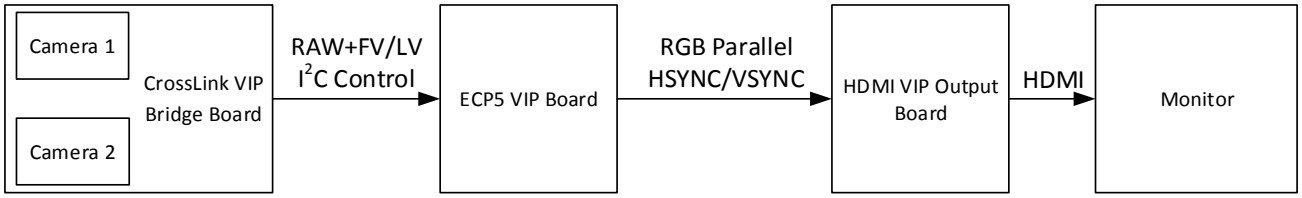

Figure 2.1. 2:1 MIPI CSI-2 to HDMI Bridge System Diagram

2.1. CrossLink

The dual-camera-to-parallel design receives the serial, source-synchronous MIPI data from two MPI CSI-2 cameras, reserializes the serial data into bytes and extracts the control signal from MIPI data packets. The byte data is sent to Byte to Pixel module that converts 32-bit byte data to 10-bit RAW data. Two separate streams of RAW data are sent to the Image merger logic that takes the data from both cameras, combines the parallel data from two data streams, and then send it to the ECP5 board. The onboard CSI-2 camera is configured through ECP5 I2C master interface on ECP5 VIP processor board.

Figure 2.2 shows the CrossLink functional block diagram.

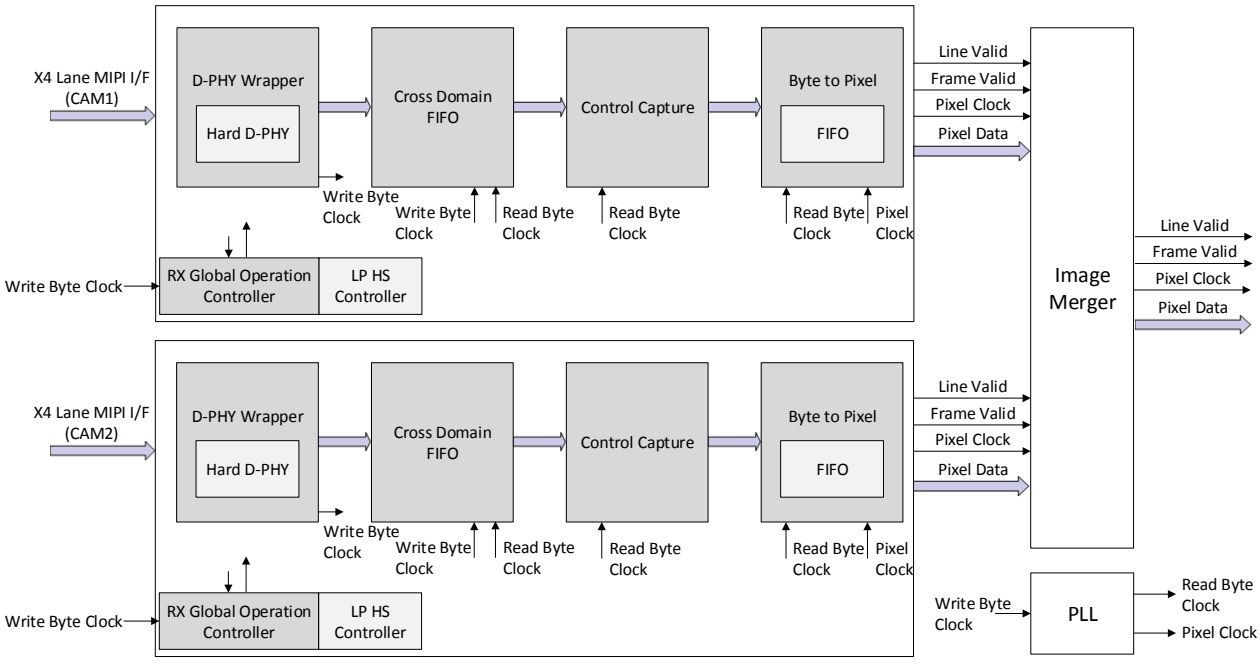

Figure 2.2. CrossLink Functional Block Diagram

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2.2. ECP5

The ECP5 FPGA receives the RAW data from CrossLink, does the fundamental image processing, and sends it to the HDMI board.

Figure 2.3 shows the Lattice Programmable Image Processing Module. This module improves the quality of an image from a sensor by:

Pixel Correction – Image sensors may convey defective pixels due to yield issues by the manufacturer. The defect correction module repairs these pixels based on X, Y coordinates loaded in its configuration registers.

White Balance – Many times an image does not use the full range of bits within each color domain. The white balance module provides gain and offset controls. These controls are used to widen the range of each color on the digital bus. This module is adjusted in real time with the help of a histogram.

Debayer – This module converts Bayer data from the image sensor to an R, G and B pixel per clock cycle.

Color Space Converter – Colors directly from an image sensor do not match the real world by default. The Color Space Converter matrix corrects this issue. There are gain and offset controls for each color, as well as the influence of one color on the other. The Color Space Converter matrix coefficients are tuned once for a particular sensor.

Gamma Correction – Common bit depth resolutions of displays are 8 bits per color. Image sensors often have a larger bit depth. The gamma correction module provides the ability to compress, but still take advantage of the larger bit depth.

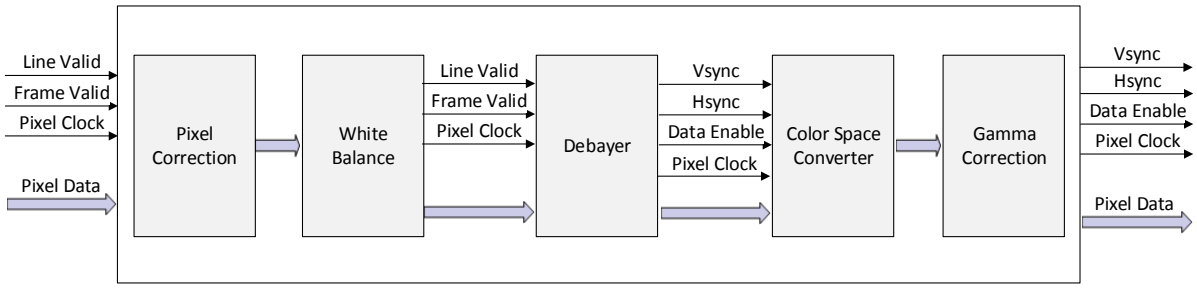

Figure 2.3. ECP5 Functional Block Diagram

2.3. SiI1136

Figure 2.4 shows the functional block diagram of the SiI1136 HDMI transmitter. This transmitter device is configured to output 1080p60 through the ECP5 I^2C Master interface on ECP5 VIP processor board. It receives RGB 8:8:8 data and control signal from ECP5 and converts it to HDMI format that is displayed on the HDMI monitor.

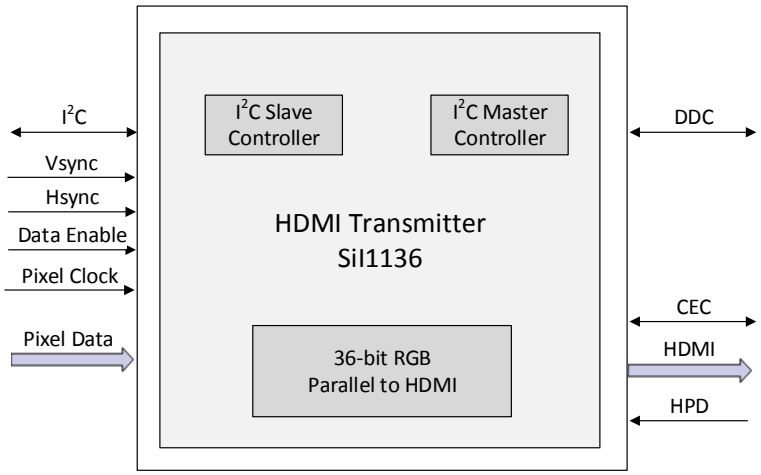

Figure 2.4. SiI1136 Functional Block Diagram

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3. Demo Requirements

The following equipment is required for the demo:

- LF-EVDK1-EVN Demo Kit
- HDMI monitor
- HDMI cable
- DC power adapter (12 V)
- Laptop/PC
- Bit/JED file
- USB 2.0 Type A to Mini-B cable*
- Lattice Diamond® Programmer version 3.7 or higher*

***Note**: Required only in re-programming.

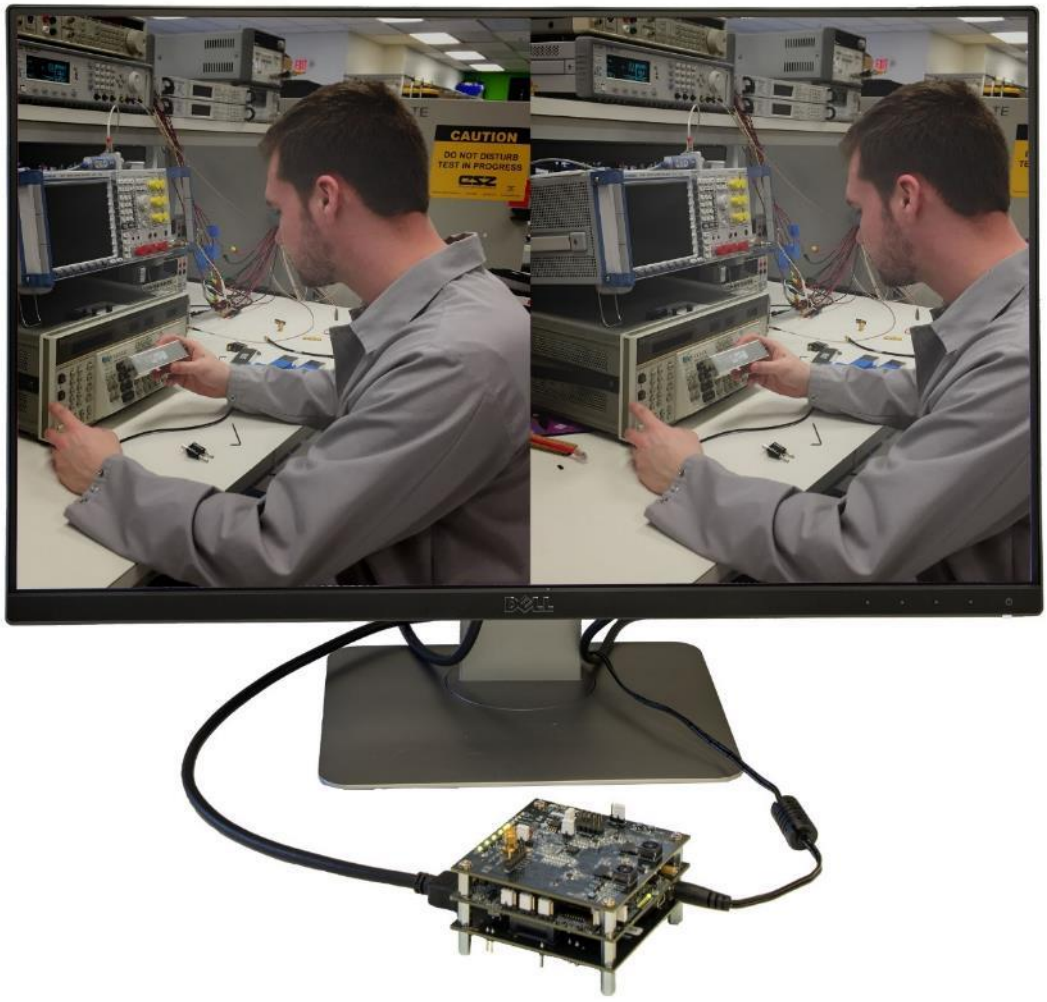

Figure 3.1. Dual Camera to HDMI Setup

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3.1. CrossLink VIP Input Bridge Board

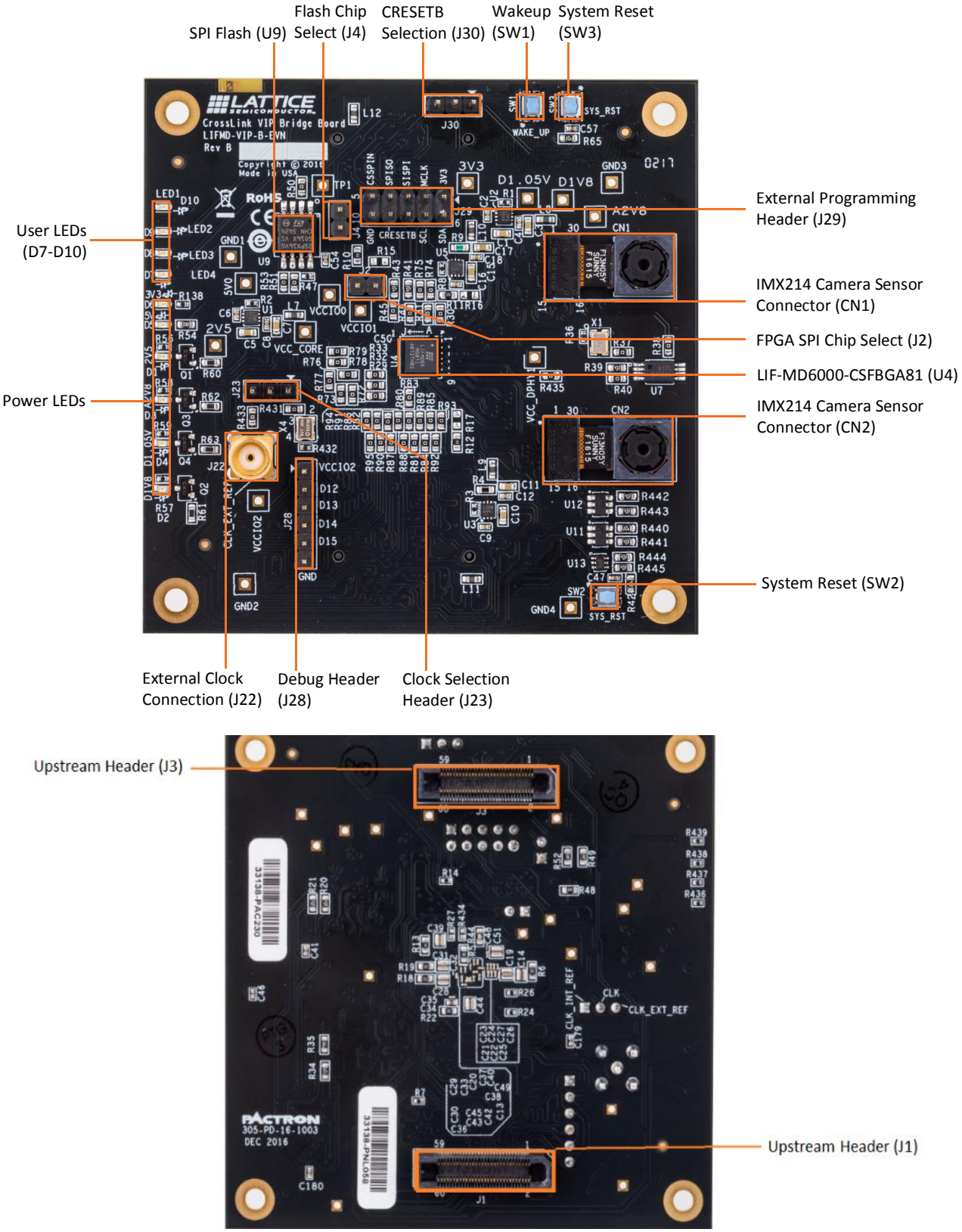

Figure 3.2.Top and Bottom View of Crosslink VIP Input Bridge Board

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3.2. ECP5 VIP Processor Board

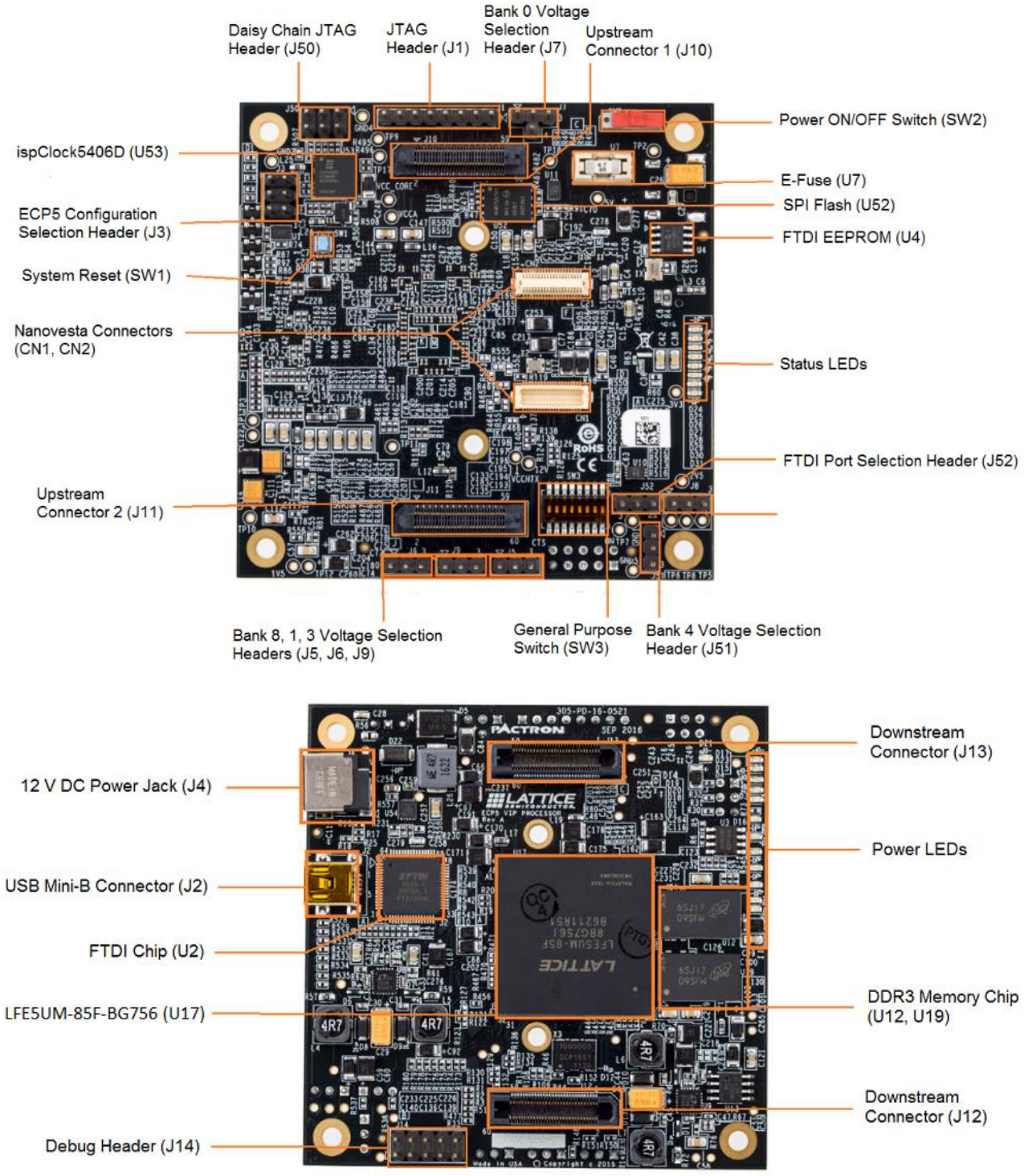

Figure 3.3. Top and Bottom View of ECP5 VIP Processor Board

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3.3. HDMI VIP Output Bridge Board

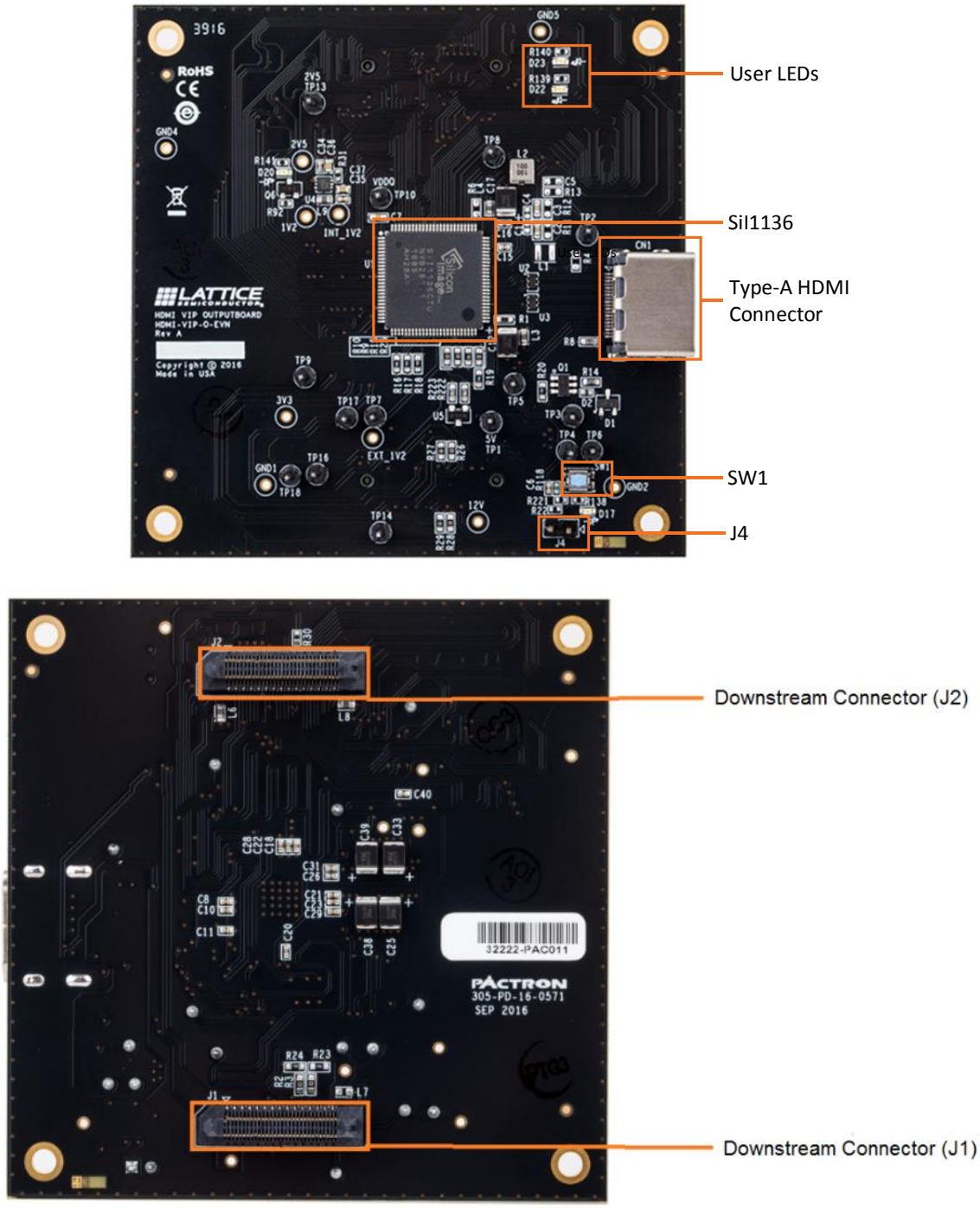

Figure 3.4. Top and Bottom View of HDMI VIP Output Board

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4. Jumper Settings

Table 4.1. CrossLink VIP Input Bridge Board

S. No.	Jumper Name	Description
1	J4	Short
2	J30	Open
3	J2	Short
4	—	All other headers should be kept open.

Table 4.2. ECP5 VIP Processor Board

S. No.	Jumper Name	Description
1	J55	Connect 2 and 3.
2	J51	Connect 1 and 2.
3	J5	Connect 1 and 2.
4	J9	Connect 1 and 2.
6	J6	Connect 1 and 2.
7	J3	Connect 1 and 2, also 5 and 6.
8	J50	Connect 1 and 2, also 3 and 5.
9	J7	Connect 2 and 3.
10	J52	Connect 1 and 2 for SPI, 2 and 3 for JTAG
11	J53	Connect 1 and 2
12	—	All other headers should be kept open.

5. Demo Procedure

To setup demonstration:

1. Connect the ECP5 VIP processor board to the wall socket using 12 V power adapter.
2. Power up the demo kit by turning on SW2 on ECP5 VIP processor board.
3. Connect the HDMI cable from CN1 of HDMI VIP output board to the HDMI display/monitor. The monitor displays the dual camera merged image as shown in Figure 5.1.
4. Press SW2 on the CrossLink VIP input bridge board if the image is not displayed.

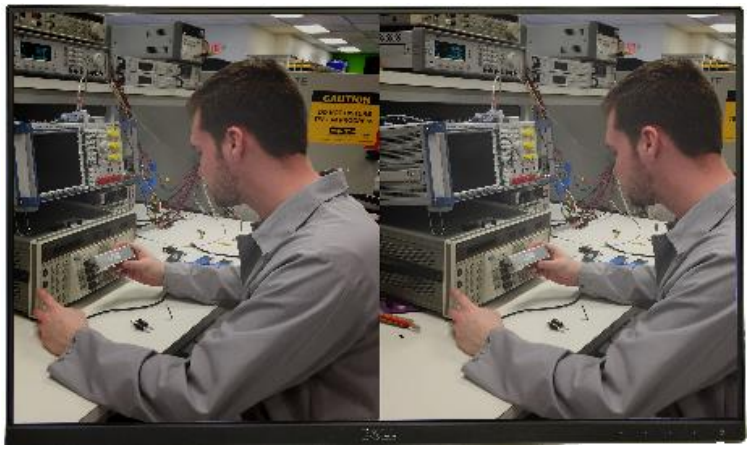

Figure 5.1. Dual Camera merged Image

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6. Demo Package Directory Structure

The demo design is available for CrossLink and ECP5 devices. The packaged design contains a Lattice Diamond project within the *\implementation\ folder configured for the CrossLink device. The “bitstream” folder includes the bit file for programming the CrossLink and ECP5 devices.

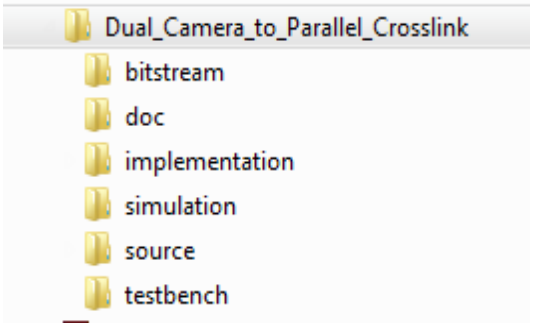

Figure 6.1. Dual Camera to Parallel CrossLink Demo Package Directory Structure

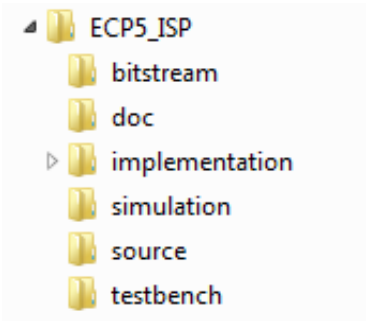

Figure 6.2. ECP5_ISP Demo Package Directory Structure

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7. Pinout Information

7.1. ECP5

Table 7.1 lists the ECP5 pinouts used for the demo.

Table 7.1. ECP5 Pinouts

Port Name	Pin/Bank	Buffer Type	Site	Properties
CSI2_sens_clk	P27/2	LVCMOS33_IN	PR44C	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[0]	A13/0	LVCMOS33_IN	PT42B	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[1]	A8/0	LVCMOS33_IN	PT20B	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[2]	F9/0	LVCMOS33_IN	PT22A	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[3]	D9/0	LVCMOS33_IN	PT22B	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[4]	C9/0	LVCMOS33_IN	PT24A	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[5]	A9/0	LVCMOS33_IN	PT24B	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[6]	C10/0	LVCMOS33_IN	PT29B	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[7]	B10/0	LVCMOS33_IN	PT31A	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[8]	A10/0	LVCMOS33_IN	PT31B	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[9]	E11/0	LVCMOS33_IN	PT33B	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_fv	K27/2	LVCMOS33_IN	PR38A	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_lv	K26/2	LVCMOS33_IN	PR38B	Pull: Down, Clamp: On, Hysteresis: On
HDMI_scl	AG1/8	LVCMOS25_OUT	PB4A	Drive:8 mA, Clamp: On, Slew: Slow
HDMI_sda	AJ1/8	LVCMOS25_OUT	PB6A	Drive:8 mA, Clamp: On, Slew: Slow
XCLR	F4/7	LVCMOS33_OUT	PL14C	Drive:8 mA, Clamp: On, Slew: Slow
clk_out	L1/7	LVCMOS33_OUT	PL29D	Drive:8 mA, Clamp: On, Slew: Slow
config_done	B16/0	LVCMOS33_OUT	PT60A	Drive:8 mA, Clamp: On, Slew: Slow
cross_link_out_1	AK32/4	LVCMOS33_OUT	PB101A	Drive:8 mA, Clamp: On, Slew: Slow
cross_link_out_2	AJ32/4	LVCMOS33_OUT	PB101B	Drive:8 mA, Clamp: On, Slew: Slow
cross_link_out_3	AM30/4	LVCMOS33_OUT	PB103A	Drive:8 mA, Clamp: On, Slew: Slow
cross_link_out_4	AL30/4	LVCMOS33_OUT	PB103B	Drive:8 mA, Clamp: On, Slew: Slow
data_enable	C25/1	LVCMOS33_OUT	PT107A	Drive:8 mA, Clamp: On, Slew: Slow
hsync	D25/1	LVCMOS33_OUT	PT107B	Drive:8 mA, Clamp: On, Slew: Slow
i2c_done	F16/0	LVCMOS33_OUT	PT56A	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[0]	T31/3	LVCMOS33_OUT	PR65B	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[10]	AC32/3	LVCMOS33_OUT	PR92B	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[11]	AD32/3	LVCMOS33_OUT	PR92C	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[1]	R32/3	LVCMOS33_OUT	PR65A	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[2]	Y32/3	LVCMOS33_OUT	PR86B	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[3]	W31/3	LVCMOS33_OUT	PR86A	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[4]	T29/3	LVCMOS33_OUT	PR53C	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[5]	U28/3	LVCMOS33_OUT	PR53D	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[6]	V27/3	LVCMOS33_OUT	PR56C	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[7]	V26/3	LVCMOS33_OUT	PR56D	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[8]	AC31/3	LVCMOS33_OUT	PR89C	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[9]	AB32/3	LVCMOS33_OUT	PR92A	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[0]	AD26/3	LVCMOS33_OUT	PR77D	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[10]	W30/3	LVCMOS33_OUT	PR65C	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[11]	T30/3	LVCMOS33_OUT	PR59D	Drive:8 mA, Clamp: On, Slew: Slow

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Table 7.1. ECP5 Pinouts *(Continued)*

Port Name	Pin/Bank	Buffer Type	Site	Properties
pix_green[1]	T26/3	LVCMOS33_OUT	PR47D	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[2]	R26/3	LVCMOS33_OUT	PR47C	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[3]	A24/1	LVCMOS33_OUT	PT101A	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[4]	T32/3	LVCMOS33_OUT	PR68A	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[5]	AC30/3	LVCMOS33_OUT	PR89A	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[6]	AB31/3	LVCMOS33_OUT	PR89B	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[7]	V32/3	LVCMOS33_OUT	PR68C	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[8]	W32/3	LVCMOS33_OUT	PR68D	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[9]	Y26/3	LVCMOS33_OUT	PR71A	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[0]	AE27/3	LVCMOS33_OUT	PR80B	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[10]	F25/1	LVCMOS33_OUT	PT110B	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[11]	F17/1	LVCMOS33_OUT	PT69B	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[1]	AD27/3	LVCMOS33_OUT	PR80A	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[2]	AB29/3	LVCMOS33_OUT	PR83B	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[3]	AB30/3	LVCMOS33_OUT	PR83A	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[4]	AB28/3	LVCMOS33_OUT	PR77A	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[5]	AB27/3	LVCMOS33_OUT	PR77B	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[6]	AC26/3	LVCMOS33_OUT	PR77C	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[7]	Y27/3	LVCMOS33_OUT	PR71B	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[8]	D24/1	LVCMOS33_OUT	PT103A	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[9]	W28/3	LVCMOS33_OUT	PR71D	Drive:8 mA, Clamp: On, Slew: Slow
pixclk_out	E25/1	LVCMOS33_OUT	PT110A	Drive:8 mA, Clamp: On, Slew: Slow
q	AG30/4	LVCMOS33_OUT	PB114B	Drive:8 mA, Clamp: On, Slew: Slow
reset_crosslink	D13/0	LVCMOS33_OUT	PT40B	Drive:8 mA, Clamp: On, Slew: Slow
reset_n	AH1/8	LVCMOS25_IN	PB4B	Pull: Down, Clamp: On, Hysteresis: On
reset_sensor	B4/0	LVCMOS33_OUT	PT4B	Drive:8 mA, Clamp: On, Slew: Slow
reveal_1	F32/2	LVCMOS33_OUT	PR23C	Drive:8 mA, Clamp: On, Slew: Slow
reveal_2	H32/2	LVCMOS33_OUT	PR23D	Drive:8 mA, Clamp: On, Slew: Slow
reveal_3	C29/2	LVCMOS33_OUT	PR11C	Drive:8 mA, Clamp: On, Slew: Slow
reveal_4	C30/2	LVCMOS33_OUT	PR11D	Drive:8 mA, Clamp: On, Slew: Slow
scl	D15/0	LVCMOS33_OUT	PT51B	Drive:8 mA, Clamp: On, Slew: Slow
scl2	A14/0	LVCMOS33_OUT	PT49B	Drive:8 mA, Clamp: On, Slew: Slow
sda	F15/0	LVCMOS33_OUT	PT51A	Drive:8 mA, Clamp: On, Slew: Slow
sda2	B14/0	LVCMOS33_OUT	PT49A	Drive:8 mA, Clamp: On, Slew: Slow
tp1	AK31/4	LVCMOS33_OUT	PB105A	Drive:8 mA, Clamp: On, Slew: Slow
tp2	AJ31/4	LVCMOS33_OUT	PB105B	Drive:8 mA, Clamp: On, Slew: Slow
tp3	AM31/4	LVCMOS33_OUT	PB107A	Drive:8 mA, Clamp: On, Slew: Slow
tp4	AL32/4	LVCMOS33_OUT	PB107B	Drive:8 mA, Clamp: On, Slew: Slow
vsync	A25/1	LVCMOS33_OUT	PT105A	Drive:8 mA, Clamp: On, Slew: Slow

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7.2. CrossLink

Table 7.2 lists the CrossLink pinouts used for the demo.

Table 7.2. CrossLink Pinouts

Port Name	Pin/Bank	Buffer Type	Site	Properties
clk_n_i	A2/61	DPHY_BIDI	DPHY1_CKN	—
clk_n_i_s	A9/60	DPHY_BIDI	DPHY0_CKN	—
clk_p_i	A1/61	DPHY_BIDI	DPHY1_CKP	—
clk_p_i_s	A8/60	DPHY_BIDI	DPHY0_CKP	—
clkin_reveal	H7/2	LVCMOS25_IN	PB16D	Pull: Up, Clamp: On, Hysteresis: On
clkout_reveal	D9/2	LVCMOS25_OUT	PB16A	Drive: 6 mA, Clamp: On
d0_n_i	B2/61	DPHY_BIDI	DPHY1_DN0	—
d0_n_i_s	A7/60	DPHY_BIDI	DPHY0_DN0	—
d0_p_i	B1/61	DPHY_BIDI	DPHY1_DP0	—
d0_p_i_s	B7/60	DPHY_BIDI	DPHY0_DP0	—
d1_n_i	B3/61	DPHY_BIDI	DPHY1_DN1	—
d1_n_i_s	B9/60	DPHY_BIDI	DPHY0_DN1	—
d1_p_i	A3/61	DPHY_BIDI	DPHY1_DP1	—
d1_p_i_s	B8/60	DPHY_BIDI	DPHY0_DP1	—
d2_n_i	C2/61	DPHY_BIDI	DPHY1_DN2	—
d2_n_i_s	A6/60	DPHY_BIDI	DPHY0_DN2	—
d2_p_i	C1/61	DPHY_BIDI	DPHY1_DP2	—
d2_p_i_s	B6/60	DPHY_BIDI	DPHY0_DP2	—
d3_n_i	B4/61	DPHY_BIDI	DPHY1_DN3	—
d3_n_i_s	C9/60	DPHY_BIDI	DPHY0_DN3	—
d3_p_i	A4/61	DPHY_BIDI	DPHY1_DP3	—
d3_p_i_s	C8/60	DPHY_BIDI	DPHY0_DP3	—
fv	J3/1	LVCMOS25_OUT	PB43C	Drive: 6 mA, Clamp: On
lv	H3/1	LVCMOS25_OUT	PB43D	Drive: 6 mA, Clamp: On
pixdata[0]	F9/2	LVCMOS25_OUT	PB2A	Drive: 6 mA, Clamp: On
pixdata[1]	F8/2	LVCMOS25_OUT	PB2B	Drive: 6 mA, Clamp: On
pixdata[2]	G9/2	LVCMOS25_OUT	PB2C	Drive: 6 mA, Clamp: On
pixdata[3]	G8/2	LVCMOS25_OUT	PB2D	Drive: 6 mA, Clamp: On
pixdata[4]	E9/2	LVCMOS25_OUT	PB6A	Drive: 6 mA, Clamp: On
pixdata[5]	E8/2	LVCMOS25_OUT	PB6B	Drive: 6 mA, Clamp: On
pixdata[6]	H9/2	LVCMOS25_OUT	PB6C	Drive: 6 mA, Clamp: On
pixdata[7]	H8/2	LVCMOS25_OUT	PB6D	Drive: 6 mA, Clamp: On
pixdata[8]	F7/2	LVCMOS25_OUT	PB12A	Drive: 6 mA, Clamp: On
pixdata[9]	E7/2	LVCMOS25_OUT	PB12B	Drive: 6 mA, Clamp: On
pixel_clk	J6/1	LVCMOS25_OUT	PB29C	Drive: 6 mA, Clamp: On
reset_n_i	J4/1	LVCMOS25_IN	PB38C	Pull: Up, Clamp: On, Hysteresis: On
tp1	D2/1	LVCMOS25_OUT	PB34B	Drive: 6 mA, Clamp: On
tp2	H6/1	LVCMOS25_OUT	PB29D	Drive: 6 mA, Clamp: On
tp3	G7/1	LVCMOS25_OUT	PB29A	Drive: 6 mA, Clamp: On
tp4	E2/1	LVCMOS25_OUT	PB38B	Drive: 6 mA, Clamp: On
tp5	J9/2	LVCMOS25_OUT	PB12C	Drive: 6 mA, Clamp: On
tp6	H4/1	LVCMOS25_OUT	PB38D	Drive: 6 mA, Clamp: On
tp7	H5/1	LVCMOS25_OUT	PB34D	Drive: 6 mA, Clamp: On
tp8	G6/1	LVCMOS25_OUT	PB29B	Drive: 6 mA, Clamp: On

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8. Ordering Information

Table 8.1. Ordering Information

Description	Ordering Part Number
Lattice Embedded Vision Development Kit	LF-EVDK1-EVN

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References

For more information, refer to:

- FPGA-DS-02012 (previously DS1044), ECP5 and ECP5-5G Family Data Sheet
- FPGA-DS-02007, CrossLink Family Data Sheet
- SiI-DS-1084, SiI9136-3/SiI1136 HDMI Deep Color Transmitter

For schematics, refer to:

- FPGA-EB-02001, ECP5 VIP Processor Board
- FPGA-EB-02002, CrossLink VIP Input Bridge Board
- FPGA-EB-02003, HDMI VIP Output Bridge Board

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

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Appendix A. Lattice Embedded Vision Development Kit Setup

Follow these steps to set up the display demo boards:

1. Connect J3 and J1 connector of CrossLink VIP input bridge board to J10 and J11 connector of ECP5 VIP board.
2. Connect J13 and J12 connector of ECP5 VIP board to J2 and J1 of HDMI VIP output board.
3. Connect one end of HDMI cable to C1 connector of HDMI VIP output board and the other end to monitor.
4. Connect the 12 V wall power adapter cable to J4 of ECP5 VIP board.
5. Open two Standalone Lattice Diamond Programmer windows, for CrossLink and ECP5.
6. ECP5 is detected when you scan the board through Lattice Diamond Programmer.
7. Program the ECP5 FPGA.
8. To scan the CrossLink pASSP, remove jumper J4 of CrossLink VIP input bridge board, and scan the device through Lattice Diamond Programmer.
9. When the CrossLink device is scanned, place J4 jumper.
10. Program the CrossLink pASSP.

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Revision History

Date	Version	Change Summary
April 2017	1.0	Initial release.

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7th Floor, 111 SW 5th Avenue
Portland, OR 97204, USA
T 503.268.8000
www.latticesemi.com