Electrostatic Discharge (ESD) Concerns for Ceramic Capacitors

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INTRODUCTION

"Static electricity" is defined as an electrical charge caused by an imbalance of electrons on the surface of a material. The imbalance of electrons produces an electric field that can be measured and that can influence other objects at a distance. "Electrostatic discharge" is defined as the transfer of charge between bodies at different electric potentials. Electrostatic discharge has been a concern for a long time. In the 1400's, static control procedures were needed to keep black powder from exploding in military forts. In the 1800's special ESD preventative techniques were introduced in paper mills. We are all familiar with the electrical shocks we feel on dry days. Charges build up on our bodies, and when we touch a grounded device like a light switch, we feel the shock. An interesting point, if we can feel the ESD discharge, it is probably over 3000 volts. If we can see the ESD discharge, it is probably over 6000 volts.

Electrostatic Discharge [ESD] has also long been associated with the manufacture and test of electronic circuits. Many of the semiconductor-based components are among the most sensitive to ESD events. Some devices [EPROM, Mosfet, GaAsfet, for example] are damaged by relatively low voltage ESD pulses - 100 to 300 volts. Others are only slightly better [VMOS, Op-Amps, Schottky Diodes, for example] are damaged by ESD pulses in the 190 to 3000 volt ranges [Ref. 2]. As a result, these parts and the circuits they are used in are carefully protected from ESD pulses.

Capacitors have mostly been considered immune from ESD pulses. Failures of capacitors seldom, if ever have been associated with ESD pulses. While there have been test methods called out in some of the automotive qualification specifications [Ref. 3], these tests primarily defined a method of testing. ESD capability requirements were only rarely specified. The reason for this general lack of concern is probably related to the relative ESD robustness of capacitors when compared to the semiconductor-based parts. In many cases, because capacitors are capable of absorbing the higher energy pulses, they themselves have been used in input line applications to reduce ESD pulse voltages to levels that the following circuitry could handle. Capacitors were far from the chief ESD concern.

What is different today? In our continuing competitive and cost conscious industry, many of the circuits are being grouped into sometimes-unlikely combinations. These are being sent to contract manufacturers for assembly. In some cases, parts themselves are being consolidated. For example, it is becoming quite common to include capacitors for filter and decoupling applications in connectors. As the major automotive OEM hands off the responsibility for the subassembly, it is common to provide specifications for its performance. These specifications sometime include ESD tests and requirements that are the same as system-level capabilities. The capacitors in this part of the circuit are commonly lower capacitance value parts. These previously were not subjected to the same level of ESD. In the same vein of cost and competition, many of the applications are being down sized. The 1206 size chip has given way to the 0805 size, and in many applications is being superseded by the 0603 size. There is more concern for the smaller chips ESD capability. Questions arise as to the proper ESD test value and the capability of the part in withstanding these levels.

Failed parts from applications have not been linked to ESD damage. However, in the tests at higher ESD pulse levels, ESD failures can occur. There appears to be an increase in interest in knowing what levels of ESD voltage capacitors can withstand, and the dynamics involved.

OBJECTIVES

KEMET became interested in ceramic capacitors capability to withstand ESD pulses a few years back. This paper reports on an expansion of the work first presented at CARTS '96 by John Prymak [Ref. 1]. We will explore:

1. ESD test methods - this will be very brief as these are well documented in other publications.
2. A review of the method of determining the voltage applied to capacitors as a result of ESD voltage pulses.
3. Analysis and prediction of the effect of parameters that may affect the ability of the part to withstand ESD voltage levels.

ESD TEST METHODS

The methods of testing parts for ESD damage are defined in IEC 801-2 and some automotive sector specifications. These sector specifications have been combined lately in the Automotive Electronics Council document AEC Q 200 [Ref. 3]. Many test models have been proposed. There are two prominent models. The first is the Human Body Model [HBM]. The HBM is designed to emulate the effect of discharge from the electrostatic build up on the human body to the circuit under test. The second is the Machine Model [MM], designed to emulate the effect of discharge from machines into the circuit. The HBM is most commonly called out in qualification specifications.

During ESD testing a source capacitor is charged up to the test voltage level. The source capacitor is then discharged into the capacitor on test. The source capacitor value is important, as it plays a role in determining the voltage applied to the capacitor under test. AEC Q200 defines the source capacitor for the HBM to be 150 pF. There are various voltage test levels. For Direct Contact testing [the source capacitor circuit is in direct contact with the capacitor or part under test], the voltage levels are specified as ranging from 1000 volts to 8000 volts. For Air Discharge testing [the voltage is first discharged through air and then through the capacitor under test], the voltage levels are specified as ranging from 12,000 to 25,000 volts. The selection of voltage levels for direct contact and air discharge testing probably lies in the ESD event itself. In practice, if an object is charged to voltages higher than 8000 [possibly as low as 6000], it will cause a discharge [spark] in air. This will occur prior to being able to discharge through the part. One of the unique features of the ESD event is the extremely fast rise time and short duration of the pulse. There is also a potential for variation in results depending on the connection methods and wire lengths. The inductance of these lead lengths can cause quite a variation in current magnitudes. There is a lot more information regarding these tests in the literature for those who are interested in more theory and details.

APPLIED VOLTAGE LEVELS

John Prymak reported on an analytical method of determining the actual voltage applied to the capacitor when ESD pulses are applied [Ref. 1]. The theory is simple. Conservation of Charge must apply. The charge [Q in coulombs] of the source capacitor is easily calculated as the capacitance value times the voltage applied. It may be good to look at examples. The source capacitor is defined as 150 pF. Let's work with an ESD test voltage of 8000 volts. The charge would be 150×10^{-9} times 8000 volts, or 1.2 micro coulombs. As the voltage is discharged into the capacitor under test, the charge must be conserved. That is the final charge must also equal 1.2 micro coulombs. In the final circuit configuration, the total capacitance is made up of the source capacitance plus the test capacitance. The voltage can be calculated by dividing the charge by the total capacitance. Going back to our example, the charge is 1.2 micro coulombs. If the capacitor under test is 1000 pF, the total capacitance will be 150 plus 1000 or 1150 pF. The voltage applied is then $1.2 \times 10^{-6} / 1150 \times 10^{-9}$, or 1043 volts. It is easy to see that the value of the capacitor under test is a determinate value in the final voltage. These are simple calculations. For ideal capacitors, the results are easily shown in graphical form. In Figure 1, the applied voltage as a result of ESD pulses is plotted for the lower range of capacitance values. These values are typically C0G dielectric, and primarily used in applications such as timing and filtering circuits. Figure 2 and 3 show the same information for a slightly higher range of capacitance values. These could be either X7R or C0G dielectric. This range is primarily used in input and output filtering circuits. Figure 4 again shows the same information for the higher ranges of ceramic capacitors, commonly used as decoupling capacitors. Again, all of these plots are for ideal capacitors and do not consider performance characteristics that may affect these calculations. In addition, they do not consider the effect of air discharge across the terminations in air, which also will limit the voltage applied (more about this later).

Important conclusions…

a) For a specific ESD test level, the lower the value of the capacitance under test, the greater the voltage applied.

b) Higher values of capacitance can withstand higher levels of ESD pulses.

c) A good estimate of voltage applied to ideal capacitors as a result of ESD pulses can be made.

d) The actual applied voltage is also limited by air discharge, which is a function of the case size.

CAPACITOR CAPABILITIES

With some idea on how much voltage might be applied to the capacitor in an ESD test pulse, the next step is to estimate if the capacitor can withstand this level. The ESD pulse event is a very unique transient, having very fast rise times and a very short duration. Since the ESD capability is dependent on the capacitor value and the dielectric material, a very large number of tests would be required. We have thought it might not be important to estimate the ESD capability of each part. Given the performance of a few parts, and information

about the effects of the various parameters, judgment can be made about increasing or decreasing ESD capability. The voltage rating, dielectric materials, chip sizes, and voltage coefficients were investigated to determine their impact on the relative ESD capability.

- ***Dielectric materials and Rated Voltage***

The equation that establishes the capacitance value is simple:

$$C \sim A[n-1]/t$$

The capacitance is proportional to the area of one electrode [A], times the number of active layers [n-1], divided by the thickness of one layer [t]. The voltage rating is also proportional to the dielectric thickness [t]. Higher voltage ratings require thicker dielectric layers. The number of layers and electrode area are limited by the size of the chip. Increasing the dielectric thickness [for increased voltage ratings] will reduce the maximum capacitance value available in that size and voltage rating. This is further illustrated in the following tables of maximum capacitance ratings from one manufacture.

Table 1. Maximum capacitance in pF (C0G).

	200 V	100 V	50 V
1206	22,000	100,000	220,000
0805	6,800	22,000	100,000
0603	560	4,700	22,000

Table 2. Maximum capacitance in pF (X7R).

	200 V	100 V	50 V
1206	22,000	100,000	220,000
0805	6,800	22,000	100,000
0603	560	4,700	22,000

Ceramic capacitors are traditionally over designed when it comes to voltage ratings. This over design is much greater in the lower capacitor values in particular. Over design has become a 'fact of life'. Ceramic capacitors are tested at higher multiples of rated voltage than any other capacitor family. Ceramic capacitors also are recognized as being able to withstand very high voltage transients. These tests include outgoing inspection tests, qualification tests, and evaluation tests. The test that is commonly used to evaluate the ceramic dielectric materials capability of withstanding high voltages is the "Ultimate Voltage Breakdown" test, or simply "UVBD." In this test, continuously increasing voltage pulses are applied to the capacitor, until the dielectric breaks down, and the capacitor becomes a short circuit. These pulses are much longer in duration than those of an ESD pulse, and have a greater effect on the dielectric at lower peaks. However, the relative UVBD capabilities indicate the impact of various materials and designs on the ESD capability. During UVBD testing, the dielectric will breakdown along the grain boundaries. Variation in grain boundaries results in variations in the UVBD values [see Figure 5]. [Dielectric voids and other defects that are large enough to affect the UVBD results are largely eliminated in standard Insulation Resistance and Dielectric Strength tests]. Thicker dielectric layers will increase the UVBD values, as the distance along the grain boundaries is greater. The UVBD values of C0G dielectric materials will also be higher than that for X7R with the same voltage ratings. This is a result of the denser grains of the C0G. The failure signature is also different for UVBD failures than it is for ESD failures. The UVBD failure typically results in a spider web of cracks emanating from a spot breakdown area. This is typical of an Electrical Overstress {EOS} failure. The ESD failure signature is typically a single crack emanating from the tip of one of the electrodes and traveling to the nearest adjacent electrode. This is typical of the unique very fast ESD event.

A good way to visualize UVBD data is in a histogram format. Histogram data of C0G and X7R capacitors at various voltage ratings are presented in Figures 6 through 11. Calculations are shown for the mean, maximum, minimum, standard deviations, and mean - 3 sigma data points. The mean - 3 sigma points are plotted versus the voltage rating for C0G and X7R dielectric materials in Figure 12. While the failure signature is different for UVBD compared to UVBD, some conclusions can still be drawn.

Important conclusions …

a) C0G will withstand higher levels of ESD for the same voltage rating and capacitance value.

b) Higher voltage ratings are important if higher ESD levels were going to be involved [200 volts would be ideal].

c) For the same chip size, as the voltage rating increases, the maximum capacitance available decreases.

- ***Chip Size***

Chip size is another important variable. From the capacitance value tables above, the maximum capacitance value available in the same voltage rating decreases as the chip size decreases. This should also be apparent from observation of the capacitance equation. Smaller physical size will result in less electrode area. However, if the capacitance value, in

the same voltage rating, is available in a smaller size, the ESD capabilities should be the same. [Except for one caveat, external air discharges - see more below.]

One of the competitive factors in today's competitive market is product miniaturization. This drives the designer to look at ever reducing chip sizes. Reducing the chip capacitor size in ESD critical applications may reduce its ESD capability level. For example, if the desired capacitance cannot be achieved in the smaller chip with the higher voltage rating, it is tempting to reduce the voltage rating to maintain the same capacitance value. As we have seen above, this will reduce the ESD capability level. Another approach is to reduce the capacitance value so that the higher voltage rating may be kept. Again, this may reduce the ESD capability level. In addition, from a capacitor designer view, some of the over design factors need to be removed. Less total electrode area is available, so dielectric thickness needs to be reduced to get equivalent capacitance values. The part is still more than capable of the design voltage rating, but the over design capabilities are reduced.

Reduction of chip size in ESD critical applications can be taken too far. The termination bands for smaller chips are closer to each other. For the smaller size [0603 and even 0805] chips, the air [also a dielectric] may breakdown [spark] prior to any failure in the capacitor. This effect takes place long before the expected dielectric breakdown level of air is reached. This is an interesting characteristic, and if the breakdown of air can be made to be consistent, then this would protect the capacitor. This is not as easy as it seems. The dielectric characteristic of air is highly dependent on the relative humidity and cleanliness of the air. In addition, the surface of the capacitor is not to be coated with other materials [conformal coats, potting materials, etc.]. Cleanliness of the capacitor surface itself also can play a role. Experience also shows that ESD test personnel are not comfortable with this air breakdown and may classify them as failures during the tests.

Important conclusions:

a) Chip size has little effect on basic ESD capability, providing the same capacitance value is available at the same voltage rating.

b) For smaller chip sizes, the maximum available capacitance at the same voltage rating decreases.

c) Reduction of chip size should be evaluated carefully for ESD critical applications. This is especially true if it is necessary to trade off voltage rating or capacitance value.

d) Use of 0603 chip sizes will most likely result in lower ESD levels. Air Breakdown is a factor to be considered.

e) Chip sizes smaller than 0603 should not be used in ESD critical applications.

f) Putting all this together, if a high ESD voltage requirement is imposed, the best choice is 1206 chip size with a 200-volt rating.

- ***Voltage Coefficient***

C0G dielectric materials are close to ideal. The capacitance value is not affected by changes in ambient temperature, applied voltage, or other application related items. If the capacitance value required is available in the necessary voltage rating, C0G should always be the first choice.

X7R (and Y5V) dielectric materials are ferroelectric materials. As a result, the dielectric constant varies as a result of external stimuli such as temperature and voltage. Variation of capacitance with temperature is a well-known characteristic. This should have little affect though as the sources of ESD charge are not as likely to be getting near the product when it is at - 55 C or + 125 C. Variation of capacitance with applied voltage [described as the voltage coefficient] is a much less remembered characteristic. For X7R [as well as Y5V] as the applied voltage is increased, the capacitance value is decreased. Typical voltage coefficients (capacitance reduction from 0 VDC to Rated VDC) run in the neighborhood of - 20 to - 30 %. However, the resultant voltages from ESD pulses are much greater than the rated voltage. See Figures 13 and 14 for measured and extrapolated voltage coefficient curves. Since the capacitance decays as voltage is applied, the calculation of charge and voltage is not as straight forward as it was for the ideal capacitor. The calculation now involves integration:

$$C = \int CV + VdC/dV$$

Where then term “dC/dV” represents the changing capacitance with changing voltage. In figure 15, the applied voltage as a result of ESD pulses is shown when calculated as above. The range of capacitance values shown is the mid range X7R values. The ideal response for these values was shown in Figure 3. In Figure 16, the ideal and non- ideal responses are compared for a 2,200-pF capacitance value.

Voltage coefficients also vary with the dielectric thickness. Thinner dielectric layers [lower voltage ratings], have greater voltage coefficients. This effect is shown in Figure 17. The 200-volt rating again shows superior performance. Smaller size chips also might use thinner dielectric layers for the same voltage

rating. This would also influence the voltage coefficient.

Y5V dielectric materials have a greater voltage coefficient than X7R dielectric materials. Figure 18 shows this impact on final voltage, the Y5V dielectric materials having a greater impact. Y5V dielectric materials are primarily used for higher value capacitors, but in some cases, they are used in place of X7R to reduce costs.

- ***Important Conclusions***
  - C0G dielectric materials are close to ideal, and are not affected by voltage coefficients.
  - X7R dielectric materials are Ferro electric. This effect increases the voltage applied.
  - Y5V dielectric materials are also Ferro electric. The impact of voltage coefficient is greater.
  - Higher voltage ratings are again desirable to reduce the impact of the voltage coefficient on the voltage applied.
  - Smaller size chips may also influence the impact of the voltage coefficient

OVERALL SUMMATION

Ceramic capacitors can still be considered immune from ESD pulses under almost all conditions.

In electronic circuits, where it is necessary to provide ESD protection because of semiconductor ESD capabilities, it is not necessary to be concerned about the ESD capabilities of capacitors.

Failures of capacitors in applications have not been isolated to ESD pulses. [Billions of parts are used every year in all types of applications.]

Failures of capacitors may occur in ESD test situations when the ESD pulse level is very high, and the capacitance value is low.

For specific ESD type applications, a best choice selection of capacitor can be made based on known relationships.

Parts with C0G dielectric materials will perform better than X7R and Y5V of the same capacitance value, voltage rating, and chip size. Superior UVBD performance is one of the reasons. The other is the Ferro electric properties of the X7R and Y5V.

For critical ESD applications, choose 1206 size chips. The use of 0805 size may be tolerable. Use of 0603 size requires careful evaluation, and the result most likely will be a lower ESD capability. 0402 size chips should not be used in ESD critical applications.

Protective coating (for example, conformal coats and potting) can eliminate the protective spark gap mechanism. In critical ESD applications, these should be avoided.

References:

1. ESD Susceptibility of Ceramic Multilayer Capacitors - J. Prymak an Phil Stair , CARTS 1996
2. Basics of Electrostatic Discharge" by The ESD Association Special to Compliance Engineering Magazine from The ESD Association Web Site @ http:\\www.eosesd.org
3. CDF - AEC - Q200 Rev. A, dated August 18, 1997 -- Attachment 2, available from the Automotive Electronics Council.

Human Body Model (150 pF) Final Voltage
Ideal (C0G) Capacitance [low-C range]

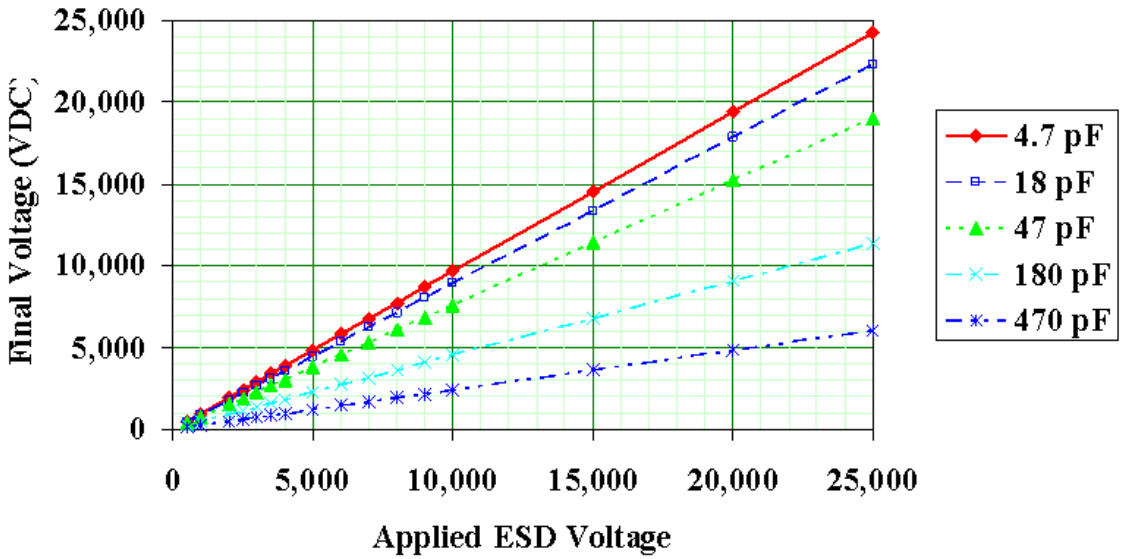

Figure 1

Human Body Model (150 pF) Final Voltage
Ideal (C0G) Capacitance [mid-C range-1]

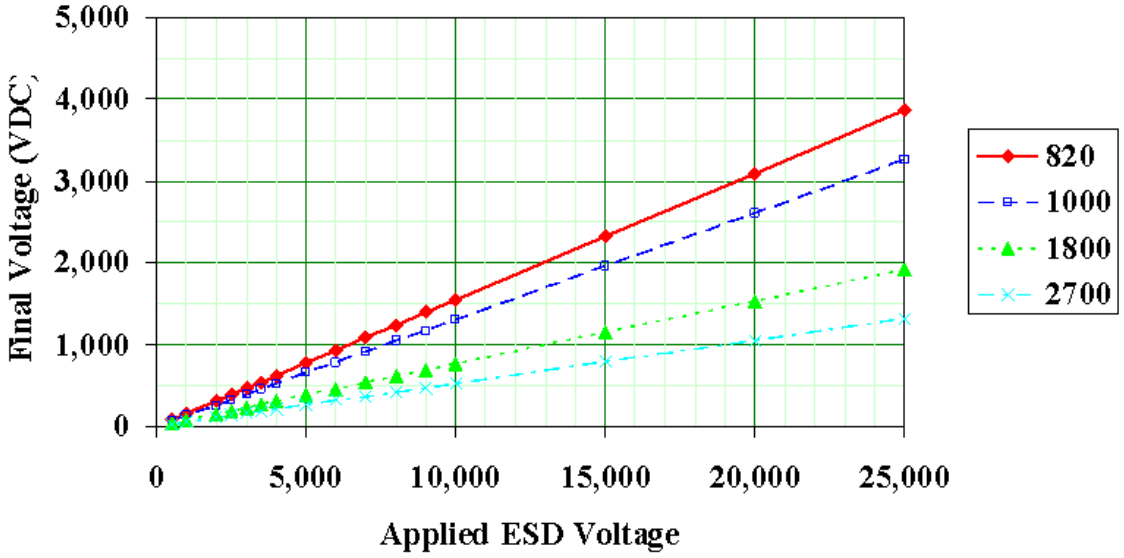

Figure 2

Human Body Model (150 pF) Final Voltage
Ideal (C0G) Capacitance [mid-C range-2]

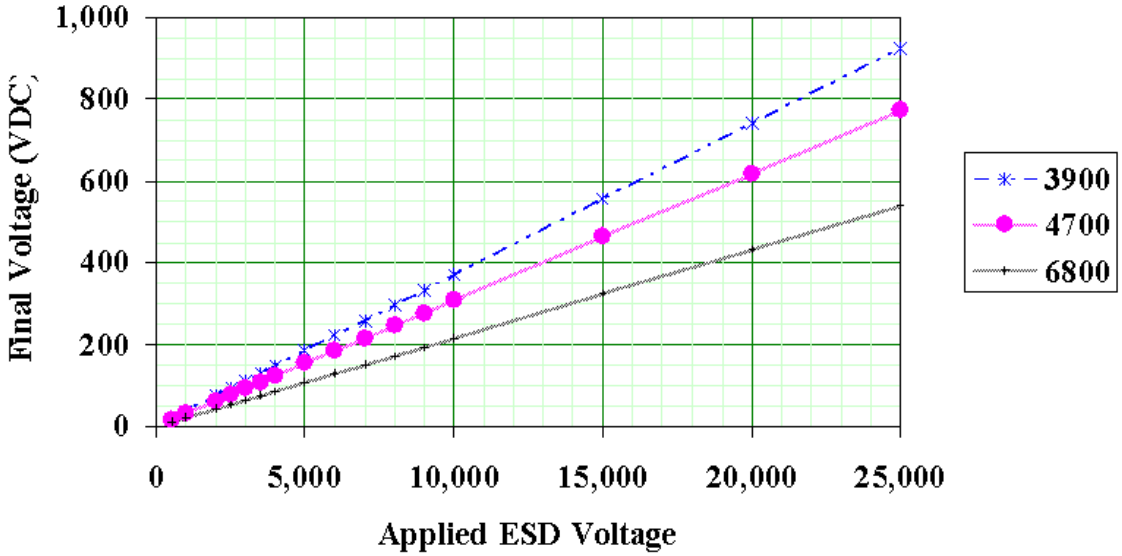

Figure 3

Human Body Model (150 pF) Final Voltage
Ideal (C0G) Capacitance [decoupling range]

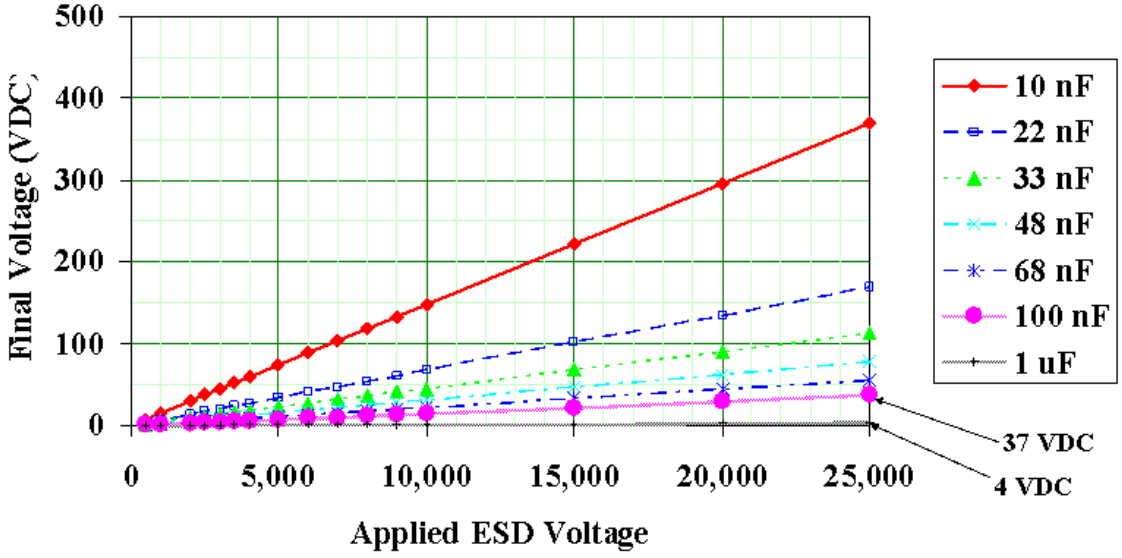

Figure 4

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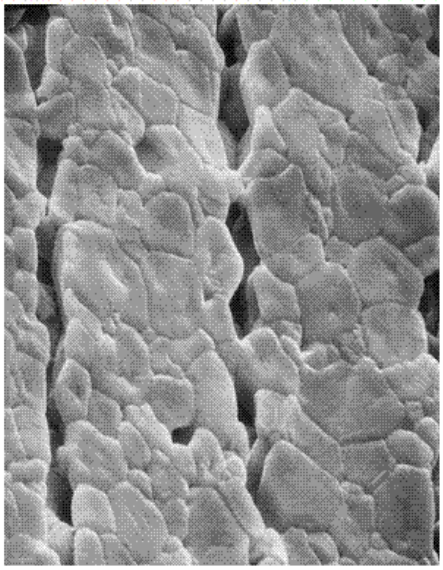
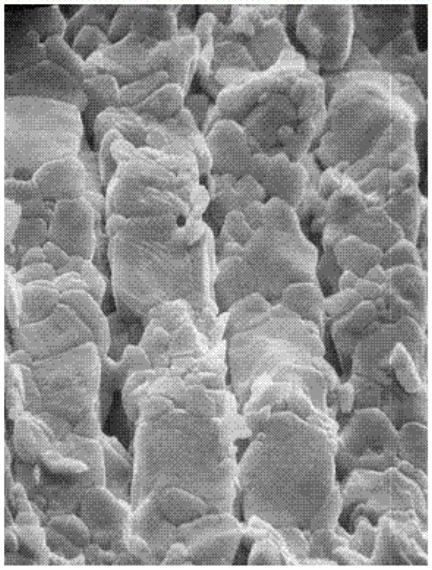
Grains of ceramic dielectric





6 micron **3 micron**

Figure 5

UVBD Histogram ... 100 Volt C0G

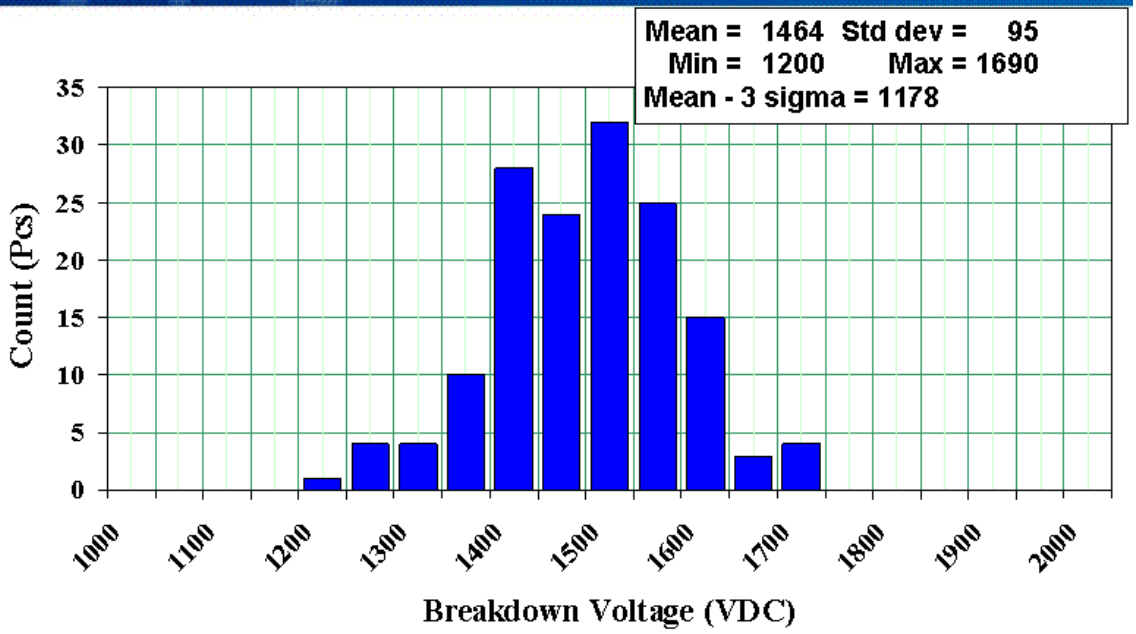


Figure 6

UVBD Histogram ... 50 Volt C0G

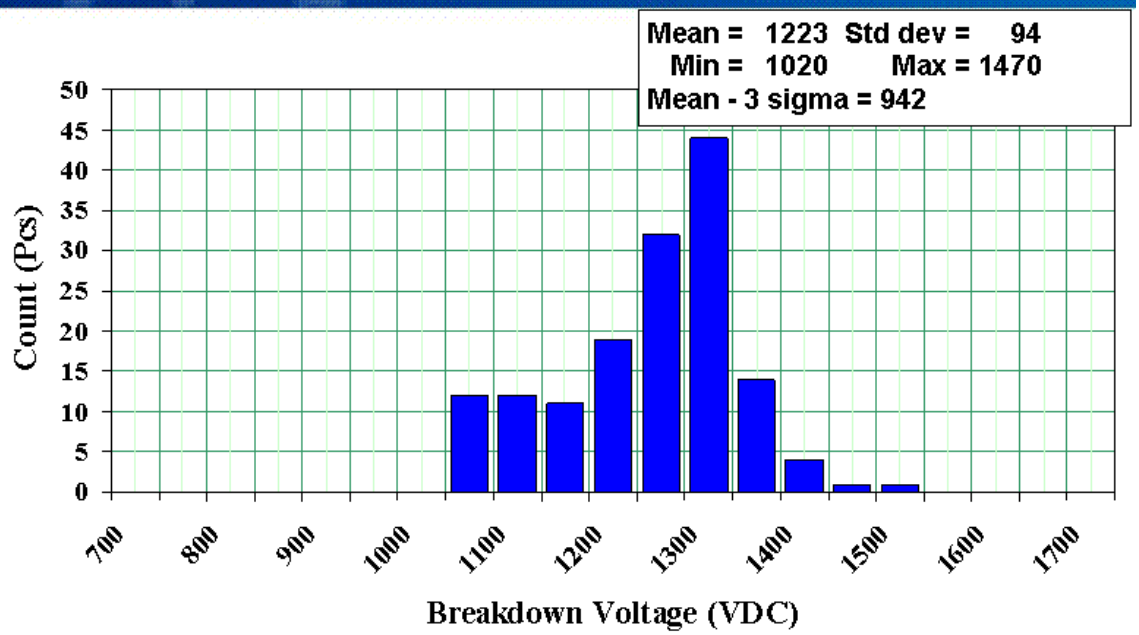


Figure 7

UVBD Histogram ... 200 Volt X7R

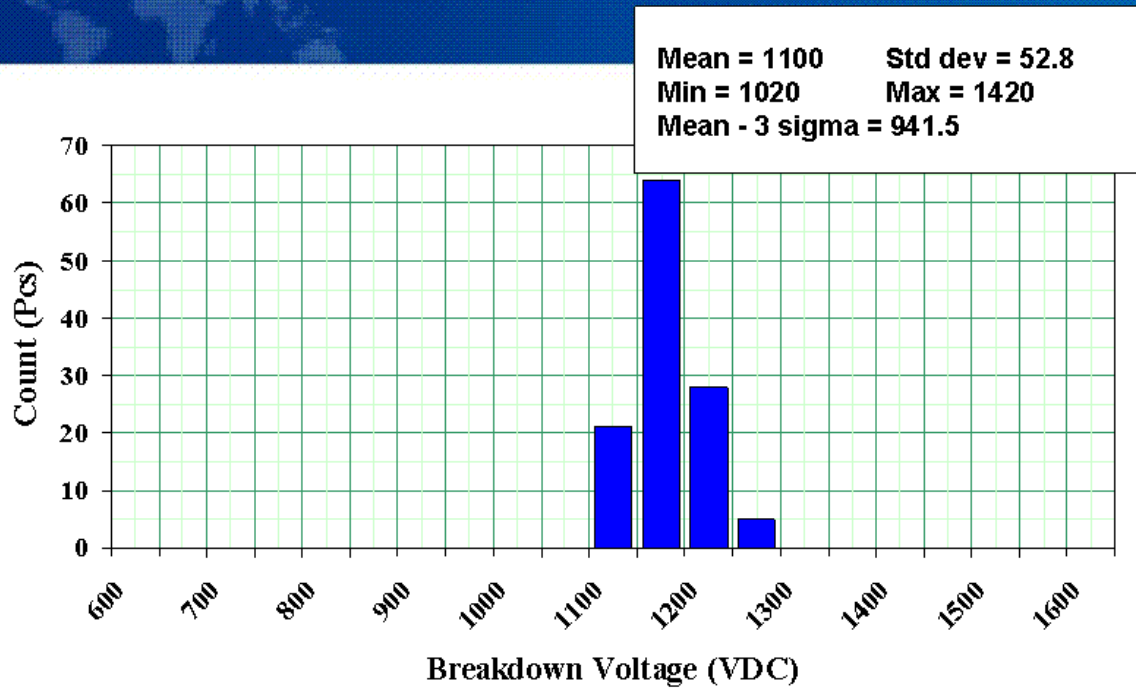


Figure 8

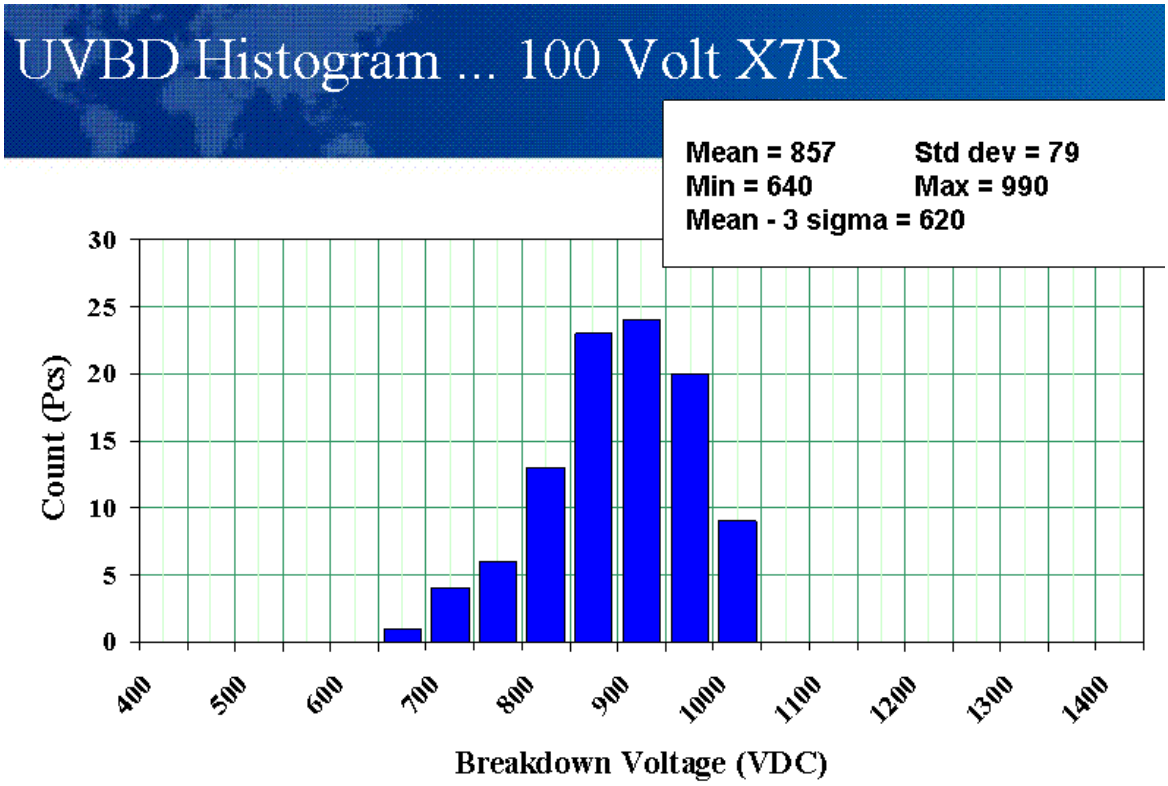


Figure 9

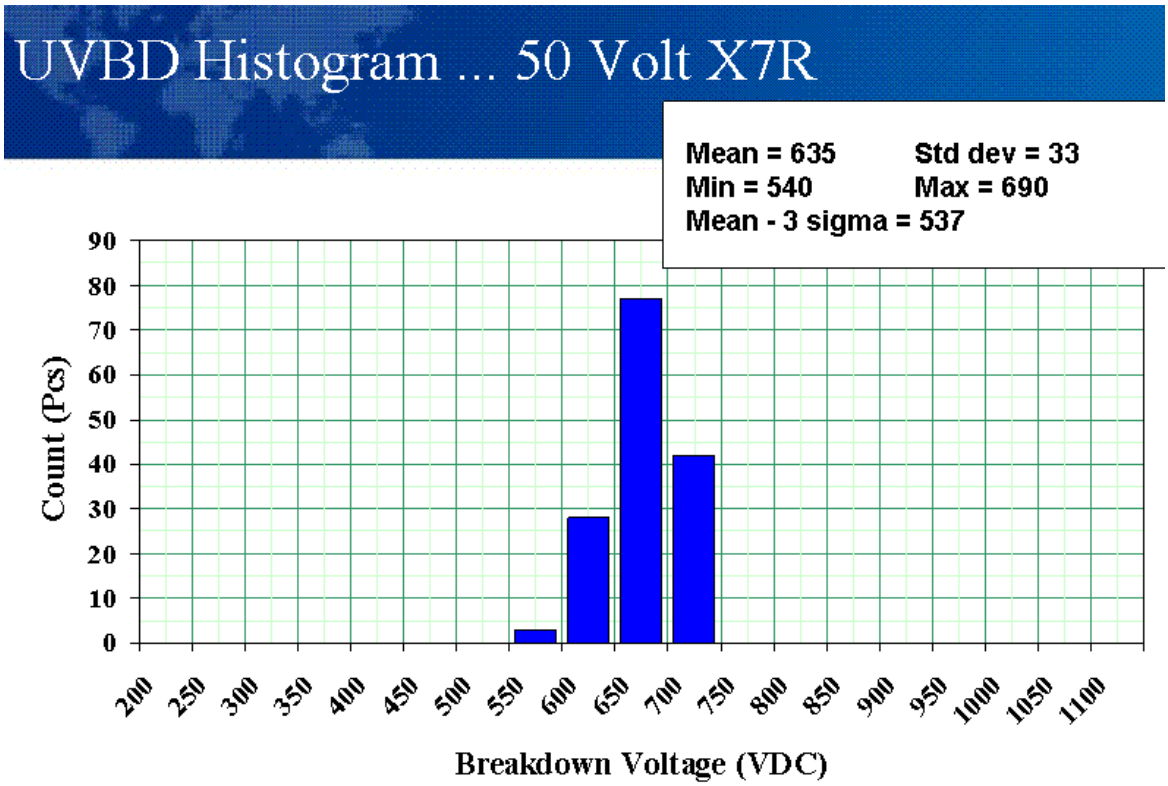


Figure 10

UVBD Histogram ... 16 Volt X7R

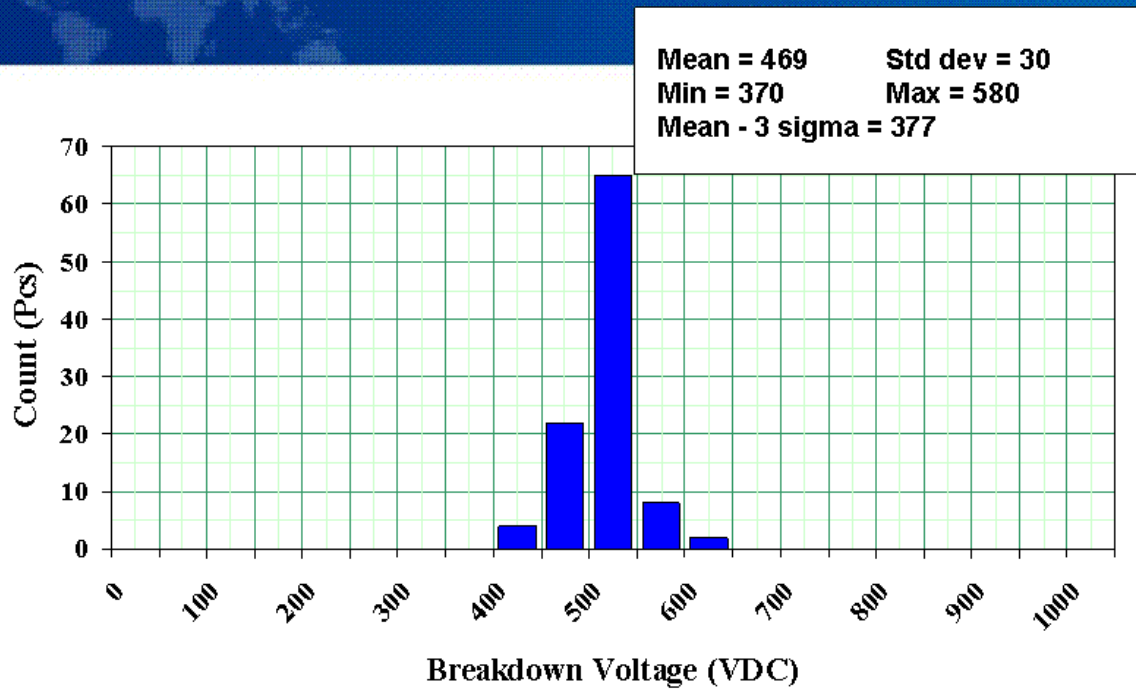


Figure 11

UVBD range vs. Volt. Ratings C0G

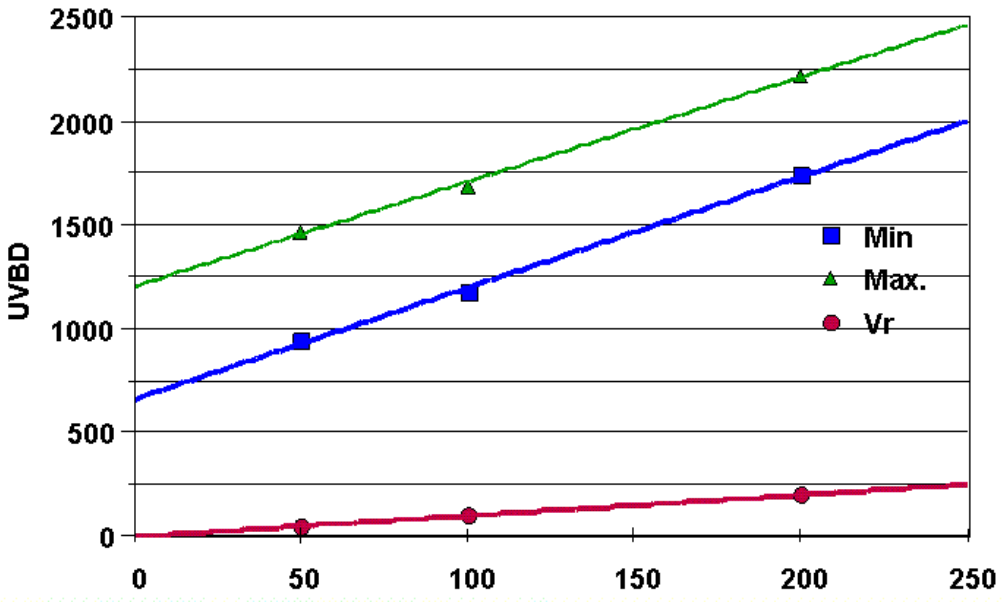


Figure 12

Measured Voltage Coefficient

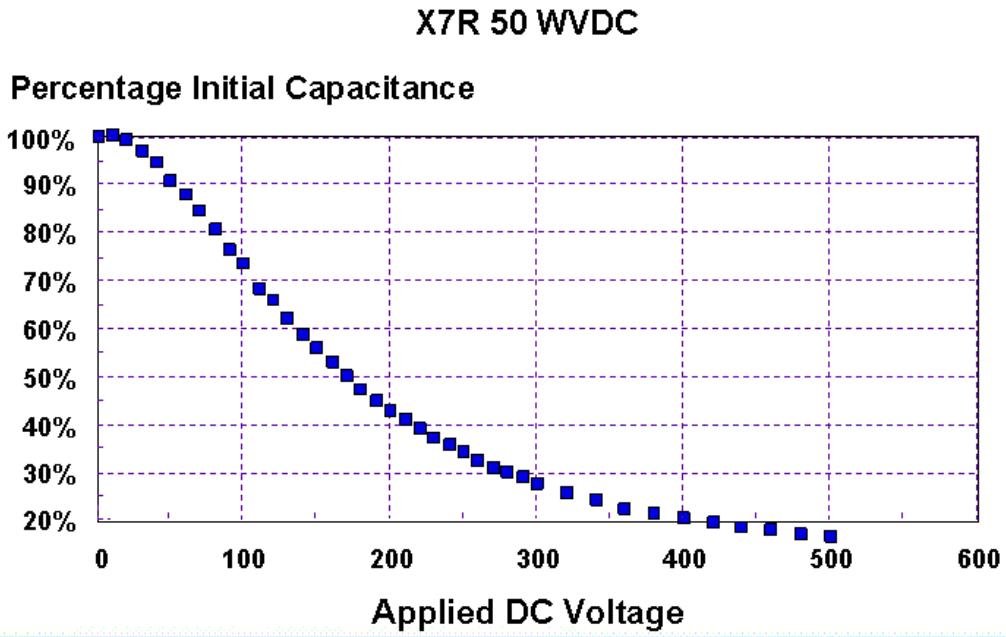


Figure 13

Voltage Stress Extrapolated (X7R & Y5V)

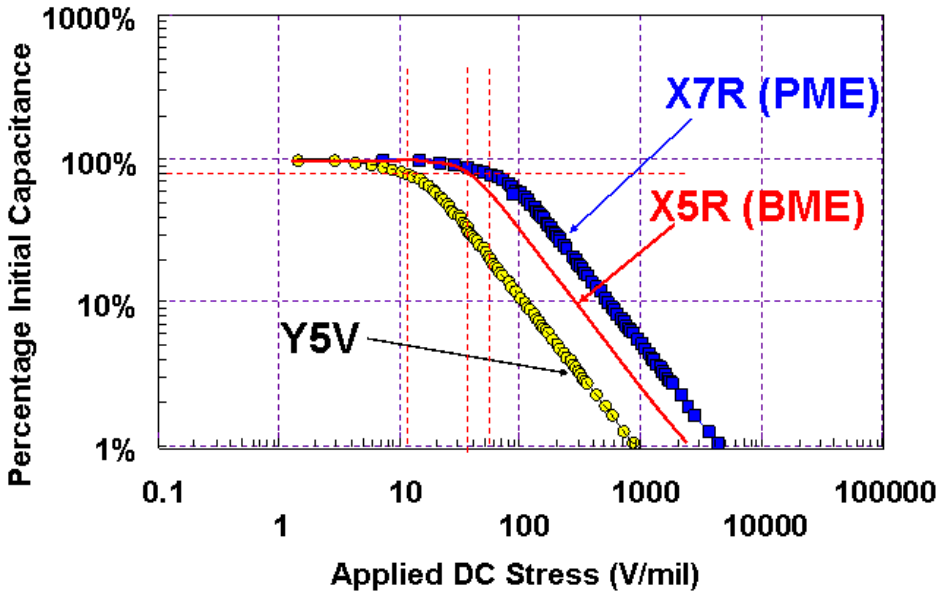


Figure 14

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Final vs. Applied Voltage
X7R – 100 WVDC Designs vs. Capacitance

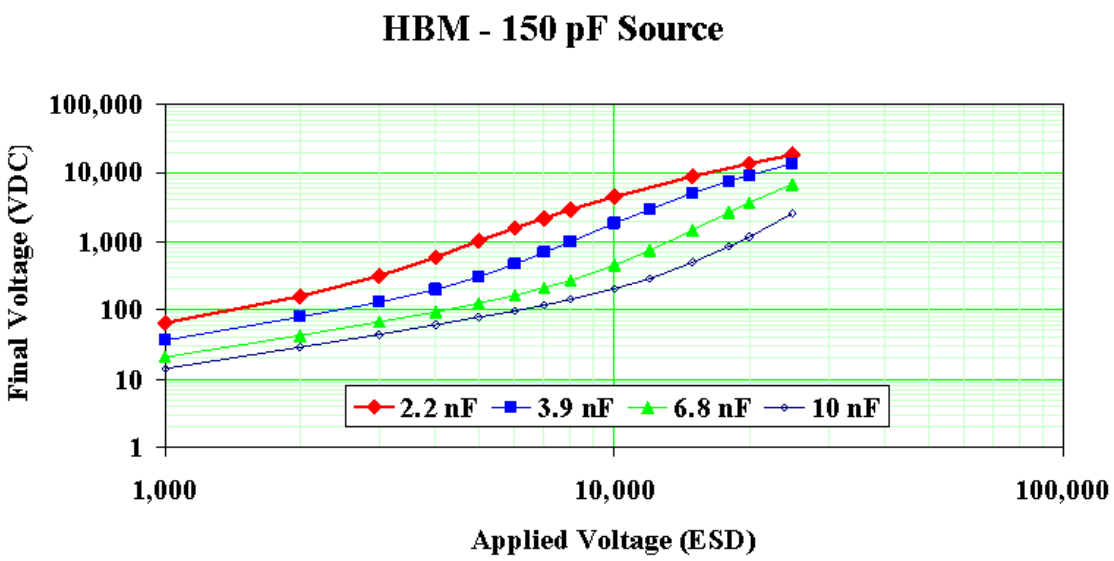

Figure 15

Final vs. Applied Voltage
X7R – 100 WVDC Designs vs. Capacitance

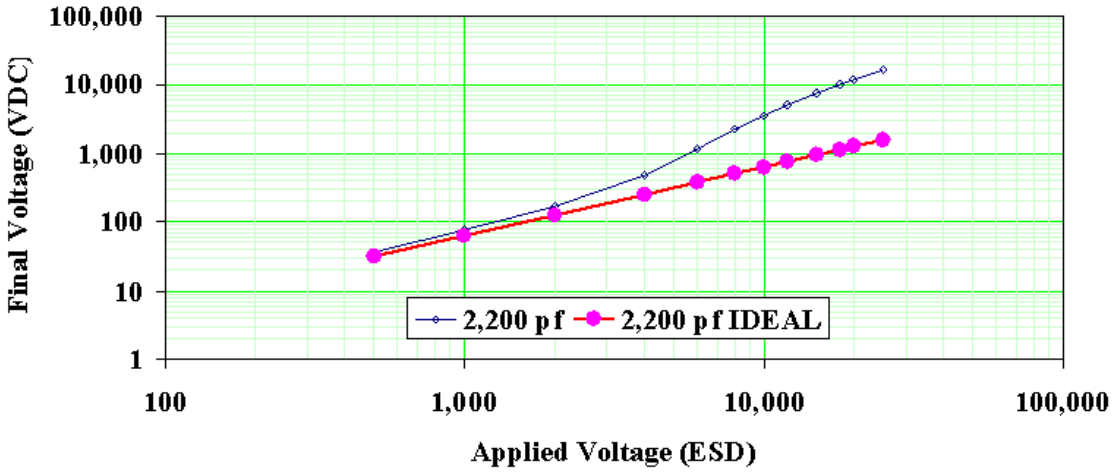

Figure 16

1999 CARTS Proceedings, New Orleans, LA

Final vs. Applied Voltage
2.2 nF - X7R vs. WVDC Designs

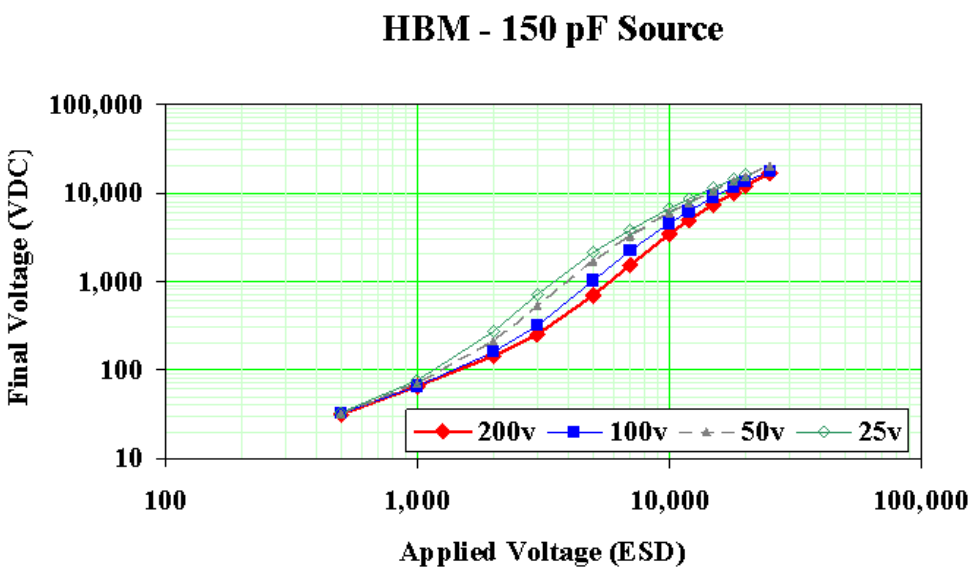

Figure 17

Final vs. Applied Voltage
2.2 nF - X7R vs. WVDC Designs

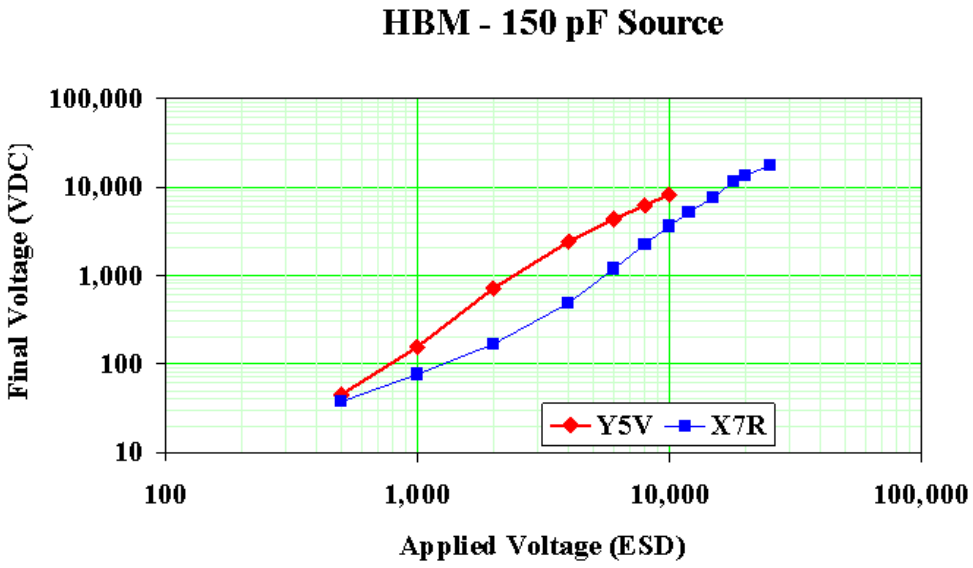

Figure 18

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