IFX007T

High Current PN Half Bridge

About this document

Scope and purpose

This Application Note is intended to provide information and hints for a high current design, using PWM control with the Industrial & Multipurpose NovalithIC™ half-bridge IFX007T for the industrial and multimarket environment.

Note: *The following information is only given to help with the implementation of the device and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

Abstract

This device contains one P-channel high-side MOSFET and one N-channel low-side MOSFET with an integrated driver IC in one package. The Industrial & Multipurpose NovalithIC™ IFX007T is the interface between the microcontroller and the motor, equipped with diagnostic and protection functions.

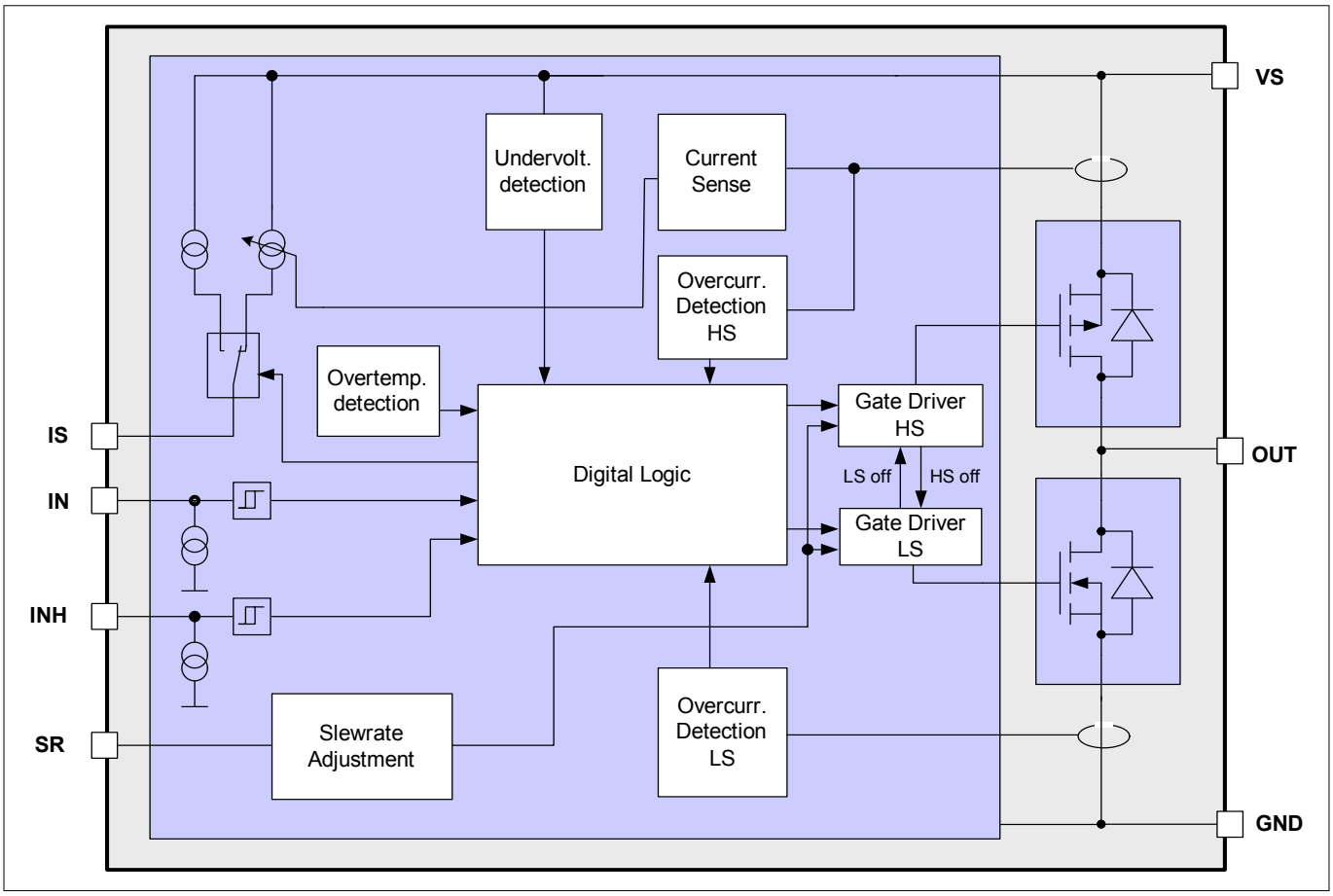

Figure 1 Block Diagram IFX007T

As both the high-side and low side switch are placed on one single leadframe this results in many system benefits: Resulting from the low distance between the high-side MOSFET and the low-side MOSFET the stray inductance between them is minimal thus minimizing negative voltage spikes at OUT during switching and improving EMC. As the voltage level of the leadframe is on the output of the half-bridge, only one single cooling area is required (on OUT potential) for the device, thus being used for both a high-side or low-side current

switching. For a state of the art N-channel solution, usually two cooling areas are required, each for the high-side and low-side MOSFET.

Due to the p-channel highside switch the need for a charge pump is eliminated thus minimizing EMI. Interfacing to a microcontroller is made easily by the integrated driver IC which features logic level inputs, diagnosis with current sense, slew rate adjustment, dead time generation and protection against overtemperature, undervoltage, overcurrent and short circuit.

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1 Motor Configurations

Electrical motors are built with various architectures. Mechanically commutated motors with brushes, so called DC motors or electrically commutated motors, so called BLDC motors (BrushLess DC motors). Due to the flexibility of the half-bridge concept, the Industrial & Multipurpose NovalithIC™IFX007Tcan support all of them.

Using NovalithIC™ controlling a DC-motor/BLDC-motor has the following advantages:

- Extremely low parasitic inductances between high-side and low-side MOSFET.
- Optimized switching performance of the MOSFET's to reduce power losses and EMC emission.
- Driving the motor with PWM for torque and speed control.
- Integrated freewheeling transistor.
- Integrated current measurement.
- Integrated diagnosis and protection.
- Microcontroller compatible input pins.
- Small and PCB-area saving package.

1.1 Half-bridge configuration for mono-directional motor control

Figure 2 shows the design of a mono-directional motor control with Industrial-NovalithIC™.

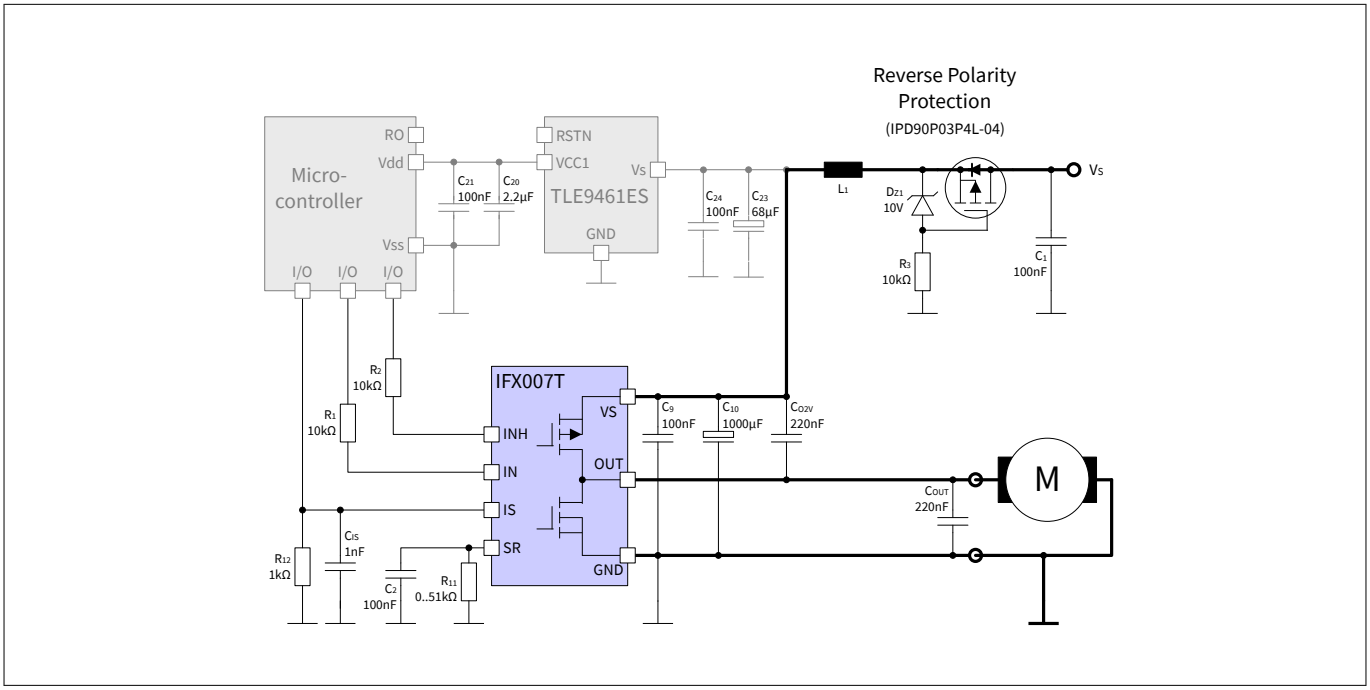

Figure 2 Application circuit for a monodirectional motor with IFX007T

1.2 H-Bridge configuration for bidirectional motor control

With the NovalithIC™IFX007T, it is easy to build an H-bridge for bidirectional DC motor control by simply combining two devices in H-bridge configuration, as it is shown in ***Figure 3***.

Motor Configurations

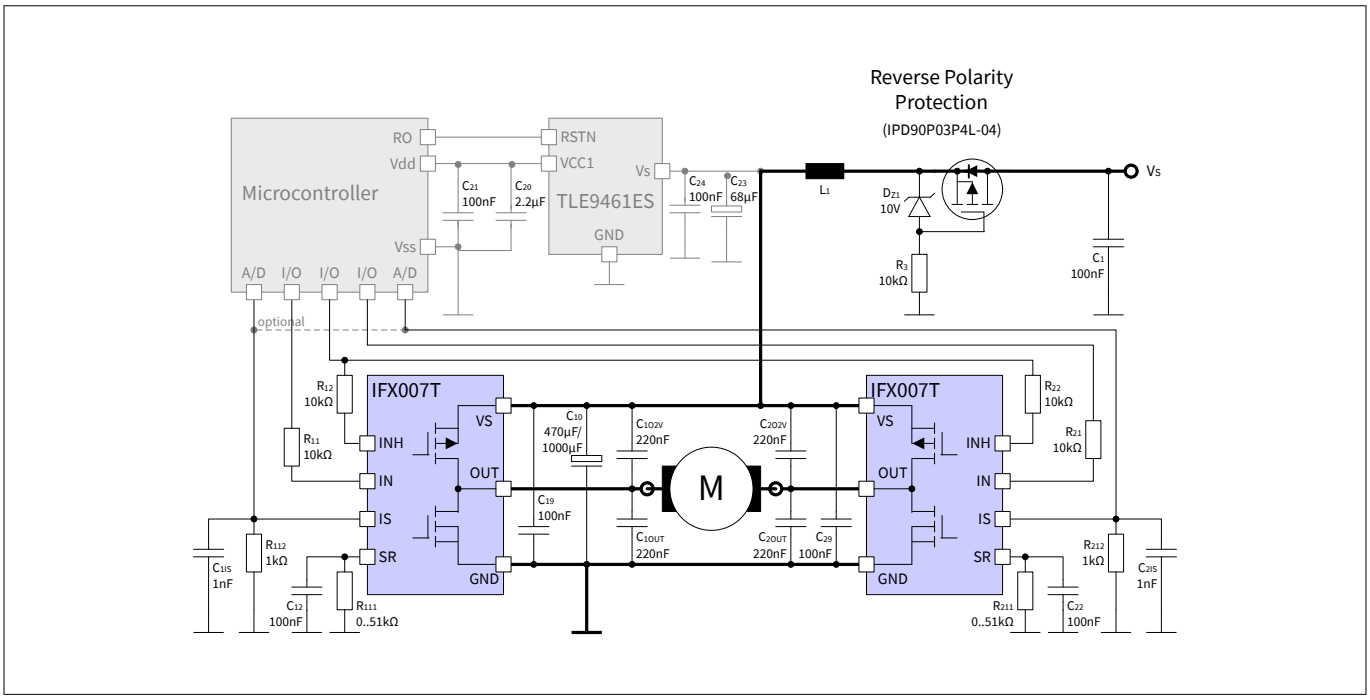

Figure 3 Application circuit for a bidirectional motor with IFX007T H-bridge

2 Parasitic Inductance

In high-current applications, which the NovalithIC™is designed for, special care must be taken for parasitic inductors. The same is valid in case of very high frequencies, which are interesting with regard to EMC considerations.

Each kind of wire in the application is an inductor, e.g. PCB wires, bond wires, etc. The wire inductance can be estimated with

- 1mm PCB wire length approximately 1.2 nH
- 1 PCB via approximately 1 nH

The voltage drop of a wire can be calculated in the following way:

$$U_L = L \cdot \frac{dI}{dt}$$

Equation 1

As can be seen from this equation, care must be taken with the parasitic wire inductors with increasing current and decreasing switching time. The NovalithIC™ is designed to switch high currents very quickly. This means in applications with NovalithIC™, the parasitic inductors are relevant and special care must be taken.

2.1 Measuring signals at NovalithIC™

The parasitic inductance also has an influence on the measurement results. To measure the true signals at the NovalithIC™ it is mandatory to position the measurement probes directly at the device, as it is shown in ***Figure 4***. The probe is connected directly to the V_S-pin of the NovalithIC™ and the reference signal directly to the GND-pin of the device.

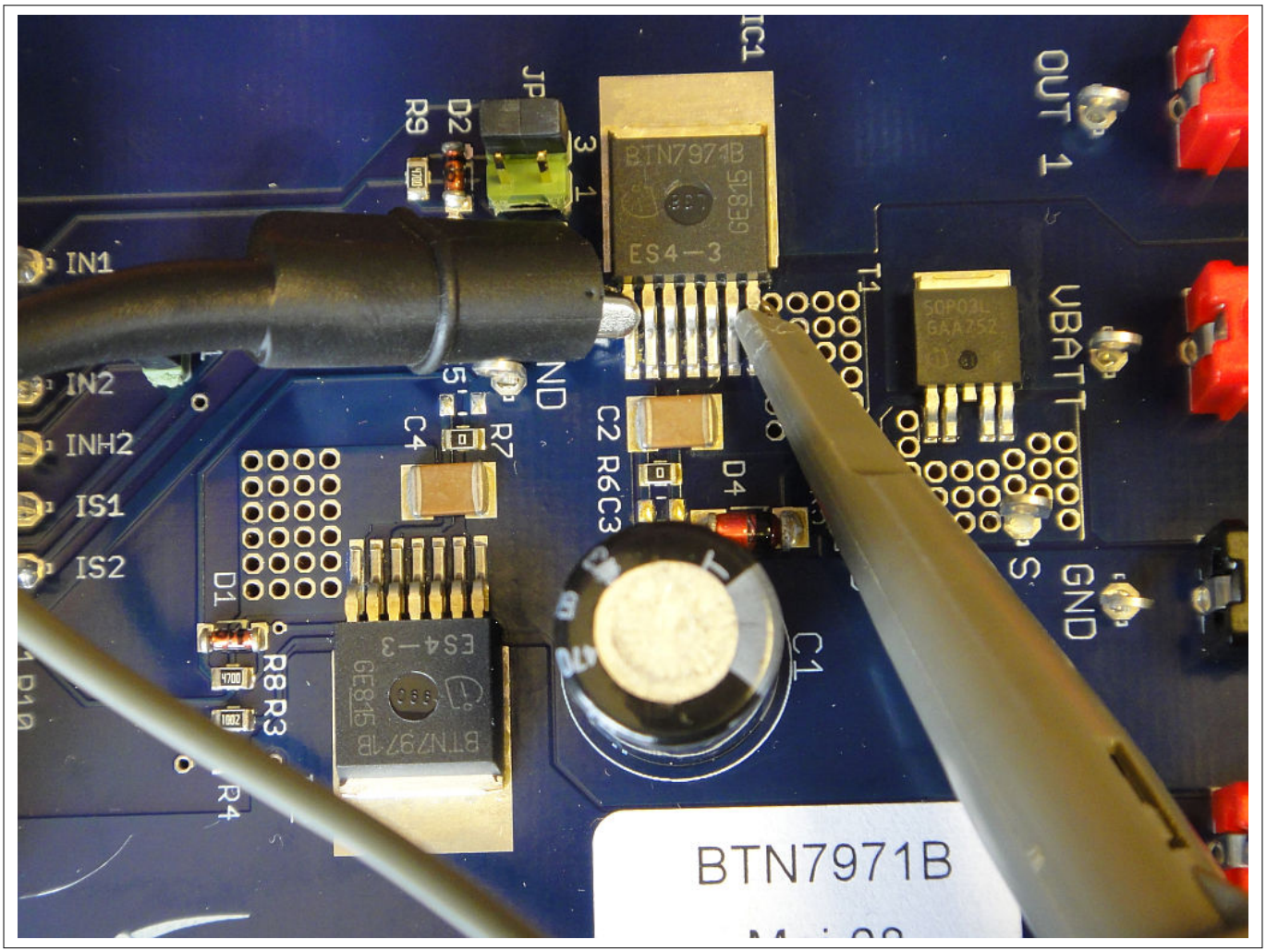

Figure 4 Measuring V_s with Probe and Reference Directly Connected to NovalithIC™

Doing so enables to monitoring of the NovalithIC™ supply voltage when high currents are switched. For example when a short-circuit current is switched, this is the only possibility for measurement if the DC-link capacitor is sufficient to keep the supply voltage above the undervoltage detection threshold (also see ***Chapter 3.2***).

3 Design Guideline

For a safe and sufficient motor control design, discrete components are needed. Some of them must be dedicated to the motor application and some to the NovalithIC™.

3.1 Schematic and layout design rules

Figure 5 and ***Figure 6*** show an example of a schematic plus a corresponding layout for a half-bridge motor control with NovalithIC™.

The best performance in terms of parasitic inductance and EMC can be reached with a GND plane, which we strongly recommend be used.

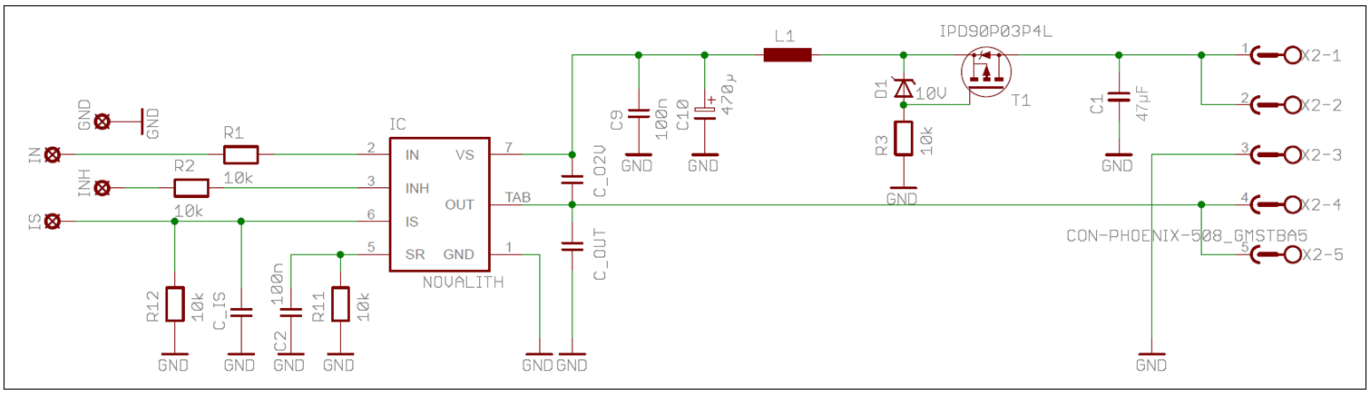

Figure 5 Example of a half-bridge schematic with NovalithIC™

Important design and layout rules:

The basis for the following items is the parasitic inductance of electrical wires, as described in ***Chapter 2***.

- C10, so called DC-link capacitor: This electrolytic capacitor is required to keep the voltage ripple at the V_S-pin of the NovalithIC™ low during switching operation (the measurement procedure for the supply voltage is described in ***Chapter 2.1***). It is strongly recommended that the voltage ripple at the NovalithIC™ V_S-pin to GND-pin be kept below 1 V peak-to-peak. The value of C10 must be aligned accordingly. See ***Equation 10***. Most electrolytic capacitors are less effective at cold temperatures. It must be assured that C10 is also effective under the worst case conditions of the application. The layout is very important. As shown in ***Figure 6***, the capacitor C10 must be positioned with very short wiring at the NovalithIC™. This must be done to keep the parasitic inductors of the PCB-wires as small as possible.
- C9: This ceramic capacitor supports C10 to keep the supply voltage ripple low and covers the fast transients between the V_S-pin and the GND-pin. The value of this ceramic capacitor must be chosen so that fast V_S-ripple at the NovalithIC™ does not exceed 1 V peak-to-peak. The layout wiring for C9 must be shorter than for C10 to the NovalithIC™ to keep the parasitic PCB-wire inductance as small as possible. In addition the parasitic inductance could be kept low by placing at least two vias for the connection to the GND-layer.
- C_O2V: This ceramic capacitor is important for EMI in order to avoid entering electromagnetic disturbances into the NovalithIC™ as much as possible. Good results have been achieved with a value of 220 nF. In terms of layout, it is important to place this capacitor between “OUT” and “V_S” without significant additional wiring from C_O2V to the V_S- and OUT-line.
- C_OUT: This ceramic capacitor helps improve the EMI and the ESD performance of the application. Good results have been achieved with a value of 220 nF. To keep the RF and ESD out of the board, the capacitor is most effective when positioned directly on the board connector. In addition, the parasitic inductance could be kept low by placing at least two vias for the connection to the GND-layer.
- C1: This ceramic capacitor helps to improve the EMI and the ESD performance. In combination with L1 and C10 plus C9 a Pi-filter improves the electromagnetic emission on the V_S-line. Layout rules are the same as for C_OUT.

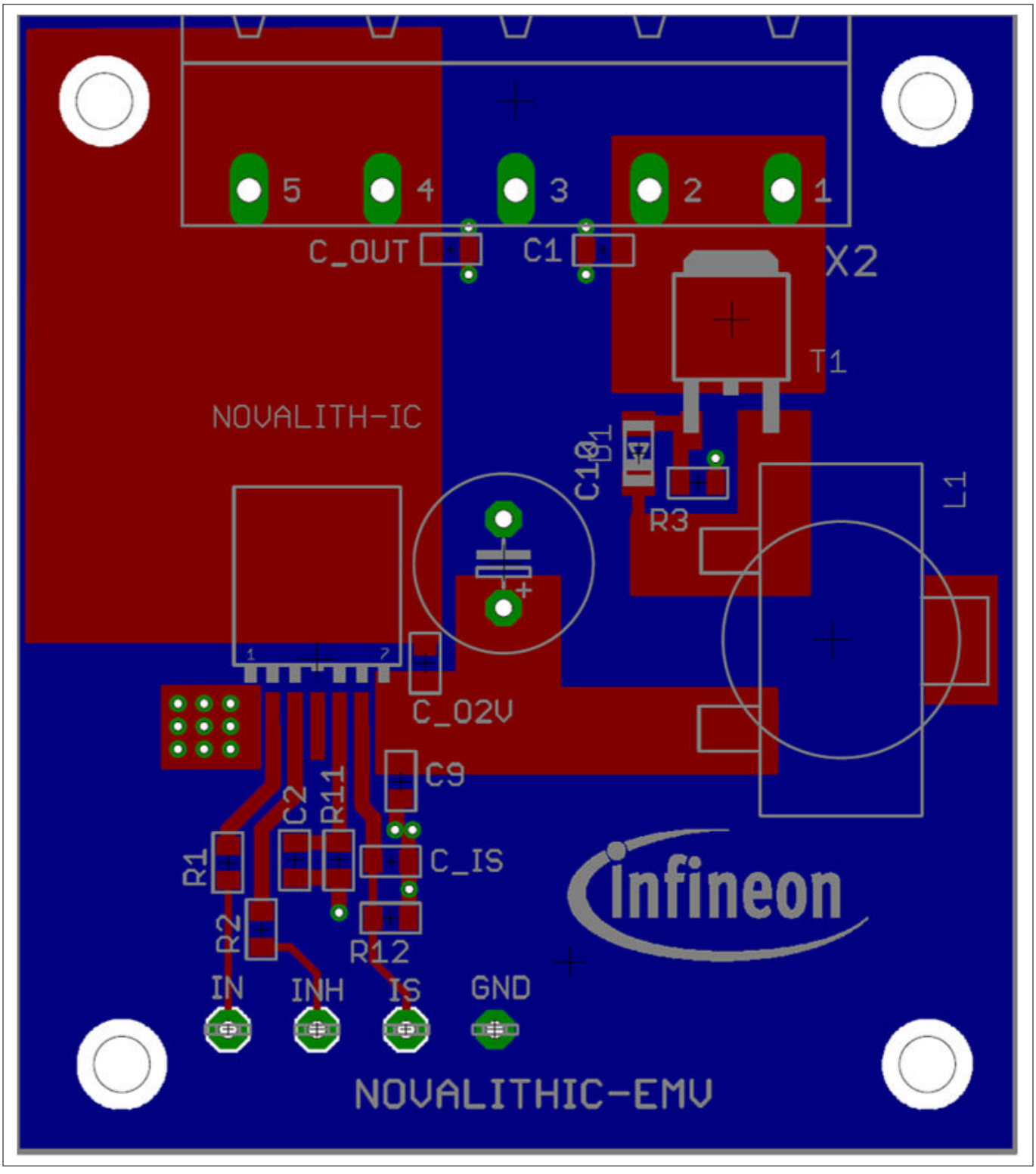

Figure 6 Example of an half-bridge layout with NovalithIC™ (not true to scale)

Other components:

- T1, D1 and R3: Reverse polarity protection. See ***Chapter 3.5***.
- R11: Slew rate resistor according to data sheet.
- C2: Stabilization for slew rate resistor (R11).
- R12: Resistor to generate a current sensing voltage from the IS current.

- C_IS: Ceramic capacitor for EMI improvement. GND connection with at least two GND-vias. A good value is 1 nF. In case the current should be measured during the PWM-phase, this capacitor must be adapted to the ON-time inside the PWM-phase.
- R1 and R2: Device protection in case of µC pins shorted to V_S.

3.2 DC-link capacitor

For the stability of the DC-link voltage a sufficient capacitor is mandatory (in and ***Figure 5*** it is C10). This is one of the most important component in a motor design with semiconductor switches.

The DC-link capacitor could be insufficient, because:

- The capacitor value is too small.
- The ESR of the capacitor is too high.
- When cold the capacitor value is too small.
- The distance between the DC-link capacitor and the NovalithIC™ is too large.
- The wiring between the DC-link capacitor and the NovalithIC™ is too long (see ***Chapter 2***).

The value must be chosen carefully, taking the undervoltage toggling into account, which is described in ***Chapter 3.2.2***.

BLDC applications require three NovalithIC IFX007T devices, in this case we highly recommend to use one DC-link capacitance for each device. Please be noticed that the DC-link capacitance should be placed very close to the NovalithIC pins. The parasitic inductors of the PCB-wires in between should be kept as small as possible.

3.2.1 Calculation of the DC-link capacitor and Pi-filter

As already mentioned in the design- and layout-rules of ***Figure 5*** the voltage ripple at the NovalithIC™ V_S-pin must not exceed 1 V peak-to-peak. The necessary DC-link capacitor can be estimated in the following way:

Motor control with PWM means for the DC-link voltage to provide energy pulses during the “ON-phase” of the PWM cycle. The DC-link pulses are shown in ***Figure 7***.

This energy must be provided by the DC-link capacitor. This can generally be described with

$$E = \frac{1}{2} \cdot C \cdot V^2 = P \cdot T$$

Equation 2

$$C = C_{DC-link}$$

Equation 3

The voltage at the DC-link capacitor consists of the DC-part and the delta voltage from the supply ripple:

$$V = V_{S,DC} + \Delta V_S$$

Equation 4

The total power in this system consists of the DC-power plus the power of the energy pulse (E_{pulse}), which provides the energy to the motor during the ON-phase of the half bridge.

$$P = P_{DC} + \Delta P$$

Equation 5

The maximum pulse length is determined by the PWM frequency, theoretically at a duty cycle of 100%:

$$T = T_{pulse} = T_{PWM} = \frac{1}{f_{PWM}}$$

Equation 6

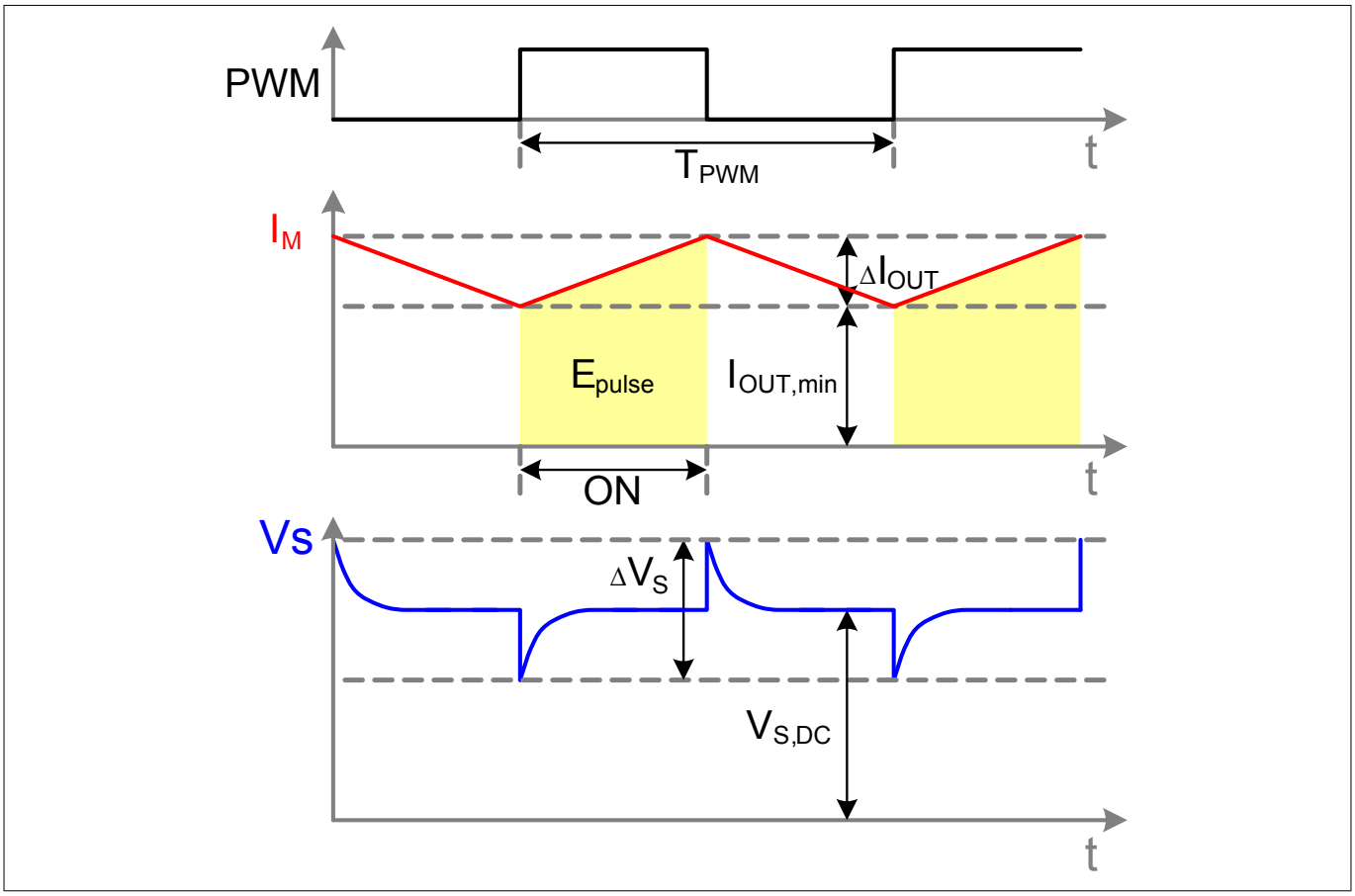

Figure 7 PWM control (PWM = IN-pin-signal, I_M = motor current and V_S = V_S-pin-voltage @ NovalithIC)

Insertion of ***Equation 3*** to ***Equation 6*** into ***Equation 2***

$$E = \frac{1}{2} \cdot C_{DC-link} \cdot \left(V_{S,DC} + \Delta V_S\right)^2 = \left(P_{DC} + \Delta P\right) \cdot T_{PWM}$$

Equation 7

$$\frac{1}{2} \cdot C_{DC-link} \cdot \left(V_{S,DC}{}^2 + 2 \cdot V_{S,DC} \cdot \Delta V_S + \Delta V_S{}^2\right) = P_{DC} \cdot T_{PWM} + \Delta P \cdot T_{PWM}$$

Equation 8

$$\cancel{\frac{1}{2} \cdot C_{DC-link} \cdot V_{S,DC}^2} + C_{DC-link} \cdot V_{S,DC} \cdot \Delta V_S + \underbrace{\frac{1}{2} \cdot C_{DC-link} \cdot \Delta V_S^2}_{negligible} = \cancel{P_{DC} \cdot T_{PWM}} + \Delta P \cdot T_{PWM}$$

Equation 9

Finally the equation to calculate the DC-link capacitor is:

$$C_{DC-link} \geq \frac{\Delta P \cdot T_{PWM}}{V_{S,DC} \cdot \Delta V_S}$$

Equation 10

Based on ***Equation 2*** and referring to the energy of on single pulse, as marked with E_{pulse} ($\approx \Delta P \bullet T_{PWM}$) in ***Figure 7***:

$$\Delta P = V_S \cdot I_{nom} \approx V_S \cdot \left(I_{OUT,min} + \frac{1}{2}\Delta I_{OUT}\right)$$

Equation 11

The DC-link capacitor is primarily the energy buffer for the switching process of the PWM motor control. Secondly it is part of the Pi-filter. This means first the DC-link capacitor must be calculated according to ***Equation 10***. Based on this, it is recommended that the second capacitor of the Pi-filter C1 be estimated with:

$$C_1 = \frac{1}{10} \cdot C_{DC-link} = \frac{1}{10} \cdot C_{10}$$

Equation 12

Generally the border frequency of the L_1-C_1-filter is determined with

$$f_g = \frac{1}{2 \cdot \Pi \cdot \sqrt{L_1 \cdot C_1}}$$

Equation 13

We recommend setting the border frequency f_g to half the value of the PWM -frequency f_{PWM}.

$$f_g = \frac{1}{2} \cdot f_{PWM} = \frac{1}{2 \cdot \Pi \cdot \sqrt{L_1 \cdot C_1}}$$

Equation 14

$$L_1 = \frac{1}{\Pi^2 \cdot f_{PWM}^2 \cdot C_1}$$

Equation 15

Summary

1. Calculate the DC-link capacitor with ***Equation 10***.
2. Calculate the other capacitor of the Pi-filter with ***Equation 12***.
3. Calculate the inductor of the Pi-filter with ***Equation 15***.
4. Do not forget the important layout rules and how to measure the supply voltage correctly.

3.2.2 Undervoltage toggling

The power supply cable of most modules in a car are several meters long. The longer the supply cable is, the higher its parasitic inductance. In addition, most modules have a Pi-filter at the supply line with a inductor for EMC reasons. The sum of the supply line inductances have a significant influence on the V_s-voltage. When switching the motor ON during a normal motor start or PWM control, with a insufficient DC-link capacitor the

supply voltage drops below the undervoltage threshold and the NovalithIC™ is switched to tristate. The supply voltage recovers above the undervoltage threshold and the NovalithIC™ switches on again, again dropping below the undervoltage threshold ...

This effect can result in frequencies higher than 100 kHz, as is shown in ***Figure 8***. The device will be damaged by the power dissipation of the switching losses, which is faster than the reaction time of the over temperature shut down, because of the high switching frequency.

The undervoltage toggling will be worse if the OUT is shorted to GND.

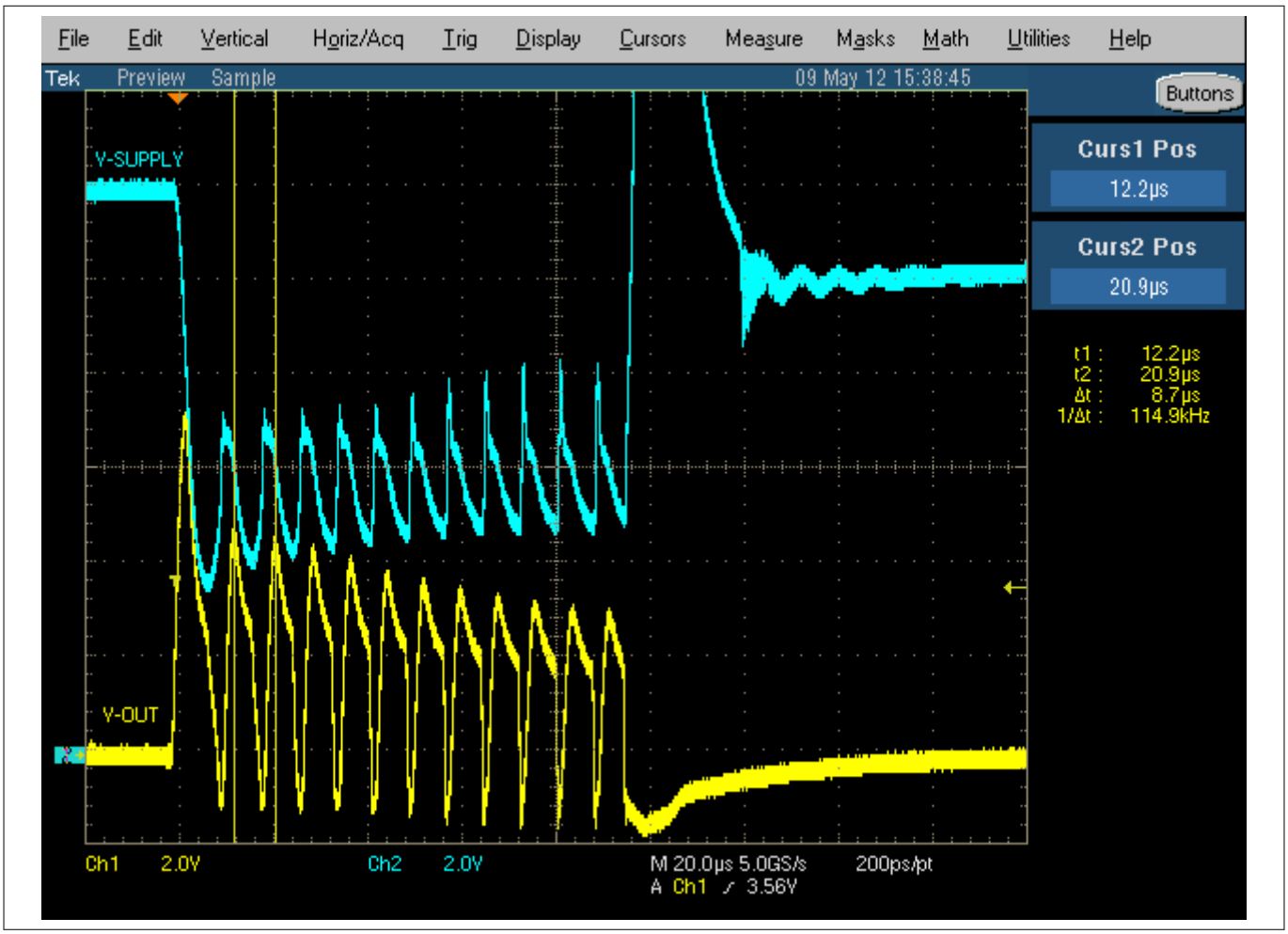

Figure 8 Undervoltage toggling started by short to GND and enabled by an insufficient DC-link capacitor

With a sufficient DC-link capacitor the supply voltage drop is limited so as not to reach the undervoltage threshold, as is shown in ***Figure 9***.

The “ON-time” is limed to 100 µs by the IN-signal, as shown in ***Figure 9***. Only the DC-link capacitor is switched between the two measurements.

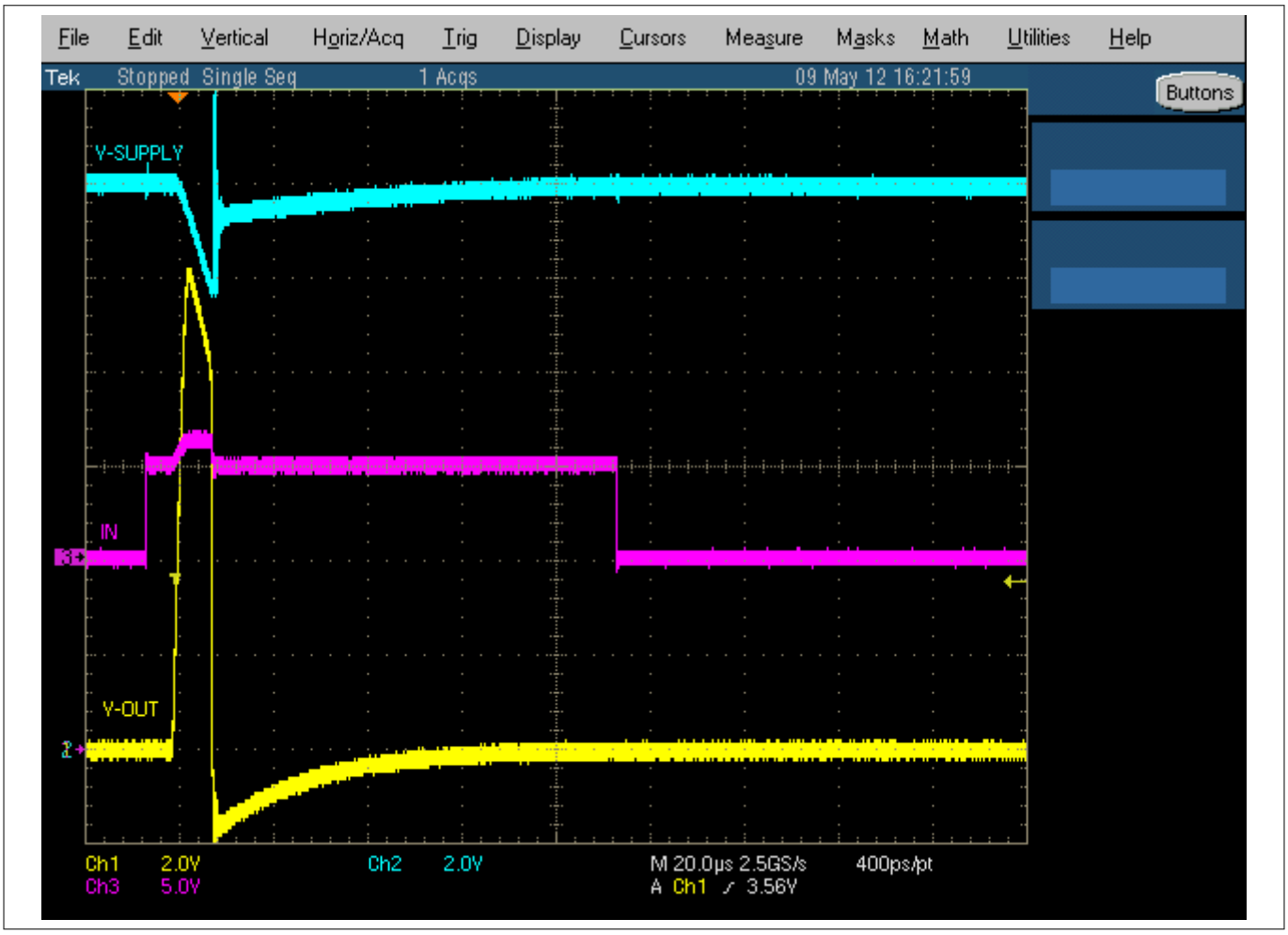

Figure 9 The sufficient DC-link capacitor avoided undervoltage -toggling in case of a short to GND

3.3 Ground references

Depending on the different functionalities, different ground references for each pin of the NovalithIC™ have to be considered, especially in high current applications, in which ground shifts might occur due to parasitic inductances and line resistantaces of the PCB.

Based on the example schematic in ***Figure 5***, the different ground reference concepts are illustrated in ***Figure 10***.

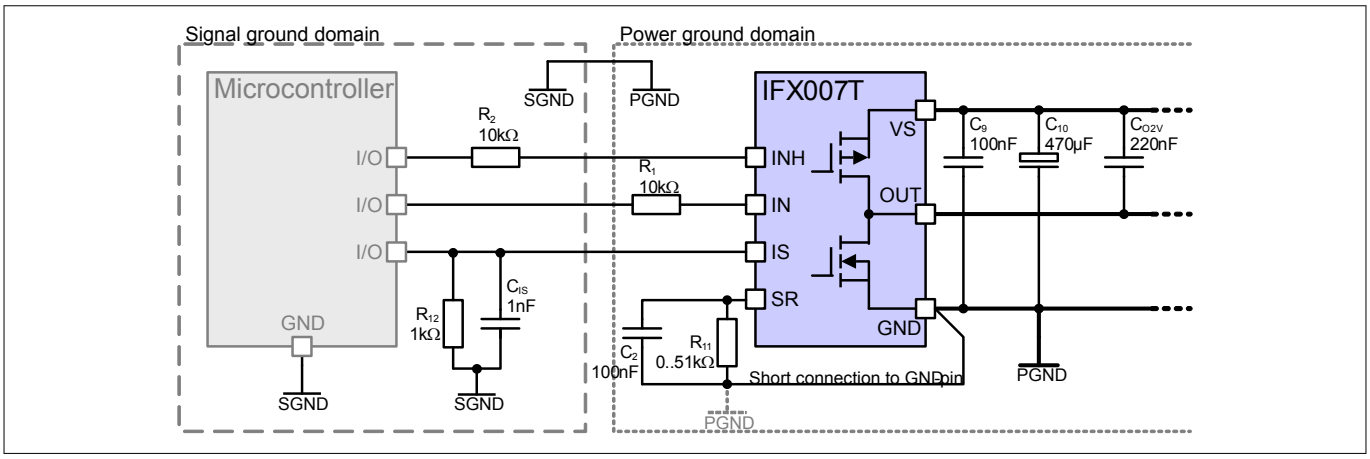

Figure 10 Simplified schematic illustrating the ground references for the signal ground (SGND) and power ground (PGND) of the NovalithIC™

Design rules for the ground reference:

- IS-pin: The reference ground for the current sense and failure flag detection is ideally the Analog-to-Digital Converter's / Microcontroller's ground as the IS-pin is a current source. If this is implemented, the absolute maximum ratings shall be respected, also in the case of a ground shift between the Microcontroller's (signal-) ground and the device's ground (GND-pin). Thus it is recommended to connect R12 and C_IS to the signal ground (SGND) as shown in ***Figure 10*** thus eliminating the influence of a ground shift.
- SR-pin: For the slew rate functionality the reference ground is the device's ground, the GND-pin. Thus R11 and C2 (in ***Figure 5*** and ***Figure 10***) should be placed close to the device and be connected directly to the device's ground with minimal wiring to prevent any influence of disturbance through ground shifts.
- IN/INH-pins: For the digital input pins IN and INH the internal ground reference is the GND-pin of the NovalithIC™ thus it has to be obtained, that a ground shift between the Microcontroller's (signal-) ground, which is controlling the pins, and the device's ground (GND-pin) isn't influencing the switching behavior and the absolute maximum ratings are respected.

3.4 Driving inductive loads over long wires

Inductive loads have a lowpass filter characteristic, like a motor. Because of this, the wire from the NovalithIC™ OUT to the motor injects electromagnetic disturbances into the OUT-pin. This antenna effect increases as the length of the motor wire increases.

The definition of a long motor wire strongly depends on the application and the environment. To provide a general idea, wire lengths of approximately 20 cm and more are considered as "long wire". The motor wire should therefore be as short as possible.

3.4.1 PWM operation

In case of a long motor wire and PWM operation the electromagnetic emission (EME) increases with the wire length and with the switching speed (inversion of $t_{r(HS)}$, $t_{r(LS)}$, $t_{f(HS)}$ and $t_{f(LS)}$). In this case it is advantageous to reduce the switching speed with the slew rate resistor at the SR-pin (see ***Figure 5***, R_{11}). Reducing the switching speed has probably a impact on the PWM-frequency, which may needs to be adapted. In any case the power dissipation and the cooling concept needs to be reviewed. The slew rate resistor at the SR-pin should not exceed the max. slew rate resistor value of the data sheet $R_{SR} \leq 51$ kΩ.

3.4.2 Current sense

A long motor wire can pick up electromagnetic disturbances which could influence the current sense signal at the IS-pin. If a high accuracy of the current measurement is needed, it is recommended to use the IS-pin as status flag diagnosis and perform the current measurement with an external shunt plus current sense amplifier. An schematic example is shown in ***Figure 11***.

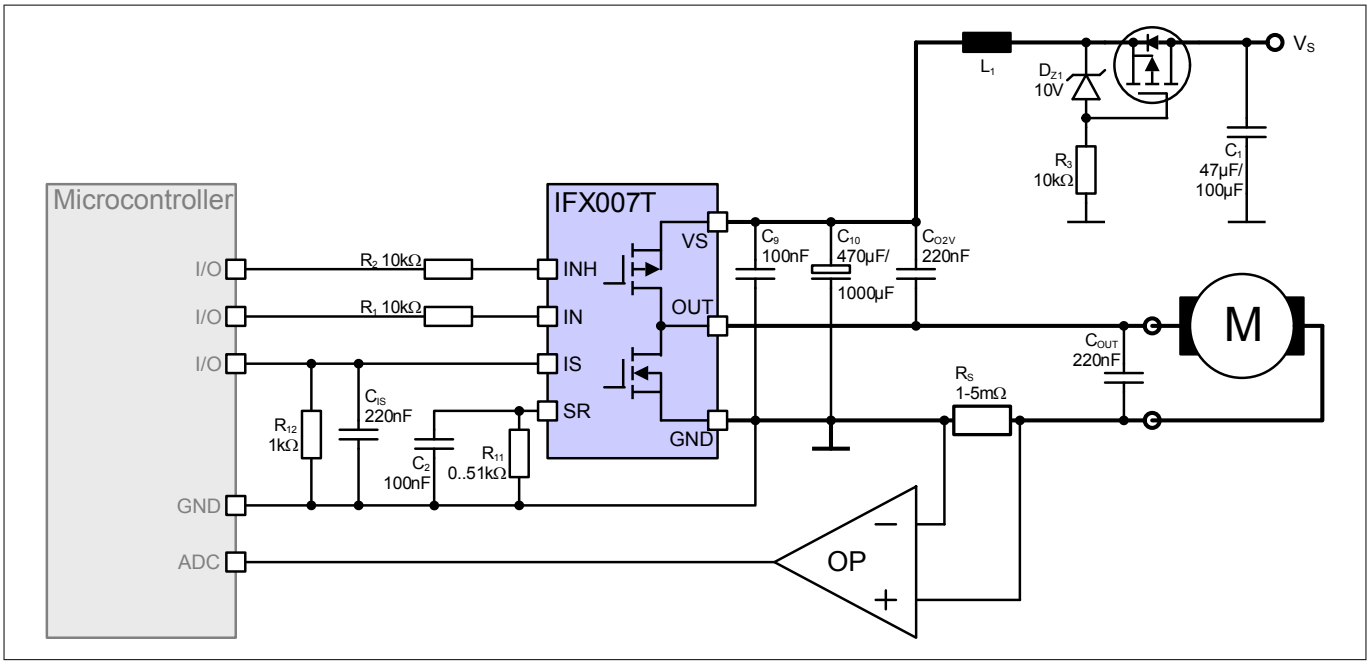

Figure 11 IFX007T with external current measurement

3.5 Reverse polarity protection

The semiconductor technology of NovalithIC™ used has a parasitic PN -diode from “GND” to the supply voltage pin “V_S”. If the supply voltage is inverted, a huge current will flow through this parasitic PN -diode and will damage the device. With reverse polarity protection, the reverse current is not possible and the semiconductor components of the design are protected.

In the schematic in ***Figure 5***, reverse polarity protection is provided with a P-channel MOSFET (IPD90P03P4L-04), a zener-diode (D_1) and a resistor (R_3).

Normal operation V_s > GND:

- P-MOSFET OFF: The application is supplied by the body-diode of the reverse polarity protection transistor (IPD90P03P4L-04), e.g. in case of a power-up. The status “P-MOSFET ON” will quickly be reached.
- P-MOSFET ON: After the power-up in which the body diode was used as a supply path, the zener diode plus the resistor will generate a gate-source voltage in the range of 10 V and the P-MOSFET is in ON-state. Only the $R_{DS,on}$ is in the power supply path.

Reverse polarity condition V_s < GND:

- The gate source voltage of the reverse polarity protection transistor is continuously “LOW” and the transistor is switched OFF. No current can flow in this state. The application will not be damaged.

3.6 Cooling

The NovalithIC™ half-bridge, driving high current generates power dissipation. These are R_{ON} losses and switching losses in case of PWM control, which heat up the device. For details, please see ***Chapter 6***. The package PG-TO263-7-1 provides a low thermal resistance which can be combined with a heat sink on the PCB to avoid exceeding the absolute maximum temperature values of the data sheet.

In ***Figure 6*** a cooling area (brown top layer, where the NovalithIC™-OUT is connected) has already been drawn. Depending on the power dissipation, other thermal sources on the PCB and the ambient temperature, the cooling needs to be carefully adapted to each application.

In addition the reverse polarity protection transistor T1 (***Figure 5*** and ***Figure 6***) generates $R_{DS,on}$ power losses and the cooling concept for this transistor must ensure that the device does not exceed the absolute maximum junction temperature.

3.7 Low inductive short circuit protection

Especially for supply voltages higher than 20 V special care has to be taken to protect the IFX007T against low inductive short circuits, especially for short PCB wiring, thus low stray resistance and inductances.

An example for such a short circuit is show in ***Figure 12***, directly at the motor connector, from the OUT-pin to ground.

In such an application scenario, the undervoltage toggling, described ***Chapter 3.2.2***, is a risk for the device. As the current increase (dI/dt) at OUT is mainly defined by the short circuit's stray inductance, the supply voltage stability has to be ensured also for the filter and reaction time for the current limitation function of the IFX007T, until the power MOSFET gets switched off.

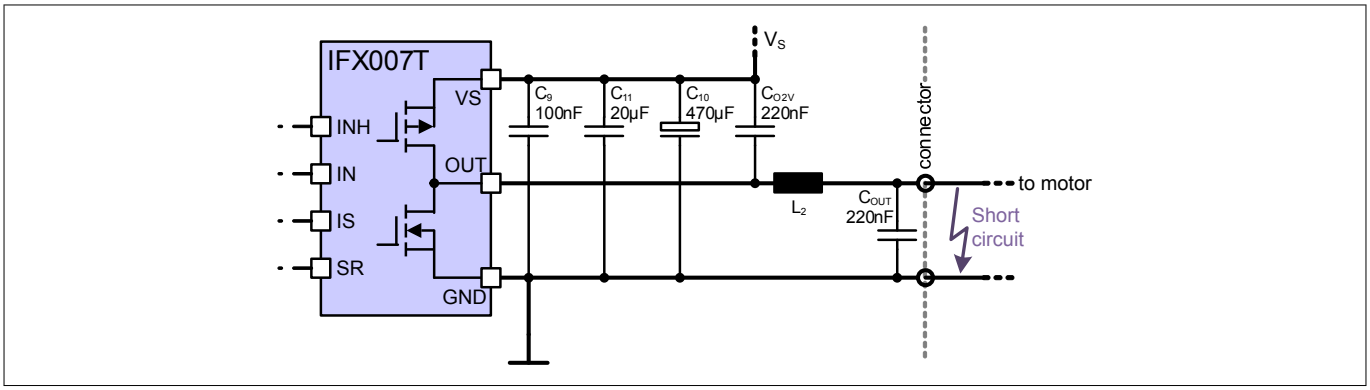

Figure 12 IFX007T example schematic for a low inductive/resistive short circuit at the connector

As a countermeasure, the following measure can be taken, which also are illustrated in ***Figure 12***

- Increase the value of the DC-link capacitor, e.g. 1000 µF.
- Use one DC-link capacitor for each IFX007T
- Minimize the ESR resistor of the DC-link capacitor.
- Minimize the stray inductance and resistance from the DC-link capacity to the VS- and GND-pin of the IFX007T, thus place it, together with C_9, as close to the IFX007T as possible.
- Placing an additional ceramic capacitors C_{11}, e.g. 10 µF in parallel to C_9 and C_{10}.
- Limiting the current peak by an additional inductor L_2 between the OUT-pin of the IFX007T and the connector/motor.
- Evaluation of the IS signal, thus recognizing an overcurrent event or fault flag (due to current limitation) and switching off the IFX007T immeditely.

A short circuit measurement is shown in ***Figure 13***.

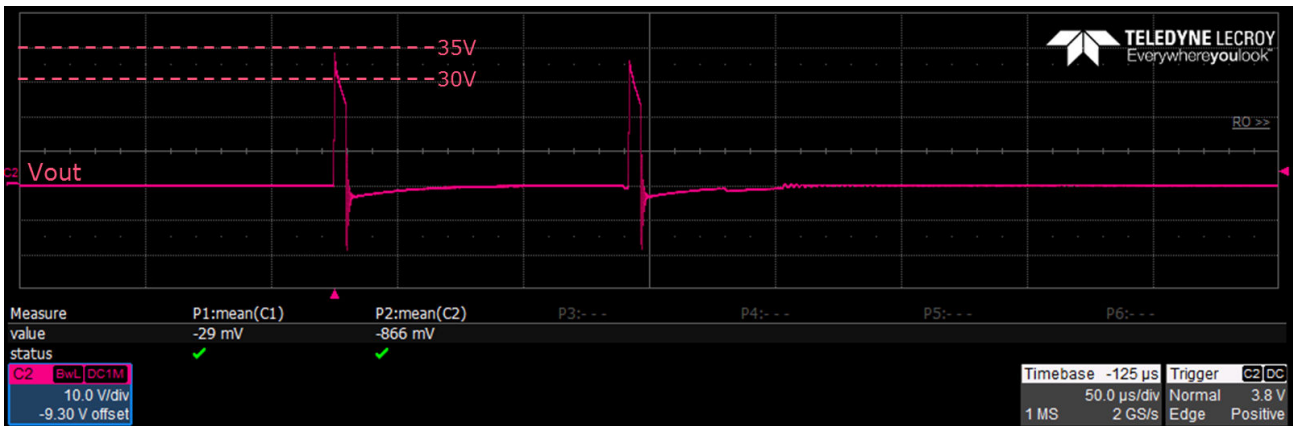

Figure 13 32V short circuit measurement

Related information

4 Current Sense Improvement

The NovalithIC™ half-bridge-family has a current sense function with an IS-pin which provides the output current divided by a factor, so called dk_{ILIS}. The precision of the current measurement could be significantly improved by eliminating the IS-offset, dk_{ILIS}-production spread and respecting the temperature dependency of the dk_{ILIS}.

The table below provides an overview of possible combinations of procedures to reduce current measurement errors.

Table 1 Current sense procedure and benefits

Procedures			Load current tolerance
Offset compensation			±28%
Offset compensation	Device dkILIS measurement		±10%
Offset compensation	Device dkILIS measurement	Temperature estimation	±6%
Offset compensation	Device dkILIS measurement	Temperature compensation	±3%

4.1 Characteristic of the dk_{ILIS}

The dk_{ILIS} has characteristic dependencies. The most important ones with respect to the supply voltage V_s and with respect to the temperature, are described in this chapter.

4.1.1 Life time drift

Life time tests of 1000 hours at 150°C with a dedicated device stress set up and with many devices from different production lots showed the dk_{ILIS} is decreasing over life time up to -3%.

4.1.2 Temperature drift of the dk_{ILIS}

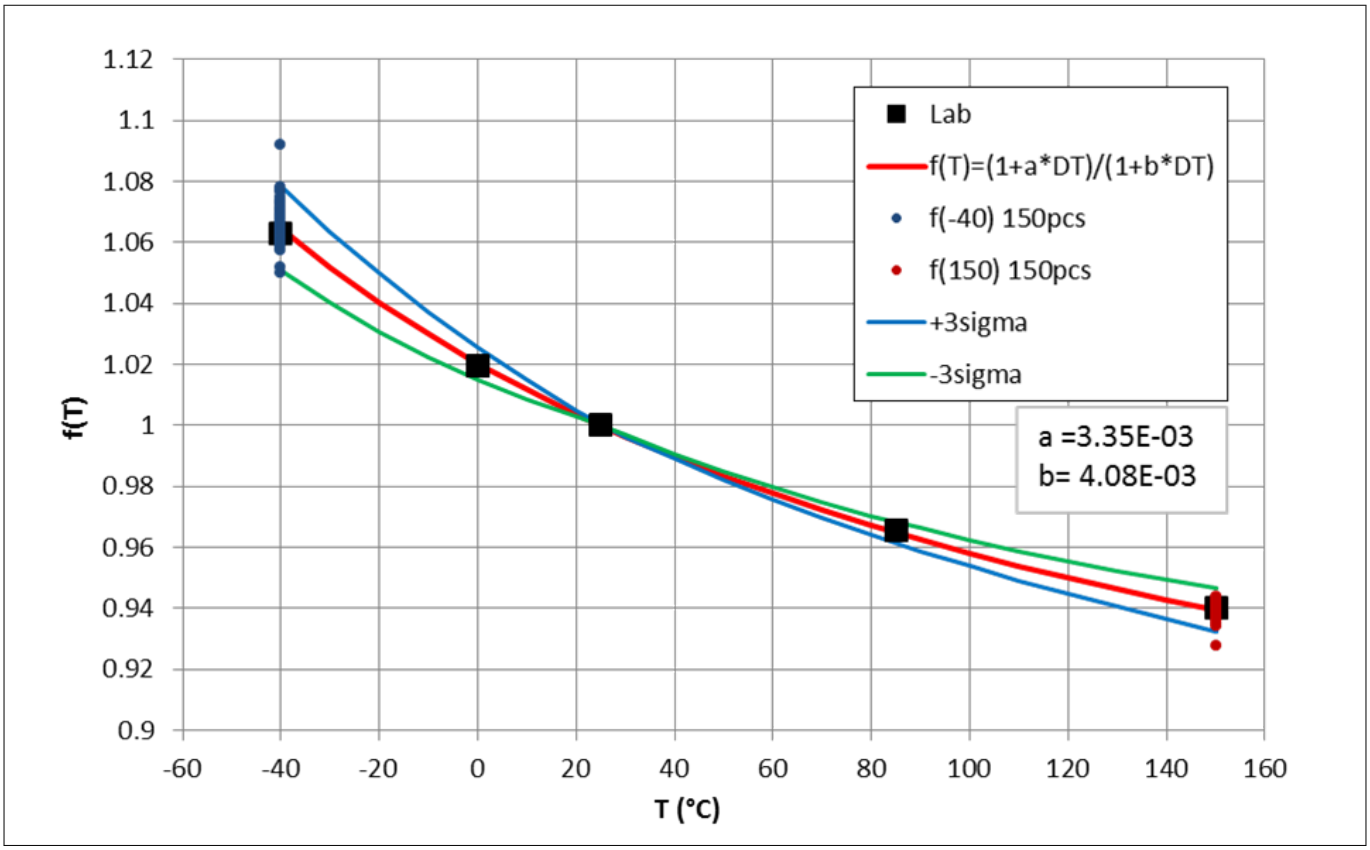

Figure 14 IFX007T dk_{ILIS} vs. temperature

The function f(T) is dependent on the temperature coefficient of the shunt resistance in the control chip (a), the temperature coefficient of the shunt (b) and DT = T - 25 °C.

Table 2 Parameters in the fitting function

a	b	DT
3.35E-03	4.08E-03	T-25°C

The red curve in ***Figure 14*** shows the typical temperature dependent dK. It can be calculated by the following equation:

$dK_{ILIS}(T) = dK_{ILIS}(25°C) \cdot f(T)$

The mean values and standard deviations in ***Table 3*** are derived from measurements.

Table 3 Mean values and standard deviations of IFX007T at -40°C and 150°C

T(°C)	-40°C	150°C
Mean	1.065	0.939
Standard deviation(σ)	4.62E-03	2.38E-03

The dKILIS points on ±3sigma curves at different temperatures can be calculated :

- +3sigma line in ***Figure 15***
  - Case 1 (T < 25°C) : $f(T)_{+3\sigma} = f(T) + 3\sigma(-40°C) * (T - 25°C) / (-40°C - 25°C)$
  - Case 2 (T ≥ 25°C) : $f(T)_{+3\sigma} = f(T) - 3\sigma(150°C) * (T - 25°C) / (150°C - 25°C)$

- -3sigma line in ***Figure 16***
  - Case 1 (T < 25°C) : $f(T)_{-3\sigma} = f(T) - 3\sigma(-40°C) * (T - 25°C) / (-40°C - 25°C)$
  - Case 2 (T ≥ 25°C) : $f(T)_{-3\sigma} = f(T) + 3\sigma(150°C) * (T - 25°C) / (150°C - 25°C)$

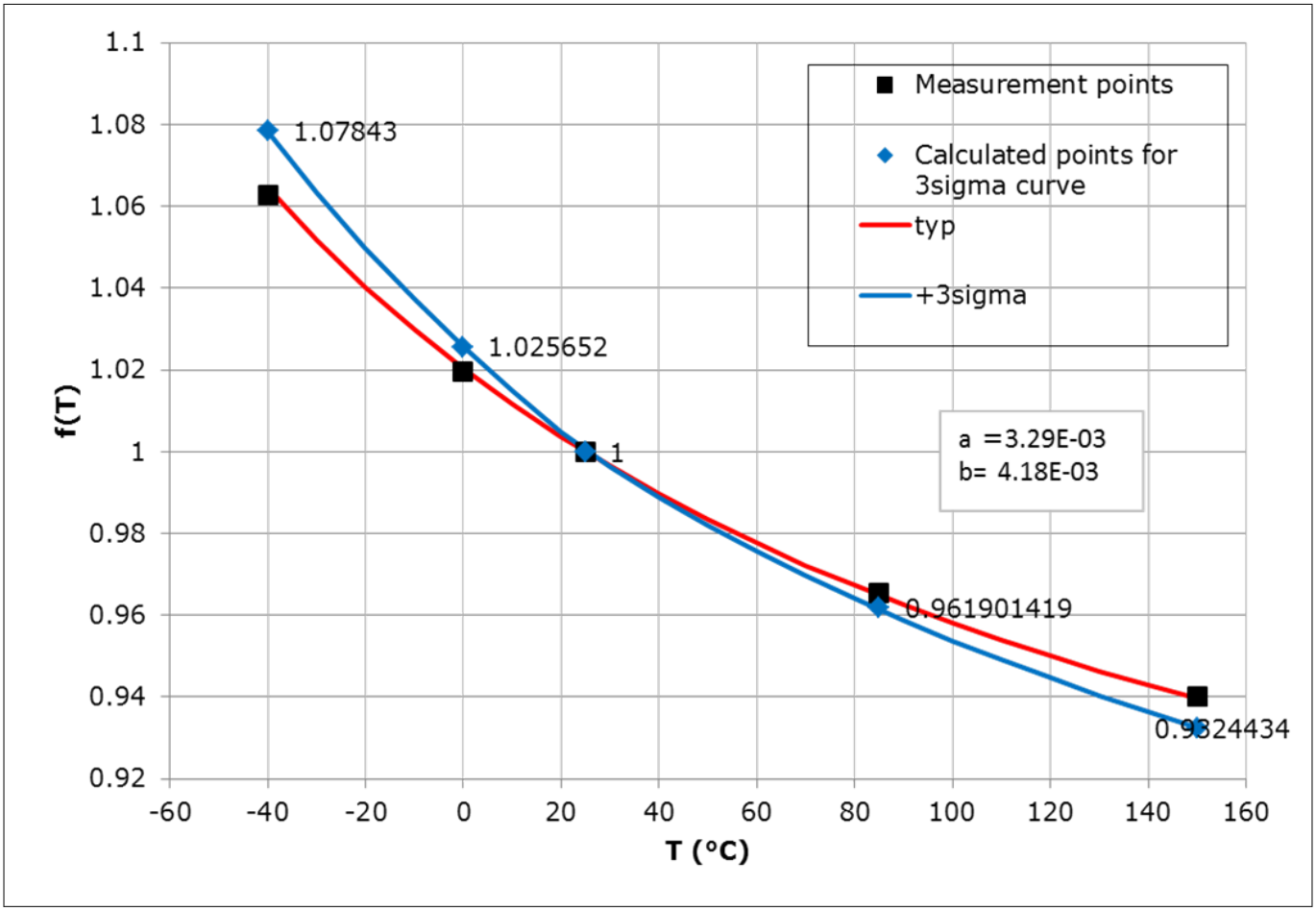

Figure 15 IFX007T +3sigma dk_{ILIS} vs. temperature

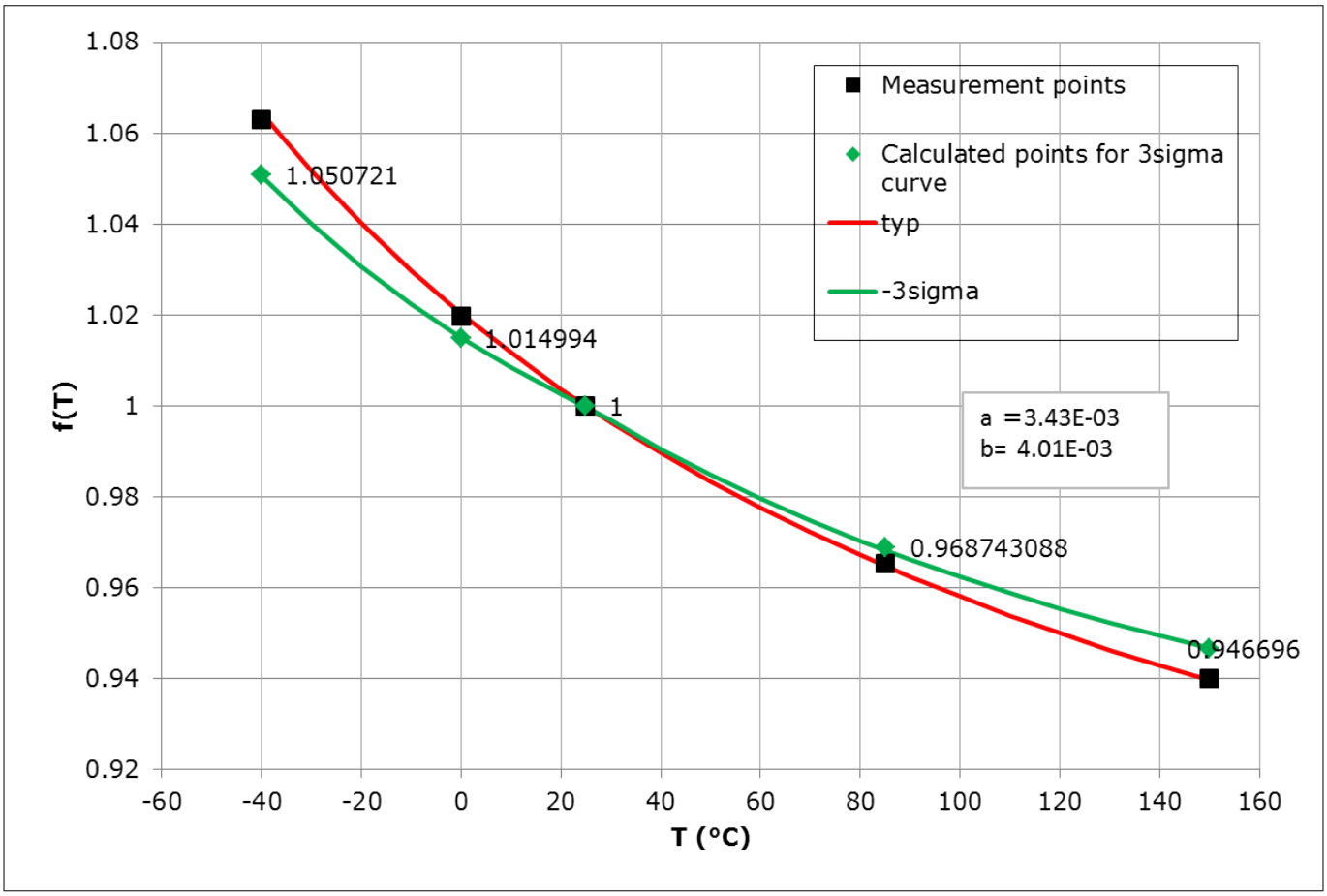

Figure 16 IFX007T -3sigma dk_{ILIS} vs. temperature

Based on the equation: f(T) = (1+a*DT)/(1+b*DT), the ±3sigma temperature shift curves are fitted to the calculated points. The equation for the ±3sigma models are shown below :

- Equation for +3sigma curve in ***Figure 15*** :
  $f(T)_{+3\sigma} = \{1+ a(+3\sigma)(T - 25°C)\} / \{1+b(+3\sigma)(T -25°C)\}$
- Equation for -3sigma curve in ***Figure 16*** :
  $f(T)_{-3\sigma} = \{1+ a(-3\sigma)(T - 25°C)\} / \{1+b(-3\sigma)(T -25°C)\}$

Table 4 Parameters in equations for ±3sigma temperature shift curves of IFX007T

Equation	a	b
$f(T)_{+3\sigma}$	3.29E-03	4.18E-03
$f(T)_{-3\sigma}$	3.43E-03	4.01E-03

4.1.3 Temperature drift of the dk_{ILIS} including aging

If the aging of the devices are taken into account, the extrem value of dk_{ILIS} over lifetime in ***Figure 14*** should be reduced by 3% as shown in and in ***Figure 17***. The orange line indicates the typical temperature drift of dk_{ILIS} inculding the aging. The equations for the typical dk_{ILIS} curve are shown below :

- Case 1 (T< 25°C) :
  $f(T) = (f(T)_{+3\sigma} + f(T)_{-3\sigma} * 097) / 2$
- Case 2 (T≥ 25°C) :

$f(T) = (f(T)_{-3\sigma} + f(T)_{+3\sigma} * 097) / 2$

The grey line indicates the minimum value over lifetime. The equations for the minimum dk_{ILIS} curve are shown below :

- Case 1 (T< 25°C) :
  $f(T) = f(T)_{-3\sigma} * 097$
- Case 2 (T≥ 25°C) :
  $f(T) = f(T)_{+3\sigma} * 097$

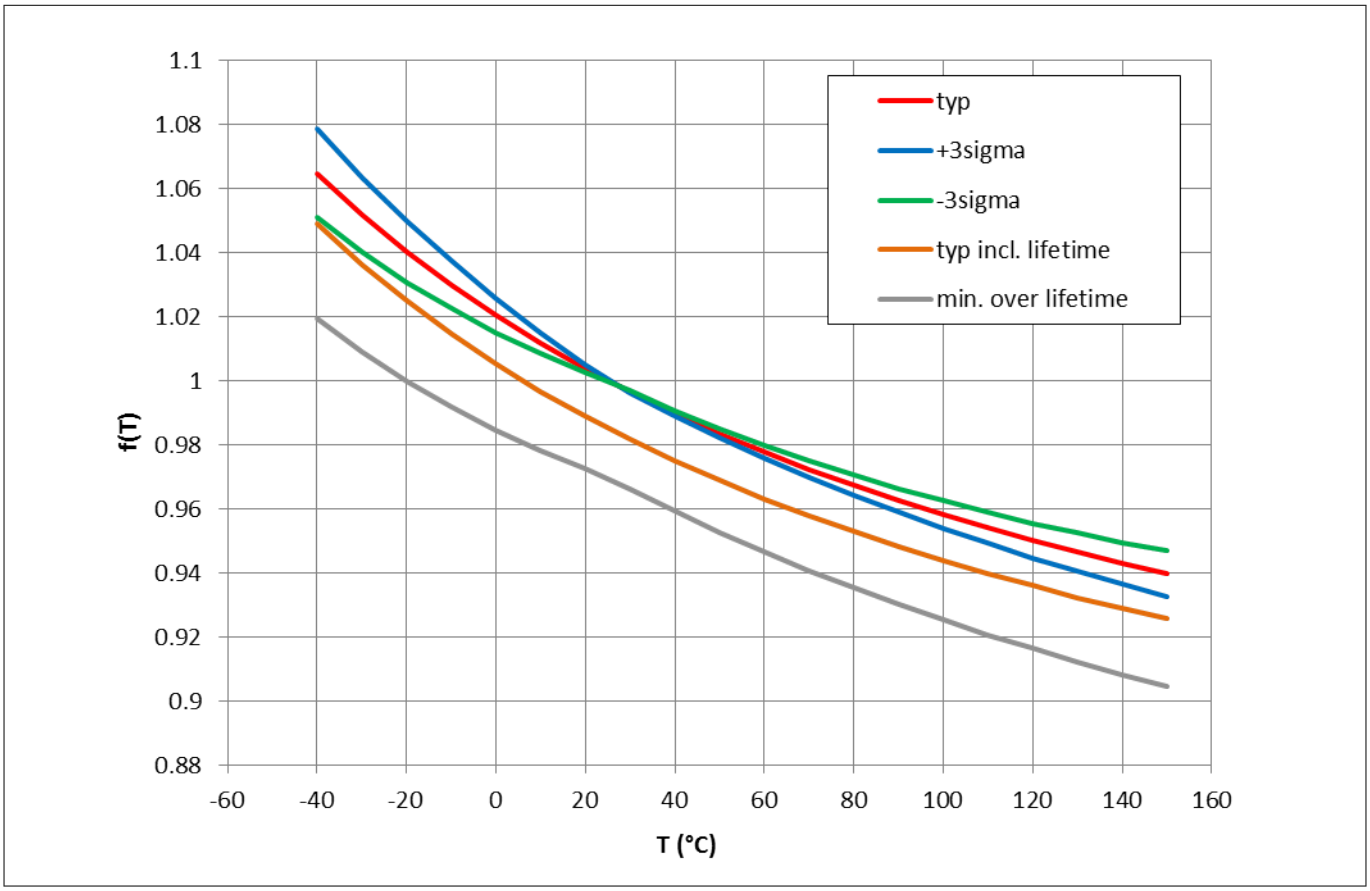

Figure 17 IFX007T temperature dependency and lifetime drift of dk_{ILIS} distribution

4.2 Offset compensation

The IFX007T is featured with an artificial offset current at the IS-pin. This is shown in ***Figure 18***.

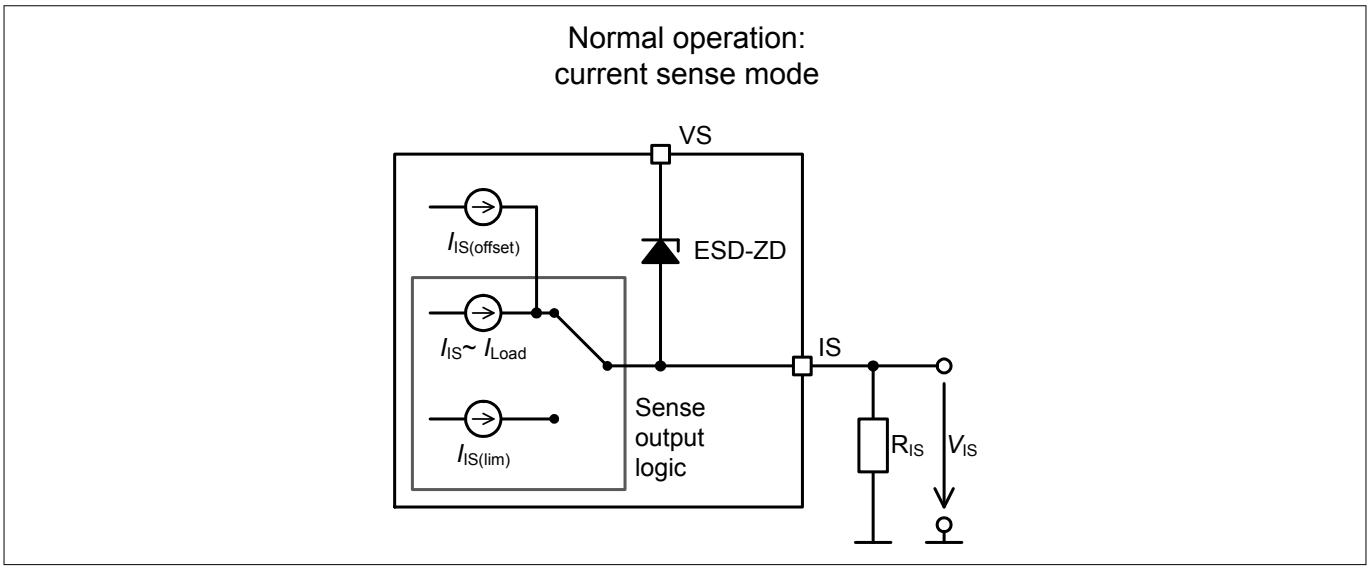

Figure 18 IS-Pin Internal Structure

With this structure, it is possible to always have a measurable offset at IS without a load current. This makes it easy to measure the offset with the microcontroller, store the offset value and process this in the current measurement procedure.

The offset must be compensated to allow a precise current measurement with the IS-pin.

The offset should be compensated before activating the load. When an application such as a fuel pump runs constantly with PWM, you can perform the offset compensation when INH=high and IN=low. In the PWM-phase, the best measurement results are achieved just before the rising edge of the IN-signal.

With this procedure, the specified dk_{ILIS} of ±28% could be reached, even for small load currents. This includes production spread, temperature dependency and aging. Most errors are caused by production spread, which could be compensated by measuring of the dk_{ILIS} of each device (device-specific dk_{ILIS}). Details of this approach are described in the relevant chapter.

4.3 Device specific dk_{ILIS}

With a measurement of the offset current and one IS-value at a certain load current at 25 °C (e.g. 20 A), it is possible to determine the individual $dk_{ILIS\text{-}device}$ and store it permanently to the microcontroller of the application. With this value, the graph in ***Figure 14*** is valid. The extreme values are indicated by the blue line (+3sigma):

- $dk_{ILIS\text{-}max\text{-}C}$ = 1.08 (blue @ -40 °C)
- $dk_{ILIS\text{-}min\text{-}H}$ = 0.93 (blue @ 150 °C)

Taking into account the aging of the device (see ***Chapter 4.1.3***) the minimum value of (blue line) must be reduced by 3% (multiplying 0.97). This means the extreme values are as follows:

- $dk_{ILIS\text{-}max\text{-}C}$ = 1.08 (blue @ -40 °C)
- $dk_{ILIS\text{-}min\text{-}H\text{-}old}$ = $dk_{ILIS\text{-}min\text{-}H}$ * 0.97 = 0.9

This could be assumed as an error of ±10% including temperature drift and aging.

In this case, the typical value should be assumed as follows:

- $dk_{ILIS\text{-}typ}$ = 0.99

The device calibration could be implemented in the module test sequence.

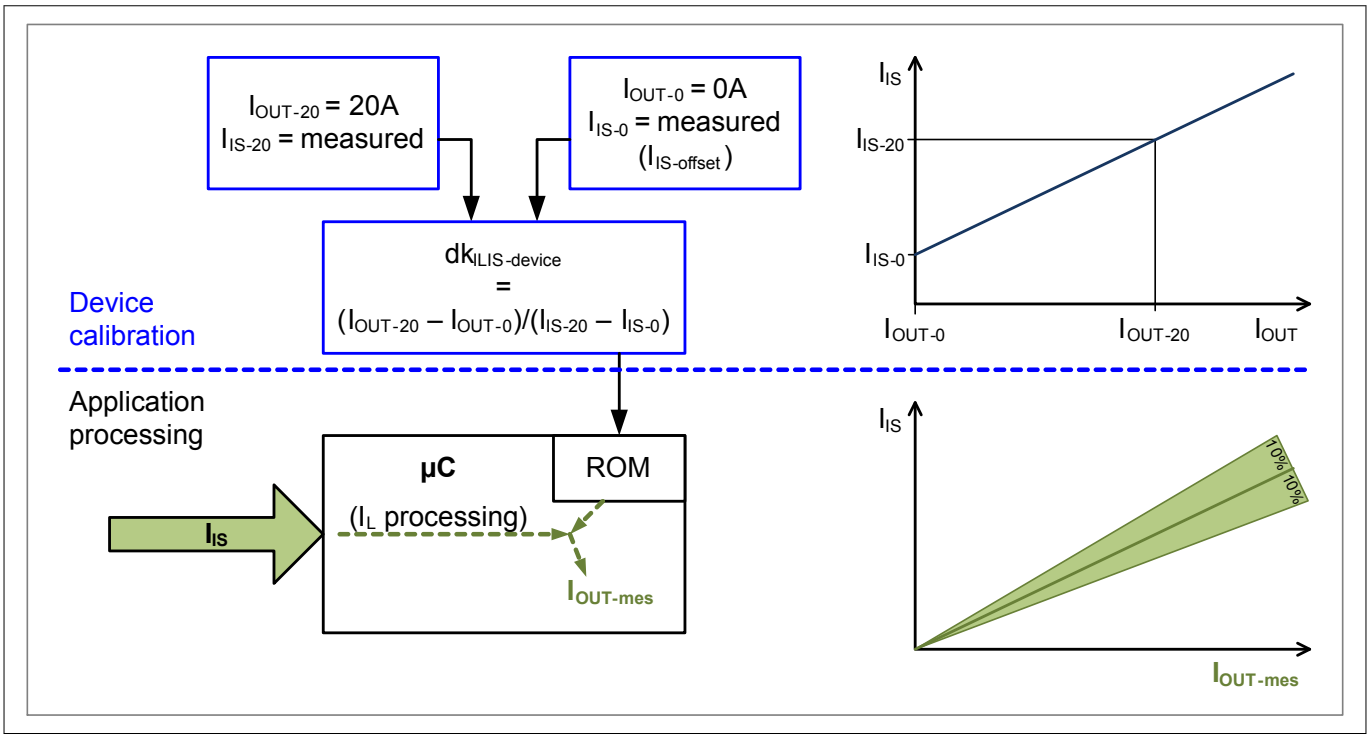

Figure 19 Generating the device fine $dk_{ILIS-device}$.

4.4 Device fine dk_{ILIS} and temperature compensation

On the other hand, the dk_{ILIS} is dependent on the temperature, which is shown in ***Figure 14***. These figures show a characteristic temperature drift with a low content of production spread. This makes it possible to measure the temperature on the PCB and reduce the temperature dependency by means of a calculation in the microcontroller. This procedure is illustrated in ***Figure 20*** .

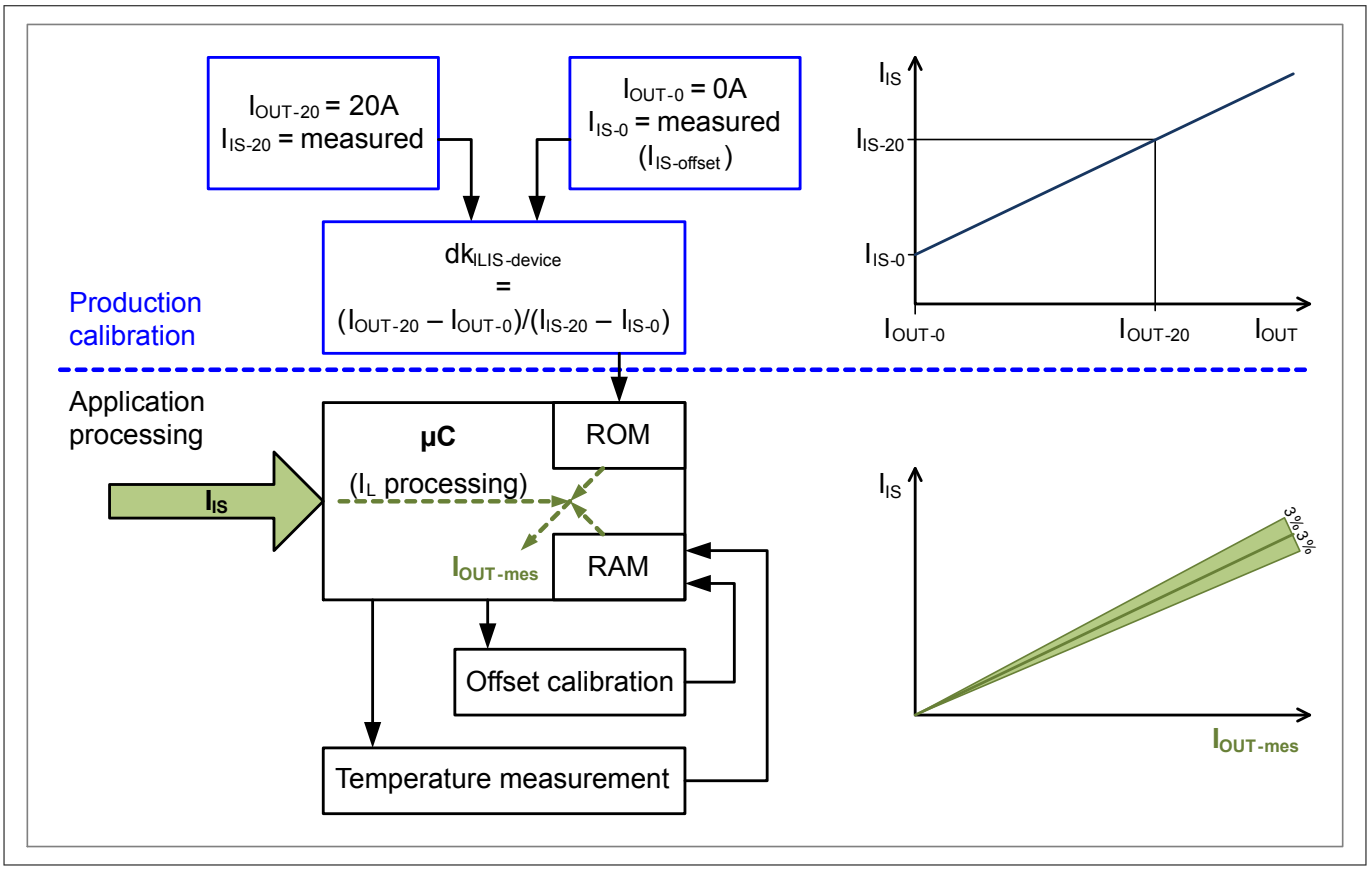

Figure 20 Load current "I_{OUT}" calculation with temperature compensation

Taking the extreme values from ***Figure 14*** :

- $dk_{ILIS-max-C}$ = 1.08 (blue @ -40 °C)
- $dk_{ILIS-min-C}$ = 1.05 (green @ -40 °C)
- $dk_{ILIS-max-H}$ = 0.955 (green @ 150 °C)
- $dk_{ILIS-min-H}$ = 0.925 (blue @ 150 °C)

Multiplying the min. values with a factor of 0.97 (-3% aging) produces the following values:

- $dk_{ILIS-max-C}$ = 1.08 (blue @ -40 °C)
- $dk_{ILIS-min-C-old}$ = 1.0185 (green @ -40 °C)
- $dk_{ILIS-max-H}$ = 0.955 (green @ 150 °C)
- $dk_{ILIS-min-H-old}$ = 0.9 (blue @ 150 °C)

Calculating the typical value for:

- $dk_{ILIS-typ-C}$ = 1.05
- $dk_{ILIS-typ-H}$ = 0.928

These values could be compensated with a temperature measurement and the characteristic from to provide the value of $dk_{ILIS-typ}$ = 1.

With this compensation, the new min. and max. values are:

- $dk_{ILIS-max-C-T}$ = 1.03 (blue @ -40 °C)
- $dk_{ILIS-min-C-old-T}$ = 0.9685 (green @ -40 °C)
- $dk_{ILIS-max-H-T}$ = 1.027 (green @ 150 °C)
- $dk_{ILIS-min-H-old-T}$ = 0.972 (blue @ 150 °C)

After temperature compensation, the min. and max. values are $dk_{ILIS-min-H-old-T}$ and $dk_{ILIS-max-C-T}$.

Ultimately, a current measurement with a precision of ±3% could be achieved!

If higher tolerances are acceptable, the temperature measurement can be less precise.

4.4.1 An example of the I_{IS} failure with a rough temperature estimation

Assuming the dk_{ILIS} was calibrated during production at 25 °C, the I_{IS} measurement failure could be reduced to ±6%, only by estimating if the temperature is above or below 25 °C. This estimation could be done e.g. by using the temperature characteristic of the $I_{IS\text{-}offset}$, which is included in the data sheet.

Temperature below 25° C:

- $dk_{ILIS\text{-}max\text{-}C}$ = 1.08 (blue @ -40 °C)
- $dk_{ILIS\text{-}min\text{-}25°C}$ = 1

Reducing the min. values with the -3% aging (multiplying with 0.97) the following values will be calculated:

- $dk_{ILIS\text{-}max\text{-}C}$ = 1.08 (blue @ -40 °C)
- $dk_{ILIS\text{-}min\text{-}25°C\text{-}old}$ = 0.97

For temperatures above 25 °C the calculation method is essentially the same.

Ultimately, a current measurement with a precision of ±6% could be achieved without any external temperature measurement!

4.5 IS-pin current sensing and fault detection

The IFX007T provides several additional sense and diagnosis functionalities, which will be explained here.

4.5.1 Current sensing concepts in applications

For monitoring purposes, the behavior of the IFX007T can be used for continuous current monitoring, even in freewheeling mode: In bi-directional motor applications with two IFX007T, the freewheeling current can be monitored at the high-side MOSFET in forward direction. As shown in ***Figure 21***, the freewheeling current $I_{FW,HS}$ can be observed with both high-side MOSFETs being closed. In the scenario shown, the IS output of the left IFX007T provides the current dependent signal, while the $I_{FW,HS}$ flows through the right IFX007T in reverse direction.

An overview about the two possible freewheeling current paths in bidirectional motor applications is provided in ***Figure 21***.

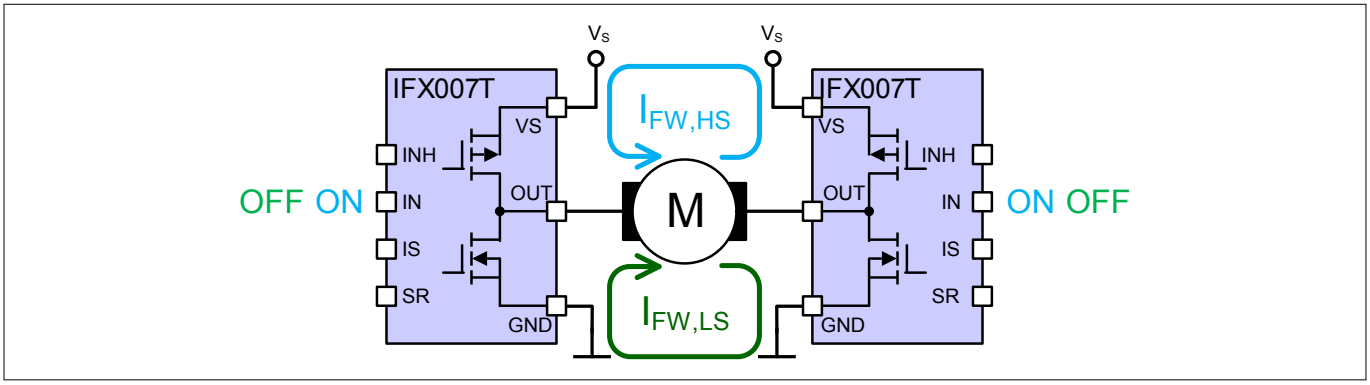

Figure 21 Two freewheeling path options for bi-directional motor applications, implemented with two IFX007T.

4.5.1.1 Advanced current sense and fault diagnosis

The IFX007T allows the following behavior and additional diagnostic possibilities:

- Offset compensation of $I_{IS(offset)}$:
  If no current is flowing through the high-side MOSFET, the current sense offset $I_{IS(offset)}$ can be monitored at the IS-pin. This can be ensured while the high-side switch is being switched off via the IN-pin and the freewheeling path doesn't go through the high-side MOSFET. If measured, this value can be used for an online offset calibration of $I_{IS(offset)}$, according to ***Chapter 4.2***. In ***Figure 22*** this scenario is marked with (2). In the case of a fault condition, the IS-pin will provide a constant current of $I_{IS(lim)}$, which can be clearly distinguished from the lower offset current $I_{IS(offset)}$.
- Online calibration of $I_{IS(offset)}$ and continuous current monitoring:
  If two IFX007T devices are deployed in H-bridge configuration, the user can choose between either monitoring the freewheeling current or the online calibration of $I_{IS(offset)}$ by adapting the freewheeling path accordingly. An offset calibration of $I_{IS(offset)}$ for both the left and right IFX007T can be carried out by choosing a freewheeling path through both low-side MOSFETs, with the freewheeling current $I_{FW,LS}$ displayed in ***Figure 21***. As previously described, the current can be monitored continuously with a freewheeling current $I_{FW,HS}$ flowing through the two high-side MOSFETs.

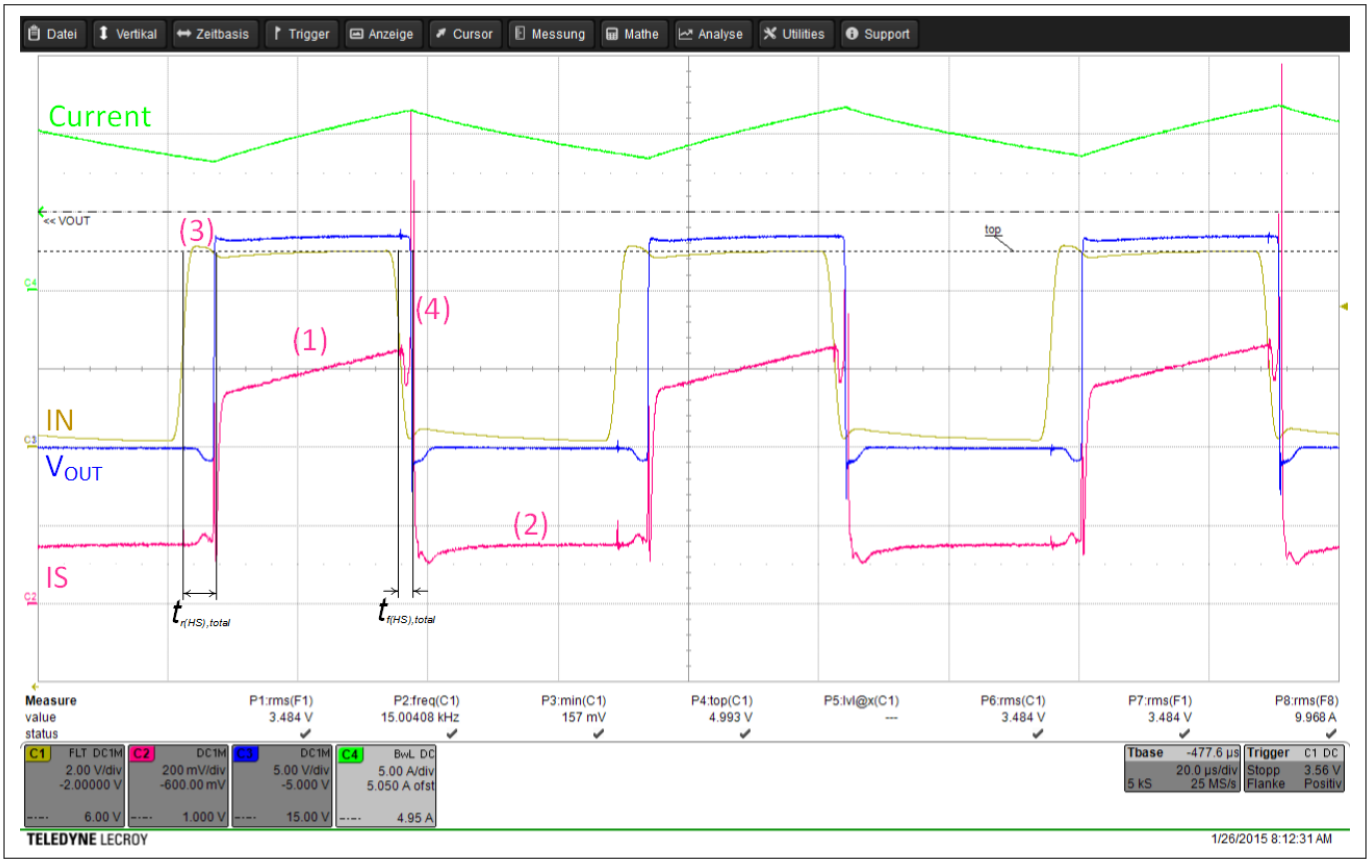

Figure 22 Measurement of a NovalithIC™, switching an inductive load to GND. (1): current sense signal, (2): current sense offset current $I_{IS(offset)}$

4.5.2 Fault detection

The current sense accuracy depends on the spread of the two parameters dk_{ILIS} and $I_{IS(offset)}$. The resulting maximal, typical and minimal behavior is displayed in ***Figure 23*** for the IFX007T. Here, the limits for the sense current in fault condition $I_{IS(lim)}$ are also shown.

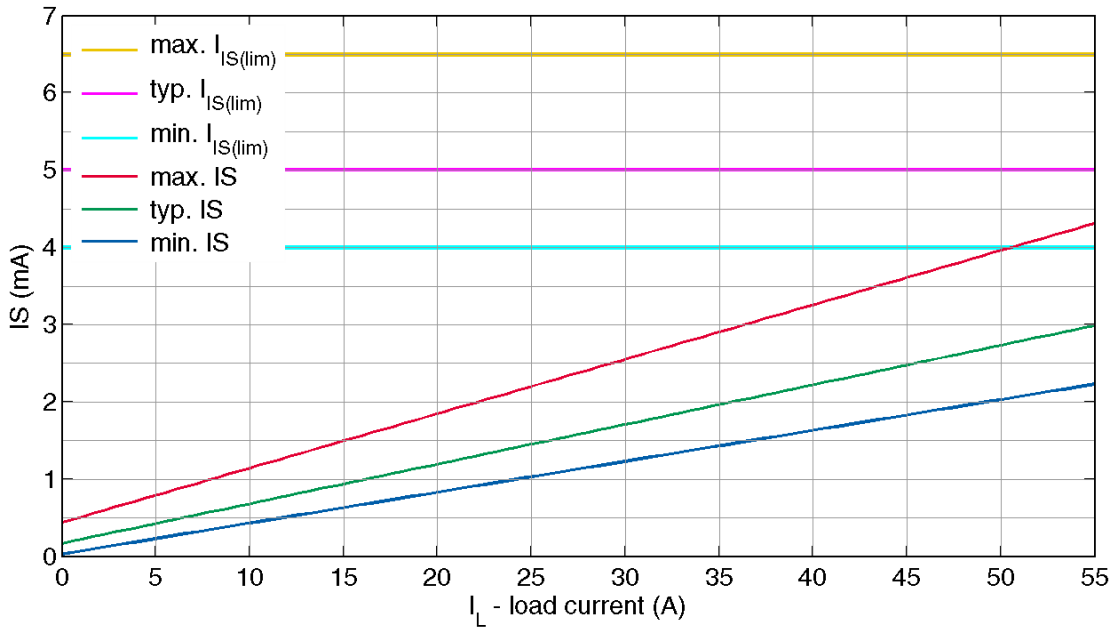

Figure 23 Behavior of the IFX007T's IS output pin for current sense and fault condition according to parameter tolerances

The possibility to distinguish whether a current sense signal or the constant sense current $I_{IS(lim)}$, indicating a fault condition, can be measured at the IS-pin is also an important issue. Therefore the fault distance between the two states is further considered. The combined (possible) output options for both states can be seen in ***Figure 23*** for the IFX007T. For a worst case combination of the three parameters $I_{IS(lim)}$, dk_{ILIS} and $I_{IS(offset)}$, provided in the data sheet for the given tolerances, there is a current range, where it is not possible to distinguish the right operation mode, whether there is a fault or not.

The corresponding break-even point for the IFX007T can be calculated for the load current I_L :

$$I_L = dk_{ILIS} \cdot \left(I_{IS} - I_{IS(offset)}\right) = dk_{ILIS} \cdot \left(I_{IS(lim)} - I_{IS(offset)}\right)$$

Equation 16

$$I_L = 14 \cdot 10^3 \cdot (4\,\text{mA} - 385\,\mu\text{A}) \approx 50,6\,A$$

Equation 17

For such a system, it wouldn't be possible to distinguish easily between the fault condition current $I_{IS(lim)}$ and a current sense signal, for I_L > 50 A for the IFX007T. For a more precise consideration, also the temperature dependency of $I_{IS(lim)}$, dk_{ILIS} and $I_{IS(offset)}$ has to be considered. For the given critical area for load currents I_L > 50 A, especially the parameters dk_{ILIS} and $I_{IS(lim)}$ have the greatest influence. The temperature dependency of dk_{ILIS} is described in ***Chapter 4.1.2***, and of $I_{IS(lim)}$ in ***Chapter 4.5.2.1***:

- For a rising temperature, the fault condition current $I_{IS(lim)}$ increases, and vice versa.
- For a rising temperature the dk_{ILIS} decreases and vice versa.

This relationship is also illustrated by ***Figure 24***.

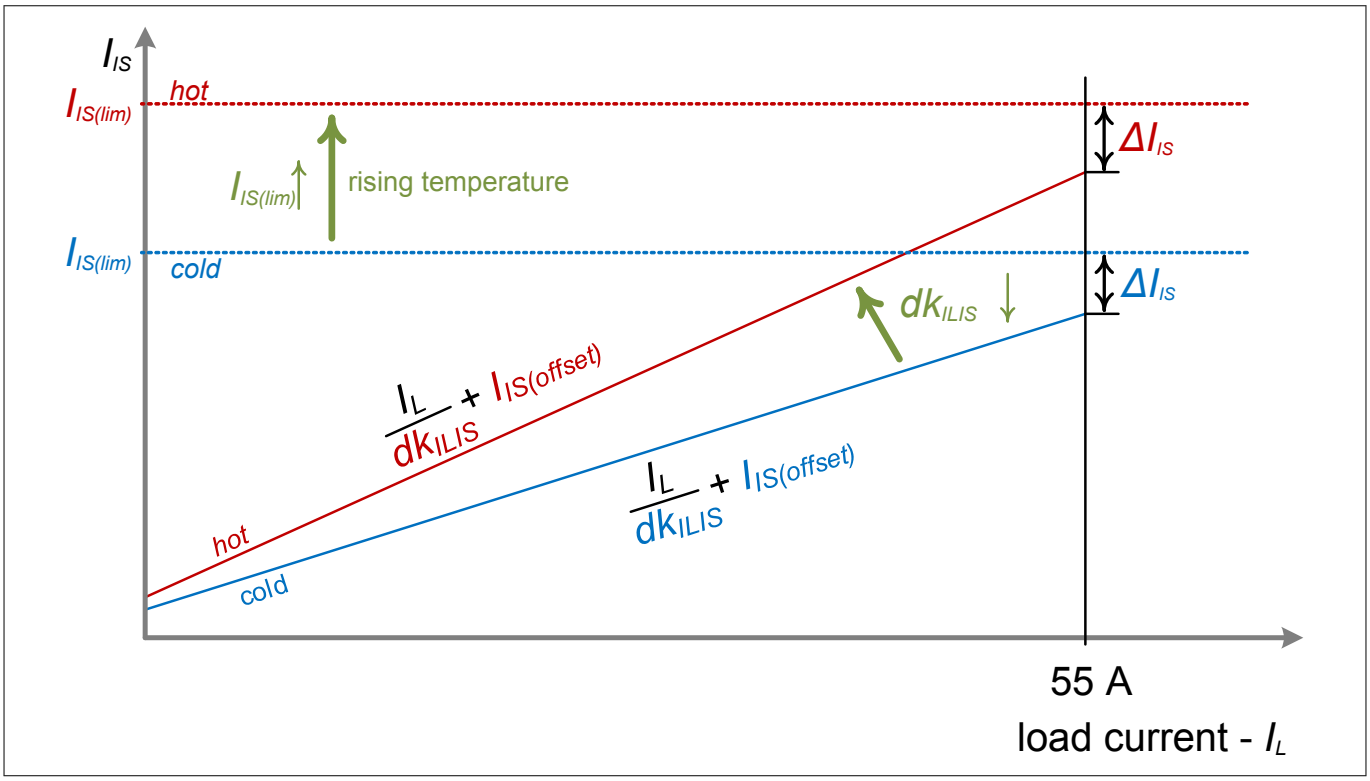

Figure 24 Illustration of the temperature dependencies of the fault distance and relevant parameters

Additionally the difference between the fault condition current $I_{IS(lim)}$ and the sensed current $I_{IS}(I_L)$ can be calculated as follows:

$$\Delta I_{IS} = I_{IS(lim)} - I_{IS(I_L)} = I_{IS(lim)} - \left(\frac{I_L}{dk_{ILIS}} + I_{IS(offset)}\right)$$

Equation 18

Equation 18 shows, that for a rising temperature, both $I_{IS(lim)}$ and $I_{IS}(I_L)$ (due to I_L / dk_{ILIS}) increase.

Combining the spread of dk_{ILIS} and $I_{IS(lim)}$ over temperature, this behavior results in a ΔI_{IS} that, at the min. current limitation detection level $I_{CLx0,min}$, is typically above 0,75 mA for the IFX007T, shown in ***Figure 25*** and ***Figure 26***. To summarize, we can say that it is possible to distinguish between a current sense signal $I_{IS}(I_L)$ and a fault condition current $I_{IS(lim)}$ for any temperature.

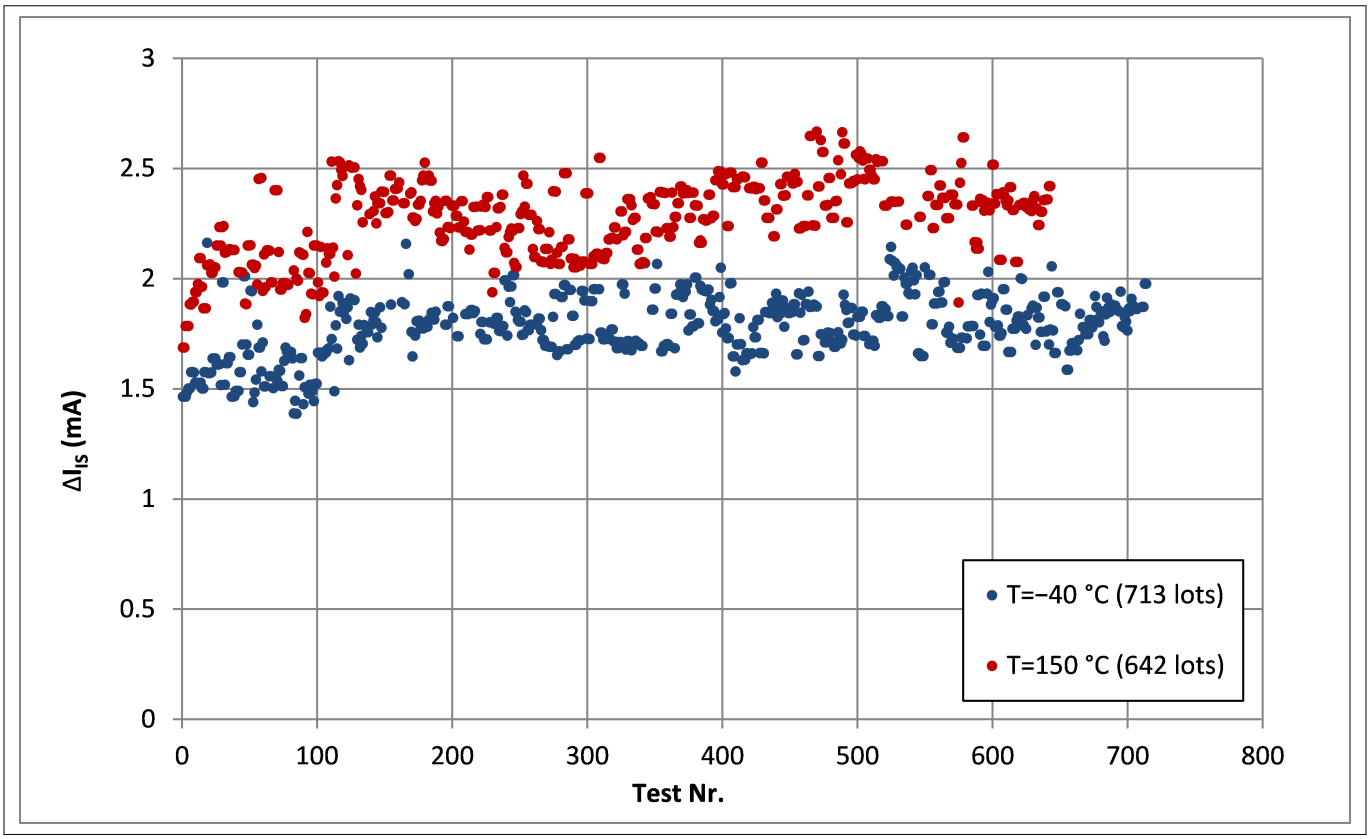

Figure 25 Temperature dependent ΔI_{IS} for IFX007T, according to *Equation 18*, for the median value of each lot and temp. at the min. current limitation detection level $I_L = I_{CLx0,min}$ = 55 A.

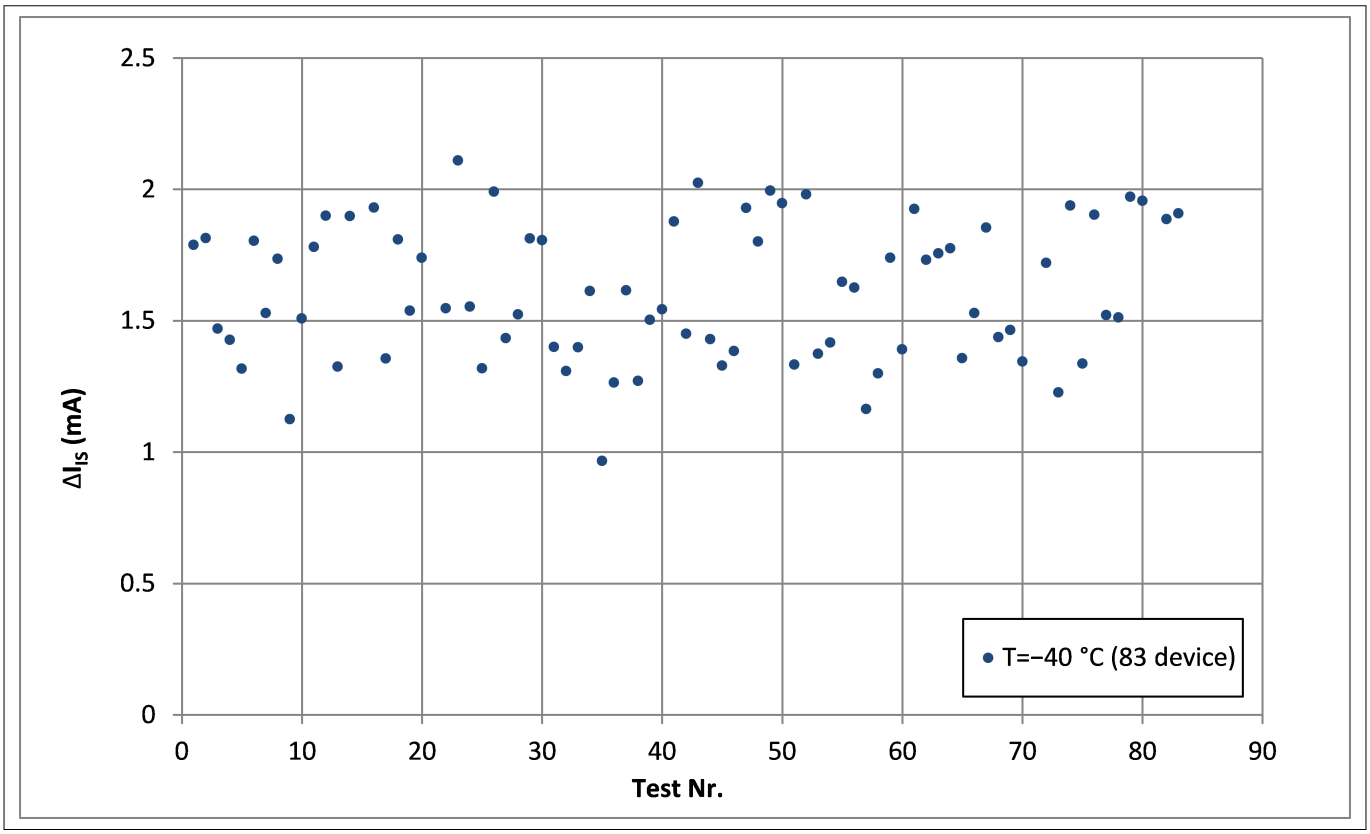

Figure 26 Temperature dependent ΔI_{IS} for IFX007T, according to *Equation 18* calculated individually for each tested device of lot 85 for −40°C in *Figure 25*, with $I_L = I_{CLx0,min} = 55$ A.

4.5.2.1 Temperature drift of the IS-pin's current in fault condition $I_{IS(lim)}$

The characteristics of the $I_{IS(lim)}$ vs. temperature and production spread is shown in *Figure 27* for the IFX007T, including a series of lab measurement points for one device.

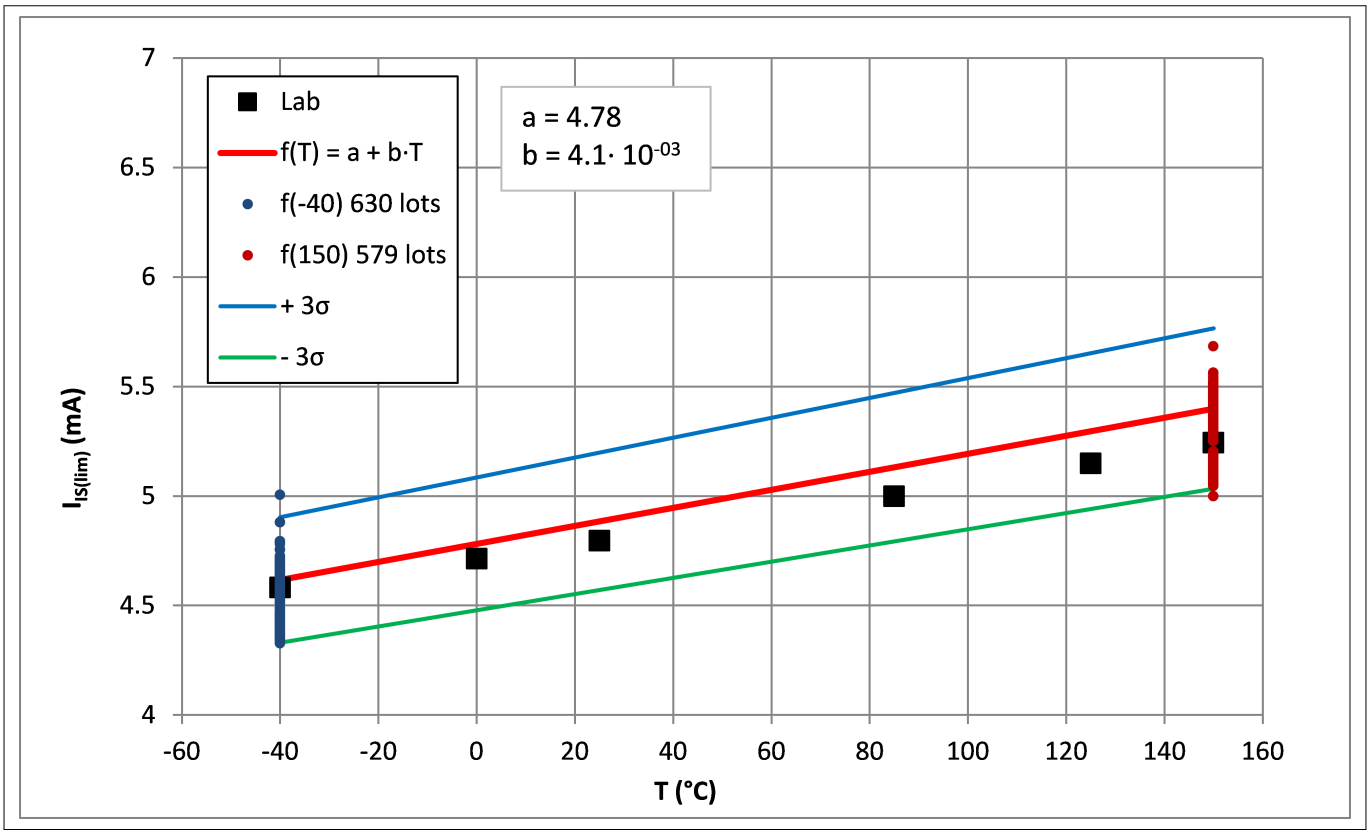

Figure 27 IFX007T $I_{IS(lim)}$ vs. temperature

4.5.2.2 Failure detection flow chart

The consideration of ΔI_{IS} above provides a procedure for detecting fault conditions ($I_{IS(lim)}$):

- Calibration of $I_{IS(lim)}(T_0)$ for a specific temperature T_0: Calculation of offset a with the given / typical slope b. Ideally measurement of $I_{IS(lim)}(T_1)$ for a second temperature T_1, to perform a two point calibration and calculate both offset a and slope b for each individual device.
- Calculation of temperature dependent $I_{IS(lim)}(T)$ = f(T) while the device is operating according to ***Chapter 4.5.2.1***.
- If a current limit of $I_{IS} = I_{IS(lim)}(T)$ - 0.75 mA is exceeded, a fault condition is detected.

Additional measures are available for ascertaining fault conditions. ***Figure 28*** describes a possible procedure. Carrying out a plausibility check after detecting a potential fault allows you to determine if a specific load current value in the current range of $I_{IS(lim)}$ is possible at a specific operating point.

If this is the case, check whether that value stays in a certain range by performing a series of measurements. Depending on the application, the scattering of the current sense signal of an electric motor should be much higher than that of the constant fault current. An additional way of validating a fault condition is by measuring the IS output pin for a low IN input pin. As illustrated in ***Figure 21***, the fault condition can be monitored by choosing the low-side freewheeling path, ensuring that no current is flowing through the high-side MOSFETs. The fault condition current $I_{IS(lim)}$ can be clearly distinguished from the lower offset current $I_{IS(offset)}$. For applications running with a PWM duty cycle of 100%, the duty cycle must be reduced for certain cycles in order to validate a fault condition. This fault detection procedure is summarized in ***Figure 28***.

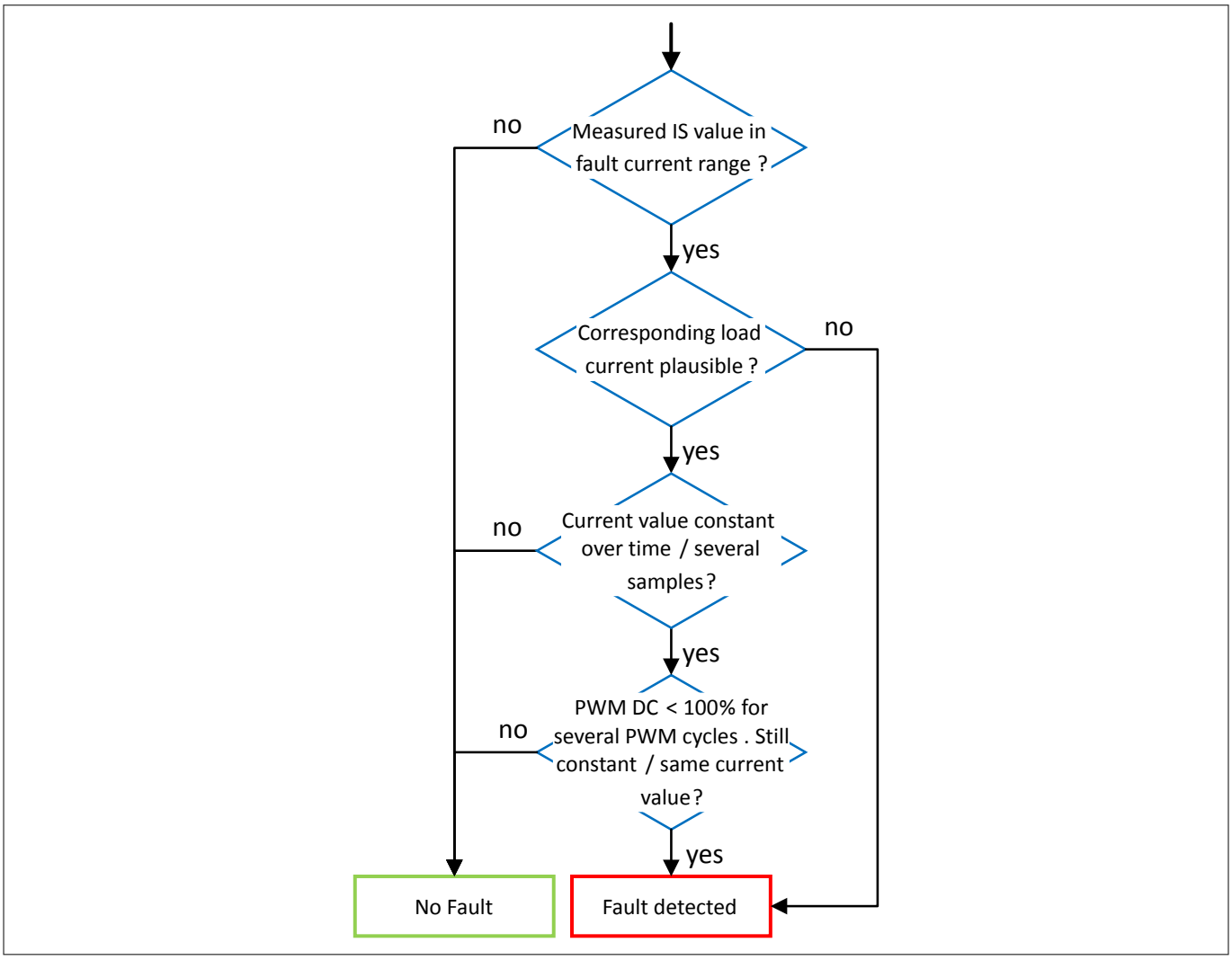

Figure 28 Possible fault condition validation process flow

4.5.2.3 Lowpass filtered current sense signal

The procedure from ***Figure 28*** can be implemented with the sense current I_{IS} being measured by a phase current measurement, as described in ***Chapter 5.4.2***, or by a being lowpass filtered. A lowpass filter, as shown in ***Figure 29***, allows to perform an uncoupled ADC measurement from the PWM generation.

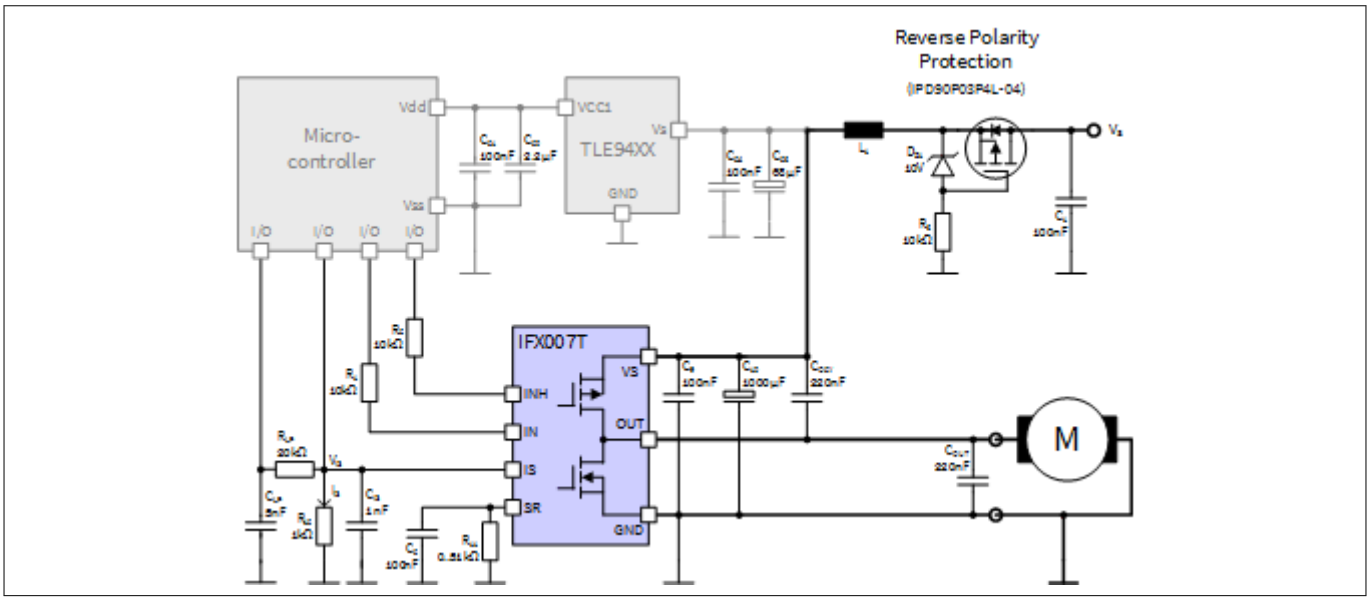

Figure 29 Application circuit including a lowpass filtered current sense signal for a monodirectional motor with IFX007T

The fault distance increases here for a decreasing (effective) duty cycle DC (for a low-side freewheeling path). The average lowpass filtered I_{IS} signal can be estimated to:

$$V_{LP} \approx \left(\frac{I_L}{dk_{ILIS}} \cdot DC + I_{IS(offset)} \right) \cdot R_{12}$$

Equation 19

Based on a measured lowpass filtered voltage V_{LP} the load current I_L can now be estimated as follows:

$$I_L \approx \left(\frac{V_{LP}}{R_{12}} - I_{IS(offset)} \right) \cdot \frac{dk_{ILIS}}{DC}$$

Equation 20

While the fault current is constant at $I_{IS(lim)}$. A possible scenario is shown in ***Figure 30***. Here, a load to ground was simulated. By changing the duty cycle for some periods, the lowpass filtered current sense signal should further decrease thus increasing the fault distance, as the average Motor current decreases and the time during which only the lower offset current is provided by the IS-pin increases.

Another way for fault detection is comparing the lowpass filtered signal V_{LP} with the I_{IS} / V_{IS} signal. As shown in ***Figure 30***, the I_{IS} / V_{IS} signal, with $V_{IS} = I_S \cdot R_{12}$, is above V_{LP} during the PWM's ON-phases and with $I_{IS} = I_{IS(offset)}$ below V_{LP} during the OFF-phase. By comparing the two signals (V_{IS} and V_{LP}), a constant fault signal $I_{IS(lim)}$ can be detected, as their are only transitions during normal operation.

Current Sense Improvement

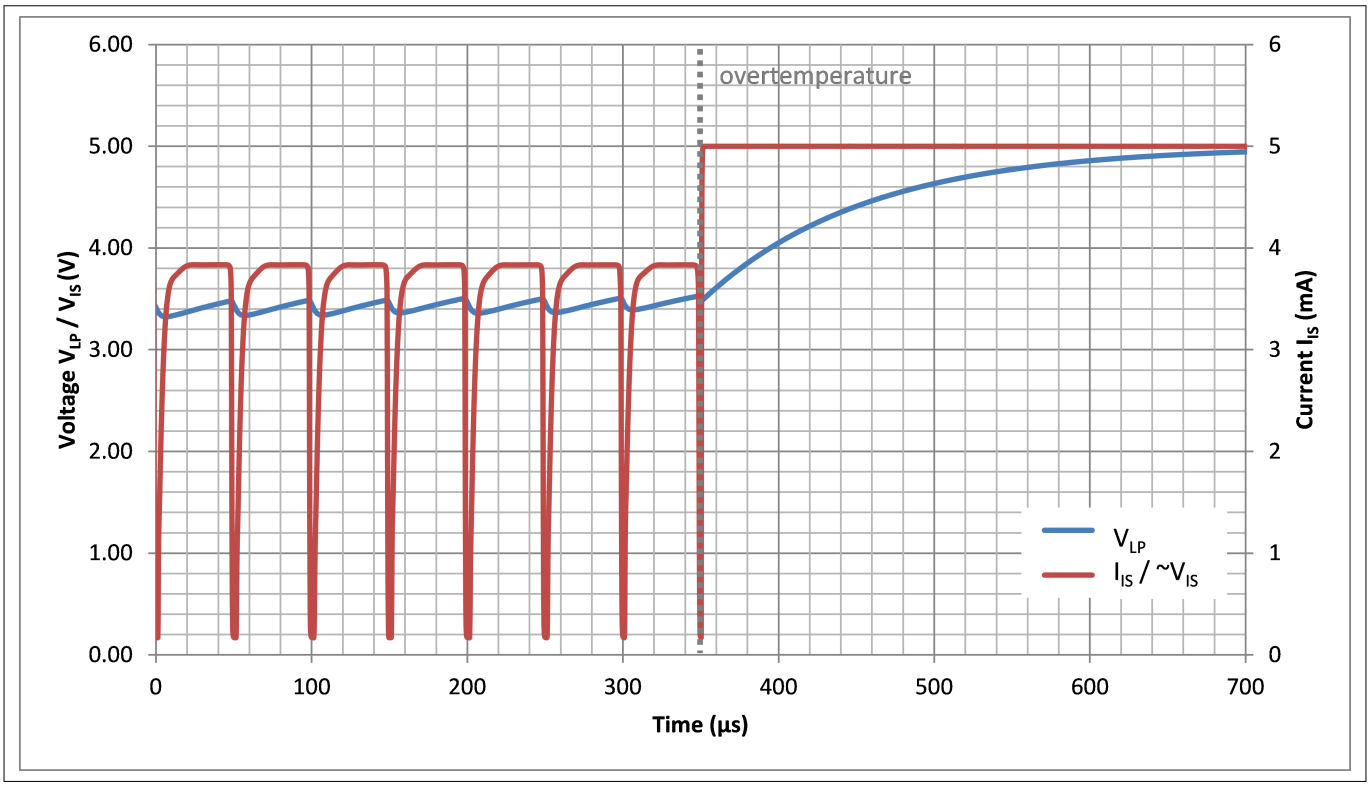

Figure 30 IFX007T simulation: Lowpass-filtered (R_{LP} = 20 kΩ; C_{LP} = 5 nF; R_{12} = 1 kΩ) current sense signal I_{IS} for ADC measurement with the fault condition current $I_{IS(lim)}$ from 350 µs. PWM operation (20 kHz; DC = 90%) with load to ground.

5 Switching Timing

For the ADC measurement of the IS-pin, the timing behavior of the IFX007T needs to be considered. As the current sense output is proportional to the current through the high-side switch, only the high-side switch behavior is considered here exemplary. The behavior of the low-side switch can be considered in an equal fashion. An overview of the rising and falling switching procedure is shown in ***Figure 31***.

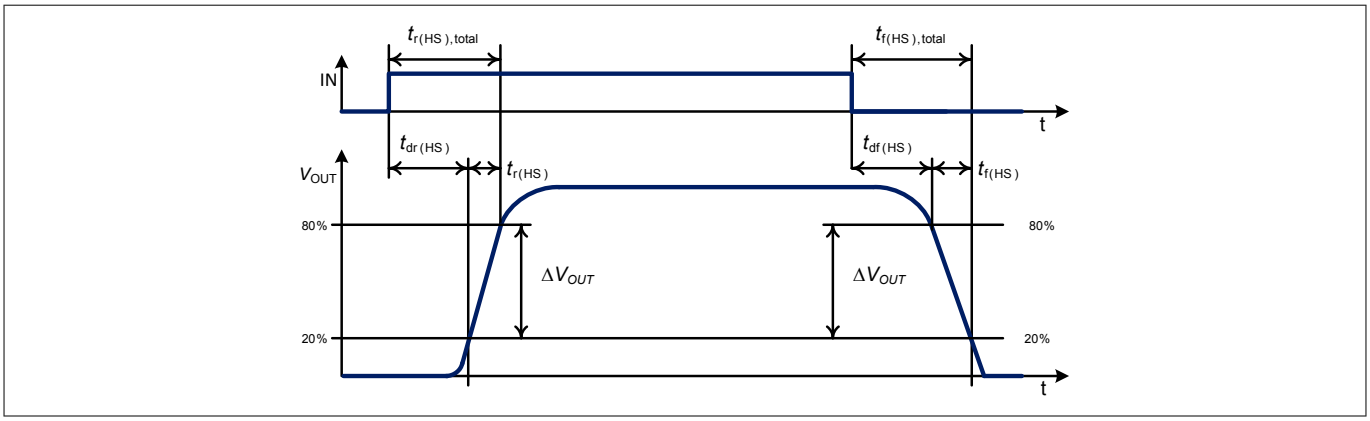

Figure 31 Timing behavior overview of a IFX007T high-side switch

As shown in the data sheet, the time between the IN-pin rising from a 0 to 1 corresponding voltage level and the IFX007T output voltage rising from (around) 0 V to 80 % of the final output voltage (typically: $V_{OUT} \approx V_S$) can be summed up to the following delay, as shown in ***Figure 31***:

$$t_{r(HS),\,total} = t_{dr(HS)} + t_{r(HS)}$$

Equation 21

For a falling edge on the IN input pin, the delay time between the falling edge of the IN input pin and the lower deviation of 20% of the $V_{OUT} \approx V_S$ voltage level of the output pin OUT is considered:

$$t_{f(HS),\,total} = t_{df(HS)} + t_{f(HS)}$$

Equation 22

The timings and slew rates of the power switches can be adjusted by connecting a resistor R_{SR} between the SR-pin and GND-pin of the device. An overview about the, in this document provided, dependencies of the chosen resistor value R_{SR} on relevant timings is given in ***Table 5***.

In the following subchapter, the IFX007T is described.

Table 5 Overview about the dynamic characteristic plots for IFX007T (R_{SR} dependency)

Pos. (in Data Sheet)[1)2)]	Parameter	Symbol	Figure for IFX007T
High Side Switch			
5.2.7	Rise-Time of HS	$t_{r(HS)}$	***Figure 32***
5.2.8	Switch ON Delay Time HS	$t_{dr(HS)}$	***Figure 33***
	$t_{r(HS)}$+ $t_{dr(HS)}$	$t_{r(HS),total}$	***Figure 34***

1 IFX007T Data Sheet, Rev. 1.0, 2018-02-21
2 Please note that the provided data is based on a limited number of production parts for a limited period of time.

Table 5 Overview about the dynamic characteristic plots for IFX007T (R_{SR} dependency) (continued)

Pos. (in Data Sheet)[1)2)]	Parameter	Symbol	Figure for IFX007T
5.2.9	Fall-Time of HS	$t_{f(HS)}$	***Figure 35***
5.2.10	Switch OFF Delay Time HS	$t_{df(HS)}$	***Figure 36***
	$t_{f(HS)}$+ $t_{df(HS)}$	$t_{f(HS),total}$	***Figure 37***
Low Side Switch			
5.2.11	Rise-Time of LS	$t_{r(LS)}$	***Figure 38***
5.2.12	Switch OFF Delay Time LS	$t_{dr(LS)}$	***Figure 39***
	$t_{r(LS)}$+ $t_{dr(LS)}$	$t_{r(LS),total}$	***Figure 40***
5.2.13	Fall-Time of HS	$t_{f(LS)}$	***Figure 41***
5.2.14	Switch ON Delay Time LS	$t_{df(LS)}$	***Figure 42***
	$t_{f(LS)}$+ $t_{df(LS)}$	$t_{r(LS),total}$	***Figure 43***

1 IFX007T Data Sheet, Rev. 1.0, 2018-02-21
2 Please note that the provided data is based on a limited number of production parts for a limited period of time.

5.1 IFX007T Switching Time Dependency on Slew Rate Resistance

Unless otherwise specified, the times are specified for V_S = 13.5 V, -40 °C ≤ T ≤ 150 °C, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}) and single pulse. The typical values are based on the test of all product in the past years. The maximum and minimum values are based on the ±3σ and are replaced by test limits in the case of exceeding the datasheet.

5.1.1 Timing behavior for rising edge on high-side switch

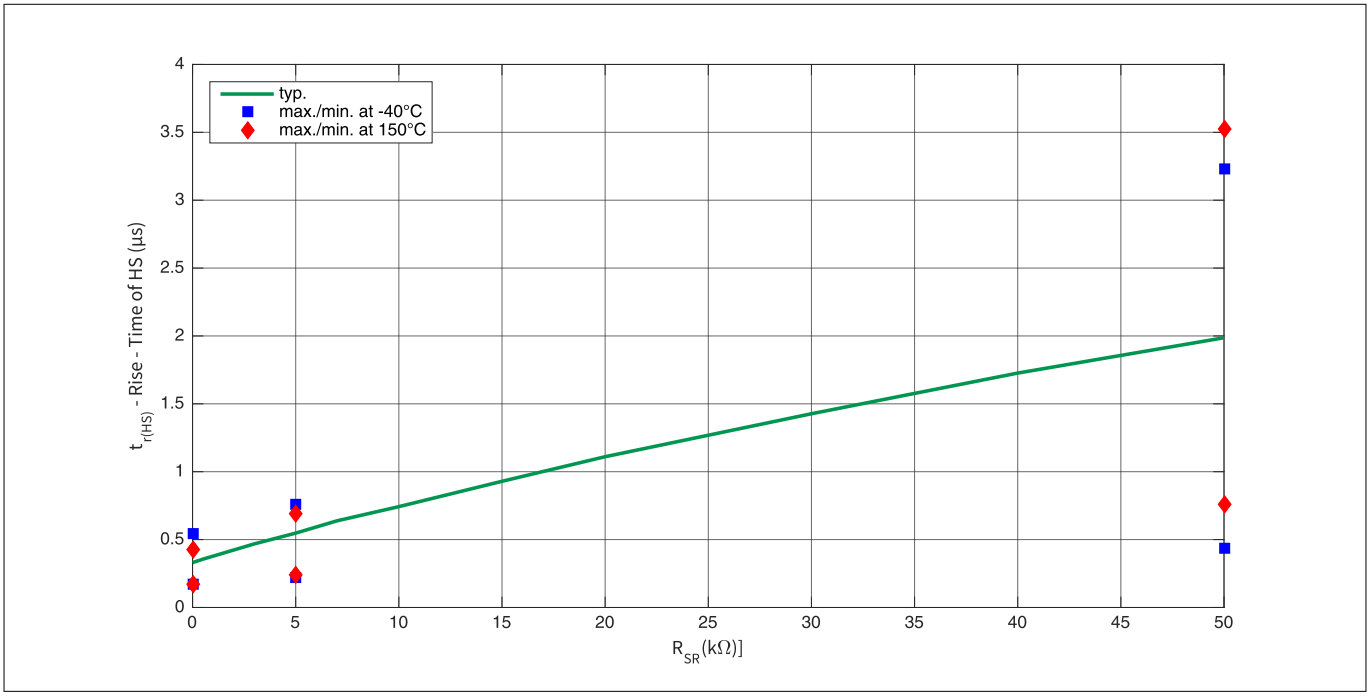

Figure 32 $t_{r(HS)}$: Dependency of the slew rate resistor R_{SR} on the rise-time of the high-side switch of IFX007T

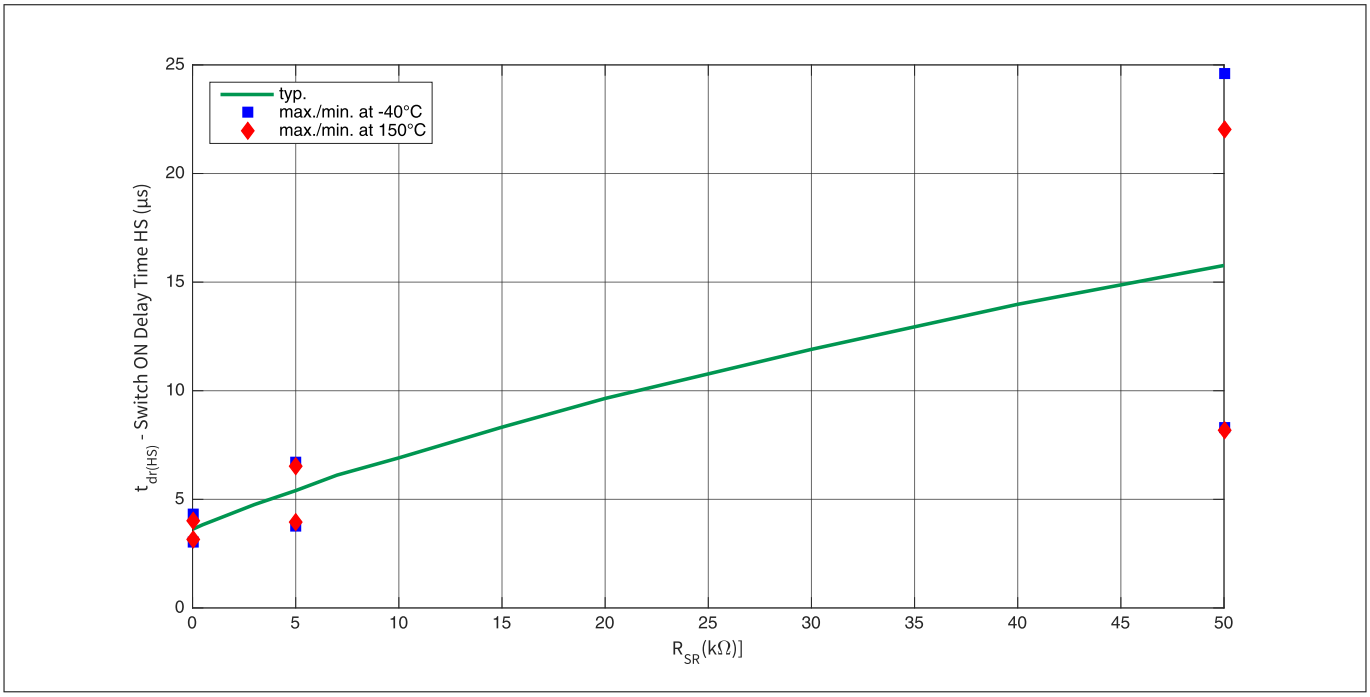

Figure 33 $t_{dr(HS)}$**: Dependency of the slew rate resistor** R_{SR} **on the switch ON delay time of the high-side switch of IFX007T**

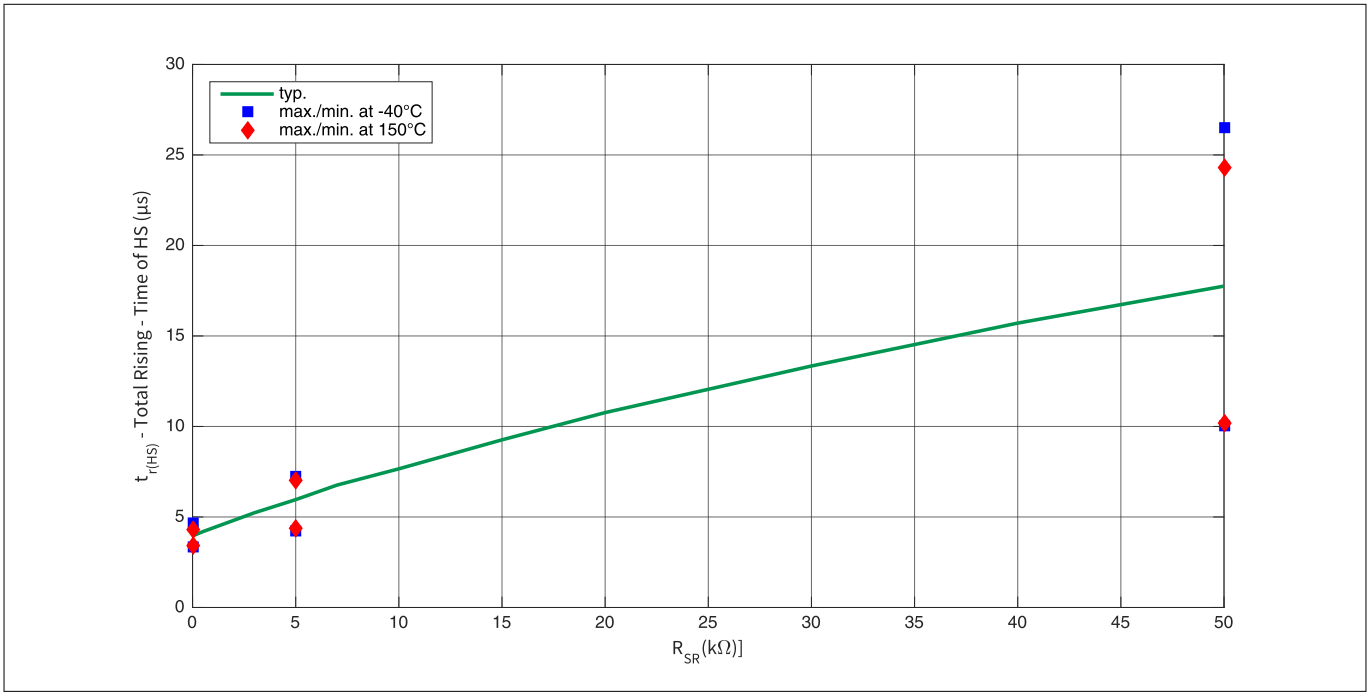

Figure 34 **Dependency of the slew rate resistor** R_{SR} **on the total rising time of the high-side switch with** $t_{r(HS),total} = t_{r(HS)} + t_{dr(HS)}$**: IFX007T**

5.1.2 Timing behavior for falling edge on high-side switch

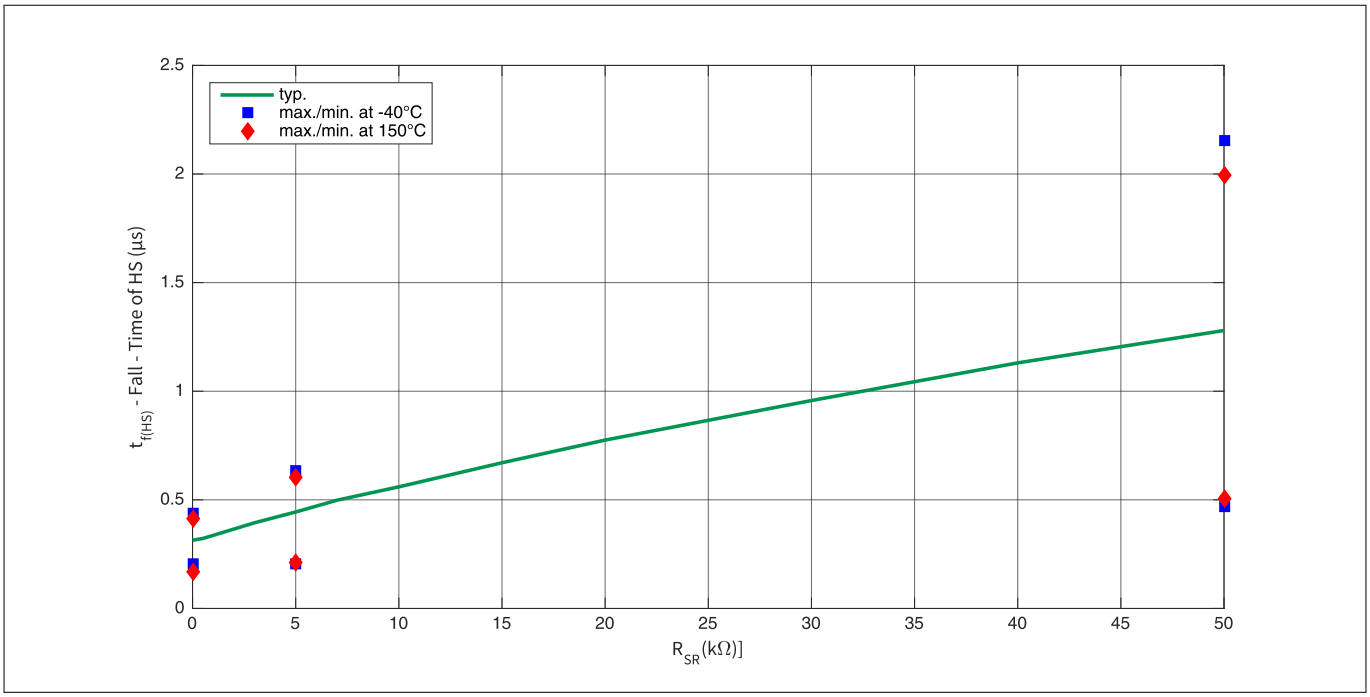

Figure 35 $t_{f(HS)}$: Dependency of the slew rate resistor R_{SR} on the fall-time of the high-side switch of IFX007T

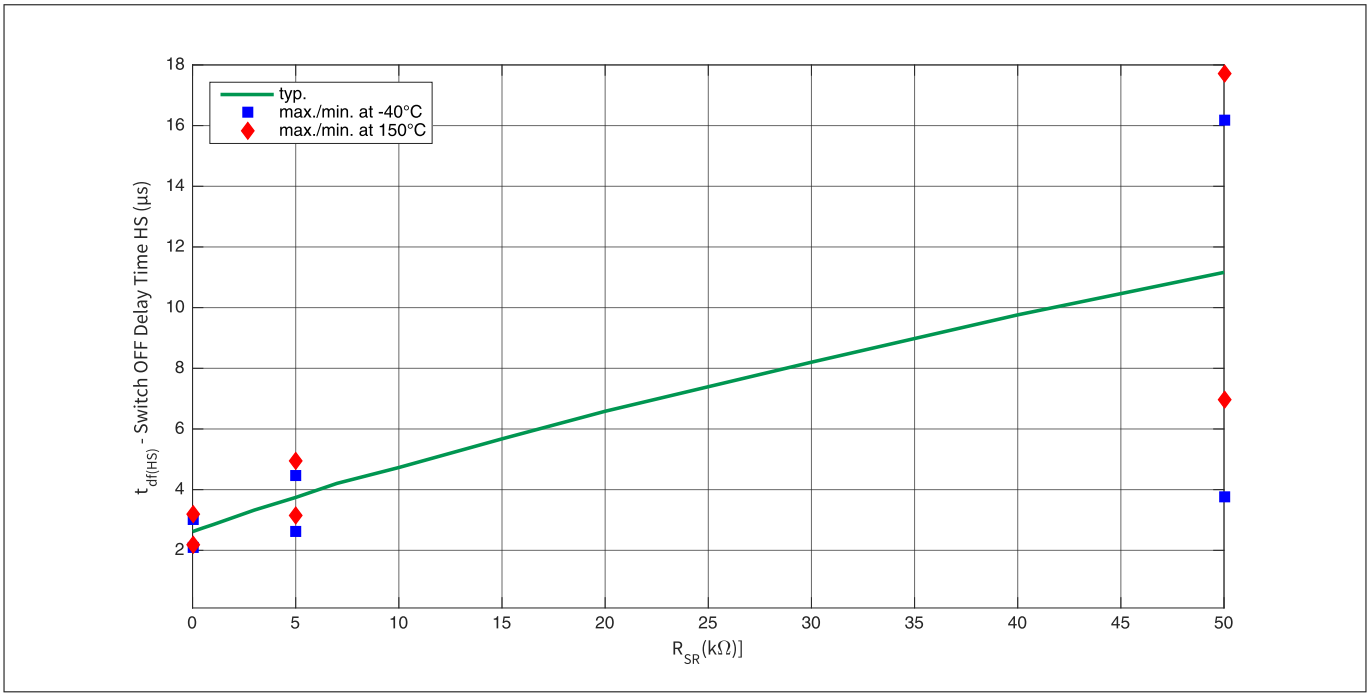

Figure 36 $t_{df(HS)}$: Dependency of the slew rate resistor R_{SR} on the switch OFF delay time of the high-side switch of IFX007T

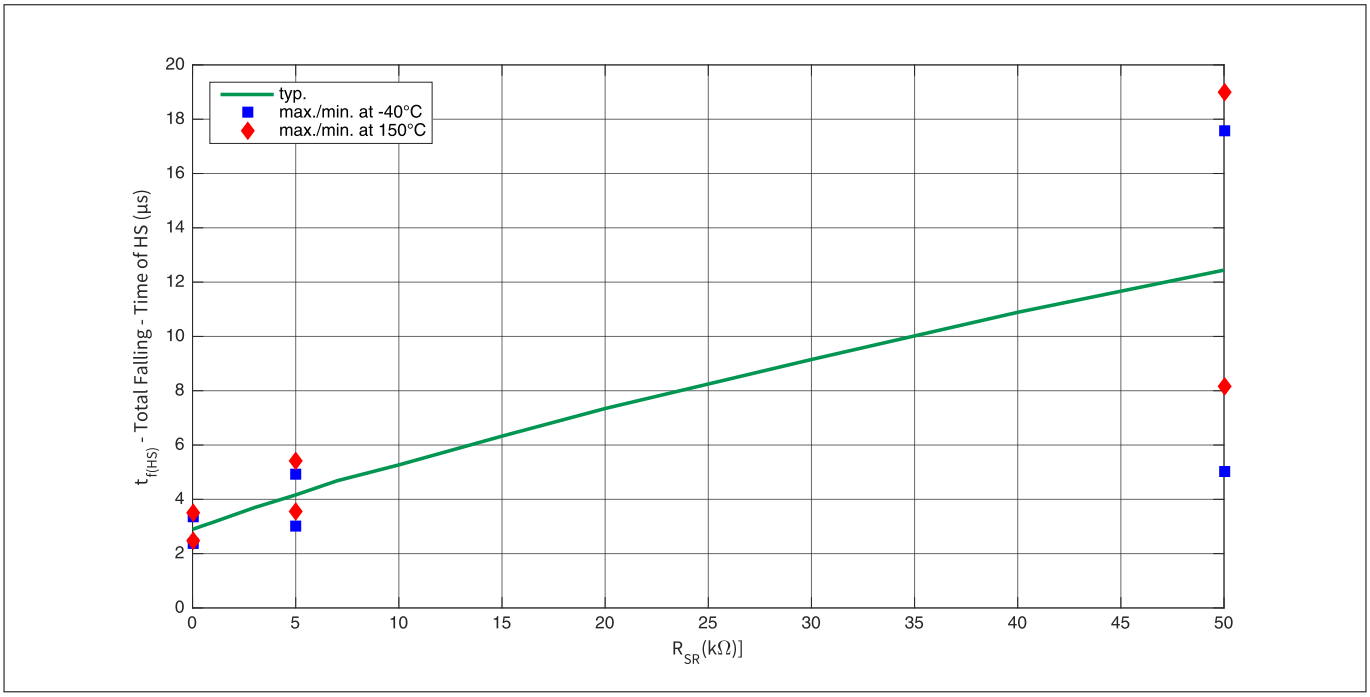

Figure 37 Dependency of the slew rate resistor R_{SR} on the total falling time of the high-side switch with $t_{f(HS),total} = t_{f(HS)} + t_{df(HS)}$: IFX007T

5.1.3 Timing behavior for rising edge on low-side switch

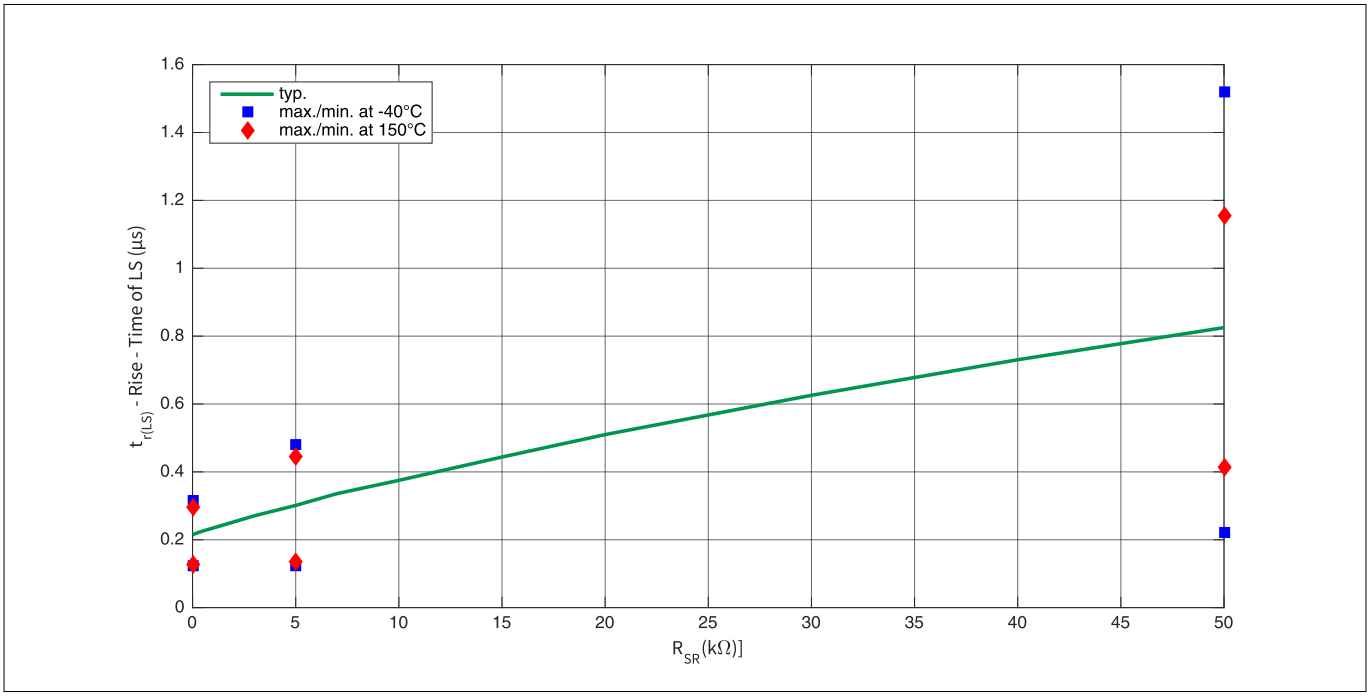

Figure 38 $t_{r(LS)}$: Dependency of the slew rate resistor R_{SR} on the rise-time of the low-side switch of IFX007T

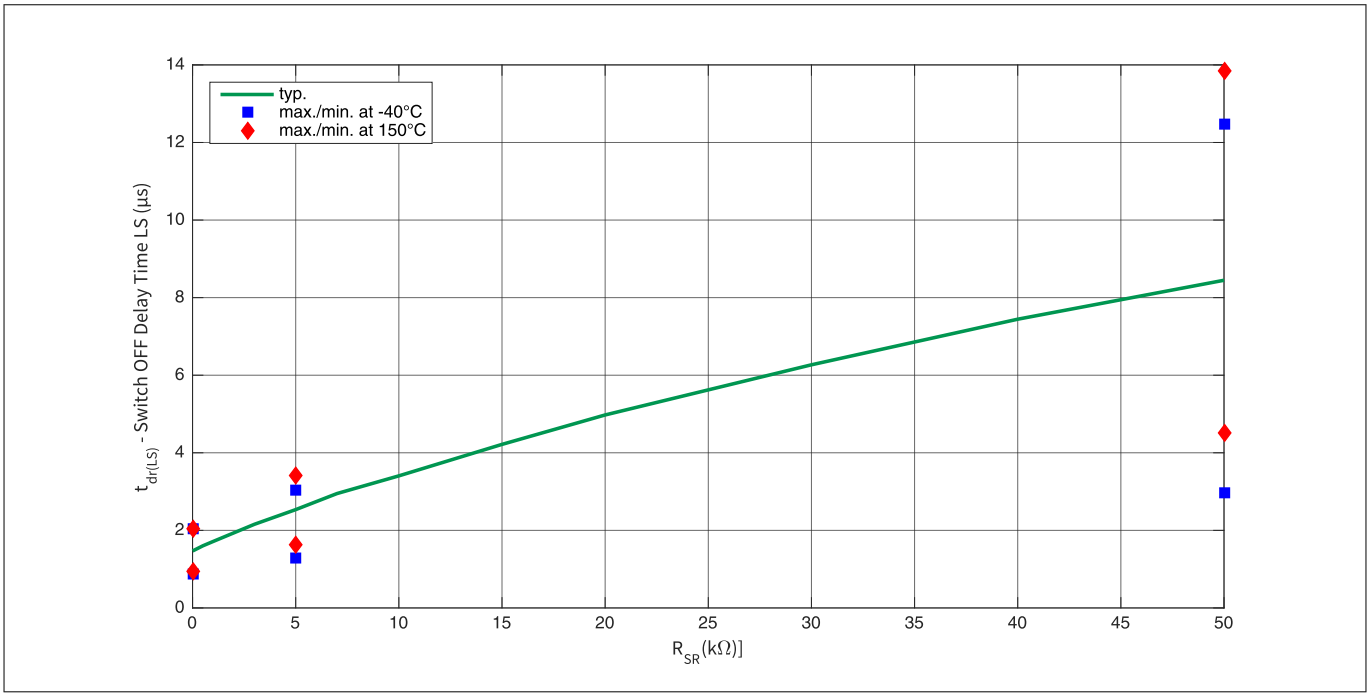

Figure 39 $t_{dr(LS)}$: Dependency of the slew rate resistor R_{SR} on the switch OFF delay time of the low-side switch of IFX007T

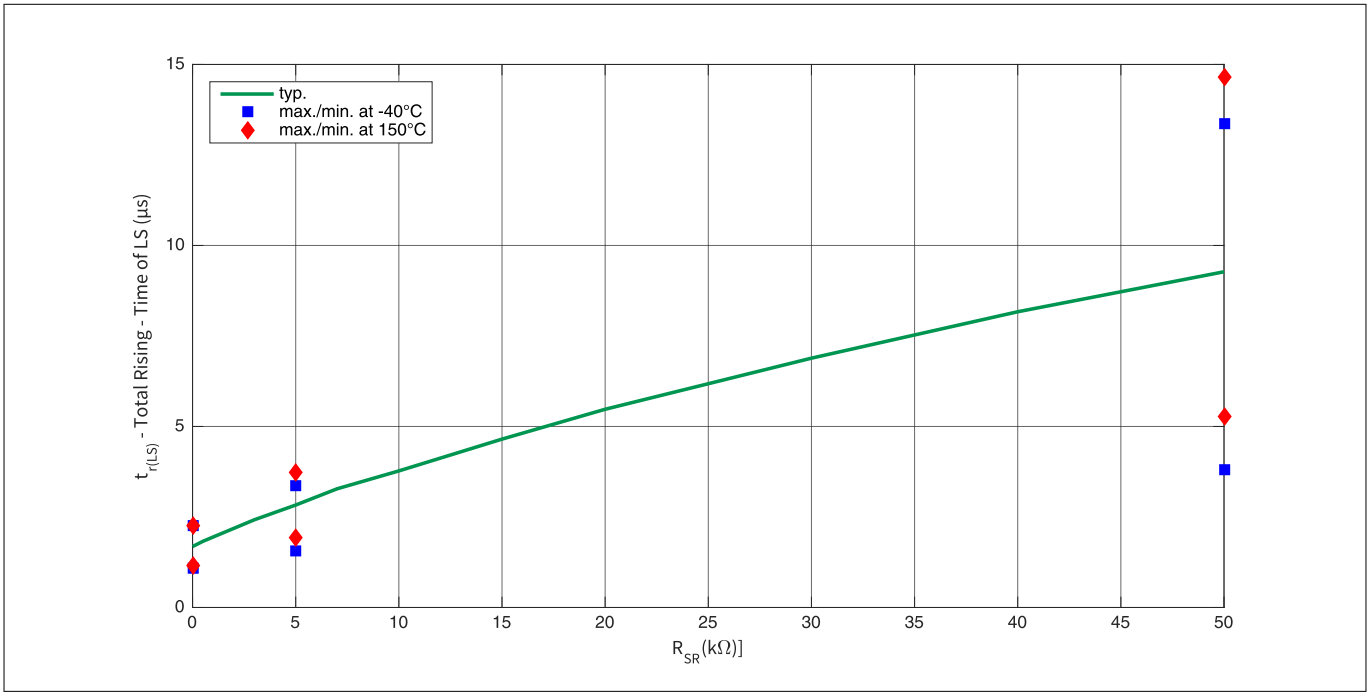

Figure 40 Dependency of the slew rate resistor R_{SR} on the total rising time of the low-side switch with $t_{r(LS),total} = t_{r(LS)} + t_{dr(LS)}$: IFX007T

5.1.4 Timing behavior for falling edge on low-side switch

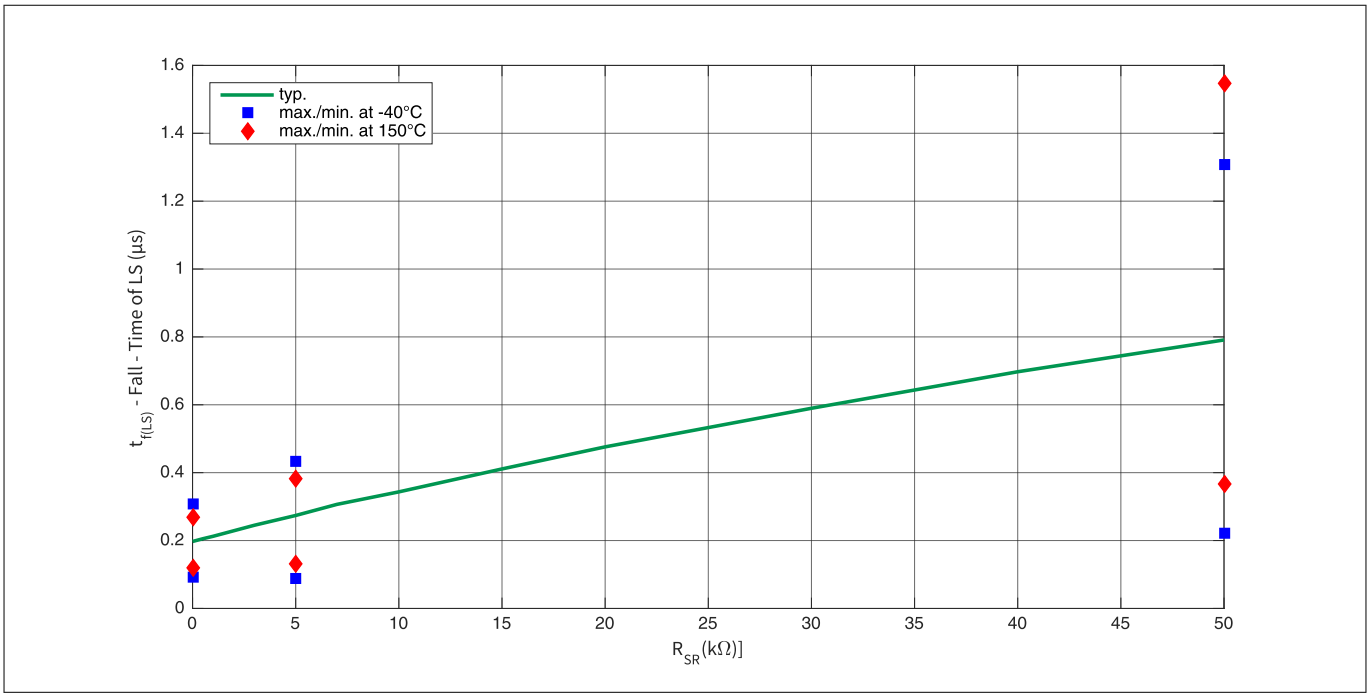

Figure 41 $t_{f(LS)}$: Dependency of the slew rate resistor R_{SR} on the fall-time of the low-side switch of IFX007T

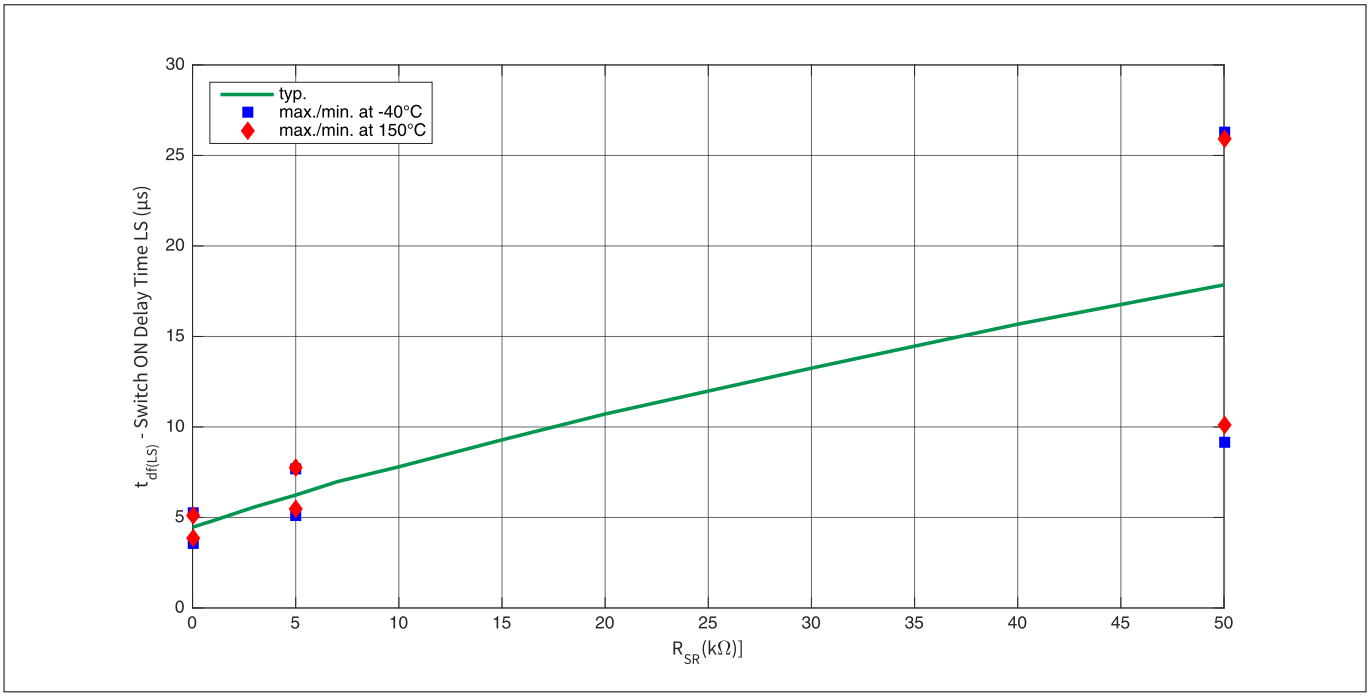

Figure 42 $t_{df(LS)}$: Dependency of the slew rate resistor R_{SR} on the switch ON delay time of the low-side switch of IFX007T

Switching Timing

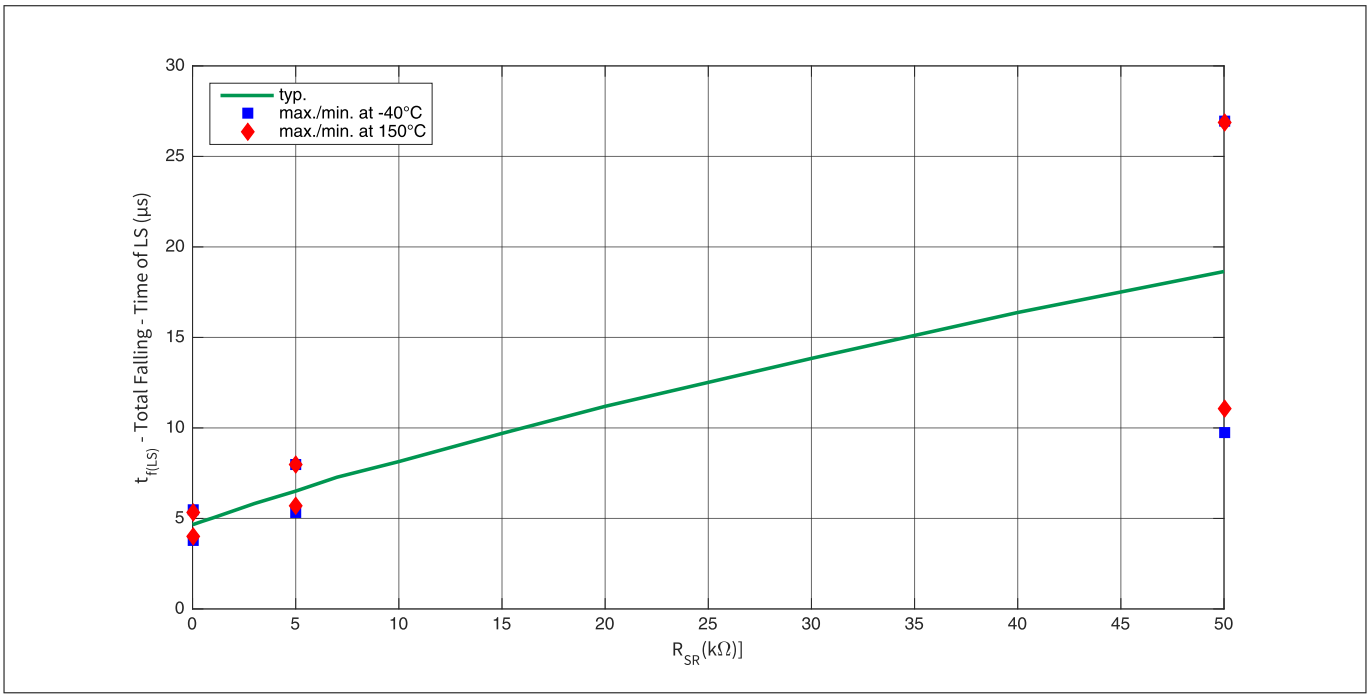

Figure 43 Dependency of the slew rate resistor R_{SR} on the total falling time of the low-side switch with $t_{f(LS),total} = t_{f(LS)} + t_{df(LS)}$: IFX007T

5.2 Error of total delay time

The resulting relative error for the ±3σ values, compared to the mean $t_{x(HS),total}$ value, is summarized in ***Figure 45***. The error is calculated as follows:

$$\text{rel, error} = \frac{t_{x(HS),\,min/max} - t_{x(HS),\,mean}}{t_{x(HS),\,mean}}$$

Equation 23

This parameter spread needs to be taken into account especially for short PWM cycle times, respectively high PWM frequencies. If the relative $t_{r(HS),total}$ / $t_{f(HS),total}$ error is in the same order of magnitude as the application's PWM cycle time, a separate calibration can be considered to measure the delay times of the individual IFX007T devices.

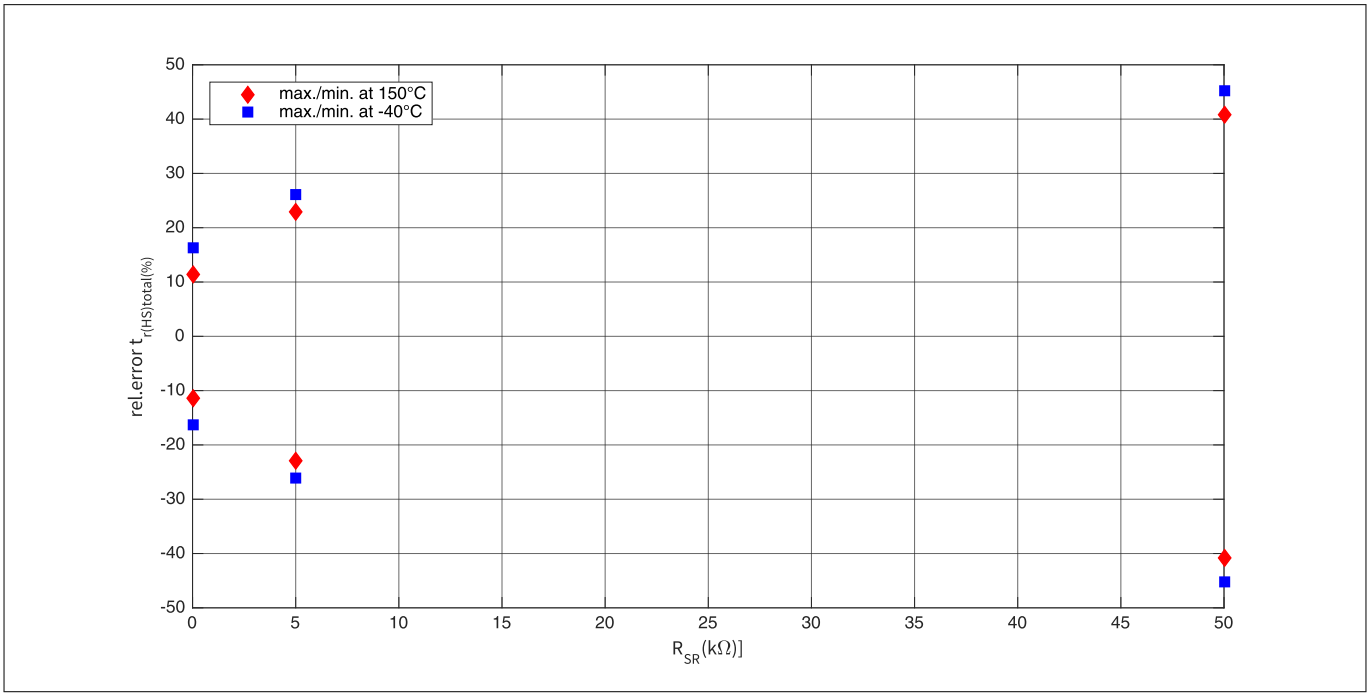

Figure 44 Relative error of the total delay time $t_{r(HS),total}$ for rising edges. Relative error according to *Equation 23* for IFX007T.

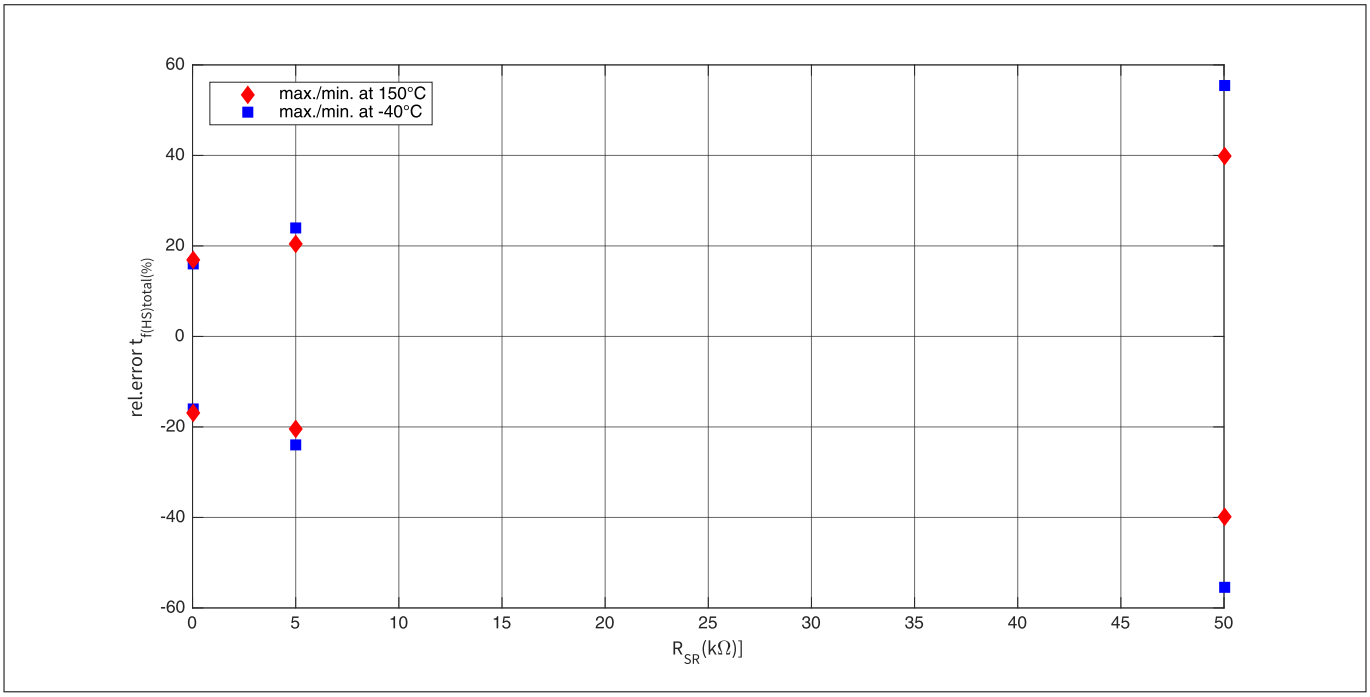

Figure 45 Relative error of the total delay time $t_{f(HS),total}$ for falling edges. Relative error according to *Equation 23* for IFX007T.

5.3 Delay time calibration

One possibility to determine the total rising time $t_{r(HS),total}$ and the falling time $t_{f(HS),total}$ respectively, is by measuring the time once in an end of line test. For such a (single) measurement, the influence of certain parameters like the supply voltage or the load current has to be considered as well and the test setup has to be adjusted accordingly.

It is also possible to use continuous calibration during operation. With such a method, the influence of changing outside parameters is constantly taken into account. In the following chapter, an output voltage (***Chapter 5.3.1***) is suggested.

5.3.1 Output voltage based calibration

This method can be implemented if both the supply voltage V_S and the IFX007T's output voltage V_{OUT} at the OUT-pin are measured. In that case it would be possible to measure the time between setting the IN input pin from low to high (or from high to low for $t_{f(HS),total}$) and the point of time, the output voltage V_{OUT} is greater than or equal to 0.8 V_S. The measurement procedure is illustrated in ***Figure 46***.

The procedure for the total falling delay time $t_{f(HS),total}$ measurement can be performed in a similar fashion: the delay time between the falling edge of the IN-pin and the lower deviation of 20% of the $V_{OUT} \approx V_S$ voltage level is considered.

If these two voltage levels are monitored during operation, an online calibration can be performed periodically, too.

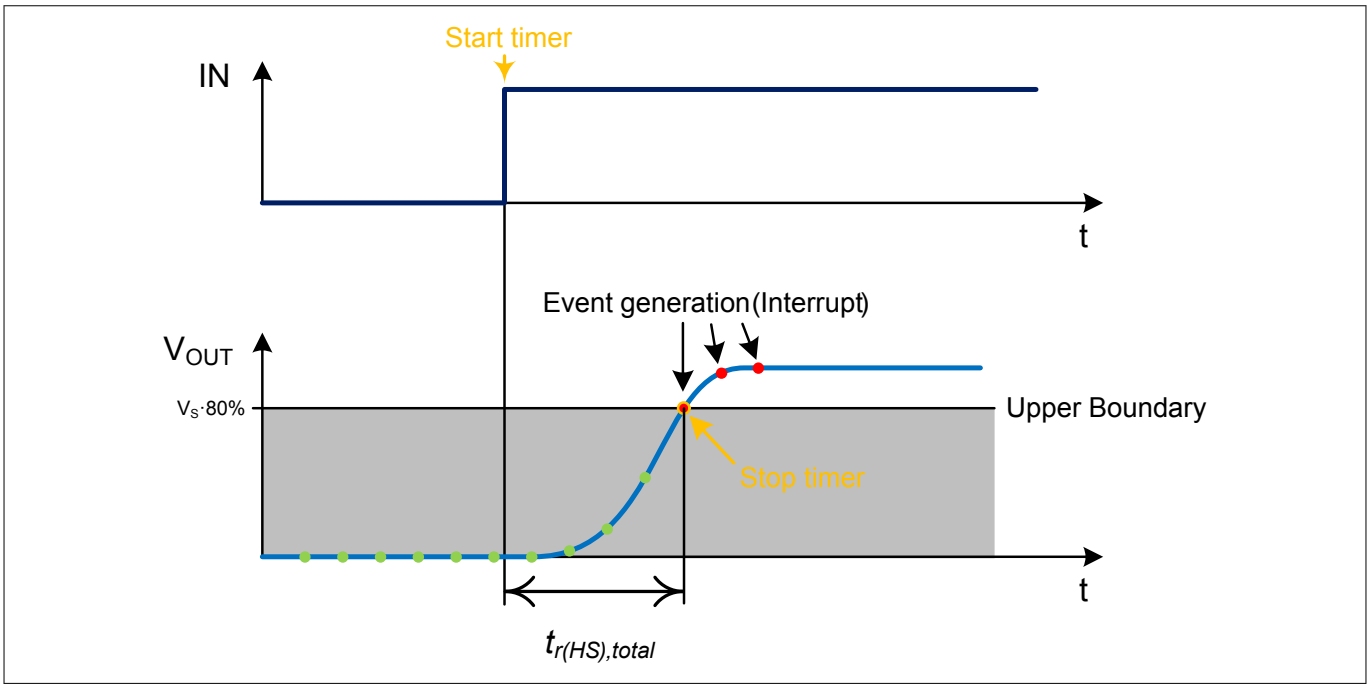

Figure 46 Measurement procedure for the total rising time $t_{r(HS),total}$ based on two voltage measurements

5.4 ADC Timing for current measurement

One way to measure the current value for motor control applications is in the center of the PWM duty cycle. The corresponding measuring time frame is summarized in ***Figure 47***. Based on the value of resistor R_{SR}, the time frame is limited by the worst case (min./max.) switching times, $t_{f(HS),total,min}$ and $t_{r(HS),total,max}$. Alternatively, the timing could be based on the delay time calibration/measurement described in the previous ***Chapter 5.3***.

5.4.1 Current sense ADC timing

Based on ***Figure 47***, the time window for an ADC measurement $t_{h(HS),meas}$ for a high output signal can be calculated as follows:

$$t_{h(HS),\,meas} = T_{ON} + t_{f(HS),\,total,\,min} - t_{r(HS),\,total,\,max}$$

Equation 24

As previously described, the on-time T_{ON} is based on the following relationship:

$$T_{ON} = T_{PWM} \cdot DC$$

Equation 25

T_{PWM} is the PWM-period-time ($T_{PWM} = 1 / f_{PWM}$) and DC corresponds to the duty cycle. This results in:

$$t_{h(HS),\,meas} = T_{PWM} \cdot DC + t_{f(HS),\,total,\,min} - t_{r(HS),\,total,\,max}$$

Equation 26

If the measurement should be started in the center of the ADC time window $t_{h(HS),meas}$, the sample delay t_{sample} has to be set to the following:

$$t_{sample} = t_{r(HS),total,max} + \frac{t_{h(HS),meas}}{2}$$

Equation 27

If the ADC measurement time window should be placed right in the center of $t_{h(HS),meas}$ for a given ADC conversion time t_{ADC}, the sample delay time t_{sample} can be calculated as follows:

$$t_{sample} = t_{r(HS),total,max} + \frac{t_{h(HS),meas} - t_{ADC}}{2}$$

Equation 28

This measurement scenario is illustrated in ***Figure 47***.

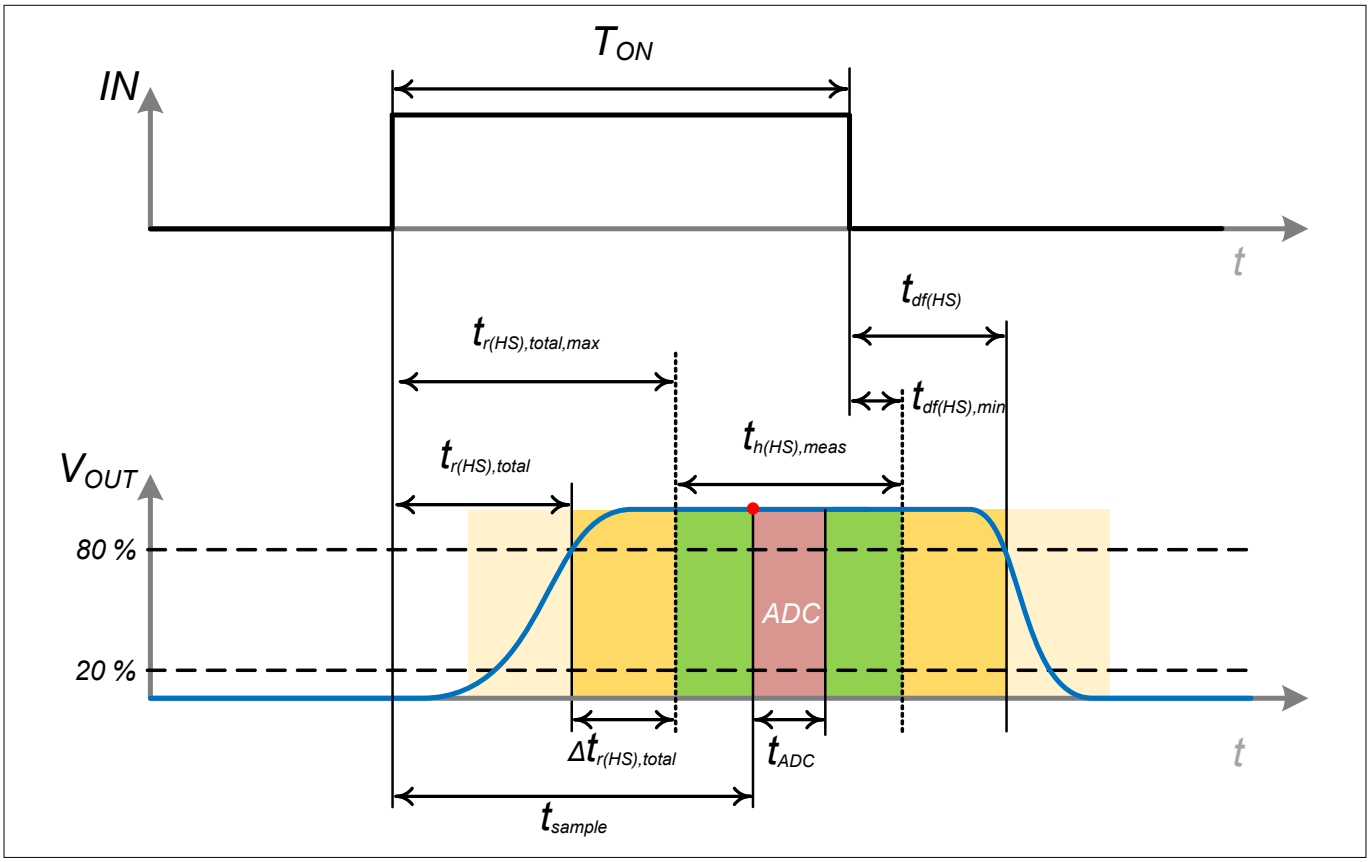

Figure 47 Timing for current measurement for high input on IN-pin, with ideal ADC sampling time window

5.4.2 Offset current calibration ADC timing

With an additional ADC measurement at low input signals, an online compensation of the IS-pin's offset current $I_{IS(offset)}$ can be executed. Based on ***Figure 48*** and comparable to the current measurement in the previous ***Chapter 5.4.1***, the different sampling timings for a low input level can be calculated in a similar fashion. The time window of the ADC measurement $t_{f(HS),meas}$ for a low output signal can be calculated as follows:

$$t_{f(HS),meas} = T_{PWM} \cdot (1 - DC) + t_{dr(HS),min} - t_{f(HS),total,max}$$

Equation 29

If the ADC measurement should be triggered right in the center of the time window $t_{h(HS),meas}$, the required sample delay t'_{sample} can be calculated according to ***Figure 48***:

$$t'_{sample} = t_{f(HS),total,max} + \frac{t_{f(HS),meas}}{2}$$

Equation 30

The resulting trigger point with the sample delay time t'_{sample} is marked in ***Figure 48*** (red).

If the ADC sampling window should be placed in the center of $t_{h(HS),meas}$, the sample delay time t'_{sample} should be set to:

$$t'_{sample} = t_{f(HS),total,max} + \frac{t_{f(HS),meas} - t_{ADC}}{2}$$

Equation 31

In the case of a fault condition, the IS-pin will provide a constant current of $I_{IS(lim)}$, instead of the current sense functionality. This current $I_{IS(lim)}$ can be clearly distinguished from the lower offset current $I_{IS(offset)}$.

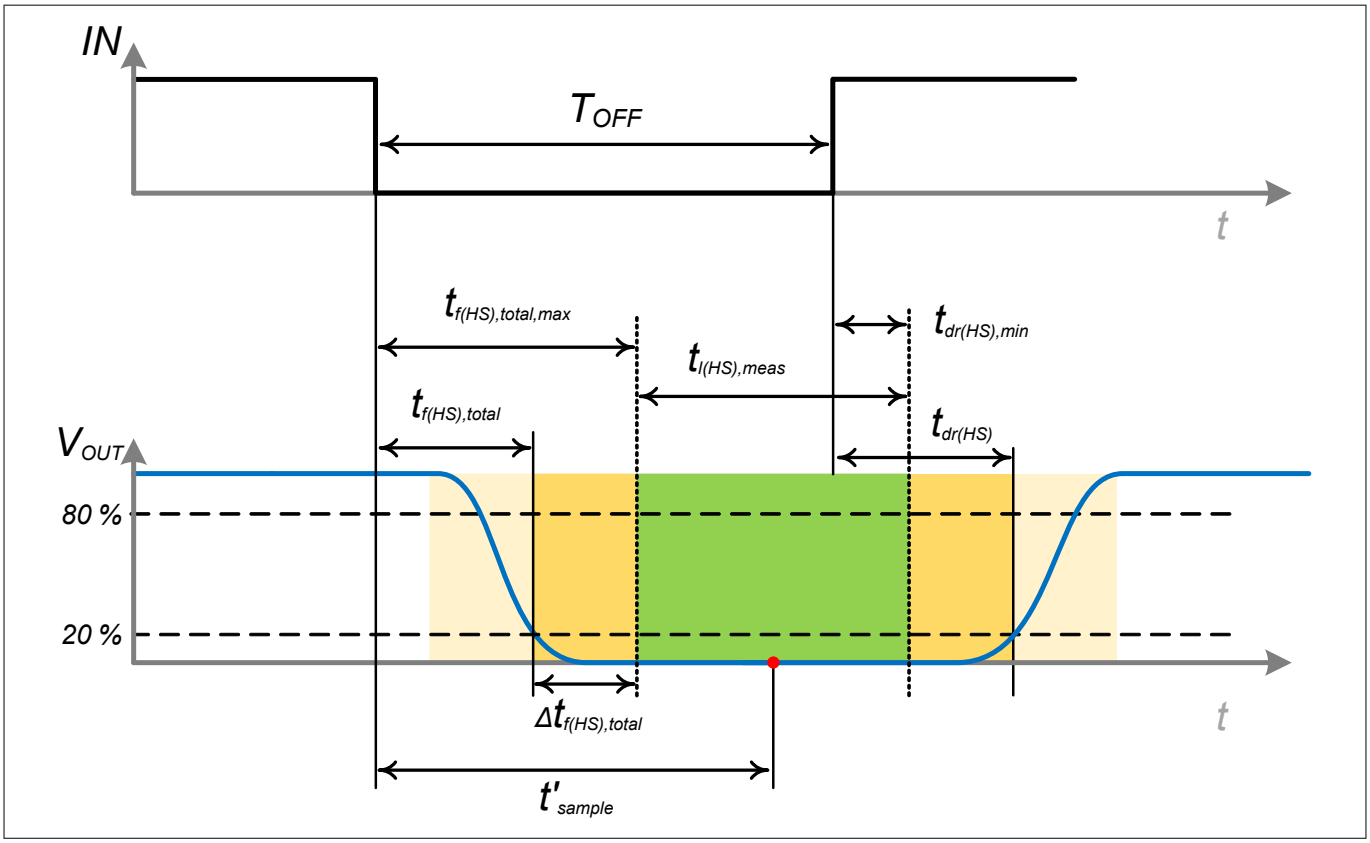

Figure 48 Timing for current measurement for low input on IN-pin

5.5 Allowed PWM setup for current sense ADC measurements

Based on the previous ***Chapter 5.4***, a relationship between the lowest possible duty cycle DC_{min}, corresponding to the minimal time $T_{ON,min}$, and the PWM frequency can be set up. The worst case (max.) ADC conversion time window is $t_{ADC,max}$. For a worst case analysis, the following assumption must be respected in any case, as the time window for the ADC measurement $t_{h(HS),meas}$, according to ***Equation 26***, has to be greater than $t_{ADC,max}$:

$$t_{ADC,\,max} \leq T_{PWM} \cdot DC + t_{df(HS),\,min} - t_{r(HS),\,total,\,max}$$

Equation 32

For certain typical values for resistor R_{SR} (1 kΩ, 5 kΩ and 10 kΩ) and certain maximal ADC conversion times $t_{ADC,max}$, the minimal duty cycles should be respected, as shown in ***Figure 49*** for R_{SR} = 1 kΩ, ***Figure 50*** for R_{SR} = 5 kΩ and ***Figure 51*** for R_{SR} = 10 kΩ.

5.5.1 Addressable min. duty cycle

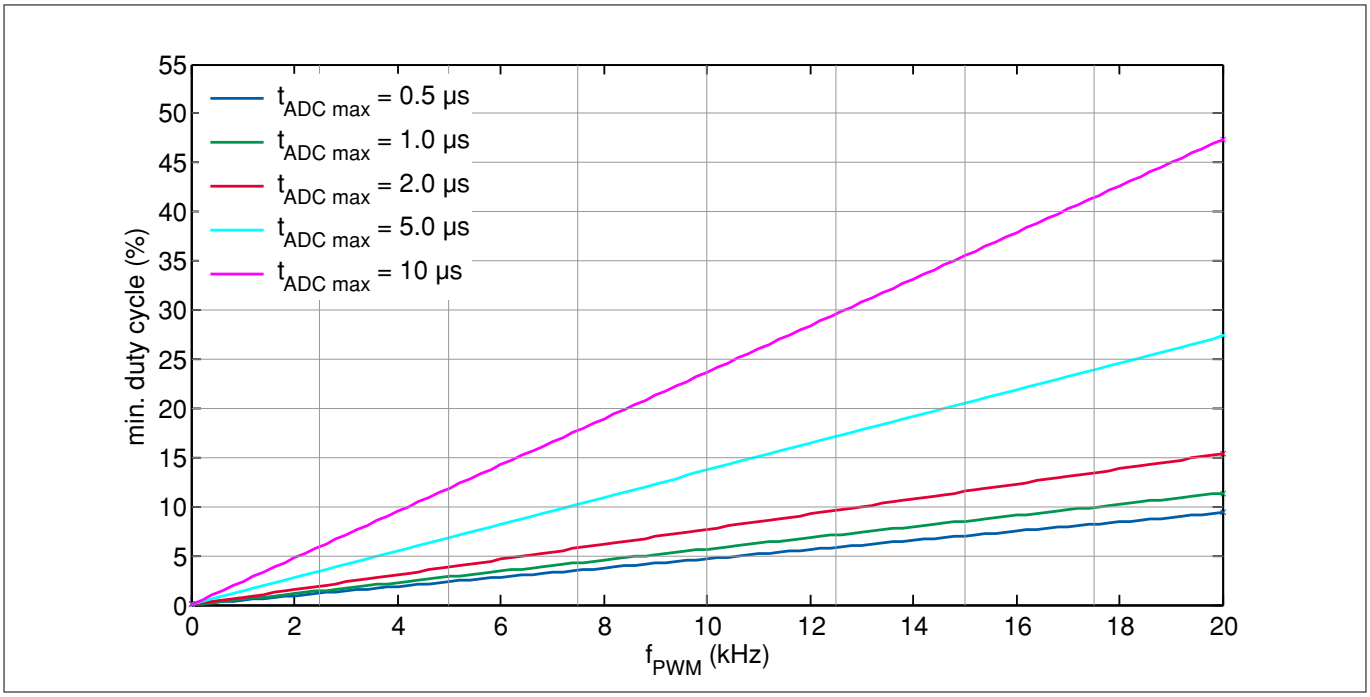

Figure 49 Minimal allowed duty cycle DC_{min} for a given PWM frequency f_{PWM}, a ADC conversion time t_{ADC} and R_{SR} = 1 kΩ, for IFX007T

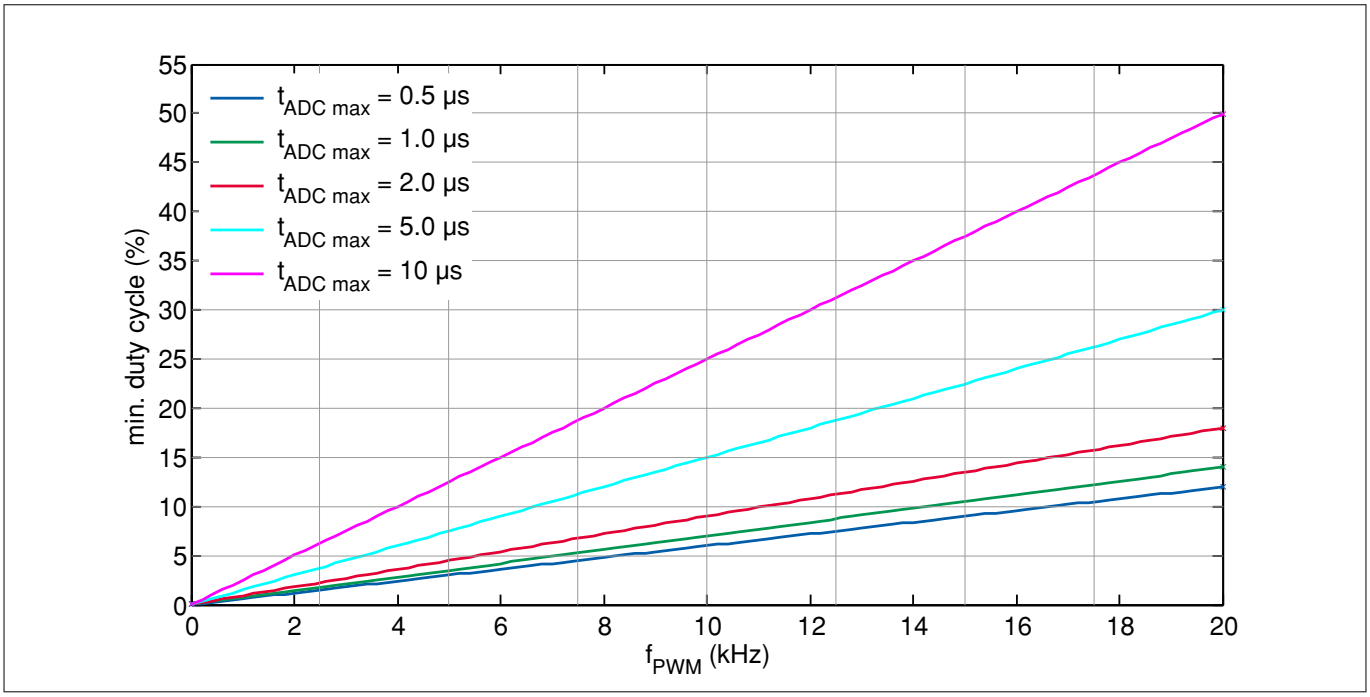

Figure 50 Minimal allowed duty cycle DC_{min} for a given PWM frequency f_{PWM}, a ADC conversion time t_{ADC} and R_{SR} = 5 kΩ, for IFX007T

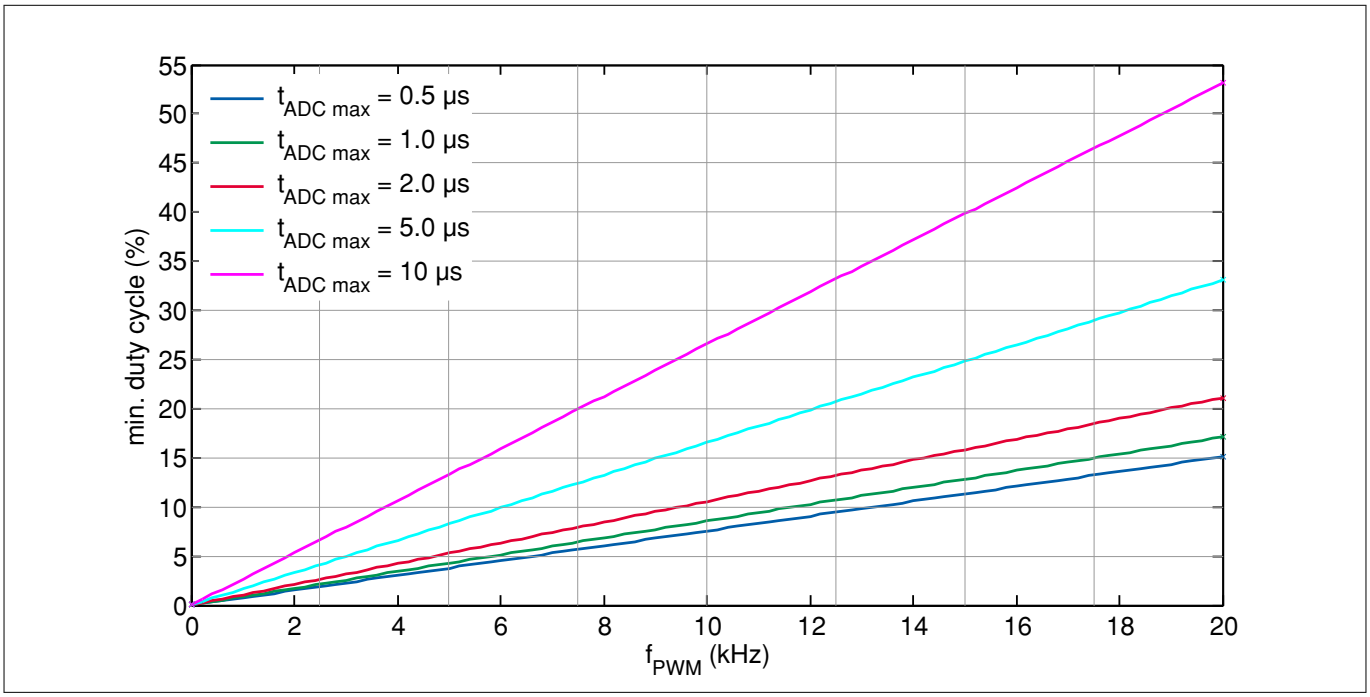

Figure 51 Minimal allowed duty cycle DC_{min} for a given PWM frequency f_{PWM}, a ADC conversion time t_{ADC} and R_{SR} = 10 kΩ, for IFX007T

5.5.2 Example calculation

For an example application, the following parameter values are assumed:

- PWM frequency f_{PWM}= 20 kHz, resulting in T_{PWM}= 1 / f_{PWM} = 50µs
- DC_{min}= 25%

Switching Timing

- R_{SR} = 1 kΩ resulting in $t_{df(HS),min}$ = 1.811 µs (see ***Figure 36***) and $t_{r(HS),total,max}$ = 5.494 µs (see ***Figure 32***)

This setup results in the max. ADC conversion time window $t_{ADC,max}$:

$$t_{ADC,\,max} = T_{PWM} \cdot DC + t_{df(HS),\,min} - t_{r(HS),\,total,\,max}$$

Equation 33

$$t_{ADC,\,max} = 50\mu s \cdot 0.25 + 1.811\mu s - 5.494\mu s \approx 8.8\mu s$$

Equation 34

5.6 Output duty cycle relationships

The output duty cycle do not have an exact linear relationship with the input duty cycle. The different PWM IN to OUT transfer functions depend on the PWM frequency and the device specific timings. Rising time, falling time and switch on/off delay times have to be taken into account for calculating the output duty cycle as shown in ***Figure 52***. The output duty cycle is mainly influenced by the switch on/off delay times. Especially for low input PWM frequency , the rising/falling times have only minor impact on DC_{OUT}.

As shown in ***Equation 35***, the $T_{ON(OUT)}$ is mainly influenced by switch on delay time, rising time and switch off time:

$$T_{ON(OUT)} = DC_{OUT} \cdot T = DC_{IN} \cdot T + t_{df(HS)} - t_{r(HS)} - t_{dr(HS)}$$

Equation 35

The output duty cycle can be derived from the formula above:

$$DC_{OUT} = \frac{T_{ON(OUT)}}{T} = DC_{IN} + f \cdot \left(t_{df(HS)} - t_{r(HS)} - t_{dr(HS)}\right)$$

Equation 36

Since DC_{OUT} is mainly influenced by switch on/off delay times, the output duty cycle equation can be simplified as:

$$DC_{OUT} = \frac{T_{ON(OUT)}}{T} \approx DC_{IN} + f \cdot \left(t_{df(HS)} - t_{dr(HS)}\right)$$

Equation 37

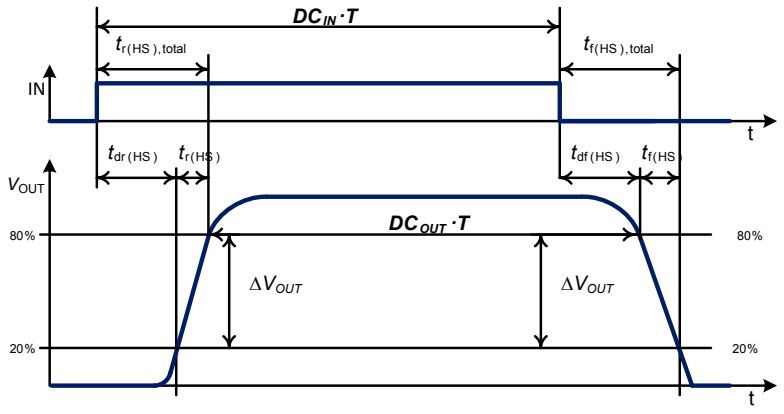

Figure 52 Definition of duty cycle for load to GND

Since the switching on/off times are adjustable by varying the slew rate resistor, the output duty cycle spread is mainly caused by the different R_{SR} values. The output duty cycle spread of IFX007T at a PWM frequency of 20 kHz is shown in ***Figure 53***. The curves are fitted to the discrete measurement data of (DC_{IN}, DC_{OUT}) points.

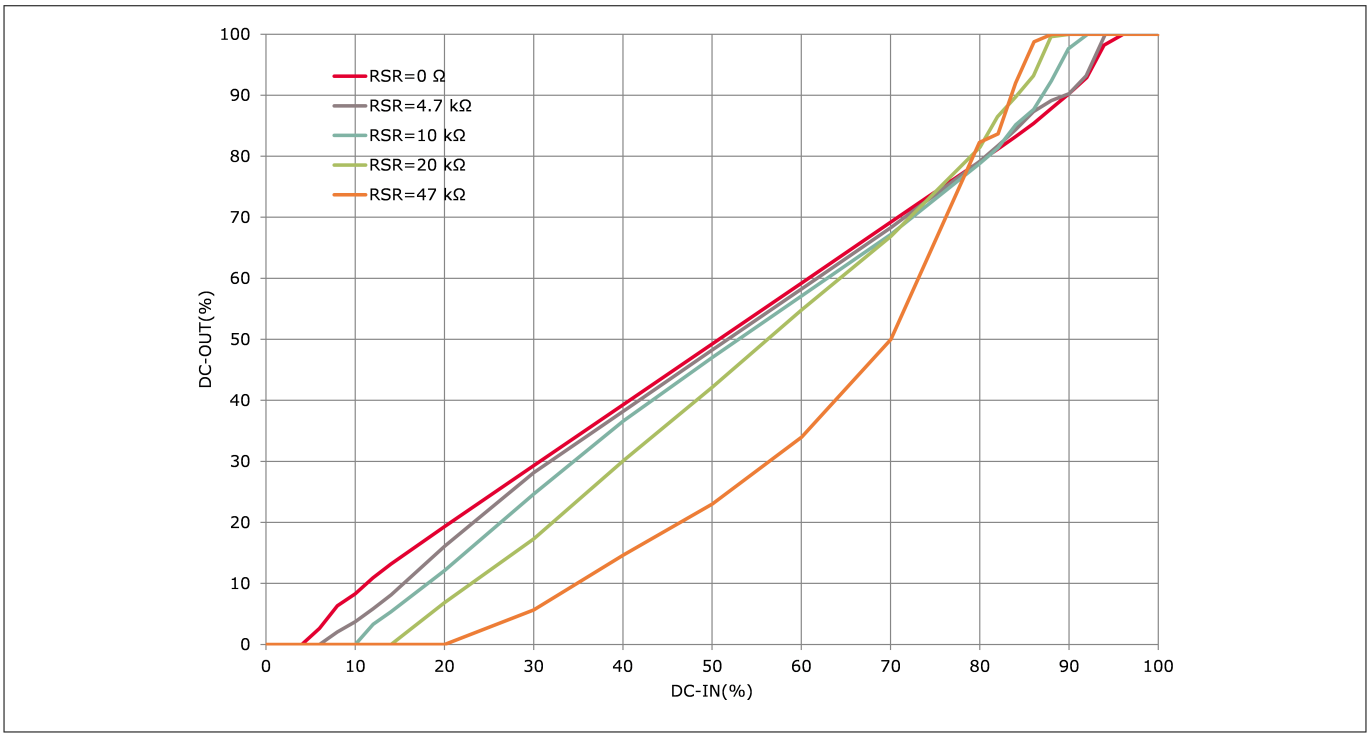

Figure 53 PWM IN to OUT, R_{LOAD} = 2 Ω, I_{LOAD} = 37 µH, PWM = 20 kHz, for IFX007T

5.6.1 Output duty cycle improvement methods

For high end applications, output duty cycle improvement methods are highly recommended to improve the precision of the DC_{OUT}. It can be implemented in two different improvement methods: by performing end of the line calibration or an output duty cycle control loop.

- End of the line calibration: This method requires the measurement of some typical and predefined testing points(several DC_{IN}) for each device. The set of the measurement data or a parameter set can be stored in a microctroller. Based on the data set, a proper input duty cycle could be selected by using curve fitting or interpolation to generate an expected output duty cycle.
- Output duty cycle control loop: It is a real time operation. Instead of measuring the predefined test points once, the output duty cycle is measured by the microcontroller during the operation continuously as shown in ***Figure 54***. The input duty cycle then is adapted accordingly by a control algorithm(e.g. PID-controller), to equal the value of a desired output duty cycle set-point. This real time calibration method also allows compensating of temperature or supply voltage dependencies during operation, thus a higher accuracy can be achieved compared to the end of the line calibration.

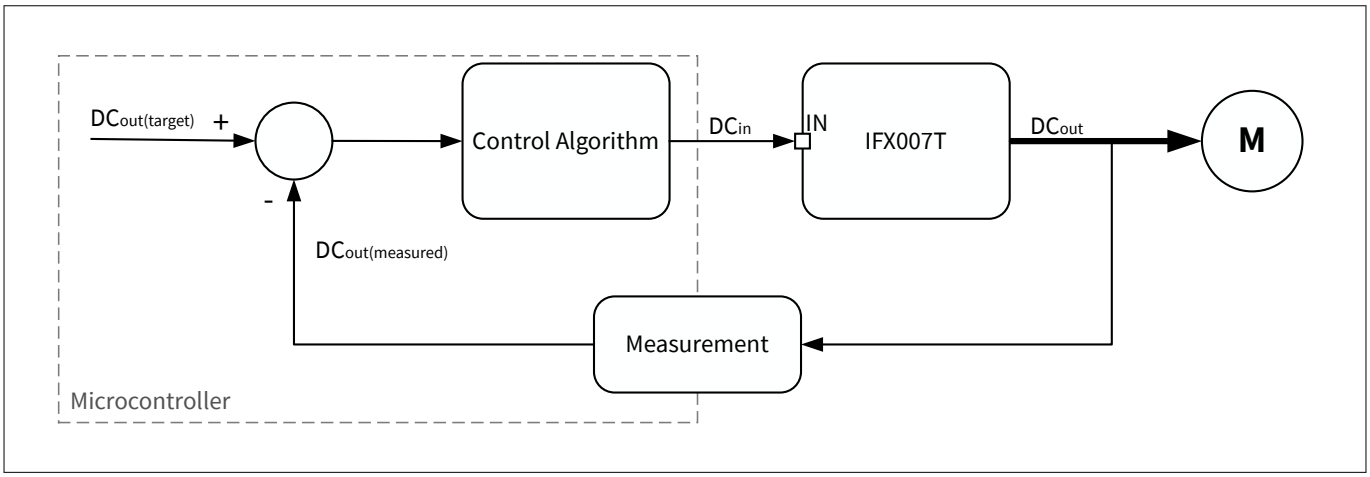

Figure 54 Output duty cycle control loop

6 Power Dissipation

The device dissipates some power. This power dissipation is generated in the top chip and in the individual MOSFETs. The high currents in the MOSFETs generate most of the power dissipation. The following consideration is based on several assumptions, so the result is ultimately an estimation which should help you understand the general trend.

The power dissipation in the MOSFETs consists mainly of conducted losses and switching losses. Losses in the body diode only occur during the cross current protection phase. They are therefore not taken into consideration.

6.1 Power dissipation of the control chip (top chip)

The control chip consumes a certain amount of current, and this causes power dissipation.

In DC-mode the following equation describes the power dissipation in the control chip:

$$P_{CC-DC} = \left(I_{Vs(ON)} + I_{IS}\right) \cdot V_S$$

Equation 38

In PWM-mode, an additional current is needed to charge/discharge the MOSFET gates. This leads to the following PWM power dissipation:

$$P_{CC-PWM} = Q_{tot} \cdot V_S \cdot f_{PWM}$$

Equation 39

Power dissipation in the control chip can be calculated as follows:

$$P_{CC} = P_{CC-DC} + P_{CC-PWM} = \left(I_{Vs(ON)} + I_{IS}\right) \cdot V_S + Q_{tot} \cdot V_S \cdot f_{PWM}$$

Equation 40

6.2 Conduction power dissipation

In the ON-state, a MOSFET has a specific R_{ON} which is listed in the data sheet. R_{ON} is different for the high-side (HS) and the low-side (LS) MOSFETs. This means that R_{ON} must be selected according to the driving situation. A current flowing through this transistor generates the following conducted losses:

$$P_{CL} = I^2 \cdot R_{ON}$$

Equation 41

In case the NovalithIC™ is driven in a static condition, ***Equation 41*** can be used to estimate the static conducted losses for the high-side or low-side MOSFET.

6.3 Power dissipation due to switching

With PWM control, switching losses need to be taken into account because they generate most of the power dissipation for high PWM frequencies. The NovalithIC™ devices are designed to drive motors or other inductive loads. This chapter deals with switching losses that are generated while driving an inductive load.

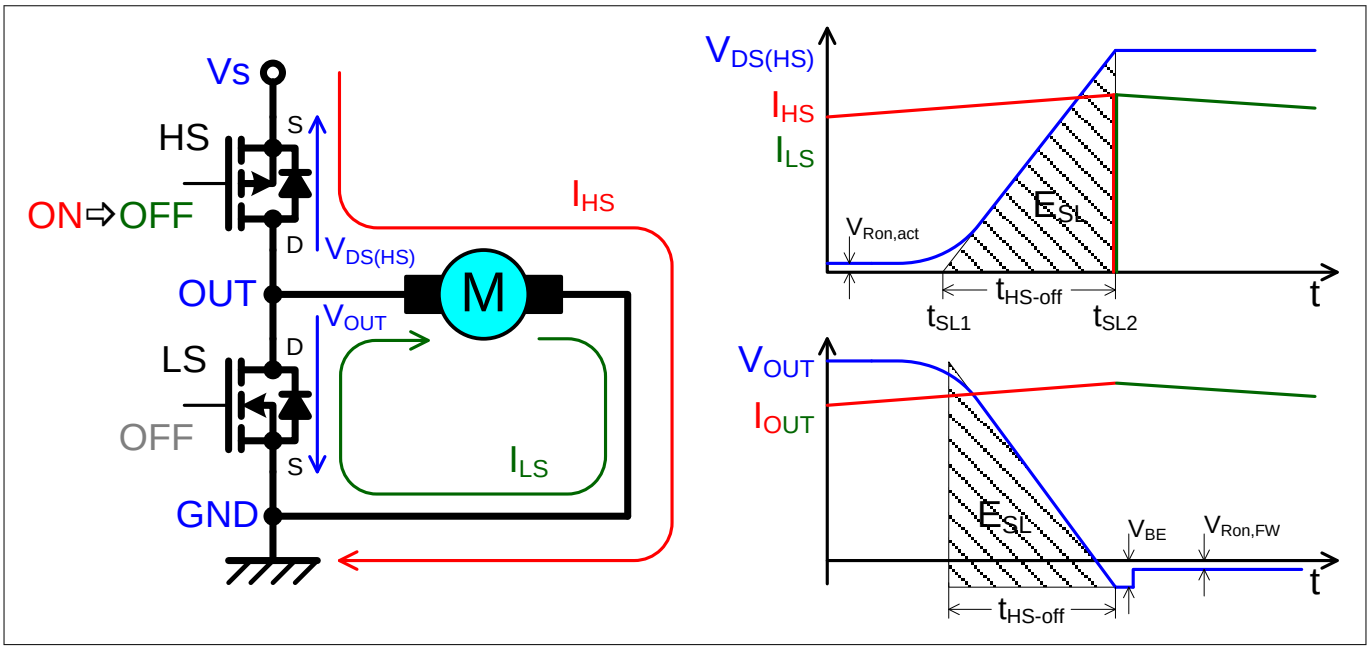

Figure 55 High-side switching scenario of IFX007T

The current in an inductor cannot be changed abruptly (rule of Lenz). As shown in ***Figure 55***, the current in the high-side (HS) MOSFET is driven by the motor inductance as long as the OUT voltage drops one V_{BE} below GND and the current is flowing through the body diode of the low-side (LS) MOSFET. This means that the current I_{HS} is flowing in the high-side (HS) MOSFET, even though this is in linear mode during $t_{HS\text{-}off}$.

The NovalithIC™ has a cross-current protection mechanism which ensures that an output MOSFET is turned on only when the other one is off. This causes a free wheeling current through the MOSFET body diode (V_{BE} in ***Figure 55***) before the resistive path is switched on. The power dissipation caused by the body diode is negligible and thus not taken into account in this estimation.

The rise- and fall- time in the data sheet is the period during which the output voltage decreases from 80% to 20%. In order to determine the switching losses, we need to determine the time required to decrease the output voltage from 100% to 0%. The $t_{HS\text{-}off}$ can be estimated from the data sheet parameters with the ***Equation 42*** accordingly.

$$t_{HS-off} = \frac{t_{f(HS)}}{0.5}$$

Factor 0.5 is related to ΔV_{OUT} from 0 % to 100 %

Equation 42

For the other switching times ($t_{HS\text{-}on}$, $t_{LS\text{-}off}$ and $t_{LS\text{-}on}$) ***Equation 42*** can be used to perform the same calculation using the corresponding data sheet parameters ($t_{r(HS)}$, $t_{f(LS)}$ and $t_{r(LS)}$).

Other assumptions, with a minor effect on the result, include the following:

- The load current during the switching process is constant.
- V_{OUT} and $V_{DS(HS)}$ have linear behavior.
- The switching times are assumed as equal and in the following always referred to as $t_{HS\text{-}off}$.

The switching energy E_{SL} is shown in ***Figure 55*** and can be estimated using ***Equation 43*** below:

$$E_{SL} = \int_{t_{SL1}}^{t_{SL2}} V_S \cdot I_{OUT}\,dt = \frac{V_S \cdot I_{OUT}}{2} \cdot t_{HS-off}$$

Equation 43

From the switching energy E_{SL} the average power loss P_{SL} can be determined with two switching times per PWM period. This is shown in ***Equation 44***:

$$\overline{P_{SL}} = \frac{V_S \cdot I_{OUT}}{2} \cdot 2 \cdot t_{HS-off} \cdot f_{PWM} = V_S \cdot I_{OUT} \cdot t_{HS-off} \cdot f_{PWM}$$

Equation 44

6.4 Entire power dissipation of the MOSFETs

The average power dissipation in PWM-mode consists of the switching losses plus the conducted losses, as shown in ***Figure 56***. We must take into account that the losses occur in the high-side (HS) and low-side (LS) MOSFET. In the example of ***Figure 55***, where the motor is connected to GND, the switching losses occur in the high-side (HS) MOSFET. The conducted losses occur in the high-side (HS) MOSFET during the ON-phase and in the low-side (LS) MOSFET in the free wheeling phase, as shown in ***Figure 56***.

In PWM-mode, the PWM-period-time is:

$$T_{PWM} = \frac{1}{f_{PWM}}$$

Equation 45

The duty cycle (DC) of the PWM-mode is the relation between the ON-time and the PWM-period-time in percent.

$$DC = \frac{T_{ON}}{T_{PWM}}$$

Equation 46

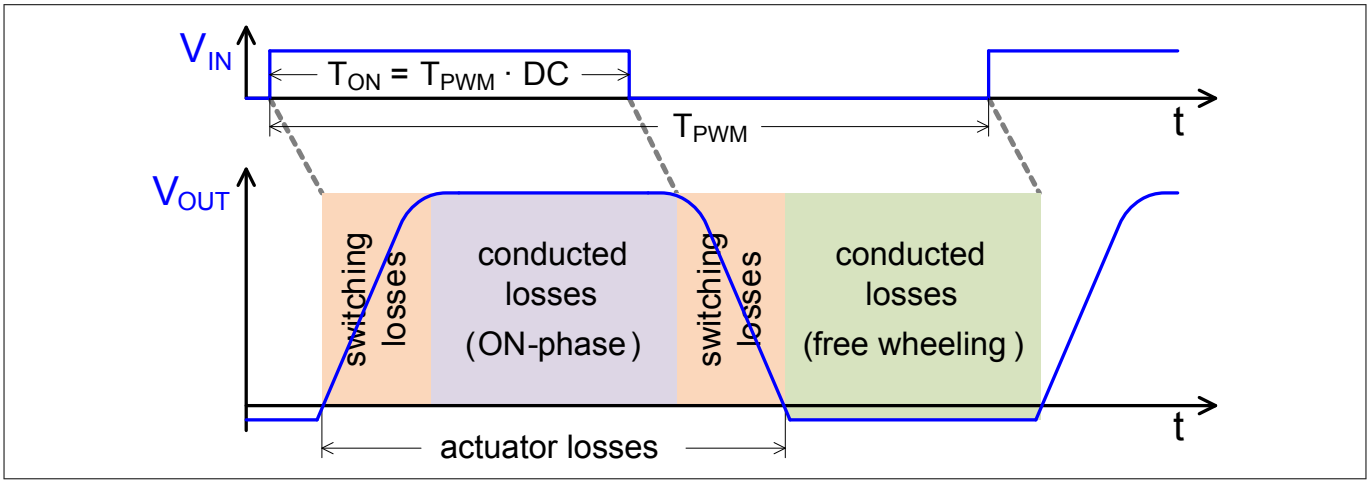

Figure 56 Entire power dissipation of IFX007T with the motor connected to GND

In ***Chapter 6.4.2*** and ***Chapter 6.4.3*** the power dissipation is estimated separately for the high-side (HS) and low-side (LS) MOSFET.

6.4.1 PWM control and the duty cycle constraints

If t_{FW} is close to or below zero, no freewheeling occurs. V_{OUT} does not go below GND. This means that only switching losses are generated. Thus, a duty cycle generating $t_{FW} \leq 0$ is insufficient to control the motor current and therefore not taken into account in the following calculations. In this case, the high-side (HS) MOSFET should be permanently on.

The same is valid for $t_{ON} \leq 0$. In this case, the low-side (LS) MOSFET should be permanently on.
Extremely low or high duty cycle values required by real applications can be achieved by increasing the switching speed and/or by increasing T_{PWM}.

6.4.2 Entire power dissipation in the actuator MOSFET

In the motor-to-GND scenario the actuator MOSFET is the high-side (HS) MOSFET, as in ***Figure 55*** and in motor-to-V_s scenario, the actuator MOSFET is the low-side (LS) MOSFET. The entire power dissipation consists of two times the switching losses plus the conducted losses in the ON-phase, as shown in ***Figure 56***. The time of the ON-phase in PWM-mode is provided by the following equation:

$$t_{ON} = T_{ON} - t_{HS-on}$$

Equation 47

As mentioned in ***Other assumptions*** on page 58 switching times are assumed as equal and named as $t_{HS\text{-}off}$:

$$t_{ON} = T_{ON} - t_{HS-off}$$

Equation 48

Equation for estimate the total conducted energy in the actuator MOSFET:

$$E_{act} = 2 \cdot E_{SL} + E_{ON} = V_S \cdot I_{OUT} \cdot t_{HS-off} + I_{OUT}^2 \cdot R_{ON,act} \cdot t_{ON}$$

Equation 49

From ***Equation 49*** the average power dissipation in the actuator MOSFET can be determined by multiplying ***Equation 49*** by f_{PWM}:

$$\overline{P_{act}} = E_{act} \cdot f_{PWM} = \left(V_S \cdot I_{OUT} \cdot t_{HS-off} + I_{OUT}^2 \cdot R_{ON,act} \cdot t_{ON}\right) \cdot f_{PWM}$$

Equation 50

Equation 50 is an estimation of the average power dissipation in the actuator MOSFET. In ***Figure 55***, this is the high-side (HS) MOSFET.

6.4.3 Entire power dissipation in the freewheeling MOSFET

In the motor-to-GND scenario, the freewheeling MOSFET is the low-side (LS) MOSFET, as in ***Figure 55***, and in the motor-to-V_s scenario, the freewheeling MOSFET is the high-side (HS) MOSFET. The entire power dissipation consists of the conducted losses in the freewheeling phase, as shown in ***Figure 56***. The duration of the freewheeling phase in PWM-mode is provided by the equation below:

$$t_{FW} = T_{PWM} - T_{ON} - t_{HS-off}$$

Equation 51

*Note: For the proper use of **Equation 51** refer to **Chapter 6.4.1**.*

Equation to determine the entire freewheeling energy in the freewheeling MOSFET:

$$E_{FW} = I_{OUT}^2 \cdot R_{ON,FW} \cdot t_{FW} = I_{OUT}^2 \cdot R_{ON,FW} \cdot (T_{PWM} - T_{ON} - t_{HS-off})$$

Equation 52

From ***Equation 52*** the average power dissipation in the freewheeling MOSFET can be determined by multiplying ***Equation 52*** by f_{PWM}:

$$\overline{P_{FW}} = E_{FW} \cdot f_{PWM} = I_{OUT}^2 \cdot R_{ON,FW} \cdot (T_{PWM} - T_{ON} - t_{HS-off}) \cdot f_{PWM}$$

Equation 53

Equation 53 is an estimation of the average power dissipation in the freewheeling MOSFET. In ***Figure 55***, this is the low-side (LS) MOSFET.

6.5 Entire power dissipation in the NovalithIC™

To determine the entire power dissipation in the NovalithIC™, combine ***Equation 50***, ***Equation 53*** and ***Equation 40***.

$$\overline{P_{Nova}} = \overline{P_{act}} + \overline{P_{FW}} + P_{CC}$$

Equation 54

Equation 54 is the average of the different power losses in one PWM period, as shown in ***Figure 56***, plus the power losses in the control chip.

6.6 Simplifications

Because the losses in the control chip are typically negligible in comparison with the losses in the MOSFETs, they are neglected in this simplification.

Taking into account that the high-side (HS) and the low-side (LS) MOSFET are in a similar R_{ON} range, the equation for determining the entire power dissipation in the NovalithIC™ can be significantly reduced by using the same R_{ON} for both the high-side (HS) and the low-side (LS) MOSFET. The more conservative approach is to use the higher R_{ON} of both.

The idea behind this is to have the same R_{ON} for the conducted losses of the ON- and the freewheeling phase, according to ***Figure 56***. Due to this simplification the energy in one PWM- period is two times the switching losses E_{SL} and R_{ON} losses during the remaining time:

$$E_{Nova} = 2 \cdot E_{SL} + P_{CL} \cdot (T_{PWM} - 2 \cdot t_{HS-off})$$

Equation 55

$$E_{Nova} = 2 \cdot \frac{V_s \cdot I_{OUT}}{2} \cdot t_{HS-off} + I_{OUT}^2 \cdot R_{ON} \cdot (T_{PWM} - 2 \cdot t_{HS-off})$$

Equation 56

From the simplified NovalithIC™ energy to the simplified NovalithIC™ power dissipation by multiplying ***Equation 56*** by f_{PWM}:

Power Dissipation

$$\overline{P_{\text{Nova},S}} = \left(V_S \cdot I_{\text{OUT}} \cdot t_{\text{HS-off}} + I_{\text{OUT}}^2 \cdot R_{\text{ON}} \cdot \left(T_{\text{PWM}} - 2 \cdot t_{\text{HS-off}}\right)\right) \cdot f_{\text{PWM}}$$

Equation 57

7 Thermal Performance

The PCB used for the simulation is compliant with JEDEC 2s2p (JESD 51-5, JESD 51-7) and JEDEC 1s0p (JESD 51-3), as described in ***Table 6***. For 1s0p, a cooling area of 600 mm² and 300 mm² is additionally considered.

Table 6 PCB specification

Dimensions	76.2 × 114.3 × 1.5 mm³	λ_{therm} [W/m • K]
Material	FR4	0.3
Metallization	JEDEC 2s2p (JESD 51-7) + (JESD 51-5) JEDEC 1s0p (JESD 51-3) + Cooling Area	388
Cooling Area	600 mm², 300 mm², footprint	
Thermal Vias	Ø = 0.3 mm; plating 25 µm; 40 pcs.	
Package Attach [50 µm]	Solder	55

The cross section of JEDEC 2s2p is shown in ***Figure 57***.

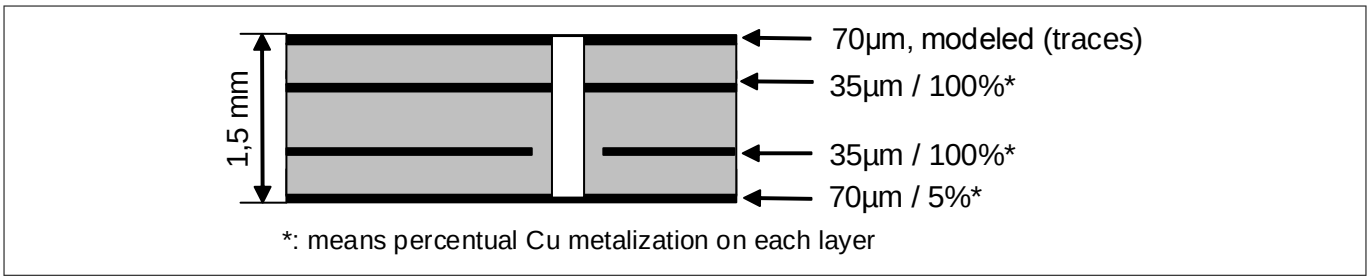

Figure 57 Cross section JEDEC 2s2p

The cross section of JEDEC 1s0p is shown in ***Figure 58***.

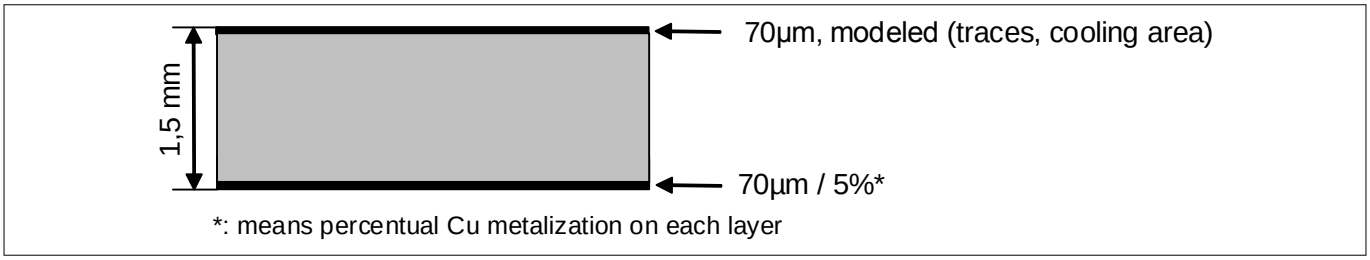

Figure 58 Cross section JEDEC 1s0p

7.1 Zth simulation results

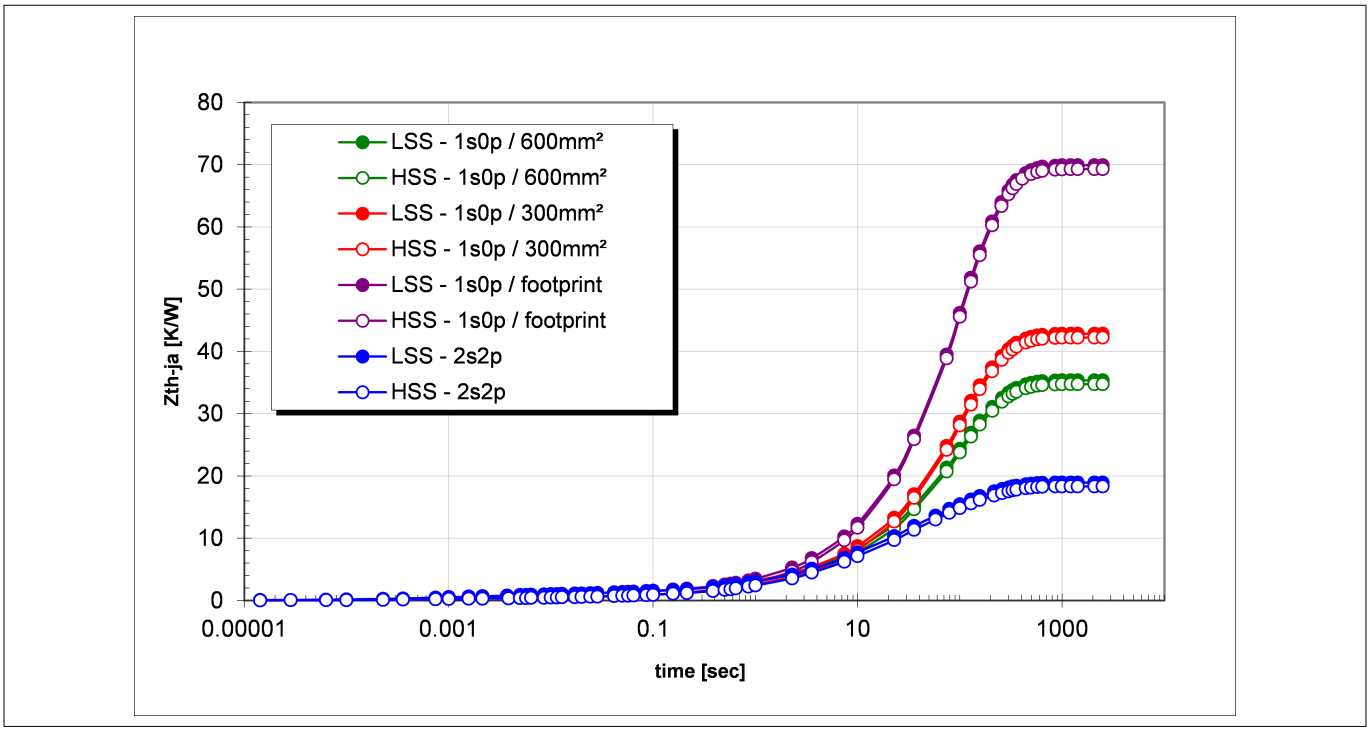

Figure 59 $Z_{th\text{-}ja}$ **for IFX007T, in PG-TO263-7-1, (LSS: low-side switch, HSS: high-side switch)**

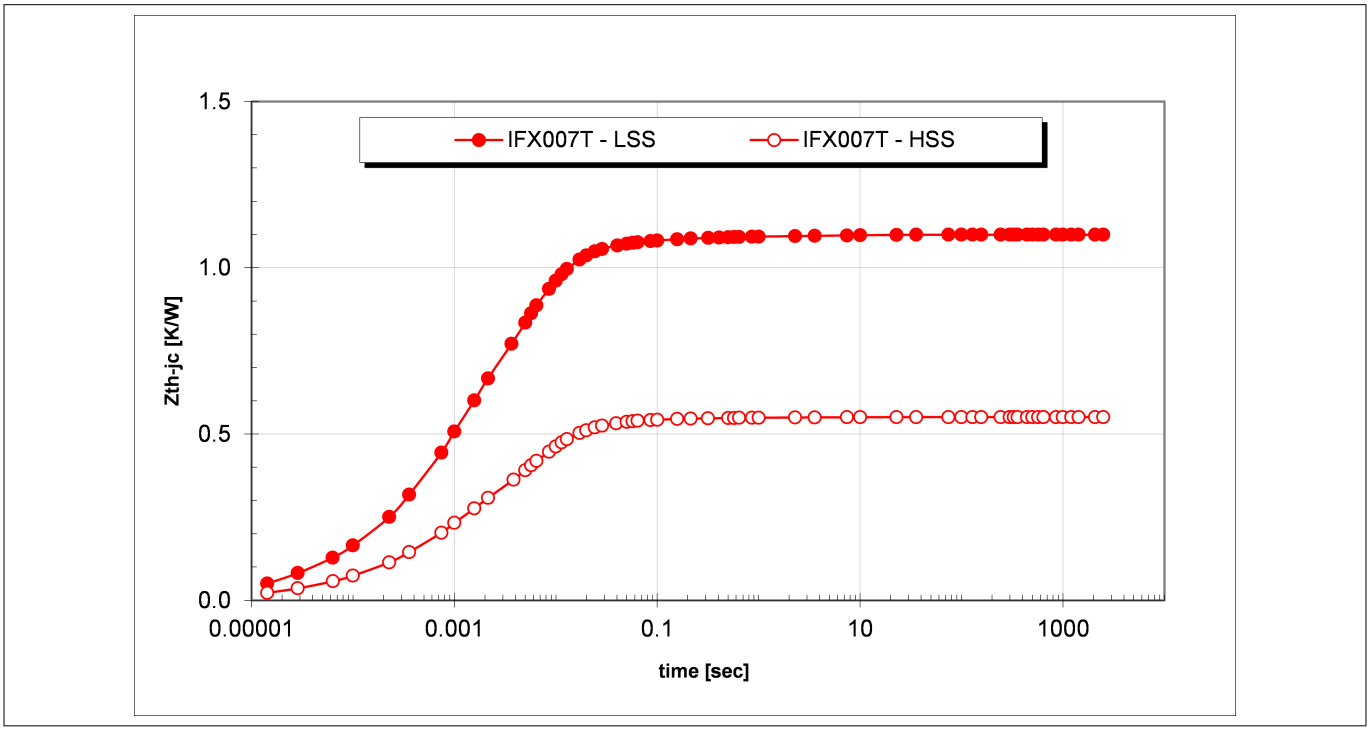

Figure 60 $Z_{th\text{-}jc}$ **for IFX007T, in PG-TO263-7-1, (LSS: low-side switch, HSS: high-side switch)**

7.2 Thermal RC-network

The thermal behavior of the IFX007T can be simulated based on the thermal RC-network shown in ***Figure 61***. The abbreviations can be found in ***Table 7***.

Table 7 Abbreviations for the thermal RC-network of IFX007T

Abbreviation	Description (temperature level)
GND	Thermal ground, corresponds to ambient temperature
CC	Control chip with temperature sensor for overtemperature detection
LS	Low-side MOSFET
HS	High-side MOSFET

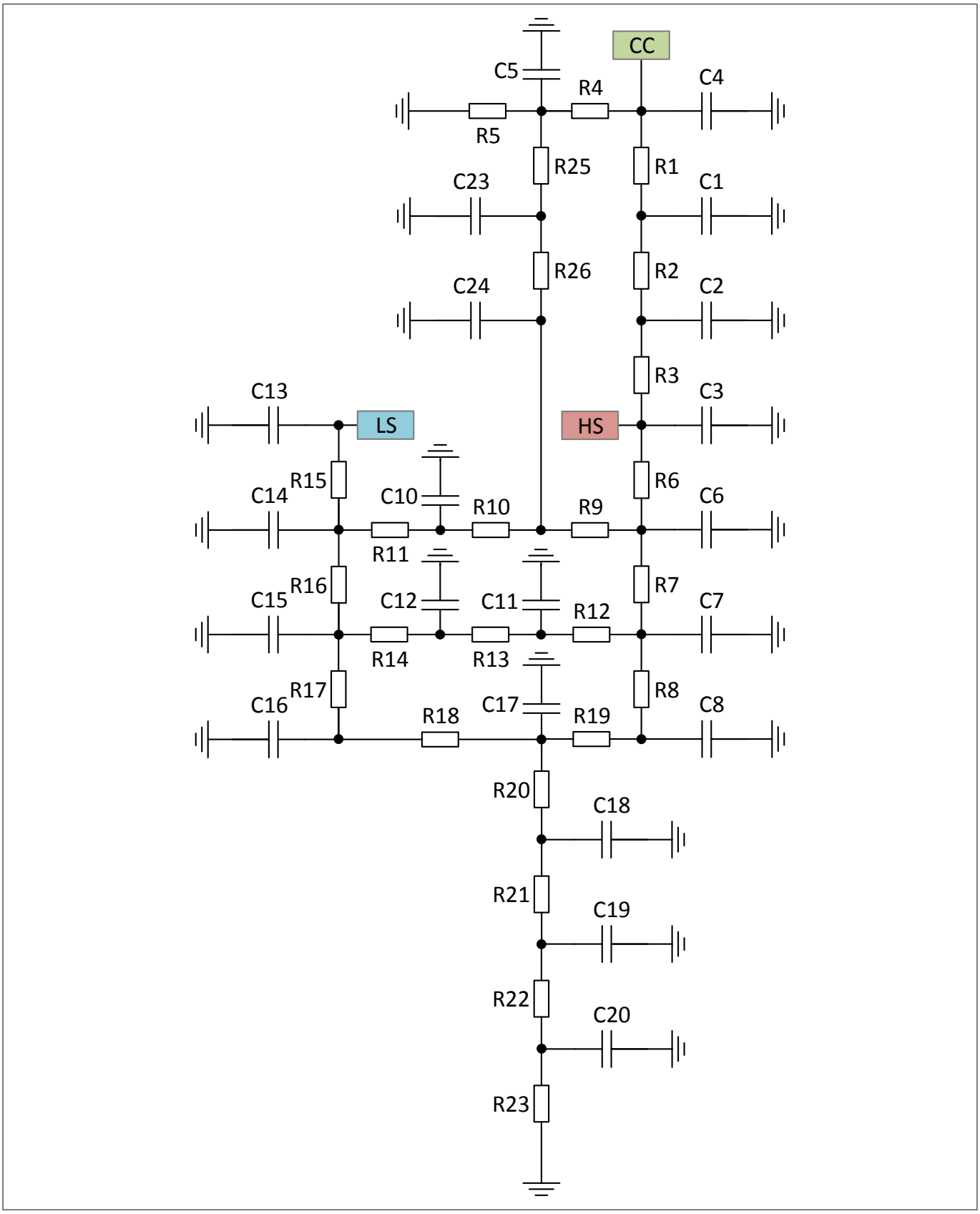

Figure 61 Schematic of the thermal RC-network for IFX007T

7.2.1 Parameters for thermal RC-network

For the thermal RC-network, which is shown in ***Figure 61***, the values of the IFX007T for the resistors can be found in ***Table 8*** and for the capacities in ***Table 9***, depending on the test condition (PCB).

Table 8 Thermal RC-network resistor values for IFX007T

Parameter	1s0p	2s2p	300 mm²	600 mm²
R1	14.7357	14.607	14.5115	14.4932
R2	1.41757	2.99853	0.892556	0.662104
R3	4.68444	2.59111	4.77943	5.04297
R4	417.267	996.831	999.052	962.665
R5	112.975	18.9927	52.4443	41.5135
R6	0.631354	0.586299	0.663352	0.592812
R7	32.786	17.7176	12.9216	10.8754
R8	238.436	60.6471	141.19	133.593
R9	0.010794	0.253683	0.0664578	0.0534714
R10	0.697554	0.0136973	0.843804	0.729177
R11	0.457247	0.800679	0.0121925	0.527079
R12	3.16907	0.309781	0.0990132	0.729318
R13	0.863968	608.83	4.30397	0.308658
R14	122.484	743.102	993.339	108.893
R15	0.922458	0.943908	1.03571	0.725828
R16	63.0068	28.9428	23.0979	13.6581
R17	16.2261	14.9297	20.1678	13.6112
R18	14.9109	0.01	18.7873	15.8732
R19	269.376	711.221	999.114	998.955
R20	31.986	15.9504	33.3671	24.8793
R21	14.5539	11.788	2.37429	2.66703
R22	19.4019	24.147	18.495	13.1898
R23	15.6402	1.70354	20.424	20.3062
R25	0.0102647	0.0180739	0.0147595	0.0992122
R26	5.9597	2.67745	2.46301	2.16571

Table 9 Thermal RC-network capacitor values for IFX007T

Parameter	1s0p	2s2p	300 mm²	600 mm²
C1	0.0109887	0.0122742	0.0117668	0.0114942
C2	4.38961E-06	1.75918E-06	1.13147E-05	0.00010077
C3	0.00361686	0.00382319	0.00452151	0.00335106

Table 9 Thermal RC-network capacitor values for IFX007T (continued)

Parameter	1s0p	2s2p	300 mm²	600 mm²
C4	0.00117385	0.00118004	0.0011766	0.00117587
C5	0.0144137	0.400558	0.186452	0.249974
C6	0.064702	0.0424699	0.0426304	0.0280119
C7	0.124171	0.0566395	0.407592	0.66619
C8	0.0184178	0.840657	0.061641	0.224521
C10	0.127647	0.0215798	0.0135012	0.130117
C11	0.219454	0.965128	0.201947	0.289226
C12	0.0757321	0.0222976	0.280791	0.460985
C13	0.0020413	0.00210601	0.00223527	0.0013234
C14	0.0489809	0.0743878	0.105303	0.018626
C15	0.28671	0.102	0.411468	0.464271
C16	0.00598831	0.0157598	0.00766389	0.00254175
C17	0.000668051	0.171968	0.0555266	0.0541936
C18	0.801461	3.05061	1.75168	0.000842353
C19	0.00214924	4.84858	0.365562	0.0312806
C20	5.63547	6.30449	2.98494	7.0397
C23	0.348292	0.184817	0.3862	0.261893
C24	0.0995441	0.242926	0.180138	0.116301

Revision History

Revision	Date	Changes
0.1	2018-08-10	Initial release.

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