Infineon® LITIX™ Basic Driver Family

# Infineon® LITIX™ Basic Driver Family

Multichannel Solutions for N-1, Open Load & Short Circuit Detection

## Application Note

V1.1, 2015-March-27

## Automotive Power

**LITIX™ Basic**
**Revision History: 1**
**Previous Version:**

| Page | Subjects (major changes since last revision) |
|---|---|
| V1.0 | Updated text and figures for TLDxxx4 series and initial release |
| V1.1 | New current values calculated with updated $K_{ALL}$ and $K_{LT}$ |
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# 1 Abstract

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*
*Note: All application diagrams shown in this application note are very simplified examples of application circuits. The function must be verified in the real application.*

This application note is intended to provide detailed application hints regarding the usage and design in of the Infineon® LITIX™ Basic Drivers. The LITIX™ Basic family is introduced, the selection of external components is shown and examples are given of typical applications and their diagnostic features.

# 2 Introduction

The Infineon® LITIX™ Basic Drivers is a family of one and three channel current sources. This application note will focus on the TLD family which has a maximum per channel output current of 120 mA for 3 channel devices and 360mA for single channel devices (power dissipation limited). The output current can be adjusted lower as needed for the application. Furthermore, some devices also offer diagnosis features and internal PWM dimming capability. Protection features are included for ESD, undervoltage lockout, overload and overtemperature.

This document describes the basic features, shows how to define the external circuitry, and gives applications examples and explanations. Design recommendations are given as well.

# 3 The LITIX™ Basic Family (TLD devices) – Operation and Features

The Infineon® LITIX™ Basic Drivers have been developed with a family concept. All devices share a common package (SSOP-14 with exposed pad). All devices are pin compatible, making a change from one device to another simple.

Figure 1 shows a matrix of the family members. The main differences are in the number of inputs (1 or 3), outputs (1 or 3) and features. The features will be discussed in detail throughout this application note.

The TLD1124, TLD1314 and TLD2314 contain the diagnostic enable (DEN) pin instead of the enable (EN) pin. These devices have the enable (EN) function internally connected. The TLDxxx4 devices are enabled when the supply voltage is greater than the Power on reset threshold $V_{S(POR)}$.

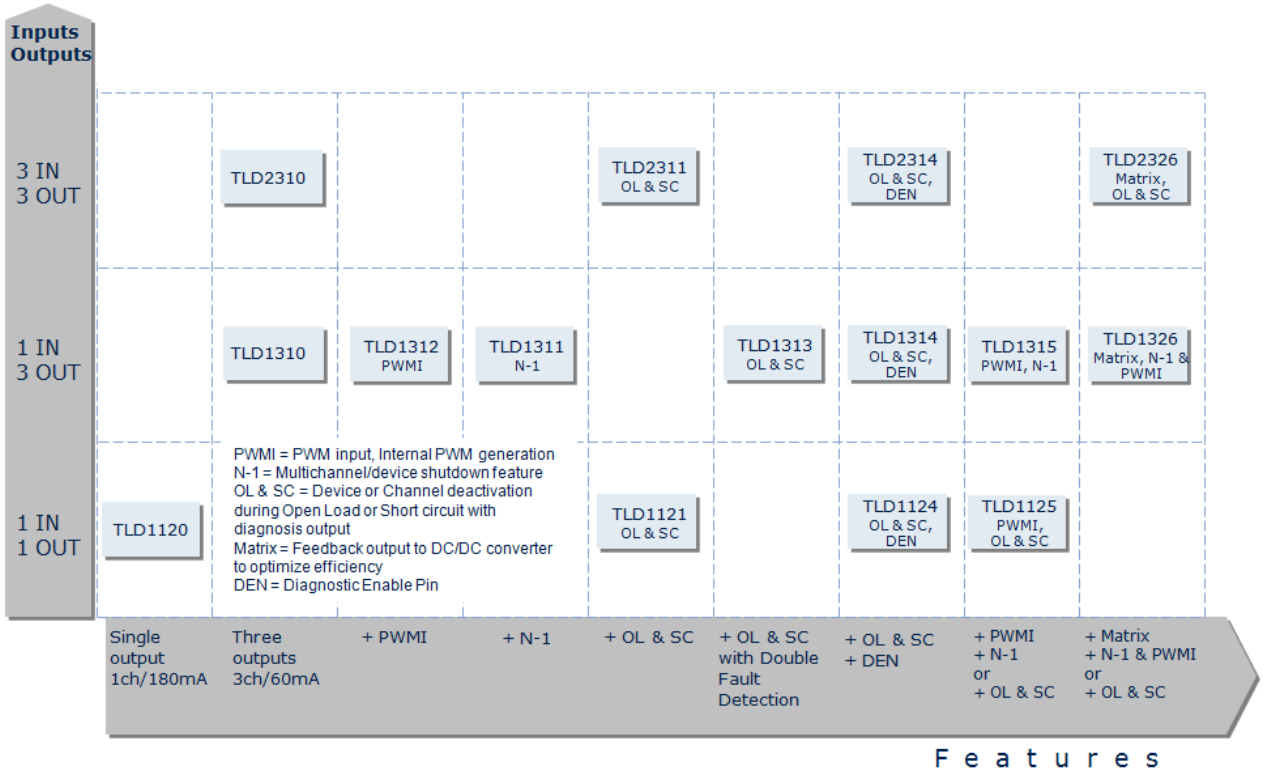



**Figure 1 Family Members of the LITIX™ Basic TLD devices**

## 3.1 Block Diagram and Basic Operation

Figure 2 shows the block diagram of the LITIX™ Basic family member TLD1310EL. This device has 1 input (IN_SET), 3 outputs (OUT1, OUT2 and OUT3), enable input (EN), supply (VS) and ground (GND) pins. The exposed pad of the package should also be connected to ground in the application.

- The output current is set via the IN_SET pins by a low power resistor to ground. For devices with 3 inputs, each output current can be set independently by each input. For devices with 1 input, only one current level can be set which is applied to all channels. The lower the resistor value, the higher the output current (the maximum output current is limited by the specific device and the thermal conditions). The current is set according to the equation $R_{SET} = k_{nom} / I_{OUT}$ , Where $R_{SET}$ is the resistor to ground at each IN_SET pin and $I_{OUT}$ the desired current, the gain factor, $k_{nom}$, is defined in the device datasheet.
- The EN pin can be used as a simple ON/OFF control pin or alternatively as a separate logic supply. The EN pin is active high and will enable the device after a Power on Reset time.
- The VS pin is the main supply pin for the device and the output load current. It is important to connect a decoupling capacitor (100nF to 1uF) near this pin to ground.
- The GND pin(s) is the ground reference for the device.
- OUT1, OUT2 and OUT3 are the high side constant current outputs which are connected to the anode of a LED or LED string (multiple LEDs connected in series).
- The function of the IN_SET pins varies by device. The basic functions are to set the output current level and control the respective outputs by using the IN_SET resistor in series to a switch to ground to turn on the respective output(s). On some devices the IN_SET pin can also function as a diagnostic pin.

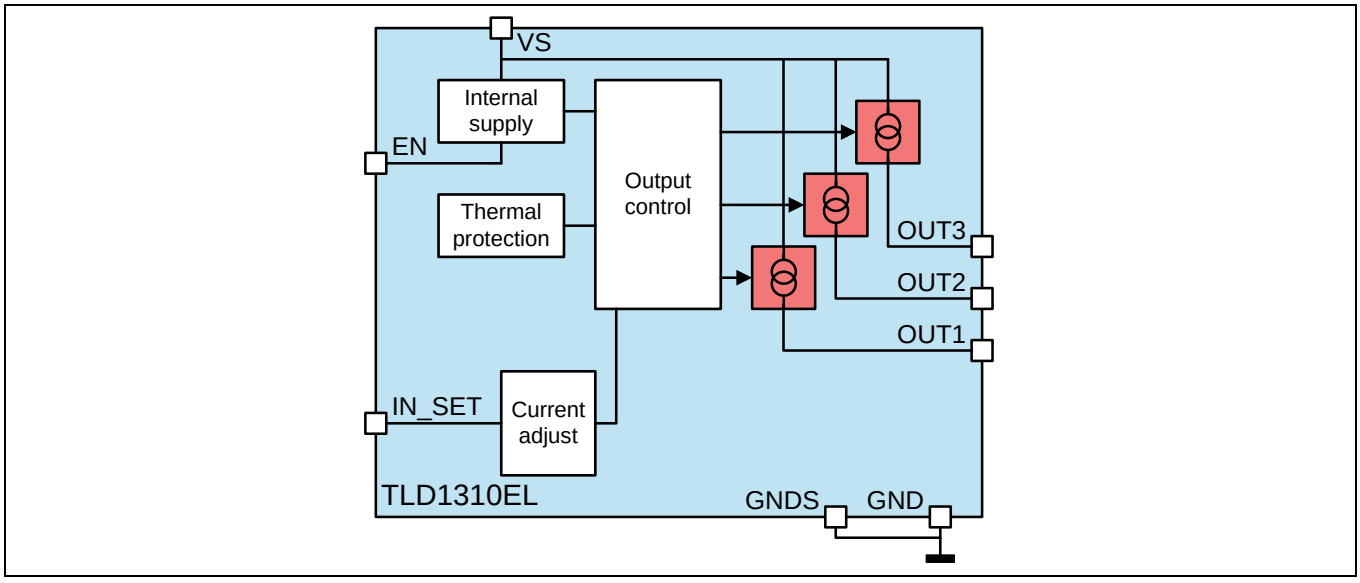



**Figure 2 Block Diagram of LITIX™ Basic device (TLD1310EL)**

Figure 3 shows the block diagram of the LITIX™ Basic family member TLD1314EL. This device has 1 input (IN_SET), 3 outputs (OUT1, OUT2 and OUT3), diagnostic enable input (DEN), status (ST), supply (VS) and ground (GND) pins. The exposed pad of the package should also be connected to ground in the application. The diagnostic enable (DEN) pin can be used to disable the diagnostic indication of the ST pin in cases of low supply voltage or other application conditions where suppression of the ST diagnostic is desired.

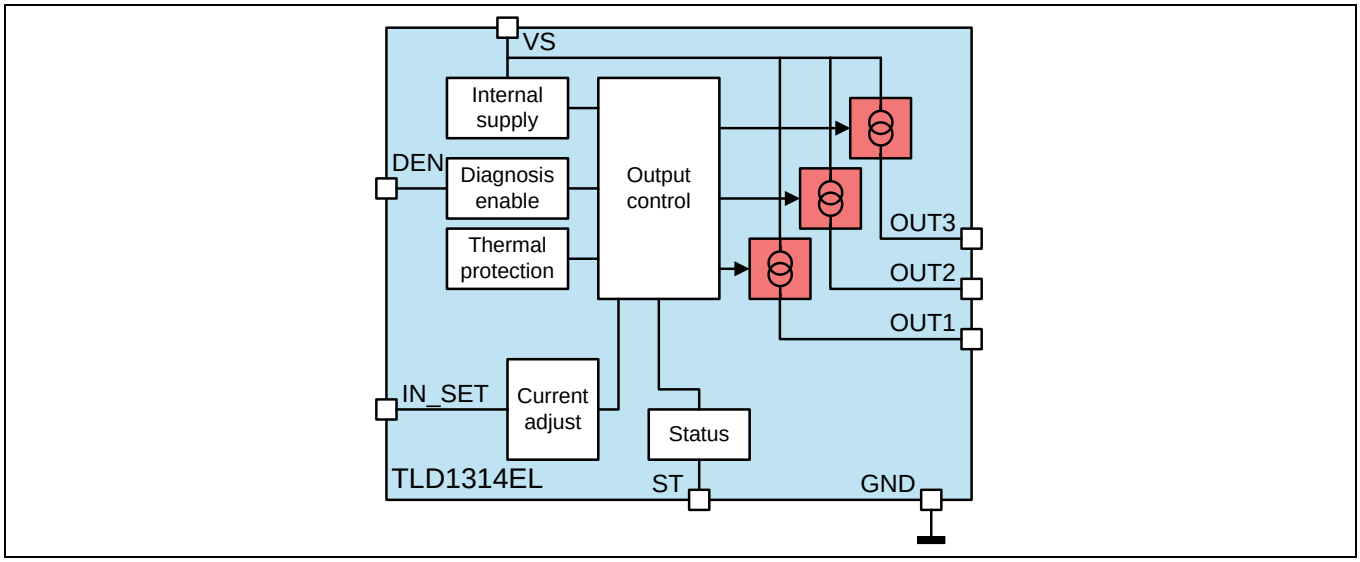



**Figure 3 Block Diagram of LITIX™ Basic device with DEN pin (TLD1314EL)**

### 3.1.1 Unused Outputs

Unused outputs on the LITIX™ Basic can be connected as follows:

- Devices with no diagnostics (TLD1310, TLD1312 and TLD2310) can have unused outputs left open. Devices with 3 inputs and diagnosis (TLD2326, TLD2314 and TLD2311) should have unused outputs and the associated IN_SET pins left open.
- Devices with N-1 detection, but no short circuit (SC) to ground diagnosis (TLD1326, TLD1311 and TLD1315), the outputs can be connected to ground, as these devices disable a shorted channel.
- The TLD1313 and TLD1314 must have the unused outputs connected via a zener diode as shown in Figure 4 to avoid shutdown due to open load detection if left open. Open load is triggered when the voltage difference between the supply and the output is too low and below the threshold $V_{PS\ (OL),}$ and short circuit to ground diagnosis if connected to ground. The clamping voltage of the zener diode should be in the range of the total LED forward voltage on the used channels. The voltage on any output (either with LED's or zener diode) must be 2.5V or greater to ensure proper operation.

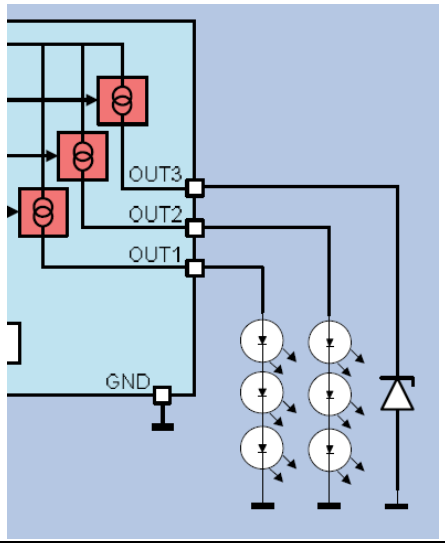



**Figure 4 Connection of unused outputs via zener diode (TLD1313 and TLD1314 only)**

### 3.1.2 Minimizing device power dissipation

To reduce power dissipation in the BasicLED when driving short LED chains, it is possible to add a zener diode or resistor in series with the LEDs. The zener diode is the preferred method. See Figure 5 .

- Caution must be used in the case of the resistor, as it has the following impact on the operation of the LITIX™ Basic in the following ways:
  - Increasing resistance in the output current path decreases the phase margin and stability of the control loop. Resistance must be below 75ohms and output wire length below 0.5 meters in order to maintain phase margin above 60 degrees.
  - During high temperature conditions, the LITIX™ Basic reduces the output current. When the output current is reduced, the voltage drop across the output stage increases, causing more power dissipation. This further reduces the current causing a potentially unintended shutdown condition.
  - It must be ensured under all application conditions that the output voltage drop with the load is at least 2.5V to ensure proper operation ($V_{OUT(CC)}$ in datasheet). For example, during startup, the voltage drop impact of the resistor (the voltage across the power stage, from Vs to the output) is zero, since the current through the resistor is zero. It is in this case for startup that the total voltage drop is at a minimum, and must be above 2.5V.
- All configurations need to be confirmed in the real application. The minimum battery voltage, Vs to output voltage drop needed for current control ($V_{PS(CC)}$) and the maximum LED voltage drop need to be considered to determine the proper zener diode or resistor values.

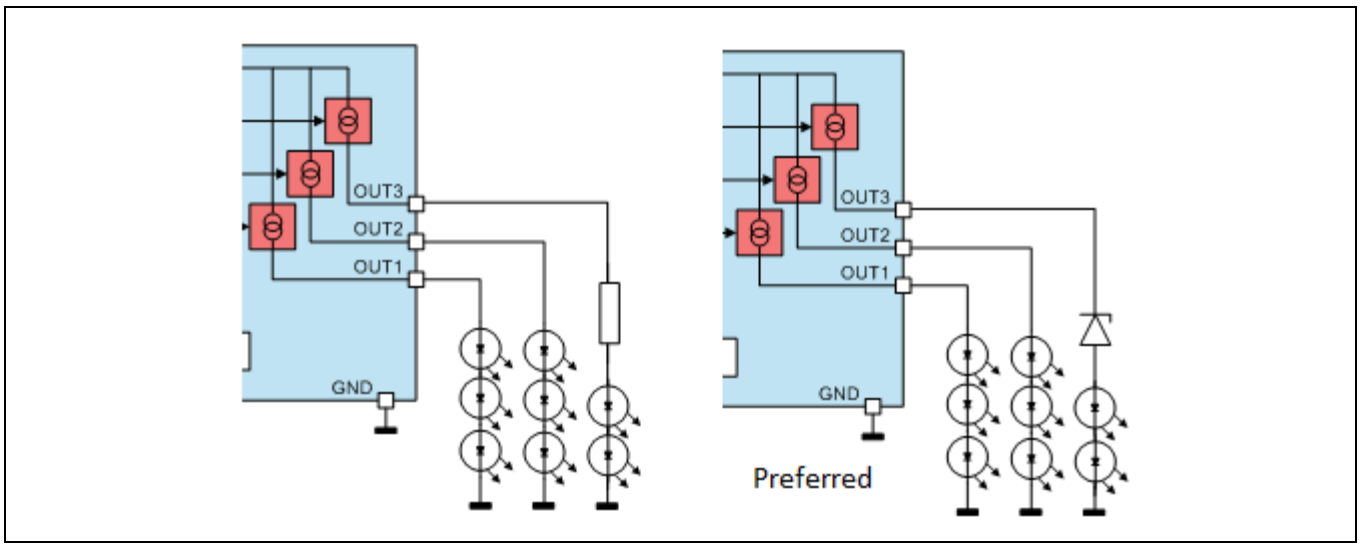



**Figure 5 Methods to reduce device power dissipation when driving short LED chains**

Further explanation of device operation and suggested application hints are in the following sections.

## 3.2 Pin and Feature Descriptions

### 3.2.1 EN (enable) pin

The block diagram for the EN pin input can be seen below in Figure 6.

NOTE: If the EN pin is not used, it should be connected to $V_S$ through a 10Kohm resistor (device enabled with $V_S$).

The EN (enable) pin has several functions and possible application uses:

- If the voltage at this pin is below the EN turn off threshold defined as $V_{EN(off)}$ in the datasheet, the device will be in the low current sleep mode. If the voltage at this pin is above the turn on threshold $V_{EN(on)}$ , the device is enabled after a maximum 50µsec power on reset delay.
    - In this way it acts as a simple enable/power on reset feature using typical logic thresholds.
    - One application example of this pin being used in this way would be when a microcontroller output or other device controls this pin and the LITIX™ Basic device directly.

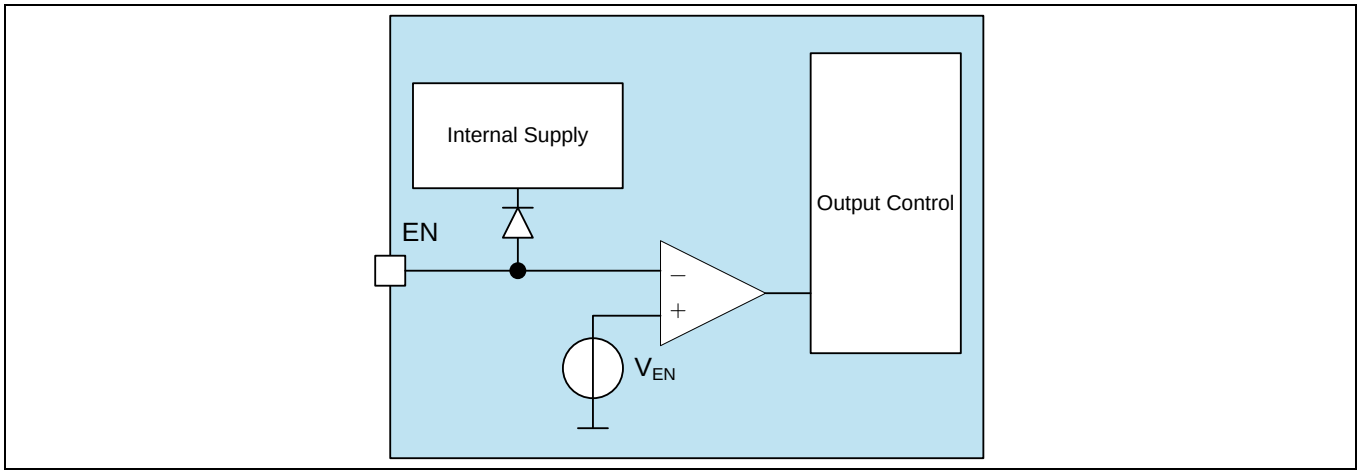



**Figure 6 Block Diagram of EN pin**

The EN pin can also be used as an alternate supply for the internal logic of the device.

- Supplying the logic from the EN pin allows the device to have a faster response time at the outputs during PWM operation, where Vs of the device is PWM controlled directly. The output response time is shorter because the POR time, $t_{POR}$ is longer than the $V_S$ turn on time, $t_{ON(VS)}$. So, if the EN pin voltage is kept above $V_{EN(on)}$, the output will respond more quickly to PWM control and achieve a wider duty cycle range. The capacitor and diode circuit below in Figure 7 is an example of a possible way in the application to keep the input to output delay as short as possible during PWM operation.
- A typical application example of this is when a Body Control Module (BCM) sends a PWM signal on $V_{BATT}$ to a lighting module.
- Another application example is when the device is fed from a DC/DC converter in the buck configuration, and the supply voltage to the LITIX™ Basic drops.

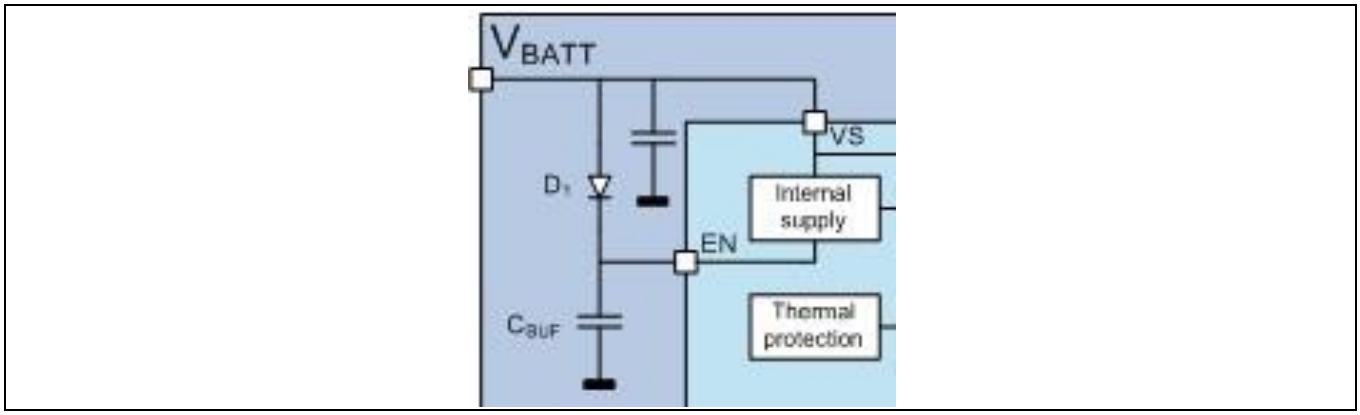



**Figure 7 EN pin used as alternate logic supply**

The capacitor $C_{BUF}$ can be calculated using the following formula:

$$C_{BUF} = t_{LOW(max)} \cdot \frac{I_{EN(LS)}}{V_S - V_{D1} - V_{S(POR)}}$$

where;

$C_{BUF}$ is the capacitor value
$t_{LOW(max)}$ is the maximum low time of the PWM signal
$I_{EN(LS)}$ is input current to the EN pin
$V_S$ is the supply voltage
$V_{D1}$ is the voltage drop across diode D1, typ. 0.6V
$V_{S(POR)}$ is the power on reset voltage level

A typical calculation example:

200Hz PWM at a minimum of 5% duty cycle → $t_{LOW(max)}$ = 0.95 x (1/200) = 4.75msec.
$I_{EN(LS)}$ = 2mA (max. from datasheet)
$V_S$ = 6V
$V_{D1}$ = 0.6V
$V_{S(POR)}$ = 4.5V (max. from datasheet)

$C_{BUF}$ = (0.00475 x 0.002) / (6 – 0.6 – 4.5) = **10.56µF**

### 3.2.2 DEN (Diagnostic enable) pin

The block diagram for the DEN pin input can be seen below in Figure 8.

The DEN (diagnostic enable) pin is a single function pin that is used to activate or deactivate the internal diagnosis functions. The diagnosis *output* functions of the ST pin or INSET pin are disabled, but the input functions of the ST pin or INSET pin are not affected by the state of the DEN pin.

The input logic of the DEN pin is active high, so the device diagnostic output is active if the voltage at this pin is above $V_{DEN(act)}$ and the diagnosis output is disabled if the voltage at this pin is below $V_{DEN(dis)}$.

Notice that this pin has a pull down current source $I_{DEN}$, which ensures the DEN pin is in a low state (diagnosis output disabled) if left open.

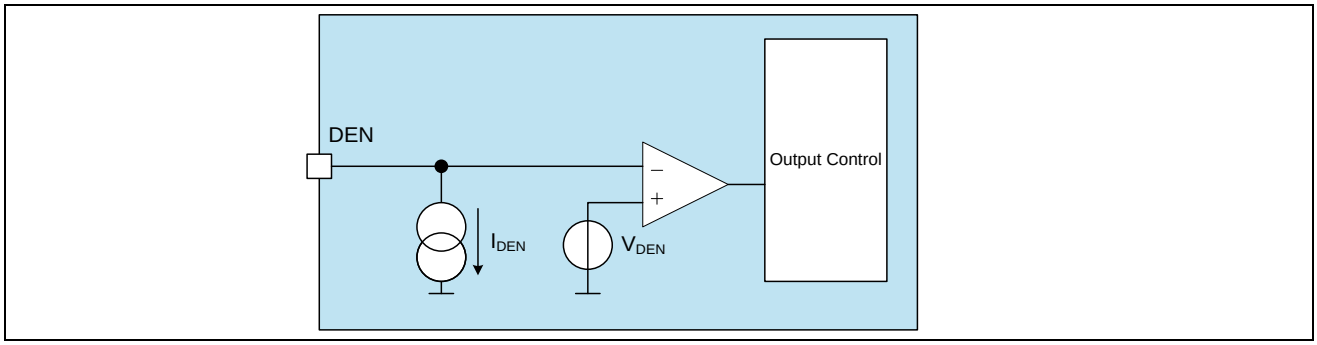



**Figure 8 Block Diagram of DEN pin**

A typical application of the DEN pin function could be to disable the diagnosis until a supply voltage is reached which is greater than the connected LED(s) forward drop voltage. This could be implemented with a zener diode connected between the supply pin and the DEN pin. Additional details will follow in the “Application examples” section.

### 3.2.3 IN_SET pin(s)

The block diagrams for the IN_SET pin for the different LITIX™ Basic devices can be seen in Figures 12, 13 and 16.

The IN_SET pin has several functions and possible application uses:

- The IN_SET pin sets the output current level (all devices) – See figure 9 below
  - Devices with a single IN_SET pin, the current for all output channels (1 or 3 outputs) is set with this single IN_SET pin.
  - Devices with 3 IN_SET pins, the 3 output channel currents are set individually.
  - A resistor is placed at the IN_SET pin to ground to set the output current level. The internal reference voltage of 1.23V typical causes a current to flow out of the IN_SET pin to ground through this resistor. The calculation of the IN_SET resistor is done using the formula below:
    - $R_{SET} = k_{nom} / I_{OUT}$,

      Where;

      $k_{nom}$ = gain factor defined in device datasheet (typ. 2250 for 1 channel devices, typ. 750 for 3 channels devices)

      $I_{OUT}$ = desired output current per channel

      $R_{SET}$ = Calculated IN_SET resistor value

      For example: If 40mA output current is desired, $R_{SET}$ = 2250 / 0.040 = 56.250KΩ

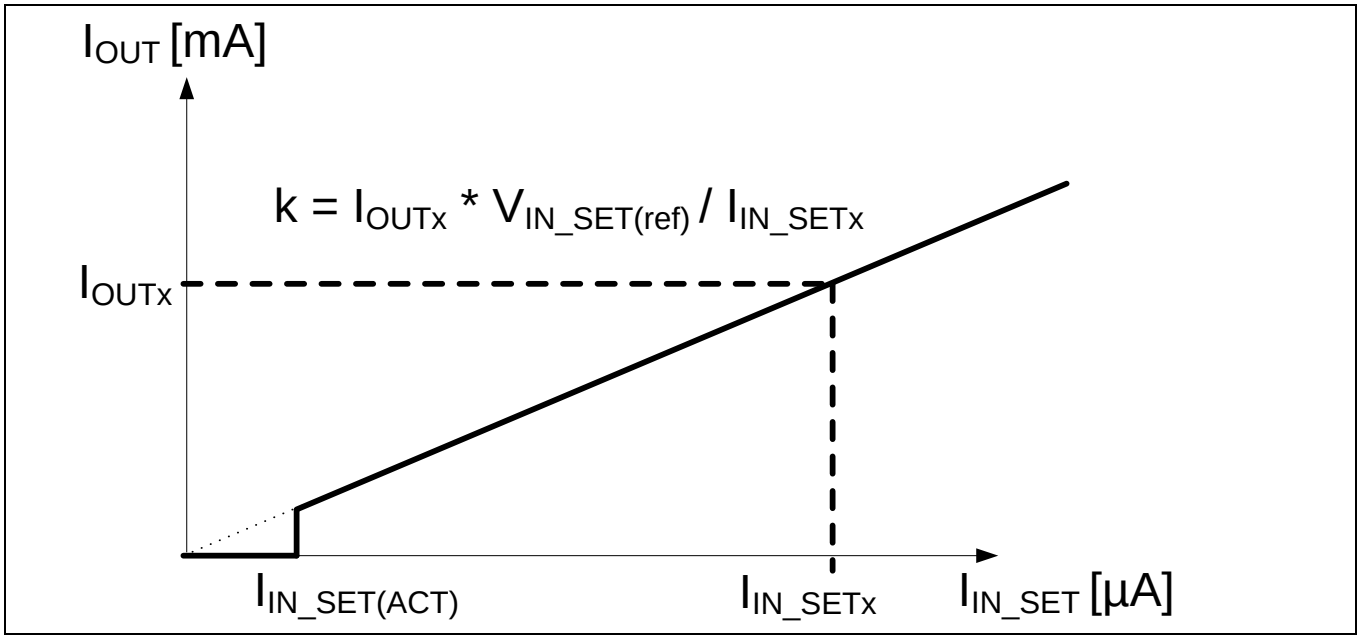



**Figure 9** **$I_{OUT}$ vs. $I_{IN\_SET}$**

*NOTE: A minimum current of $I_{IN\_SET(ACT)}$ is needed to flow in the IN_SET pin before the output current will flow. This is to prevent glowing of LED's due to small off state current leakages in the output stages of the controlling device connected to the IN_SET pin (i.e. microcontroller port, etc.).*

- Setting low output currents with high RSET values
  - Using high RSET resistor values to set output currents below 10mA should be avoided. Oscillations can occur on the output due to loss of current control. See example scope plots in Figure 10. This particular example occurred at an output current of approximately 2mA.

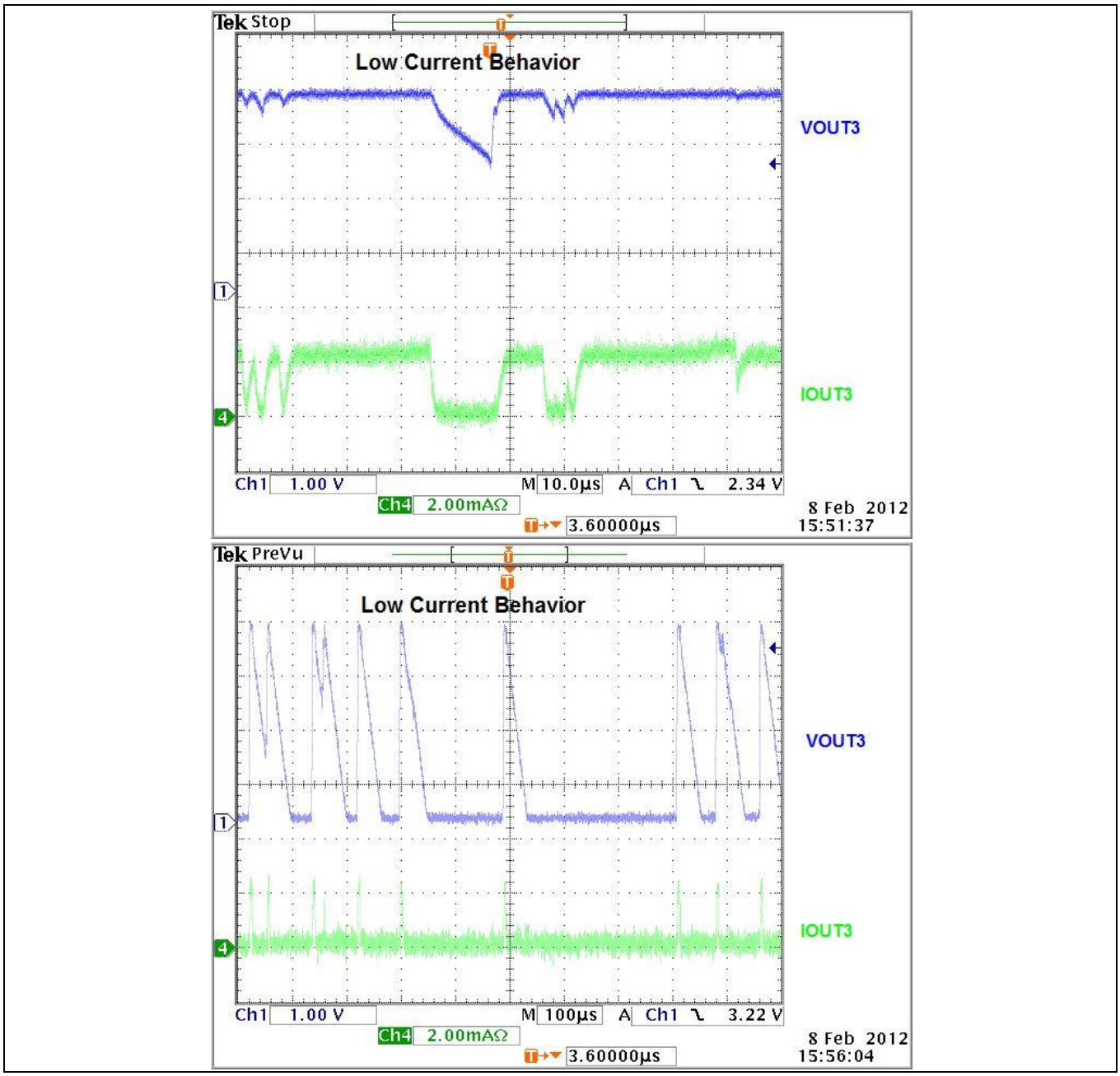



**Figure 10 Behavior with very low current setting via $R_{IN\_SET}$**

For all devices, the IN_SET pin can be used to turn the outputs on and off. A simple example interface circuit to a microcontroller is given below in Figure 11. This example circuit is applicable for devices with no diagnostics (TLD1310, TLD1312, TLD1120 and TLD2310) or all devices where diagnostics are not used or needed. For devices with the ST pin, this circuit can also be used and the ST could provide the diagnostic indication.

Figure 12 shows the Block Diagram for the IN_SET pin for the simplest LITIX™ Basic devices (TLD1310, TLD1312, TLD1120, and TLD2310). No diagnostic feedback on these devices is given.

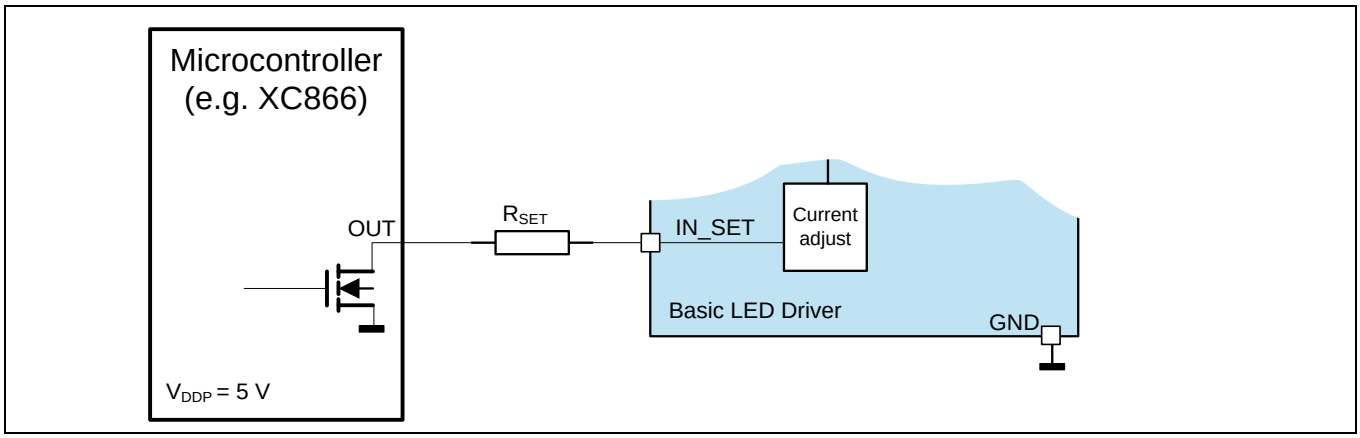



**Figure 11 Example interface of IN_SET pin to µC**

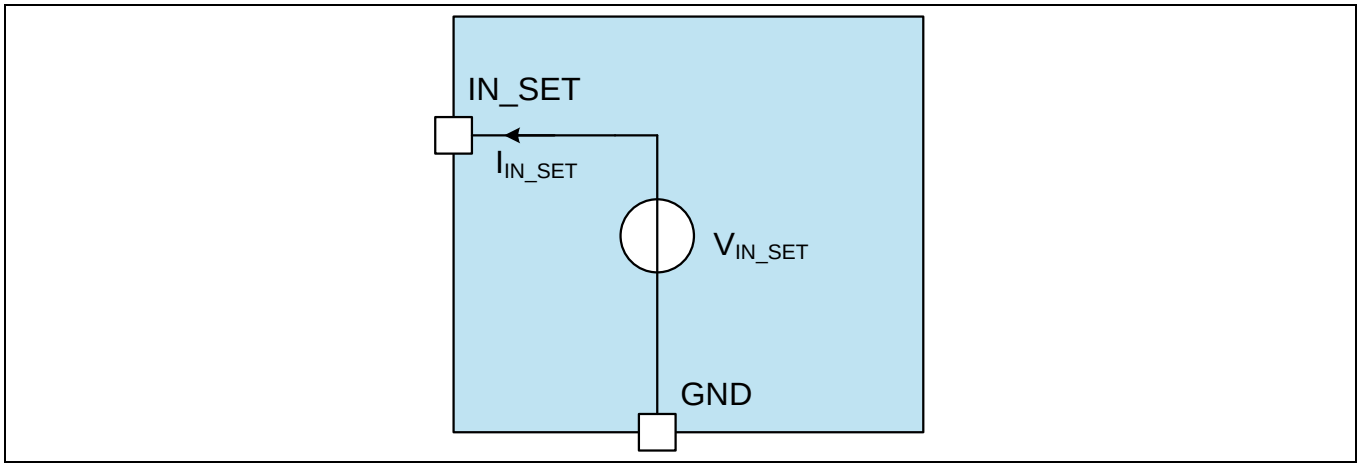



**Figure 12 IN_SET pin of some devices (TLD1120, 1310, 1312 and 2310)**

The IN_SET can be used as a diagnostic indicator on specific devices with the ST pin:

- For devices with ST (status) pin, please see Figure 13 for the block diagram of the IN_SET pin. The 3 states of the IN_SET pin are:
  - $V_{IN\_SET}$, in case of normal operation and driven by internal $V_{IN\_SET}$ reference to set output current level via $R_{SET}$ resistor.
  - $V_{IN\_SET(OL/SC/N-1)}$, in case a fault occurs (open load, short circuit to ground or N-1 detection depending on the device) and the ST pin is grounded.
  - High impedance, in case a fault occurs (open load, short circuit to ground or N-1 detection depending on the device), and the ST pin is open or connected with a high ohmic resistor to ground (ST pin to be used for diagnosis)
- The IN_SET pin can be used for diagnosis if the ST pin is connected to ground
- The IN_SET pin when used as a diagnosis pin has 2 voltage levels, one for setting the current level (1.23V typ.) and one for the diagnosis (5V typ.). This is shown in Figure 14. In case the IN_SET pin is used for diagnosis (ST pin grounded), the IN_SET pin will go to a high level state (5V typ.) when a fault is present.

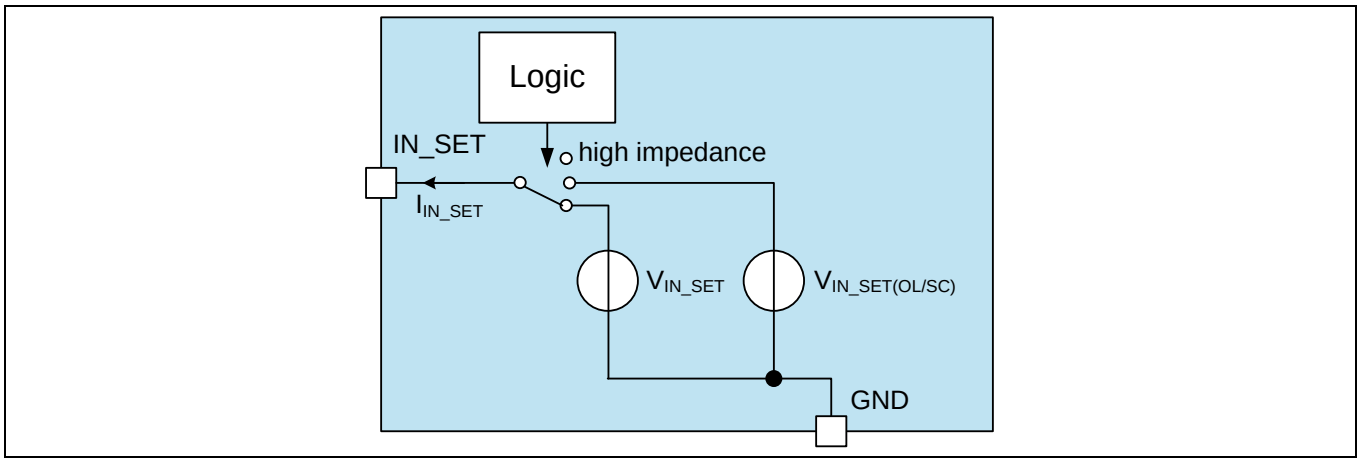



**Figure 13 IN_SET pin of devices with ST pin (TLD1121,1124,1125,1313,1314,1311,1315,2311,2314)**

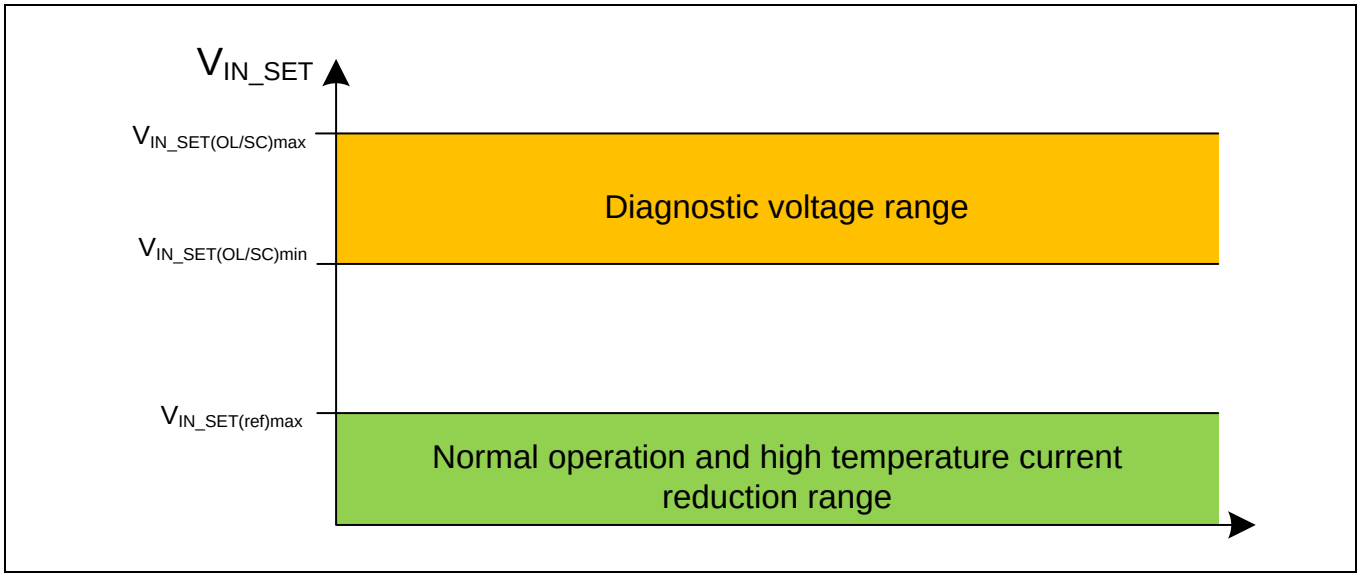



**Figure 14 Voltage domains for IN_SET pin, if ST pin is connected to GND**

To use the IN_SET diagnostics instead of the ST pin diagnostics, a possible circuit is shown in Figure 15. The voltage divider circuit allows the microcontroller to recognize a fault at its digital input pin. The microcontroller's open drain output switch to ground sets the output current and can be used to turn the channel on and off. The leakage of the open drain output switch and the monitoring input need to be considered to ensure the total leakage current is less than $I_{IN\_SET(ACT)}$. This is to avoid glowing of the LEDs when the IN_SET pin is intended to be off.

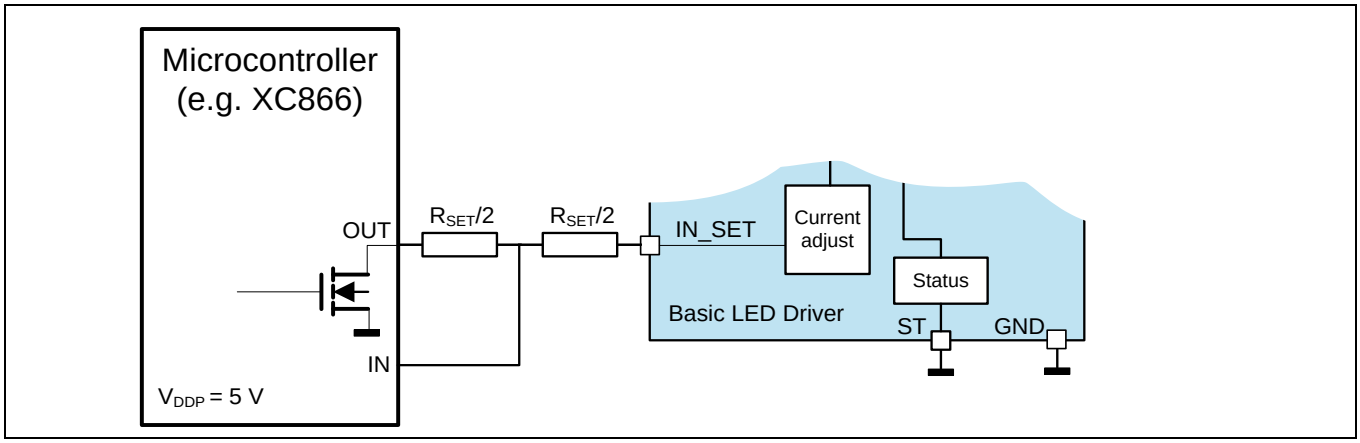



**Figure 15 Possible circuit to use IN_SET pin for diagnosis with ST pin grounded**

The IN_SET can be used as a diagnostic indicator on devices with the FB pin:

- For devices with FB (feedback) pin, please see Figure 16 for the block diagram of the IN_SET pin. The 2 states of the IN_SET pin are:
  - $V_{IN\_SET,}$ in case of normal operation and driven by internal $V_{IN\_SET}$ reference to set output current level via $R_{SET}$ resistor.
  - $V_{IN\_SET(OL/SC/N-1),}$ in case a fault occurs (open load, short circuit to ground or N-1 detection depending on the device)
- The IN_SET pin has 2 voltage domains, one for setting the current level and one for the diagnosis. This is shown in Figure 17. So the IN_SET pin will go to a high level state when a fault is present.

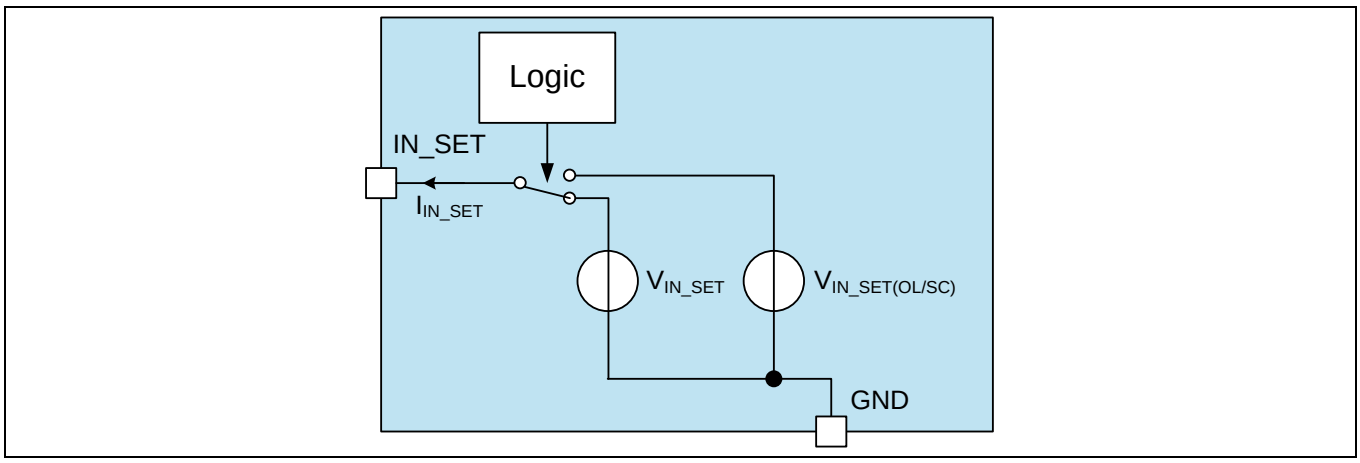



**Figure 16 Block Diagram of IN_SET pin for devices with FB pin (TLD1326, 2326)**

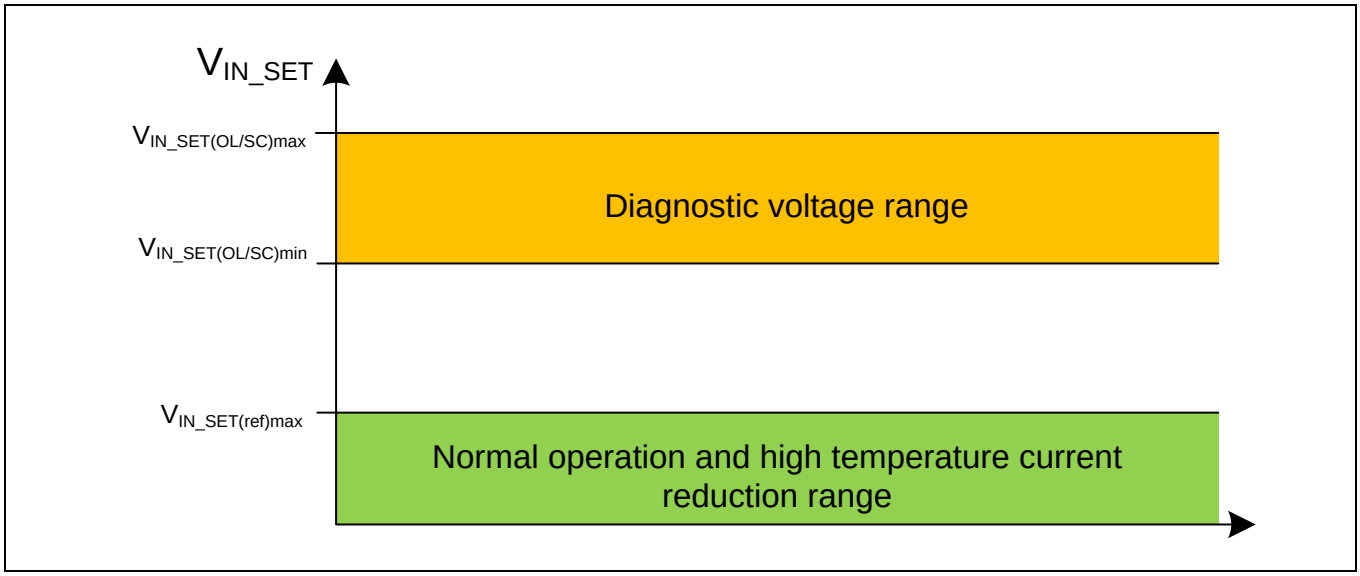



**Figure 17 Voltage domains for IN_SET pin on devices with FB pin**

To use the IN_SET diagnostics on devices with the FB pin, a possible circuit is shown in Figure 18. The voltage divider circuit allows the microcontroller to recognize a fault at its digital input pin. The microcontroller's open drain output switch to ground sets the output current and can be used to turn the channel on and off. The leakage of the open drain output switch and the monitoring input need to be considered to ensure the total leakage current is less than $I_{IN\_SET(ACT)}$. This is to avoid glowing of the LEDs when the IN_SET pin is intended to be off.

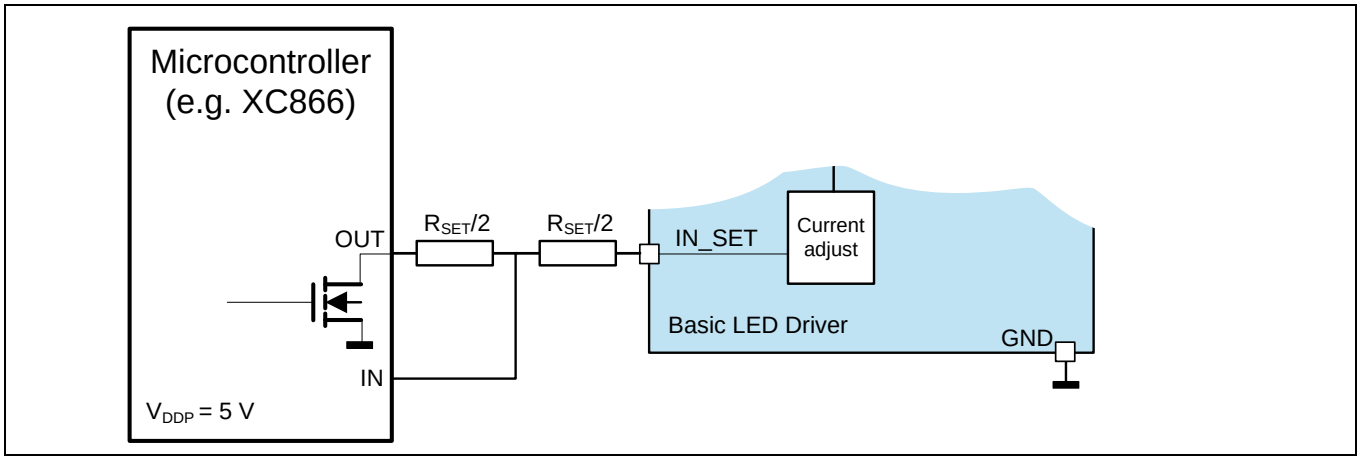



**Figure 18 Possible circuit to use IN_SET pin for diagnosis**

### 3.2.4 ST (Status) pin (TLD1124,1311, 1313, 1314, 1315, 2311 and 2314)

The block diagrams for the ST pin can be seen in Figure 19. Additional application details are given in section 4.1.1.5.

The ST pin functions as a diagnostic indicator or disable input, depending on its connection and applied voltage to the pin in the application.

- If the ST pin is connected to ground with a high ohmic (i.e. 470KΩ) resistor (with voltage at the ST pin lower than $V_{ST(L)}$) it functions as a diagnostic output. When the device is powered, and there are no faults, the ST pin is pulled to ground with the pull down current source $I_{ST(PD)}$. When a fault occurs (open load, short circuit to ground, N-1 depending on the device), the pull up current source activates and the ST pin voltage rises to $V_{ST(OL/SC/N-1)}$ after a fault detection filter time. The filter time is defined below and specified in the device datasheets:
  - $t_{OL}$ - OL (open load) detection filter time – (and a fault is not latched)
  - $t_{SC}$ - SC (short circuit) detection filter time - (and a fault is not latched)
  - $t_{N-1}$ - TLD1311, TLD1315 only: Open load N-1 detection filter time – (set by capacitor on N-1 pin) (and ST pin is latched with reset by $V_s$ or EN pin).
  - Note that for the TLD1124, 1314 and 2314, the voltage at the DEN pin must be greater than $V_{DEN(act)}$ for the ST pin to function as a diagnostic output.
- If the ST pin is connected to ground, then diagnosis via this pin is disabled and is performed via the IN_SET pin as previously described in section 3.2.2.. Note that for the TLD1124, 1314 and 2314, the voltage at the DEN pin must be greater than $V_{DEN(act)}$ for the IN_SET pin to function as a diagnostic output.
- An example circuit is given in Figure 20 for the case where the ST pin is used for diagnosis. The IN_SET resistor and IN_SET pin in this case are only used to set the output current and to turn the channel on and off.
- For applications where PWM is performed on the EN or VS pins, the output will be reset during each power cycle, so there is a short time where the output is on when a fault is present (detection filter time). Also, during a fault regardless of the state of the ST pin, a current source is connected and current flow will occur at the ST pin.
- If an external voltage above $V_{ST(H)}$ is applied to the ST pin, the entire device is switched off. This is the Disable function of this pin. This is useful when multiple devices are used for one light function and the entire light function is disabled if one LED string fails. By connecting the ST pins of multiple devices, one failure on any connected device will disable all device outputs. The next section describes the N-1 pin function in more detail. Note: For the TLD1124, 1314 and 2314, the disable functionality of the ST pin is not affected by the state of the DEN pin.

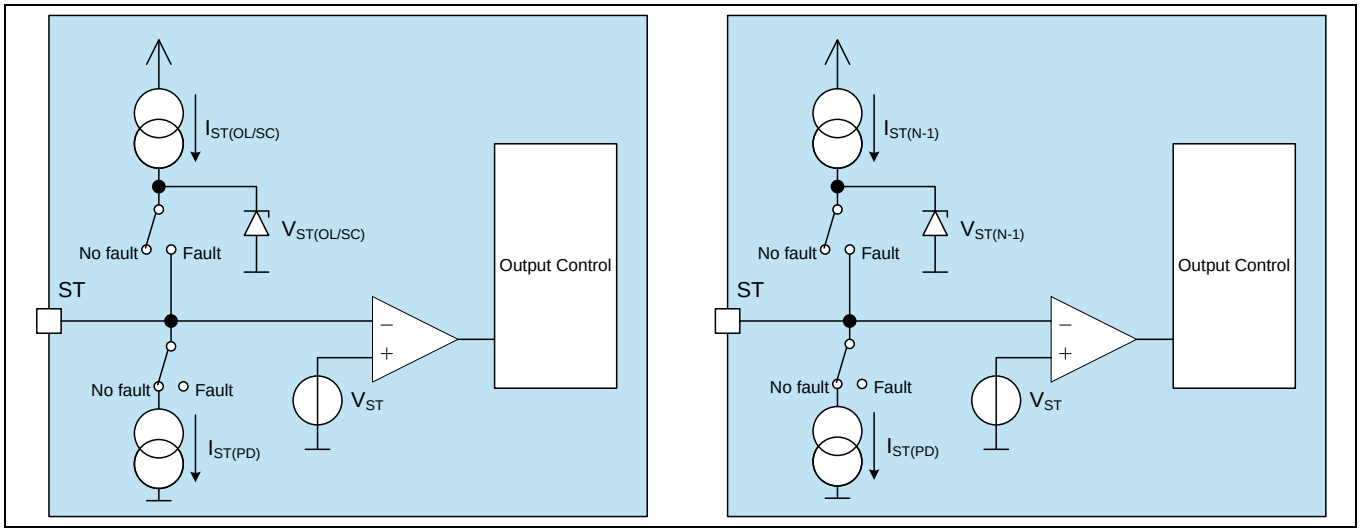



**Figure 19 Block diagrams for the ST pin**

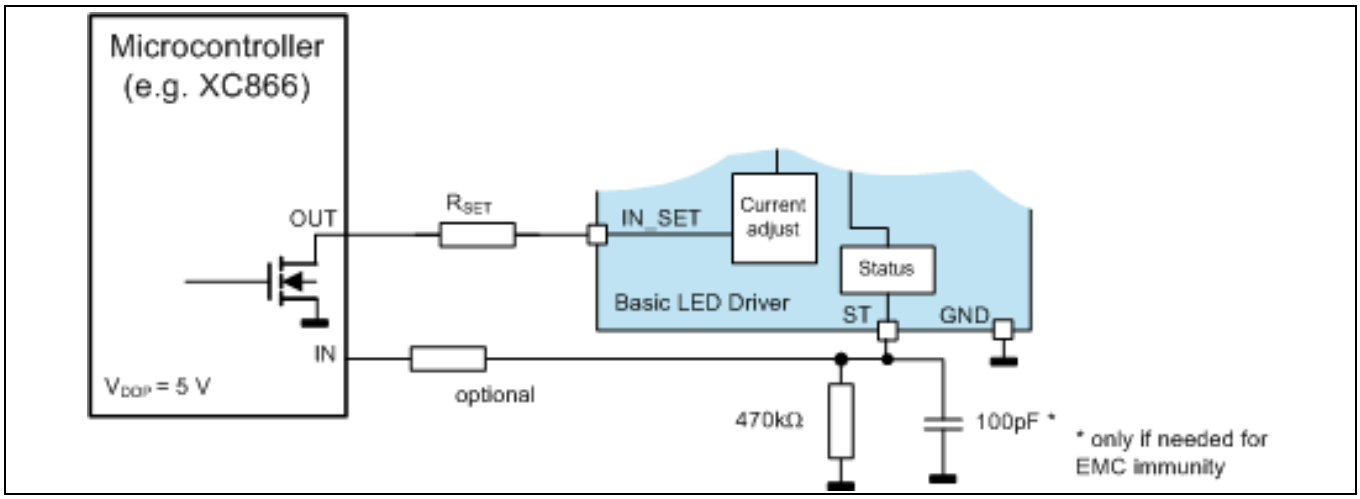



**Figure 20 Possible circuit to use ST pin for diagnosis**

### 3.2.5 N-1 pin (TLD1311, 1315 and 1326)

The block diagram for the N-1 pin can be seen in Figure 21.

- The N-1 fault detection feature is meant to be used as a way to detect error conditions in LED arrays where multiple devices are used for a common light function (i.e. rear combination lamp). Customers may require a complete deactivation of a light function, if a portion of the function cannot meet the requirements (i.e. brightness due to failure of one LED string).
- A capacitor is connected to the N-1 pin, to allow adjustment of the filter time used for N-1 fault detection. This filter time is illustrated as an example for an open load condition in Figure 22. The time is calculated using the equation below:

$$t_{N-1} = \frac{C_{N\_1} \cdot V_{N\_1(th)}}{I_{N\_1}}$$

Where;

- $C_{N-1}$ = Capacitor value on N-1 pin to ground
- $V_{N-1(th)}$ = N-1 threshold voltage, 3V typical from datasheet
- $I_{N-1}$ = charging current, 20µA typical from datasheet

An example calculation with $C_{N-1}$ = 100nF:

$t_{N-1}$ = [(0.0000001) x 3] / (0.000020) = 0.015 sec. = **15 msec.**

Corresponding worst case values can also be calculated based on the min/max values in the device datasheet, and the capacitor tolerances.

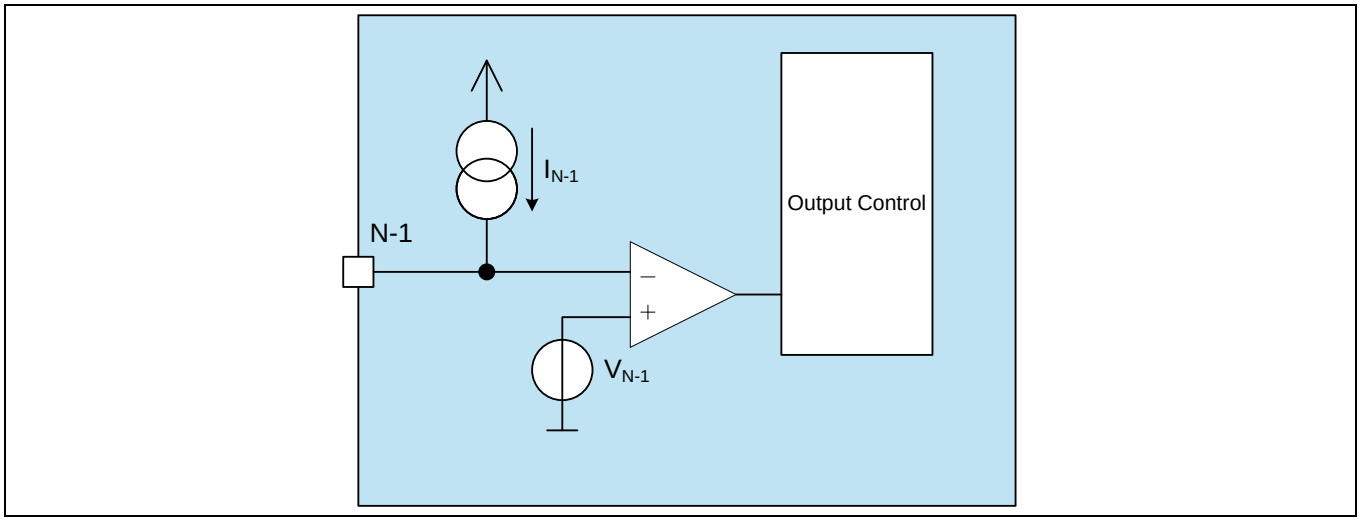



**Figure 21 Block diagram for N-1 pin**

Figures 22 and 23 show the fault timing during an open load. The IN_SET or ST pin latches the fault until the EN (or $V_S$ pin) is toggled and a POR is given.

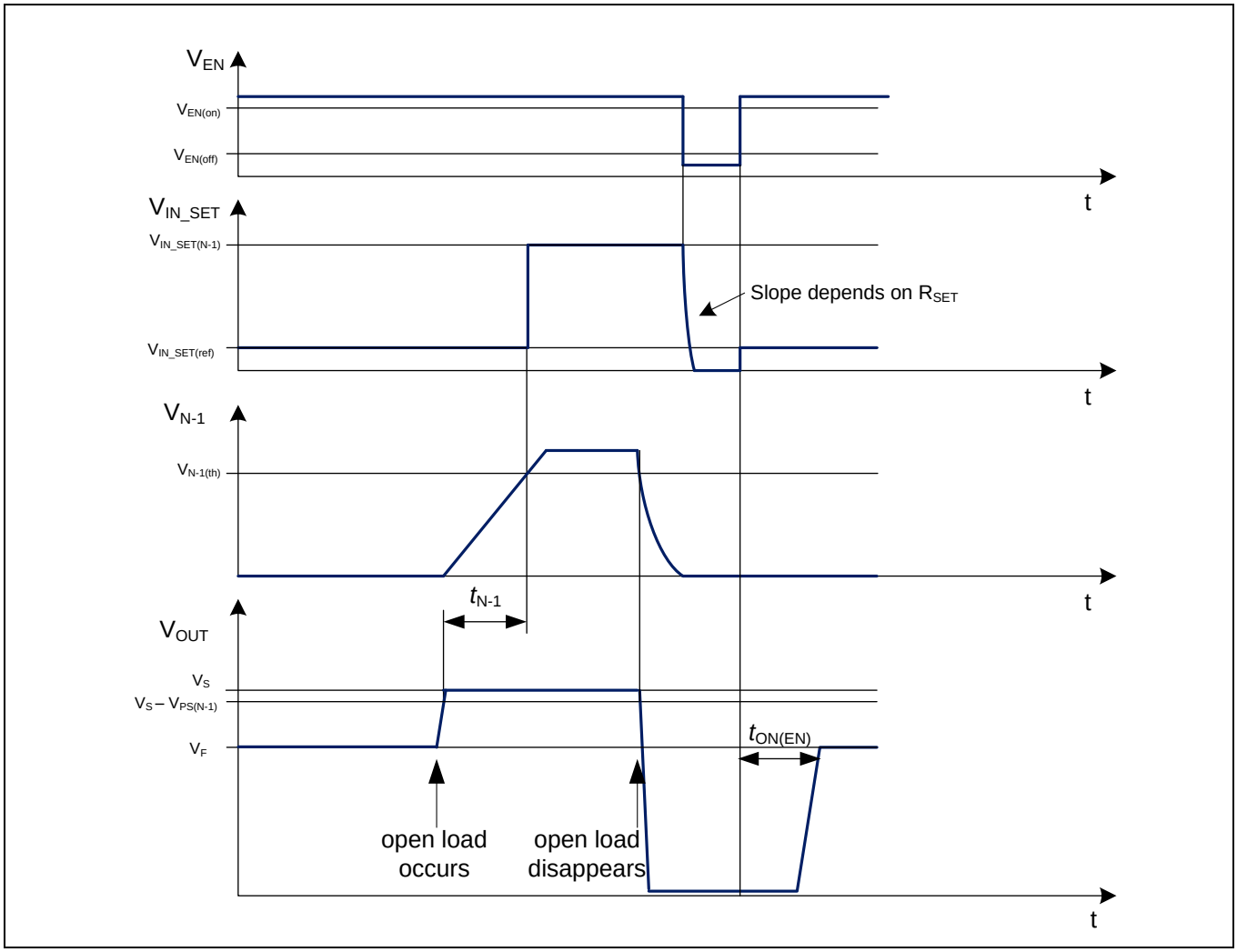



**Figure 22 Fault timing during open load (ST pin grounded, IN_SET used for diagnostics)**

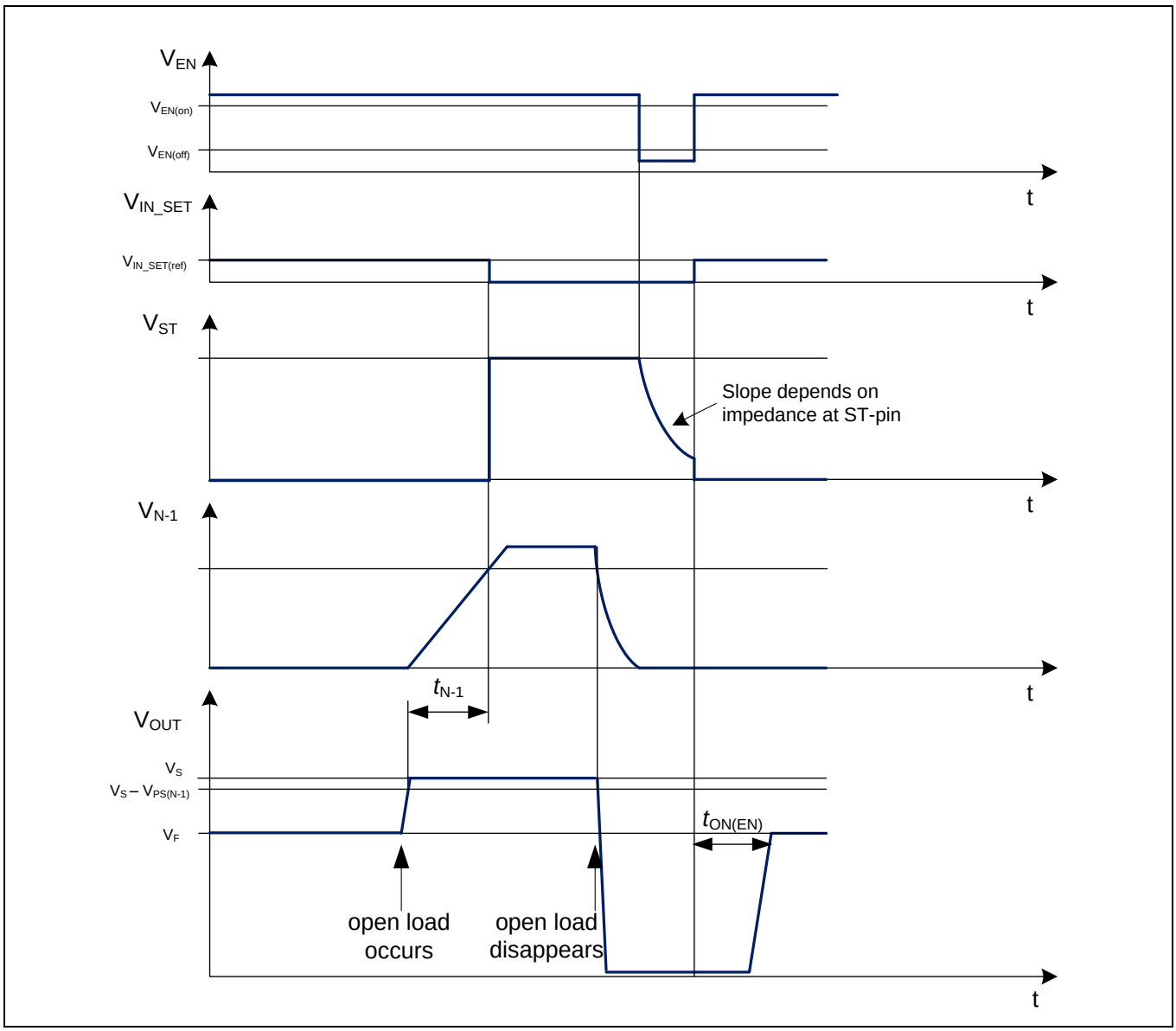



**Figure 23 Fault timing during open load (ST pin used for diagnostics)**

An example application circuit is given in Figure 24 for multiple devices controlling one light function. Further details and discussion will follow in the application example section.

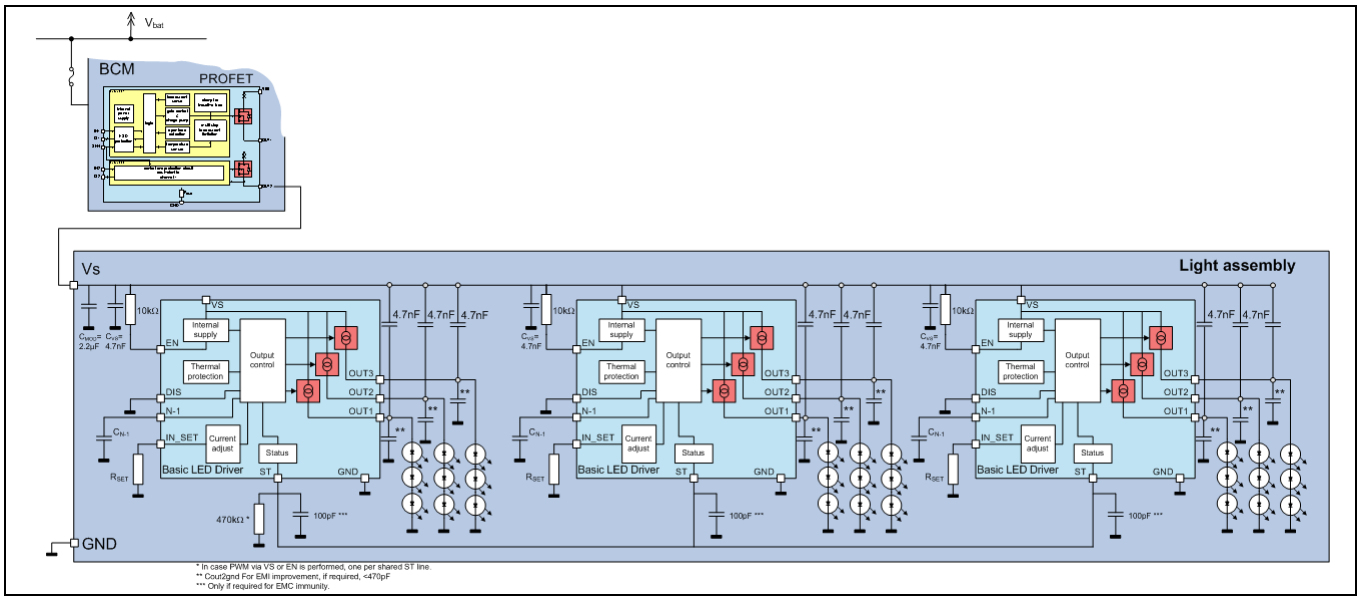



**Figure 24 Application example of N-1 detection for multiple devices controlling one light function**

### 3.2.6 D pin (TLD1125)

The block diagram for the D pin can be seen in Figure 25.

- The D pin is meant to extend the open load detection filter time, $t_{OL}$, through the use of an external capacitor to ground. If this pin is left open, the default $t_{OL}$ time will used.
- A capacitor is connected to the D pin, to allow adjustment of the filter time used for open load fault detection. This filter time is determined by the capacitor value $C_D$, the internal charging current $I_D$ and the voltage threshold $V_{D(th)}$. The time $t_{OL}$ is calculated using the equation below:

$$t_{OL} = \frac{C_D \cdot V_{D(th)}}{I_D}$$

Where;

- $C_D$ = Capacitor value on D pin to ground
- $V_{D(th)}$ = D high voltage threshold, 3V typical from datasheet
- $I_D$ = D output current, 2µA typical from datasheet

An example calculation with $C_D$ = 10nF:

$t_D$ = [(0.00000001) x 3] / (0.000002) = 0.015 sec. = 15 msec.

Corresponding worst case values can also be calculated based on the min/max values in the device datasheet, as well as the target capacitor tolerance and drift.

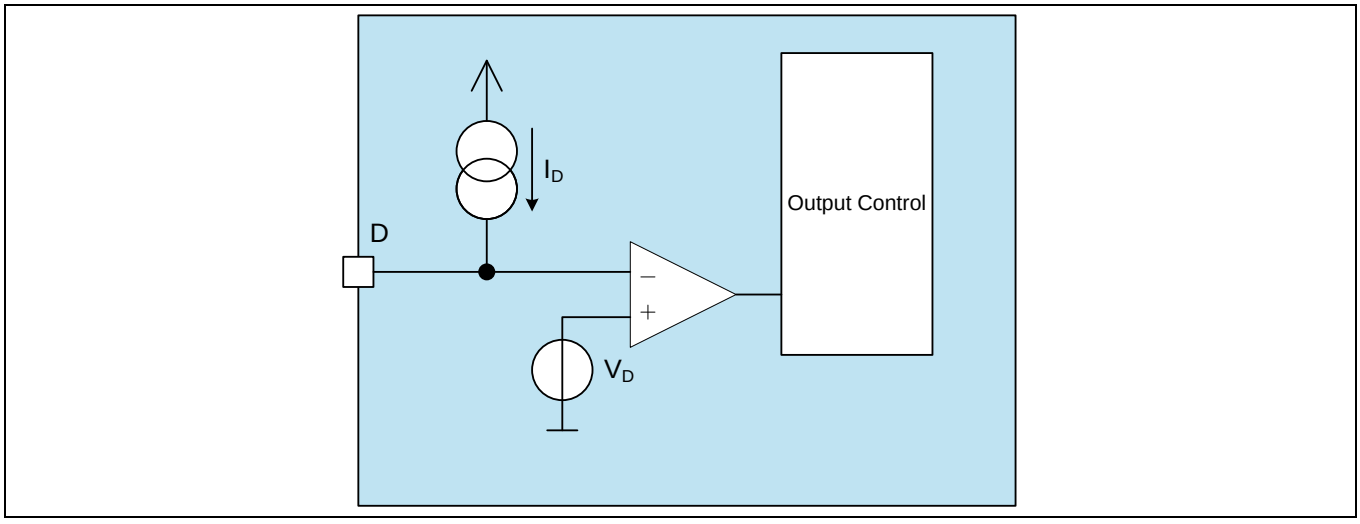



**Figure 25 Block diagram for the D pin**

### 3.2.7 PWMI pin (TLD1125, 1312, 1315 and 1326)

The block diagram for the PWMI pin can be seen in Figure 26.

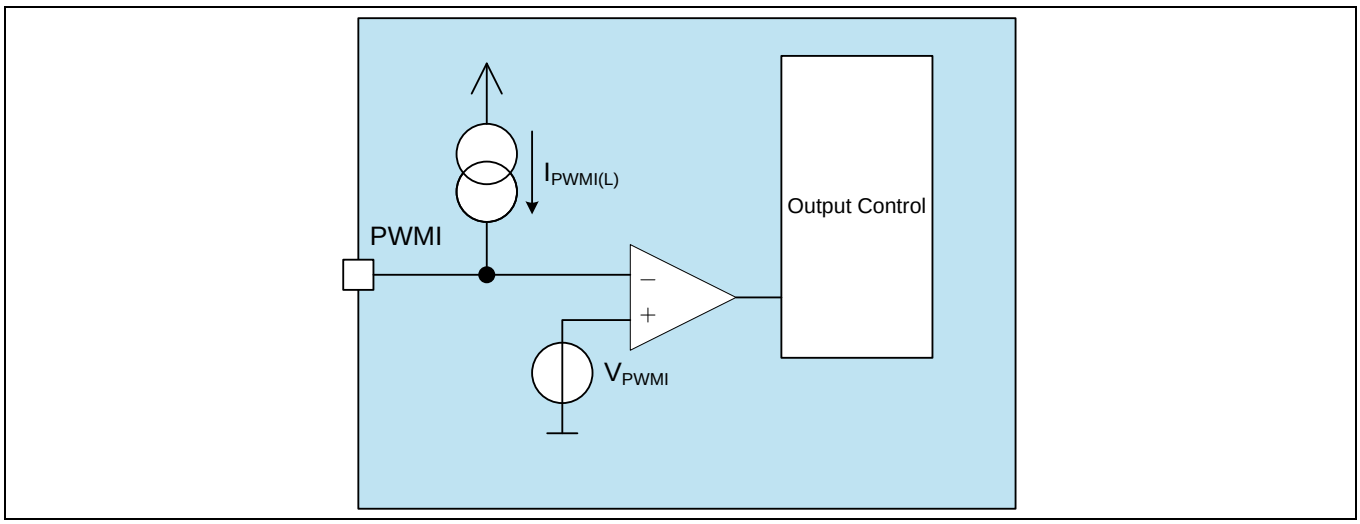



**Figure 26 Block diagram for the PWMI pin**

The PWMI pin is a dual function pin;

- It can be used as a direct PWM input (active low) with a push-pull output of a microcontroller or similar device.
- The PWM duty cycle and frequency is limited by the turn on and off times of the power stages, $t_{on(PWMI)}$ (30 µs max.) and $t_{off(PWMI)}$ (30 µs max.).
- An external RC parallel circuit can be used to activate an internal PWM unit.
    - The internal PWM unit works by charging (via pull up current source which is active when PWMI is active (low)) and discharging (via the external resistor when PWMI is inactive (high)) the external capacitor in the RC network. In this way, the upper and lower thresholds of the PWMI pin are reached at the frequency and duty cycle based on the external RC circuit. See figure 27 for the threshold definition and connection for $R_{PWMI}$ and $C_{PWMI}$.
    - The internal PWM can be used to generate 2 brightness levels (i.e. running and brake light) without the need for an external PWM source. An external switch can be used to activate a high brightness level (100% duty cycle) and when the switch is off, the internal PWM unit runs and the output is dimmed according to a PWM duty cycle and frequency set by the external RC circuit.

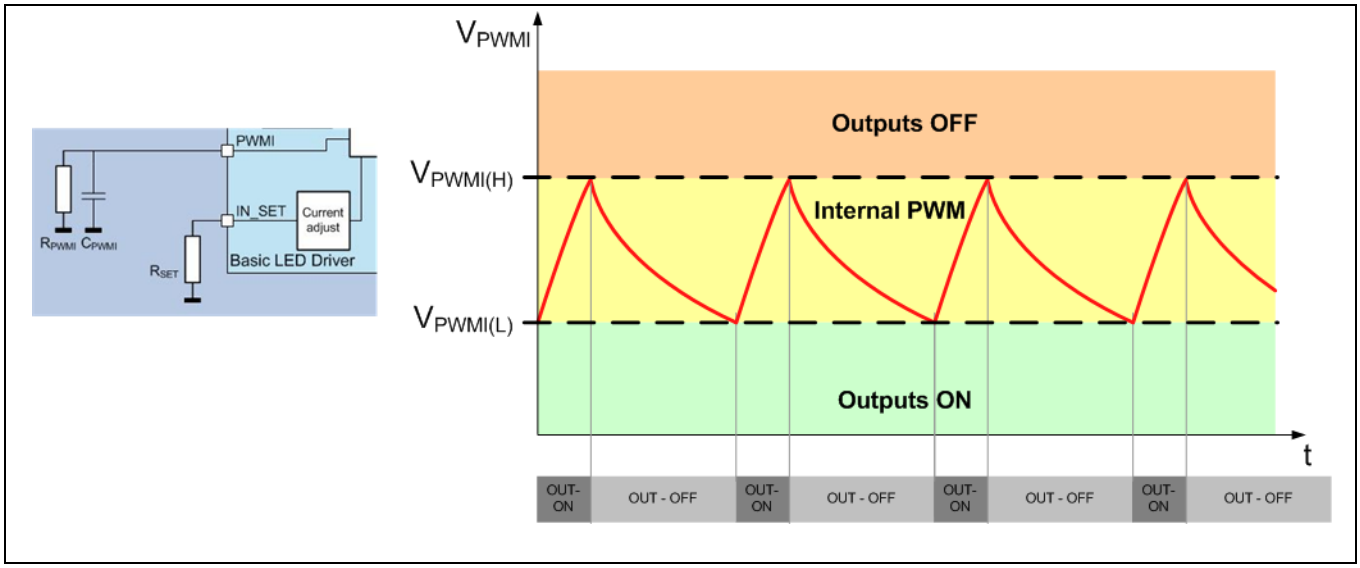



**Figure 27 Operating thresholds of PWMI pin (internal PWM unit), $R_{PWMI}$ & $C_{PWMI}$ connection to PWMI pin**

The calculation of the resistor and capacitor values are done using the formulas below. Use the typical values from the datasheet.

In terms of resistance $R_{PWMI}$ and capacitance $C_{PWMI}$ the equations are:

$$C_{PWMI} = \frac{-I_{PWMI(on)} \cdot t_{PWMI(off)} \cdot \left[ \left( \frac{V_{PWMI(L)}}{V_{PWMI(H)}} \right)^{\frac{t_{PWMI(on)}}{t_{PWMI(off)}}} - 1 \right]}{LN\left( \frac{V_{PWMI(L)}}{V_{PWMI(H)}} \right) \cdot \left[ V_{PWMI(L)} \cdot \left( \frac{V_{PWMI(L)}}{V_{PWMI(H)}} \right)^{\frac{t_{PWMI(on)}}{t_{PWMI(off)}}} - V_{PWMI(H)} \right]} \quad (1)$$

$$R_{PWMI} = \frac{t_{PWMI(off)}}{C_{PWMI} \cdot LN\left( \frac{V_{PWMI(H)}}{V_{PWMI(L)}} \right)} \quad (2)$$

Where; $t_{PWMI(on)}$ = the PWM on time

$t_{PWMI(off)}$ = the PWM off time

$R_{PWMI}$ = Resistor value connected to PWMI pin

$C_{PWMI}$ = Capacitor value connected to PWMI pin

$V_{PWMI(H)}$ = PWMI input high threshold (typical value from datasheet)

$V_{PWMI(L)}$ = PWMI input low threshold (typical value from datasheet) – PWMI is active when low

$I_{PWMI(on)}$ = Pull up current value when PWMI is active (typical value from datasheet);

defined as = $I_{IN\_SET}$ * 4 (typical)

In our example, we will assume a $R_{IN\_SET}$ value of 12KΩ, so $I_{IN\_SET}$ = 1.23V/12KΩ = 102.5µA;

Therefore $I_{IN\_SET} \cdot 4$ = 410µA = $I_{PWMI(on)}$.

Start with the desired duty cycle and frequency:

$$\text{Duty Cycle} = \frac{t_{PWMI(on)}}{t_{PWMI(on)} + t_{PWMI(off)}}$$ ; For example, say we want as close as possible to 50% duty cycle

$$\text{Frequency} = \frac{1}{t_{PWMI(on)} + t_{PWMI(off)}}$$ ; For example, say we want as close as possible to 400Hz.;

Where $t_{PWMI(on)}$ is the PWM on time and $t_{PWMI(off)}$ is the PWM off time.

50% duty cycle means the on and off times are equal: $t_{PWMI(on)} = t_{PWMI(off)} = 0.00125$sec.

Using equations (1) and (2), $C_{PWMI}$ = 253nF and $R_{PWMI}$ = 12185.3Ω as shown below:

$$C_{PWMI} = \frac{-0.000410 \cdot 0.00125 \cdot [(2/3)^1 - 1]}{LN(2/3) \cdot [\,2 \cdot (2/3)^1 - 3\,]} = \frac{-0.000410 \cdot 0.00125 \cdot (-0.3333)}{-0.405465 \cdot (-1.6667)} = \mathbf{253nF}$$

$$R_{PWMI} = \frac{0.00125}{253 \cdot 10^{-9} \cdot LN(3/2)} = \mathbf{12.185\ k\Omega}$$

The closest standard values are 270nF and 12 kΩ.

Now, using these closest standard values, let's see how close we are to our targets using equations (3) and (4):

$$t_{PWMI(off)} = R_{PWMI} \cdot C_{PWMI} \cdot LN\left(\frac{V_{PWMI(H)}}{V_{PWMI(L)}}\right) \quad (3)$$

$$t_{PWMI(on)} = -R_{PWMI} \cdot C_{PWMI} \cdot LN\left(\frac{V_{PWMI(H)} - I_{PWMI(on)} \cdot R_{PWMI}}{V_{PWMI(L)} - I_{PWMI(on)} \cdot R_{PWMI}}\right) \quad (4)$$

$t_{PWMI(off)} = 12000 \cdot 270 \cdot 10^{-9} \cdot LN\ (3/2) =$ **1.3137** milliseconds

$t_{PWMI(on)} = -12000 \cdot 270 \cdot 10^{-9} \cdot LN\ [(3-(0.000410 \cdot 12000))/((2-(0.000410 \cdot 12000))]$
$= -12000 \cdot 270 \cdot 10^{-9} \cdot LN\ [\,(-1.92 / -2.92)]$
$= -12000 \cdot 270 \cdot 10^{-9} \cdot -0.41926 =$ **1.3584** milliseconds

Actual duty cycle = 0.0013584 / (0.0013584+0.0013137) = **50.836%**

Actual frequency = 1 / (0.0013584+0.0013137) = **374.24Hz**.

*Note: The output power stages have an overtemperature current reduction feature, which will reduce the reference voltage, $V_{IN\_SET(ref)}$, and therefore the IN_SET current, $I_{IN\_SET}$. This in turn will lower the pullup current source, $I_{PWMI(on)}$ and increase the on time, $t_{PWMI(on)}$ . The off time, $t_{PWMI(off)}$ will remain the same. The result is that the duty cycle will go up when the overtemperature current reduction feature is active.*

### 3.2.8 DIS pin (TLD1311)

The block diagram for the DIS pin can be seen in Figure 28.

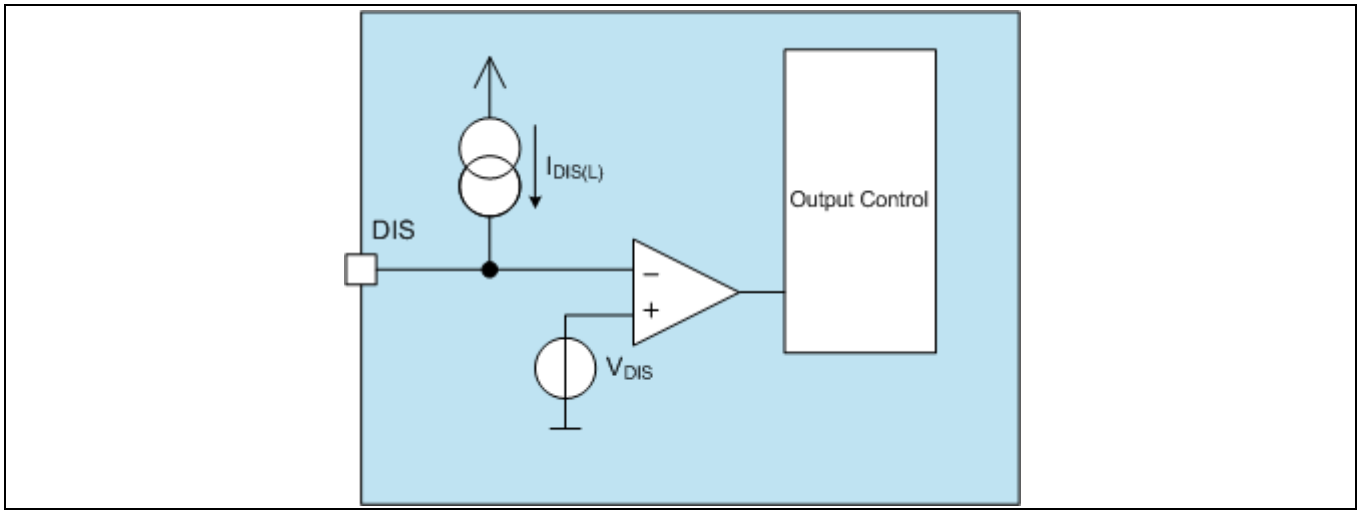



**Figure 28 Block diagram for the DIS pin**

The DIS pin is a single function pin;

- It is used as a DISABLE function, but can be used to PWM the device, if connected to a push-pull type output of a microcontroller or similar device. It can be used as a direct PWM input (low active) with a push-pull output of a microcontroller or similar device.

### 3.2.9 FB pin (TLD1326, 2326)

The block diagram for the FB pin can be seen in Figure 29.

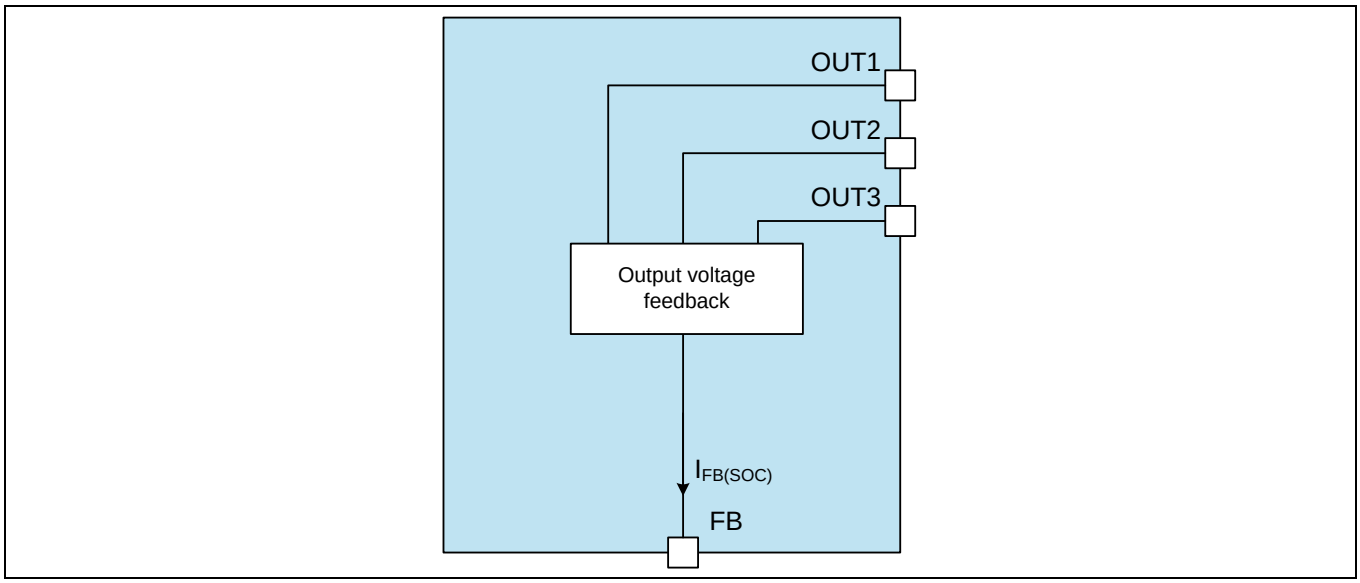



**Figure 29 Block diagram for the FB pin**

The FB pin is a single function pin;

- It is used in applications where a DC to DC converter provides the supply voltage to one or more LITIX™ Basic devices.
- It provides a voltage feedback to the external DC to DC converter to set the optimal supply voltage to the Basic device(s). This improves the overall efficiency of the system and lower overall power dissipation (since the voltage drop across the LITIX™ Basic device(s) power stages is minimized).
- The voltage feedback provided on this pin is the maximum output voltage of the 3 outputs of the given LITIX™ Basic device. This will allow adjustment based on the output with the highest number of LEDs in the chain or the output with the highest drop voltage, therefore requiring a higher supply voltage to maintain proper current control.

Application details using the FB pin are given in section 3.3.5.

### 3.2.10 Power Stages

The output power stages consist of 1 or 3 high side current sources.

- Maximum current per output is 120mA for 3 channel devices and 360mA for 1 channel devices. However, this maximum current is limited by the application's thermal resistance ($R_{thj-a}$, Thermal resistance, junction to ambient).
- Each output has a temperature dependent current reduction, which reduces the output current as the junction temperature exceeds the current reduction temperature threshold, $T_{j(CRT)}$. The output current is reduced by decreasing the internal IN_SET voltage reference, $V_{IN\_SET(ref)}$. See figure 30. This feature protects the device (and the LEDs if they are close to the device) from overtemperature. The current reduction protection eliminates possible flickering of the LEDs which could be seen with an immediate output shutdown approach. This current reduction is active only when the junction temperature is above $T_{j(CRT)}$ (140°C typ.). If the junction temperature decreases, then the output current will increase.
- The outputs may be connected in parallel to increase the current capability, however diagnostic capability will be lost on single input devices.

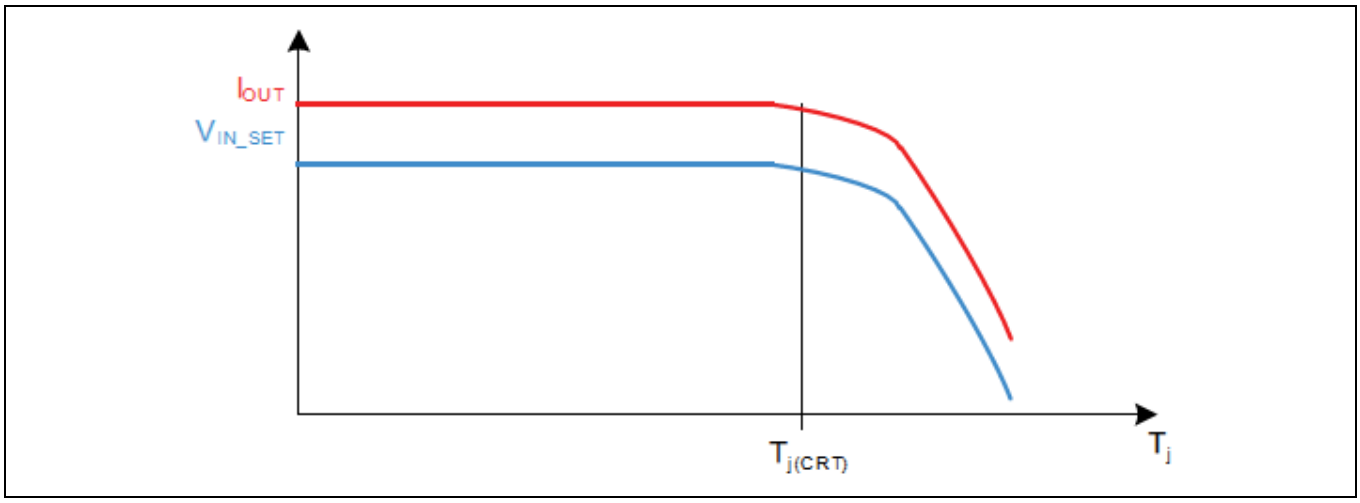



**Figure 30 Output current reduction at high junction temperature**

The control loop of the LITIX™ Basic devices depends on several conditions to maintain stability.

- The minimum supply voltage to maintain current control, specified by the datasheet parameter, $V_{S(CC)}$.
- The minimum voltage drop across the power stage, specified by the datasheet parameter, $V_{PS(CC)}$.
- The minimum output voltage needed for current control, specified by the datasheet parameter, $V_{OUTx(CC)}$.
- Conditions that do not meet the requirements of the 3 parameters above may result in output current being less than expected (not adequate voltage overhead for current drive or current control loop function). Oscillations may also occur.
- Also required is a minimum load current of approximately 10mA. See section 3.2.3 for an example of very low current settings and the output oscillations that can occur.

The main function of the power stages and control loop of the LITIX™ Basic family is to provide a stable, constant current to LED loads. This current should not vary with supply voltage (as long as the stability criteria previously described are met). A typical performance characteristic curve of output current vs. supply voltage is given in Figure 31. Here it can be seen that constant current control is not reached until the supply voltage provides adequate overhead to the power stages and control loop, in this case enough to overcome the forward voltage drop of 3 series LEDs.

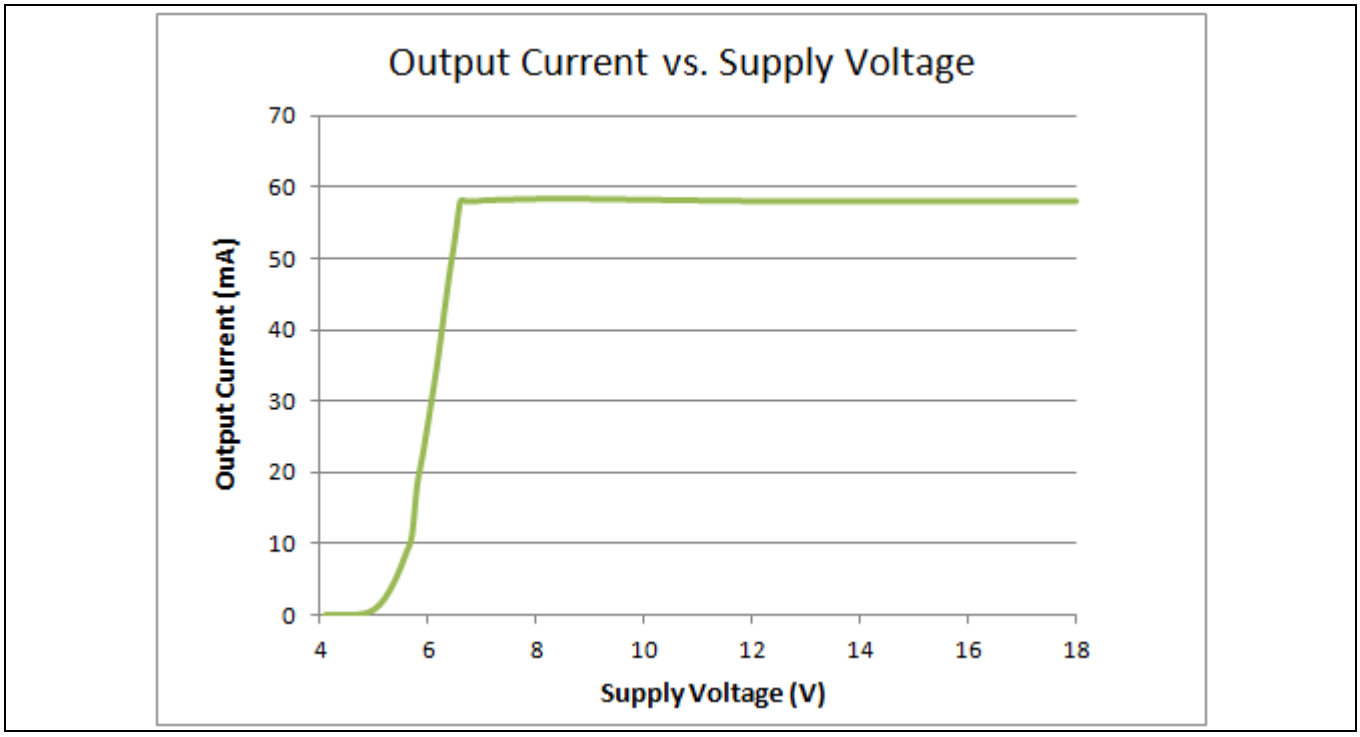



**Figure 31 Typical Device - Output current vs. Supply Voltage (RIN_SET = 13KΩ, Load = 3 series LEDs)**

### 3.2.11 Supply Pins

The supply pins of the LITIX™ Basic devices power the logic and output drivers of the device. It is important to bypass the supply pins with a capacitor to ground close to these supply pins. This is to avoid disruption of the control loop due to noise and inductivity from wiring on either the supply or output side of the power stages. A capacitor close to the Vs pins of each device should be included. Section 4.1.1.2 discusses how to size this capacitor.

Figure 32 shows a scope shot of an example of oscillation on the supply and outputs due to long wiring without a decoupling capacitor.

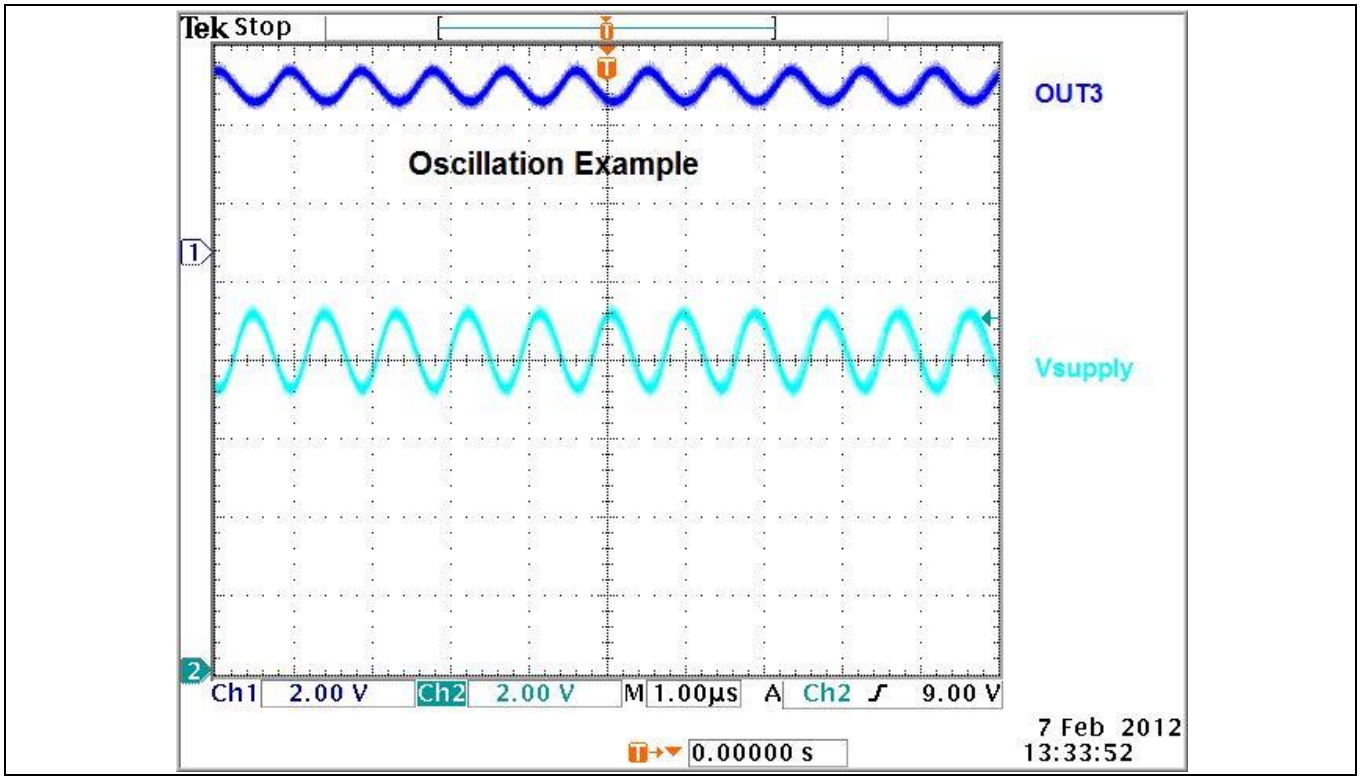



**Figure 32 Output and supply pin oscillation due to long wiring without decoupling capacitor**

## 3.3 Application Examples

The following sections discuss and show possible application circuits for some common applications of the LITIX™ Basic devices. These are certainly not the only solutions; and each circuit should be tailored and verified for each particular application.

### 3.3.1 N-1 Detection (TLD1311, 1315 and 1326)

The N-1 detection function is designed to be used in applications where multiple LED strings (and possibly multiple LITIX™ Basic devices) form a LED array. Many multiple LED string applications require that the all LED strings (entire light) be disabled when a single LED string fails; instead of operating with partial LED strings in a degraded mode. The N-1 function detects an open LED string and automatically disables the remaining outputs. The N-1 function can be viewed as a latched version of the open load detection.

As discussed in section 3.2.5, the N-1 pin is used to adjust the filter time, $t_{N-1}$ with a capacitor to ground. This filter time is the time after a fault occurs until the time the fault is reflected at either the IN_SET pin (if ST pin is grounded or not available) or the ST pin (if is open or connected with high ohmic resistor to ground).

The N-1 detection latches off the device outputs and can be reset by toggling (high then low then high) the EN or VS pin, which internally generates a power-on-reset. See Figure 33 for the fault timing example using the ST pin as the diagnostic signal (same as Figure 23).

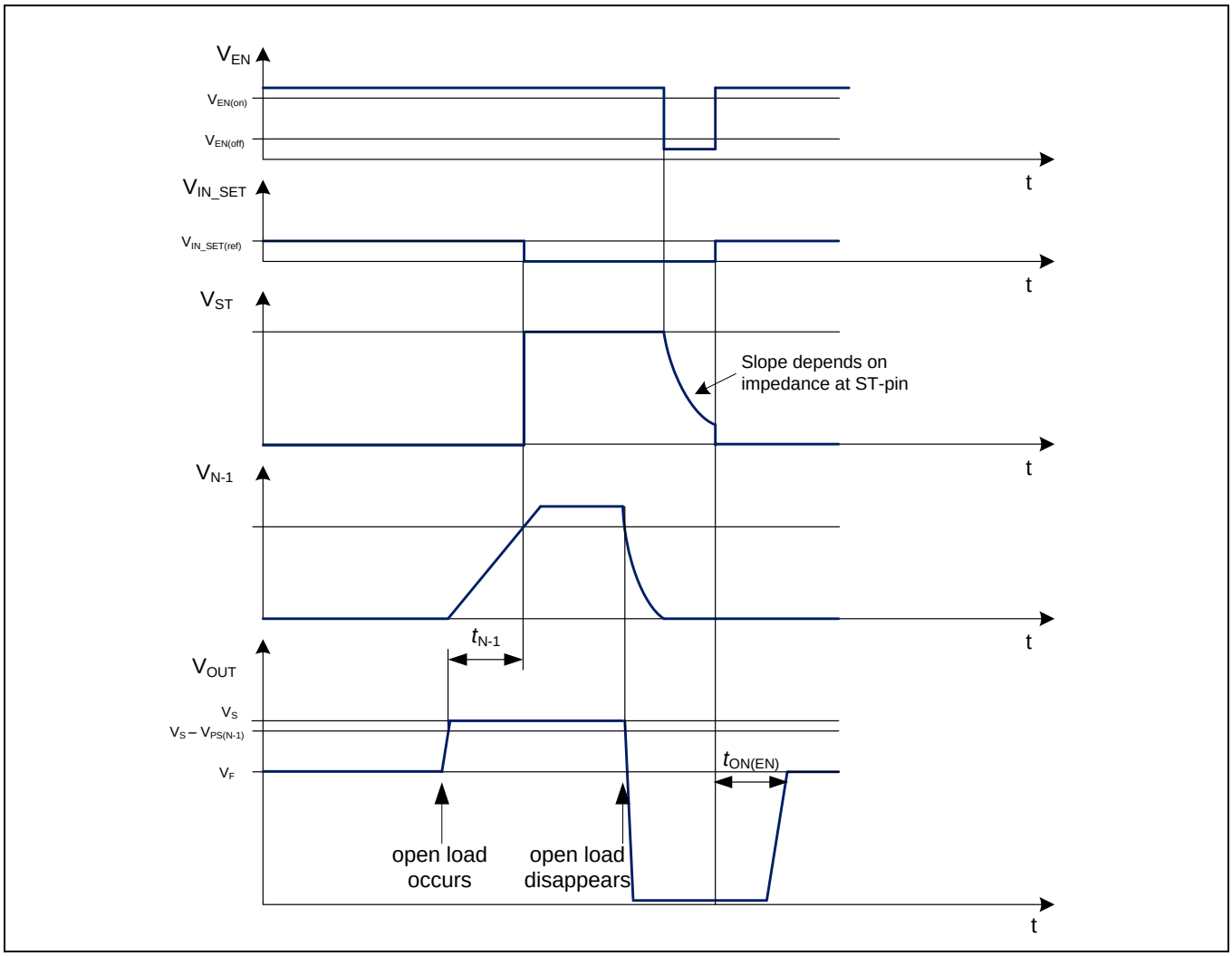



**Figure 33 Fault timing during open load (ST pin used for diagnostics)**

The ST pin also functions as a disable input if externally pulled high. Therefore, multiple devices could have their ST pins connected together and in case of a single LED string failure, the ST signal would be pulled high on all devices. By disabling all of the outputs in the LED array, an effective bulb outage failure can be detected upstream (e.g. by a body control module) supplying the LED module because the load current to the LED module would mimic an incandescent bulb outage .

See figure 34 below for an example application circuit where multiple LITIX™ Basic devices are used for a single light function. The ST pins are connected to provide the functionality previously described.

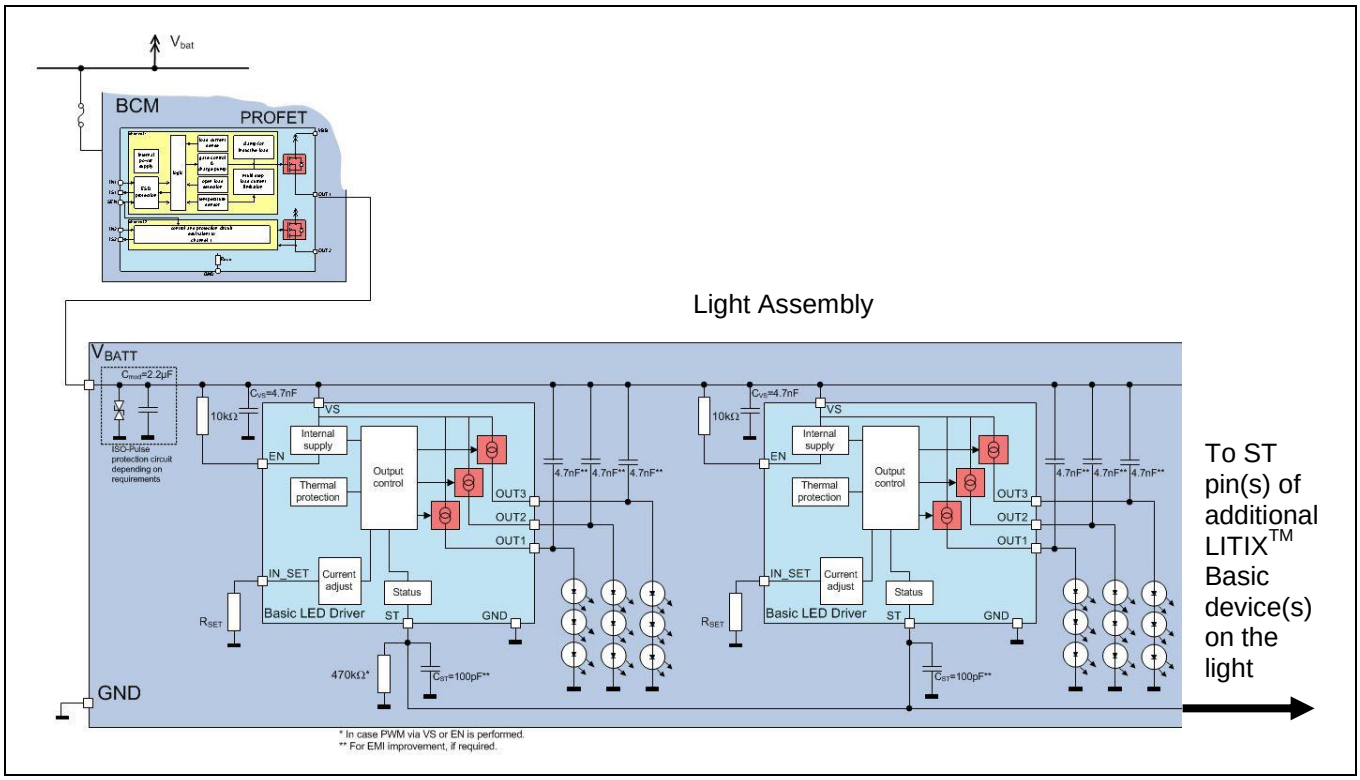



**Figure 34 N-1 detection Application Example Circuit (using ST pin)**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

During a slow ramp down of supply voltage, it is possible to generate a false diagnosis of open load, but unlikely, depending on the value of the N-1 capacitor. Typical values of N-1 capacitor (i.e. 100nF), provide much longer delay times (milliseconds for $t_{N-1}$) as compared to the open load detection delay (microseconds for $t_{OL}$). So typical decay of the supply voltage in the application will not cause an N-1 event.

This is seen since the device logic is still working but the device is not in constant current mode. The voltage drop between Vs and the output is below the open load detection voltage $V_{PS(OL)}$, for longer than the open load detection time, $t_{OL}$.

Figure 35 shows an example with a decay in the supply voltage over 500 milliseconds.

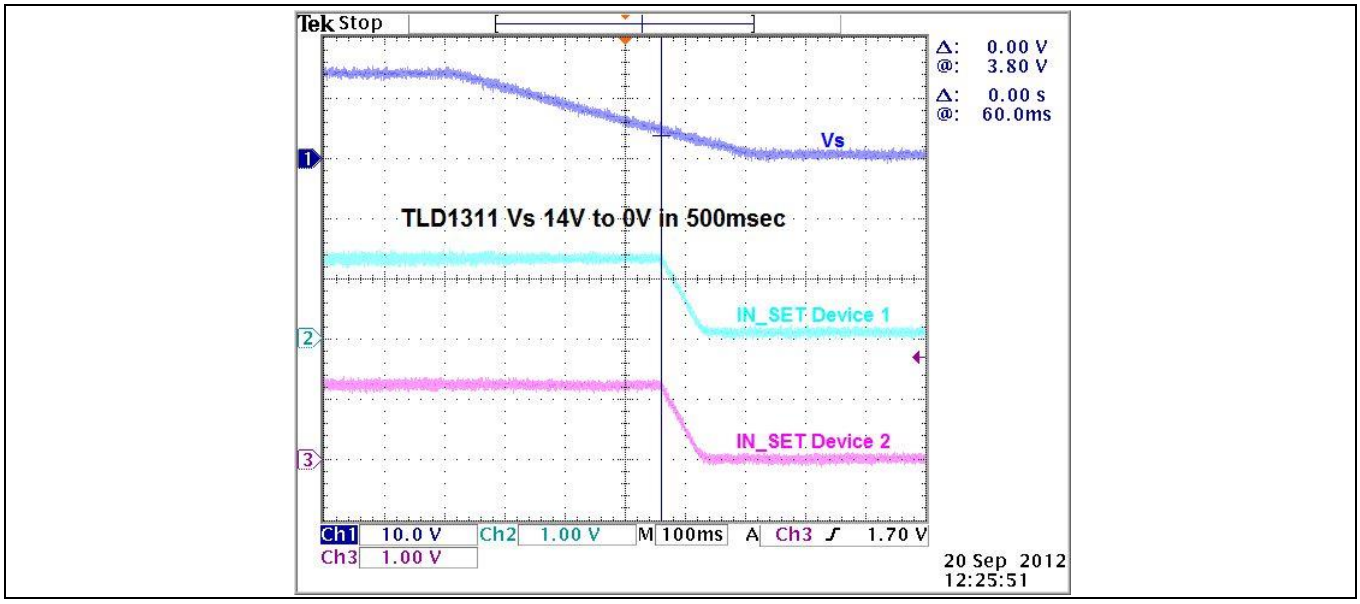



**Figure 35 500 millisecond supply voltage decay (TLD1311, IN_SET diagnosis)**

### Basic N-1 functionality for devices with ST pin

- ST pin on the affected device goes high with an open load on any output
- If the ST pins of the other devices are connected, then the high on the ST pin of the affected device turns off the other connected devices (ST disable function).
- An active-high ST signal will latch the devices off, therefore,a reset transition (low to high) is required via the EN or $V_S$ input to enable the devices again.
- If PWM is implemented as a PWM signal to either the EN or Vs pins, then the N-1 functionality will not be enabled, if the PWM frequency is above 1 / $t_{N-1}$. This is due to the continuous reset of the device(s) by the PWM signal on the EN or Vs pin, which would be faster than the N-1 filter time. So the fault is not indicated before the device is reset.

### N-1 Functionality for LITIX™ Basic devices without ST pin

The LITIX™ Basic device variant TLD1326 with the N-1 detection feature, but without the ST pin, can be used in the following way:

- For devices without ST pin, the diagnosis is reflected at the IN_SET pin, where the IN_SET voltage increases to $V_{IN\_SET(N-1)}$ after the N-1 filter time, should an open load occur on any output channel.
- The N-1 filter time is set with a capacitor to ground at the N-1 pin, as previously described.
- The IN_SET pin is diode OR connected with other LITIX™ Basic LED devices to the PWMI inputs of all devices as shown in Figure 36. When a fault occurs, the IN_SET pin goes high and also forces the PWMI of both devices HIGH and turns the outputs off.

- The N-1 diagnosis latches on (active-high). Once it is activated an external action is required to put the device into an active mode again (in this case a POR via the EN pin or $V_S$ is needed, which simply requires one of these pins to be taken low, then high).

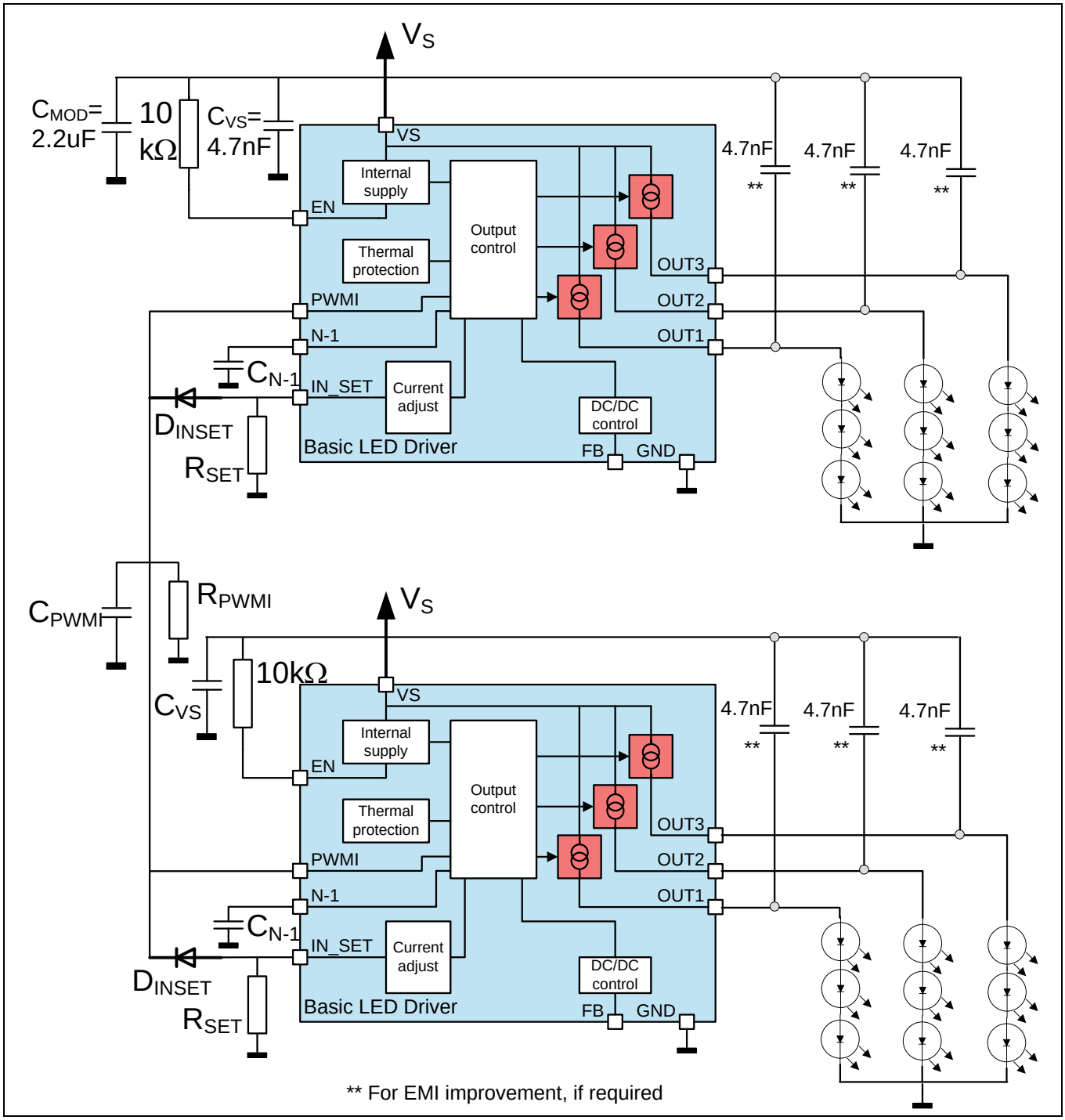
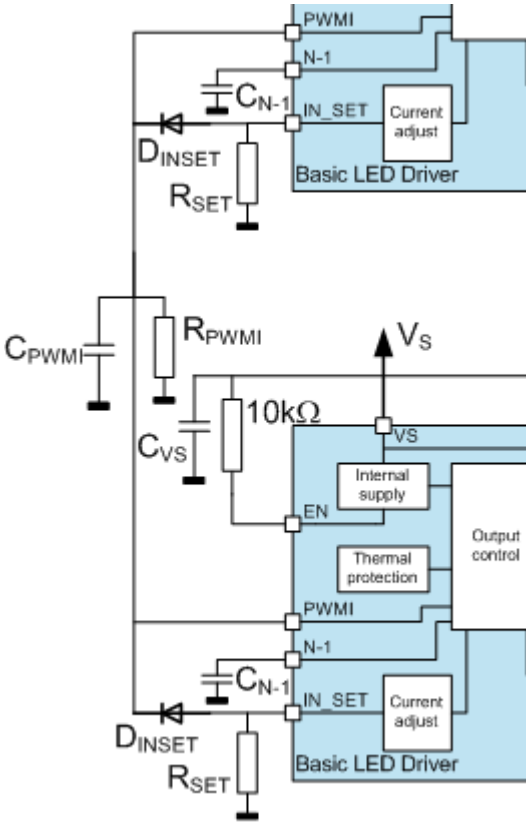



**Figure 36 N-1 detection Application Example Circuit (using IN_SET and PWMI pins)**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

**N-1 Detection – maximum number of devices, $n_{N-1}$**

The LITIX™ Basic device variants with the N-1 detection feature, will allow a maximum number of devices, $n_{N-1}$, as given by the following equations. For applications using the IN_SET and PWMI pins, details are shown below (TLD1315 and TLD1326).




$$n_{N-1} \le \frac{\left(I_{IN\_SET(OL,min)} - \frac{V_{PWMI(H,max)} + V_F}{R_{SET(min)}}\right) \cdot V_{PWMI(H,min)} \cdot R_{SET(min)}}{V_{PWMI(H,max)} \cdot 4 \cdot V_{IN\_SET(max)}}$$

Where:

$n_{N-1}$ = Maximum number of devices for N-1 detection;
$I_{IN\_SET(N-1,min)}$ = Minimum IN_SET N-1 current from datasheet;
$V_{PWMI(H,max)}$ = Maximum PWMI high threshold voltage from datasheet;
$R_{SET(min)}$ = Minimum value of $R_{SET}$ resistor;
$V_F$ = Voltage drop of diode between IN_SET and PWMI pins;
$V_{PWMI(H,min)}$ = Minimum PWMI high threshold voltage from datasheet;
$V_{IN\_SET(max)}$ = Maximum reference voltage from datasheet;

With the precondition of:

$$\frac{V_{PWMI(H,min)} \cdot V_{IN\_SET(min)} \cdot R_{SET(min)}}{(V_{IN\_SET(max)})^2 \cdot R_{SET(max)}} > 1$$

Example calculation for TLD1326EL:

$I_{IN\_SET(N-1,min)}$ = From datasheet – 3mA;
$V_{PWMI(H,max)}$ = From datasheet - 3.4V;
$R_{SET(min)}$ = 11880Ω; (12Kohm,1%)
$R_{SET(max)}$ = 12120Ω; (12Kohm,1%)
$V_F$ = 0.6V;
$V_{PWMI(H,min)}$ = From datasheet – 2.6V;
$V_{IN\_SET(min)}$ = Min.reference voltage from datasheet – 1.19V
$V_{IN\_SET(max)}$ = Max.reference voltage From datasheet – 1.27V

$$\frac{(0.003 - ((3.4 + 0.6)/11880)) \times 2.6 \times 11880}{3.4 \times 4 \times 1.27} = \frac{82.264}{17.27} = 4.76;$$

➔ **n < or = 4;**

Precondition is met:

$$\frac{3.4 \times 1.19 \times 11880}{1.27 \times 1.27 \times 12120} = 2.46.$$

So the calculation of the minimum and maximum values of $R_{PWMI}$ is as follows:

$$R_{PWMI(min)} = \frac{V_{PWMI(H,max)}}{I_{IN\_SET(OL,min)} - \frac{V_{PWMI(H,max)} + V_F}{R_{SET(max)}}}$$

$$R_{PWMI(max)} = \frac{V_{PWMI(H,min)}}{n_{N-1} \cdot 4 \cdot \frac{V_{IN\_SET(max)}}{R_{SET(min)}}}$$

For the TLD1326EL,

$$R_{PWMI(min)} = \frac{3.4}{0.003 - [(3.4 + 0.6)/12120]} = \mathbf{1273.4\ \Omega\ ;}$$

$$R_{PWMI(max)} = \frac{2.6}{4 \times 4 \times (1.27/11880)} = \mathbf{1520.1\ \Omega\ ;\ assuming\ } \boldsymbol{n_{N-1} = 4}$$

For applications using the IN_SET and DIS pins (TLD1311), the calculations are the same, substituting the PWMI pin parameters with the DIS pin parameters. The equations are given below.

$$n_{N-1} \le \frac{\left(I_{IN\_SET(OL,min)} - \frac{V_{DIS(H,max)} + V_F}{R_{SET(min)}}\right) \cdot V_{DIS(H,min)} \cdot R_{SET(min)}}{V_{DIS(H,max)} \cdot 4 \cdot V_{IN\_SET(max)}}$$

$$\frac{V_{DIS(H,min)} \cdot V_{IN\_SET(min)} \cdot R_{SET(min)}}{(V_{IN\_SET(max)})^2 \cdot R_{SET(max)}} > 1$$

$$R_{DIS(min)} = \frac{V_{DIS(H,max)}}{I_{IN\_SET(OL,min)} - \frac{V_{DIS(H,max)} + V_F}{R_{SET(max)}}}$$

$$R_{DIS(max)} = \frac{V_{DIS(H,min)}}{n_{N-1} \cdot 4 \cdot \frac{V_{IN\_SET(max)}}{R_{SET(min)}}}$$

### 3.3.2 Short Circuit to Ground Detection (TLD1121, 1124, 1125, 1313, 1314, 2311, 2314 and 2326)

The LITIX™ Basic family of devices has variants containing the Short Circuit to Ground Detection feature. This features operation will be discussed here.

- Short Circuit to Ground Detection
  - For single IN_SET pin devices (all except TLD2311, 2314 and 2326), if any output is turned on and the output voltage falls below the short circuit to ground voltage threshold, $V_{OUT(SC)}$, all outputs will be turned off after the short circuit detection time, $t_{(SC)}$.
  - For the TLD2311, 2314 and TLD2326, a short circuit on any output results in only the affected channel shutting down after $t_{(SC)}$.
  - The IN_SET or ST pin voltage will rise to the diagnostic voltage range of $V_{IN\_SET(OL/SC)}$ or $V_{ST(OL/SC)}$. This depends on the particular device and how the ST pin is connected.
  - The short circuit to ground diagnostic condition is not latched. The output will restart function after a short circuit is removed. The IN_SET or ST pin will transition to an unfaulted state after a delay of $t_{IN\_SET(reset)}$.
  - For multiple output devices with the ST pin, if it is used for diagnosis (ST pin is open or high ohmic resistor to ground), the device with turn off all 3 outputs during an open load (OL) or short circuit to ground (SC) condition. This is the disable feature of the ST pin. Regardless of how the ST pin is connected, either a pulldown current (no fault) or pullup current (fault present) will flow.
  - For devices with 1 input and 3 outputs, where the IN_SET pin is used for diagnosis (ST pin grounded), then all outputs will turn off during an OL or SC. This is the disable feature of the IN_SET pin.
  - In applications where PWM is performed via the VS pin and a short circuit to ground is present on the output, the output will turn on with each PWM cycle until the short circuit detection time is reached before turning off.

See Figures 37 and 38 for Short Circuit to Ground detection and recovery timing using the IN_SET or ST pins.

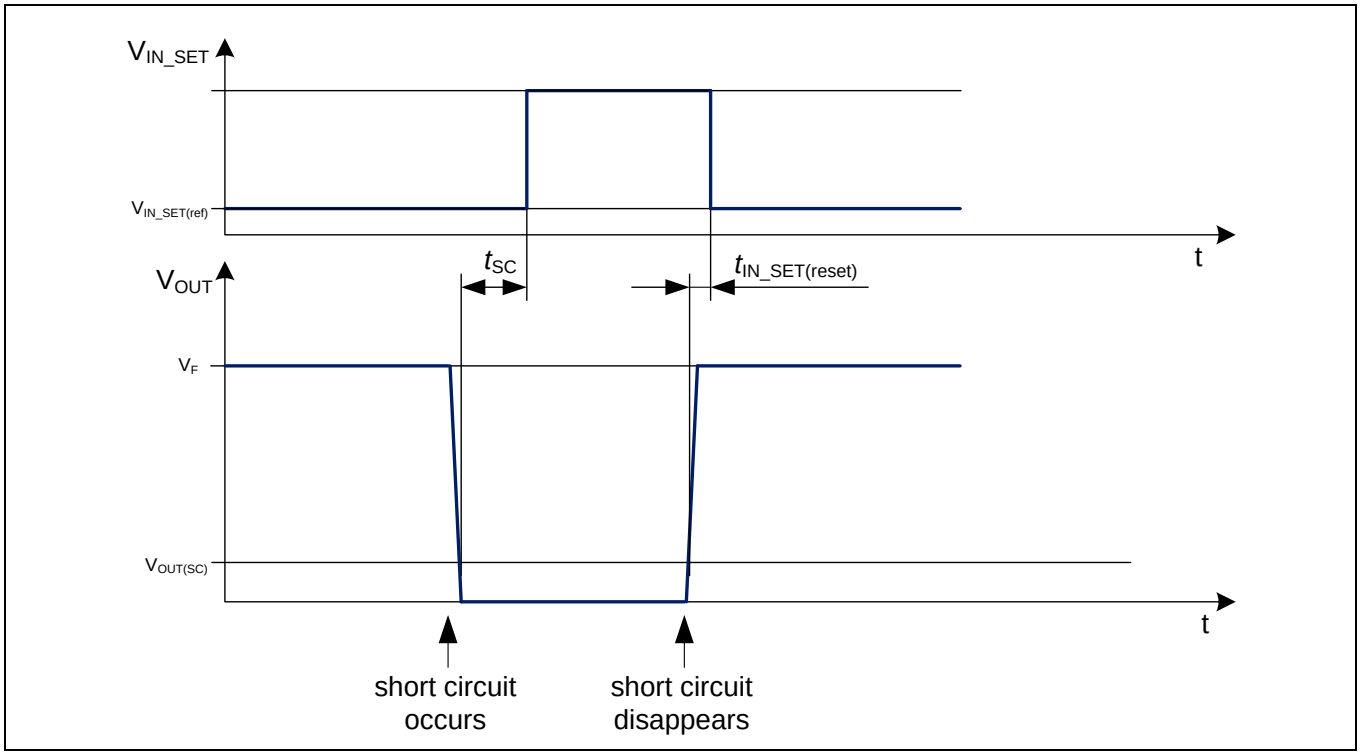



**Figure 37 Short Circuit to Ground detection and recovery timing (IN_SET pin diagnosis)**

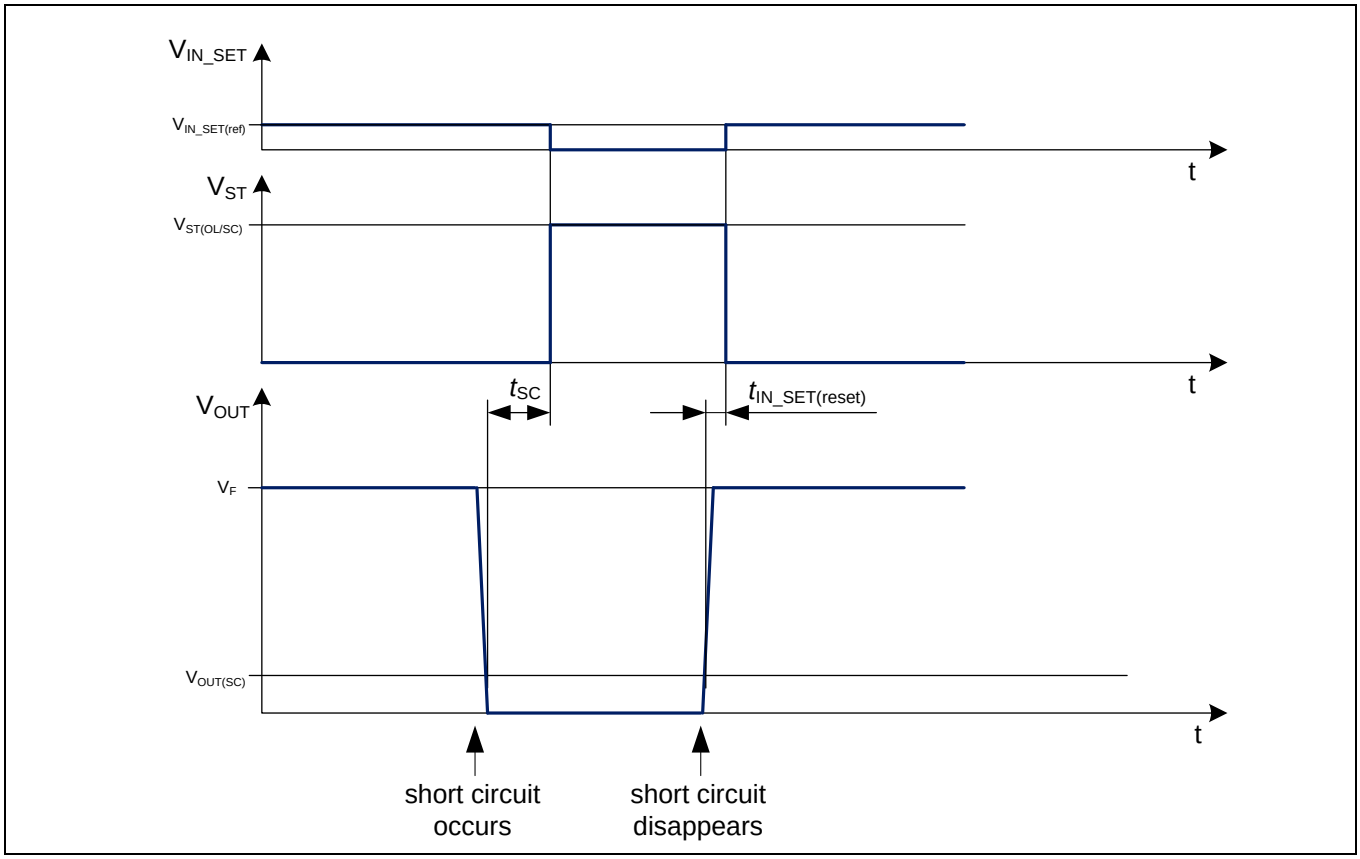



**Figure 38 Short Circuit to Ground and recovery timing (ST pin diagnosis)**

### 3.3.3 Open Load Detection (TLD1121, 1124, 1125, 1313, 1314, 2311, 2314 and 2326)

The LITIX™ Basic family of devices has variants containing the Open Load Detection feature. This features operation will be discussed here.

- Open Load Detection
  - For the devices with 3 IN_SET pins and Open Load detection (TLD2311, 2314 and 2326), if any output is turned on and the voltage across the power stage drops below the Open Load detection voltage threshold $V_{PS(OL)}$, only the affected outputs will be turned off after the open load detection time, $t_{(OL)}$.
  - For the devices with 1 IN_SET pin and Open Load detection (TLD1121, 1124, 1125, 1313 and 1314), if any output is turned on and the voltage across the power stage drops below the Open Load detection voltage threshold $V_{PS(OL)}$, all outputs will be turned off after the open load detection time, $t_{(OL)}$.
  - The IN_SET or ST pin voltage will rise to the diagnostic voltage range of $V_{IN\_SET(OL/SC)}$ or $V_{ST(OL/SC)}$. This depends on the particular device and how the ST pin is connected.
  - The diagnostic condition is not latched, the output will function normally again after the open load condition is removed. The IN_SET or ST pin will transition to an unfaulted state after a delay of $t_{IN\_SET(reset)}$.

See Figures 39 and 40 for Open Load detection and recovery timing using the IN_SET or ST pins. Figure 41 shows example scope shots for the open load diagnosis using the IN_SET pin.

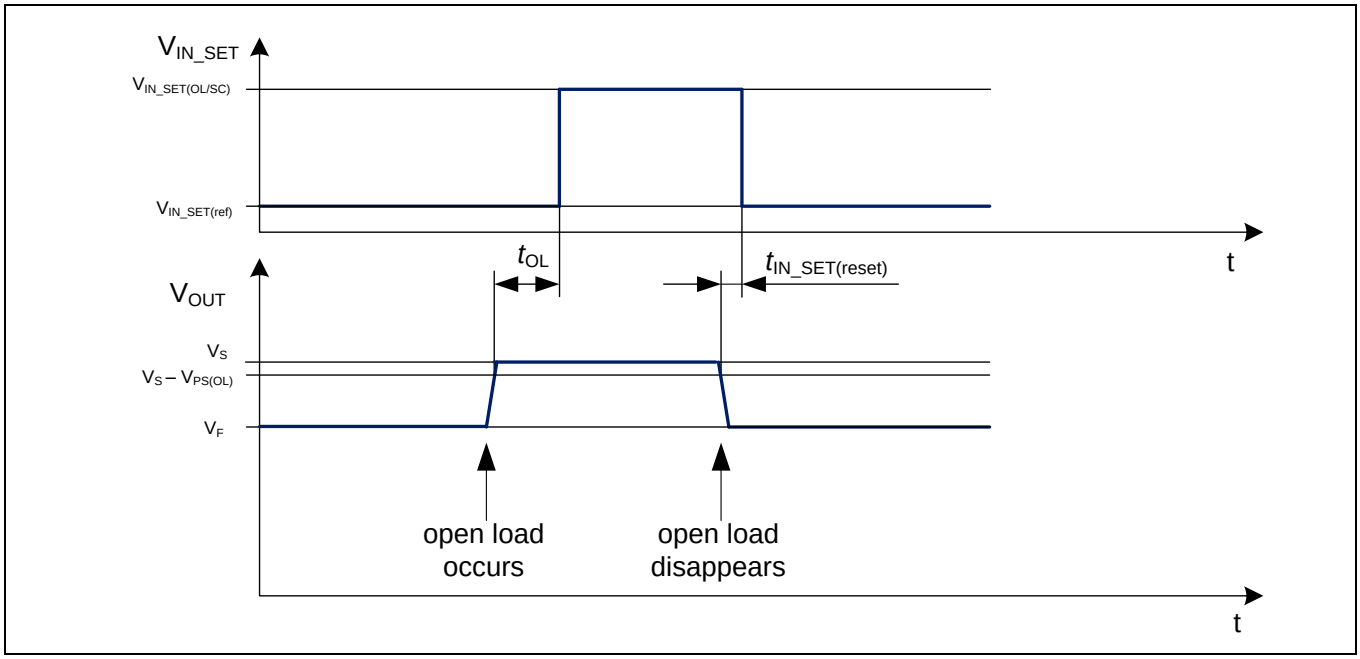



**Figure 39 Open Load Detection and recovery timing (IN_SET pin diagnosis)**

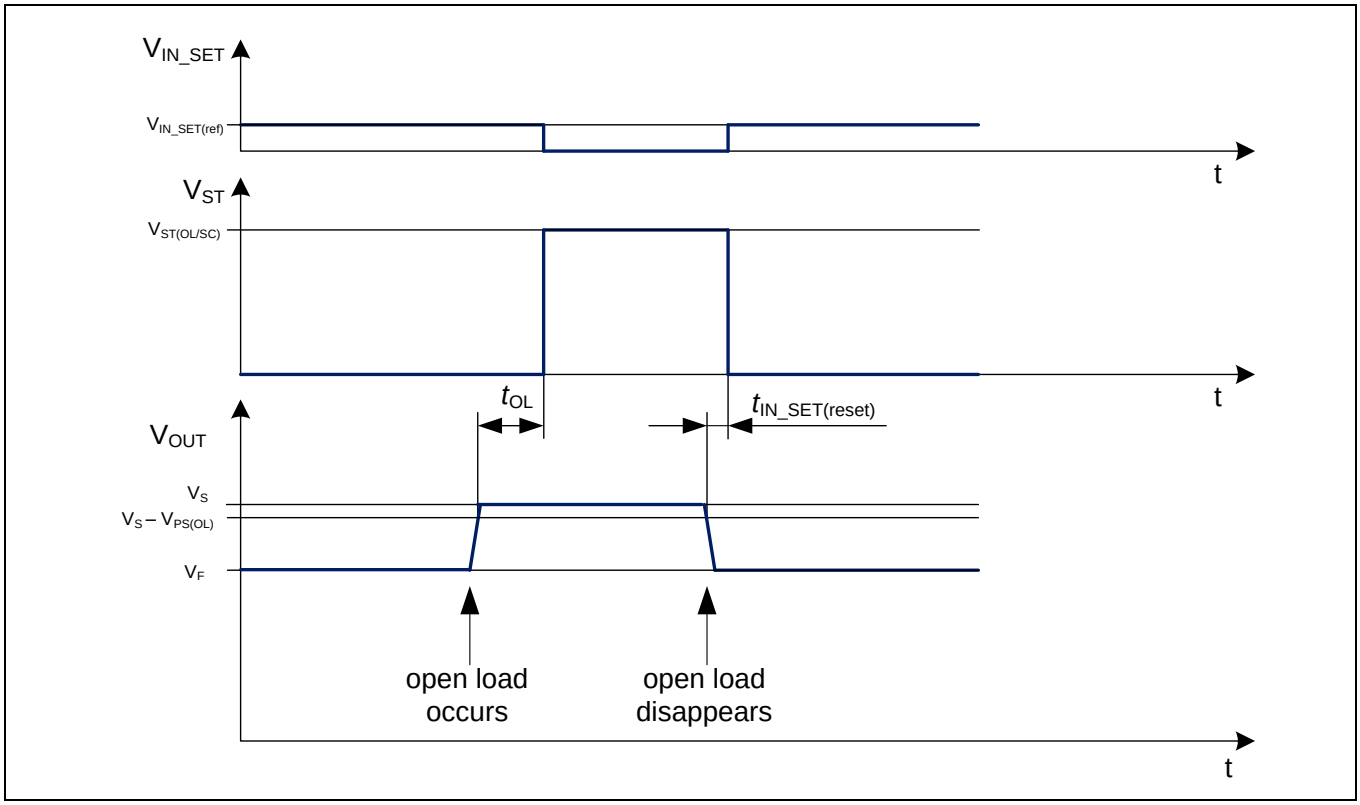



**Figure 40 Open Load Detection and recovery timing (ST pin diagnosis)**

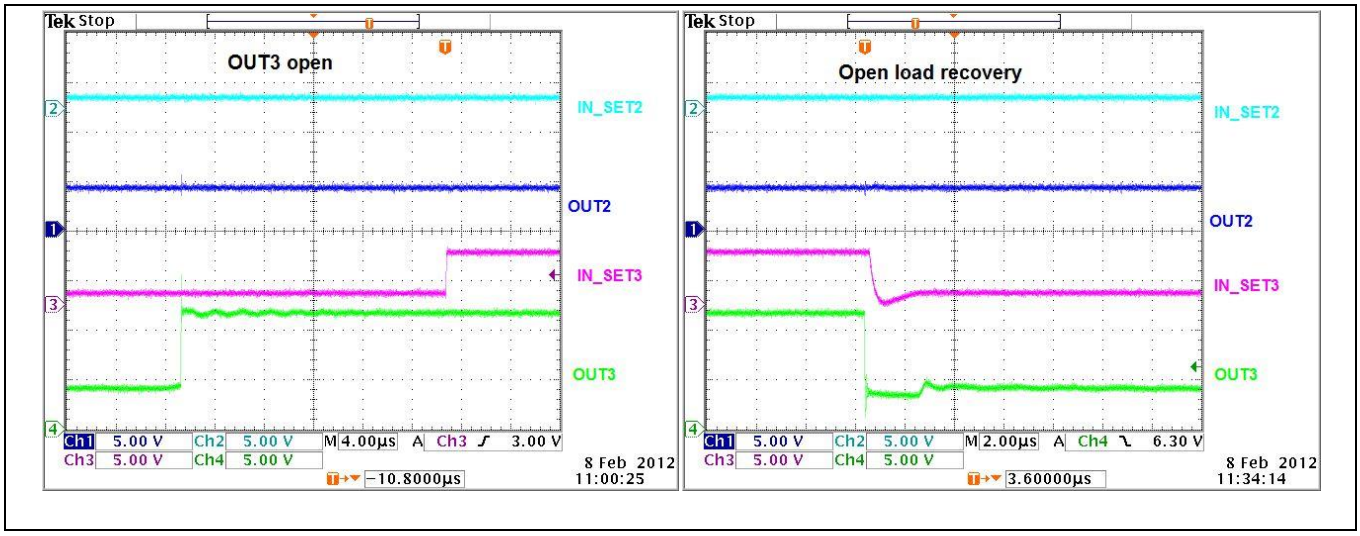



**Figure 41 Scope plots showing $t_{OL}$ delay and $t_{IN\_SET(RESET)}$ for open load (IN_SET diagnosis, TLD2326EL)**

During a slow ramp down of supply voltage, it is possible to generate a false diagnosis of open load, therefore giving a short indication on the ST pin. The example scope shots in Figure 42 illustrate this.

This is seen since the device logic is still working but the device is not in constant current mode. The voltage drop between Vs and the output is below the open load detection voltage $V_{PS(OL)}$, for longer than the open load detection time, $t_{OL}$.

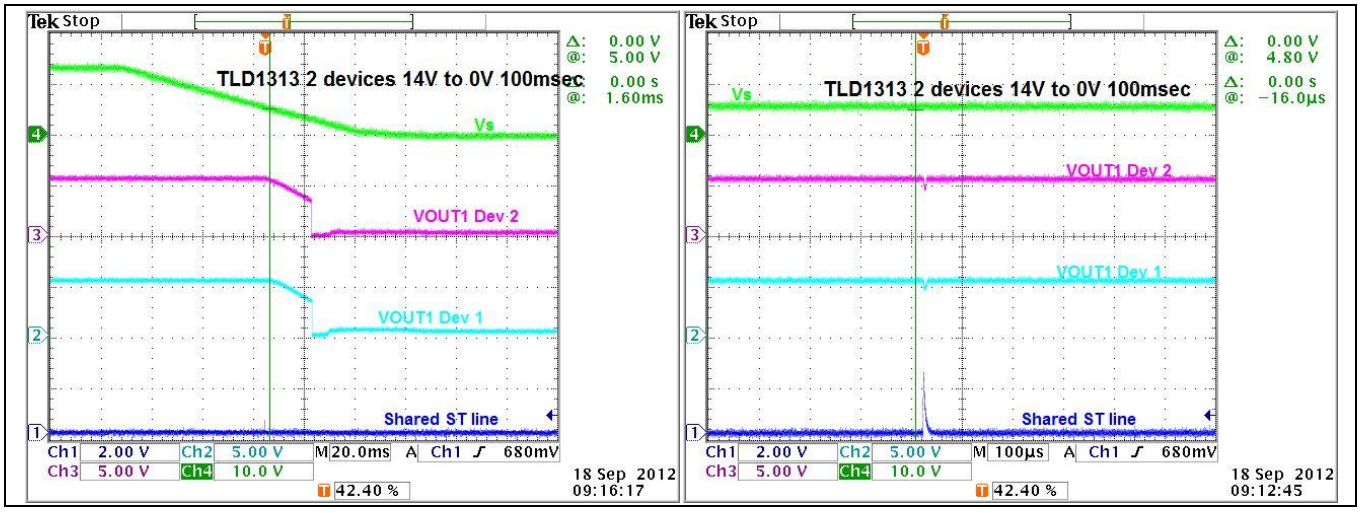



**Figure 42 Open Load indication during slow ramp down of Vs (ST pin diagnosis, TLD1313)**

Open Load and Short Circuit to Ground Detection Application Circuit (ST pin)

- Figure 43 shows a possible application circuit for diagnosing an OL or SC to ground fault. This example is for a device with an ST pin and an application which has a microcontroller available.
- If a microcontroller is not available in the application, the ST pin of each device can also be connected together to disable all devices in the application as in the N-1 detection case.
- The diagnostic condition for OL or SC to ground is not latched, the output will function normally again after the fault is removed. The ST pin will transition to an unfaulted state after a delay of $t_{IN\_SET(reset)}$ as shown in Figure 40.

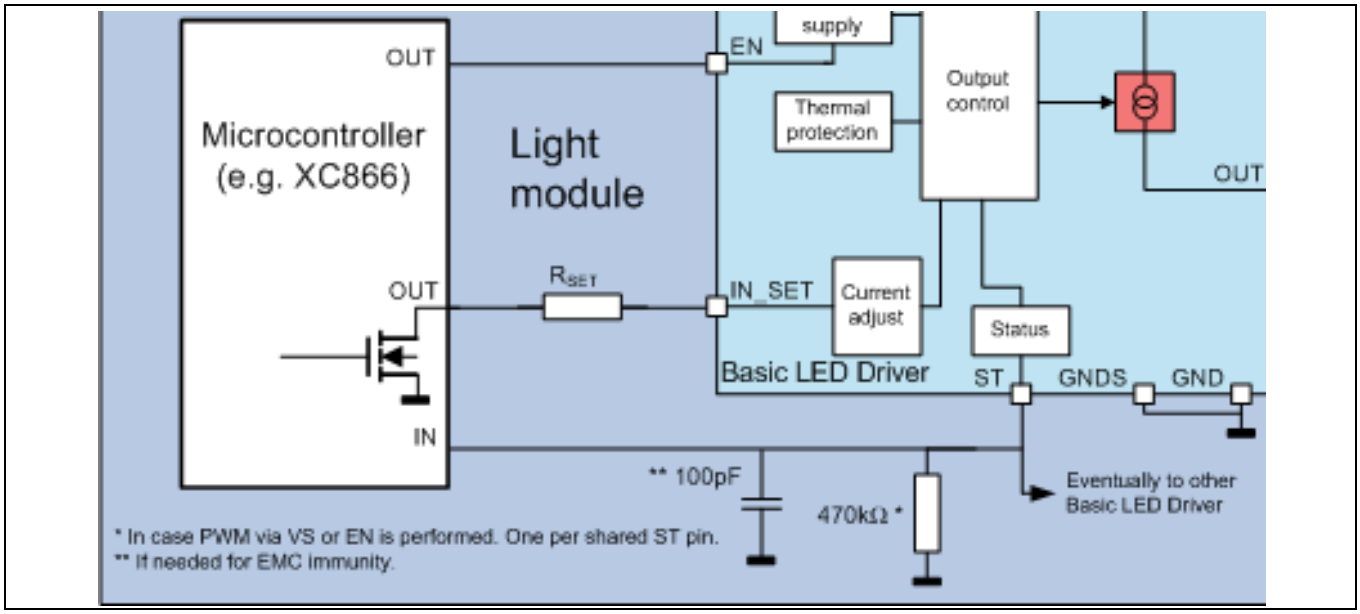



**Figure 43 Open Load and Short Circuit Detection Application Circuit (ST pin diagnosis)**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

Open Load and Short Circuit to Ground Detection Application Circuit (IN_SET pin)

- Figure 44 shows a possible application circuit for diagnosing an OL or SC to ground fault. This example is for a device where the IN_SET pin is used for diagnosis and the application has a microcontroller available.
- The open drain outputs of the micro set the current level via the RSET resistors (RSET is sum of the 2 resistors). The digital inputs of the micro sense the voltage between the 2 resistors to detect a fault.
- The diagnostic condition for OL or SC to ground is not latched, the output will function normally again after the fault is removed. The IN_SET pin will transition to an unfaulted state after a delay of $t_{IN\_SET(reset)}$ as shown in Figure 39.

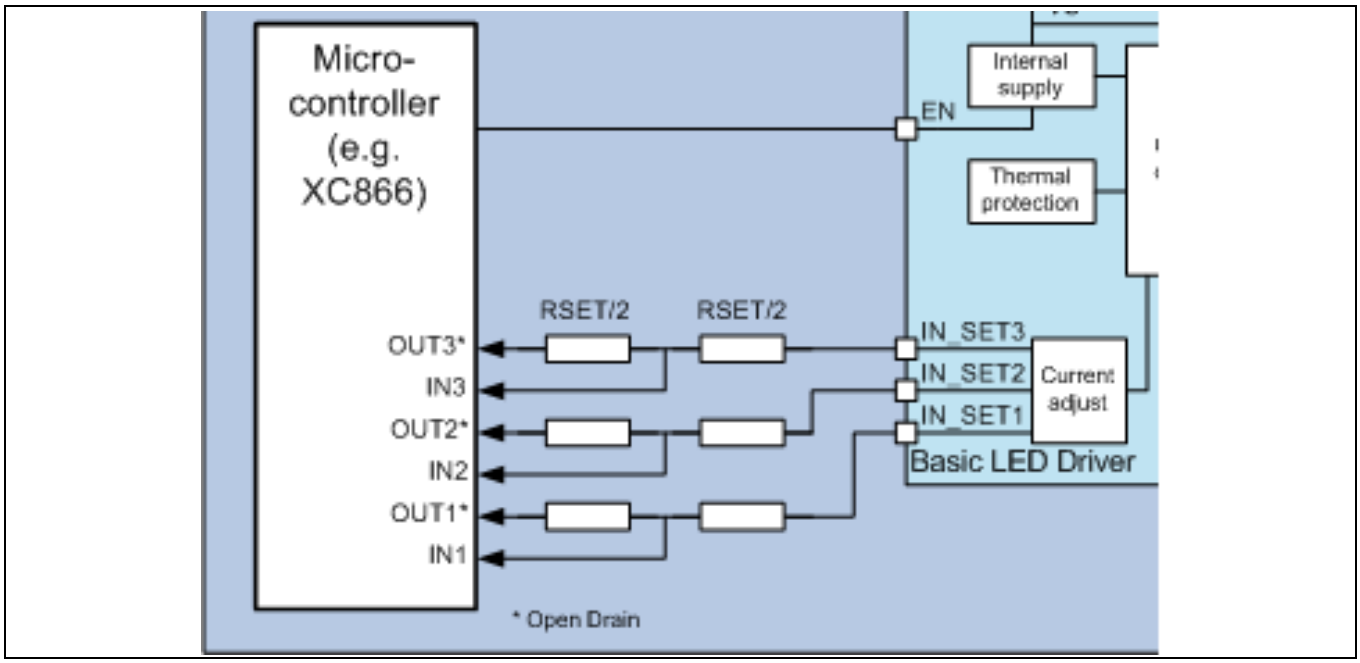


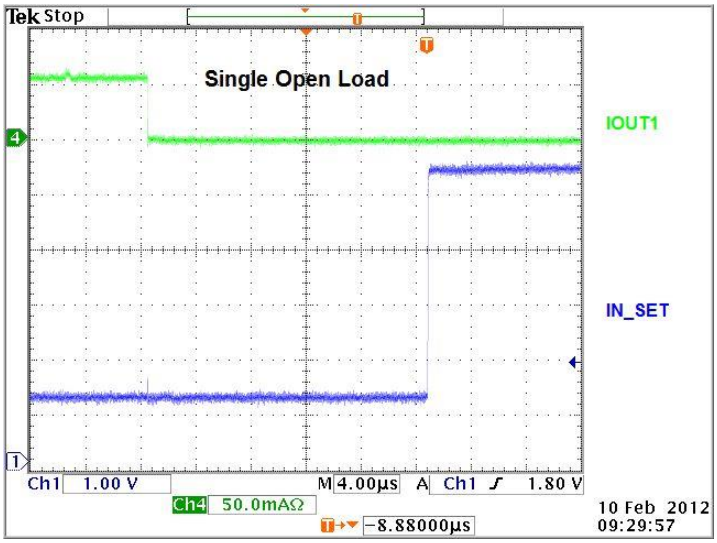

**Figure 44 Open Load and Short Circuit Detection Application Circuit (IN_SET pin diagnosis)**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

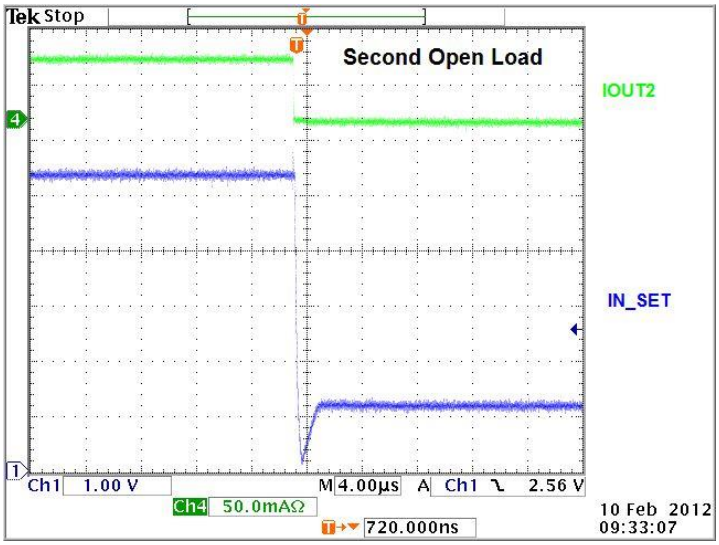
### 3.3.4 Double Fault Detection

**Double Fault Detection (Open load example)**

- The LITIX™ Basic devices have 2 ways of responding to the case where a double fault occurs, that is, when 2 channels are faulted on the same device. The way the device responds depends on each particular device and is stated on each device datasheet.
    - **Disable the diagnosis functions of the IN_SET pin**. This is to protect for false open load diagnosis during a low supply voltage or ramping voltage condition, in the operating range near the forward voltage of the connected LED strings. When the output is at or near the dropout voltage (where the supply voltage and LED forward voltage are nearly the same), this situation can occur. This case is illustrated in the scope shots below as Figure 45, where CH1 is first opened, then CH2 is opened showing that the IN_SET pin returns to a unfaulted state (the diagnosis feature of the IN_SET pin is disabled). This is implemented in the following devices with a single IN_SET pin (TLD1311, TLD1313, TLD1315 and TLD1326). The TLD1314 does not offer the double fault detection feature, because the diagnosis should be disabled at low supply voltages via the DEN pin.




CH1 Open load occurs, IN_SET diagnosis by rising to $V_{IN\_SET(OL/SC)}$

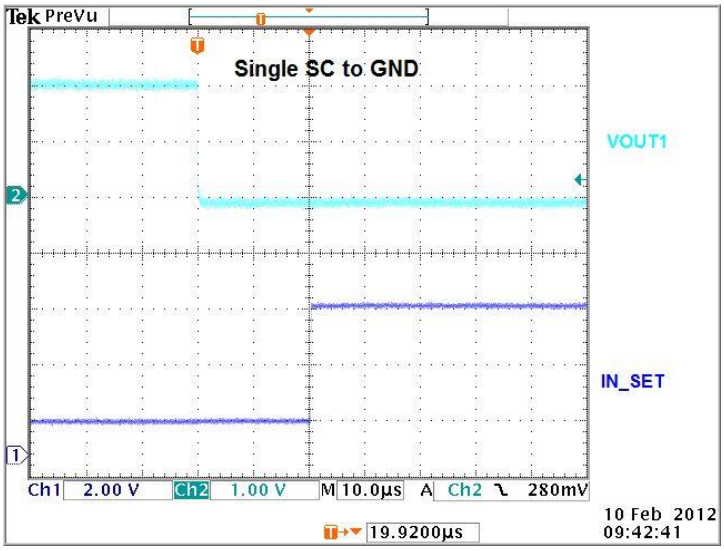



CH2 Open load occurs which is a Double Fault, diagnostics are disabled

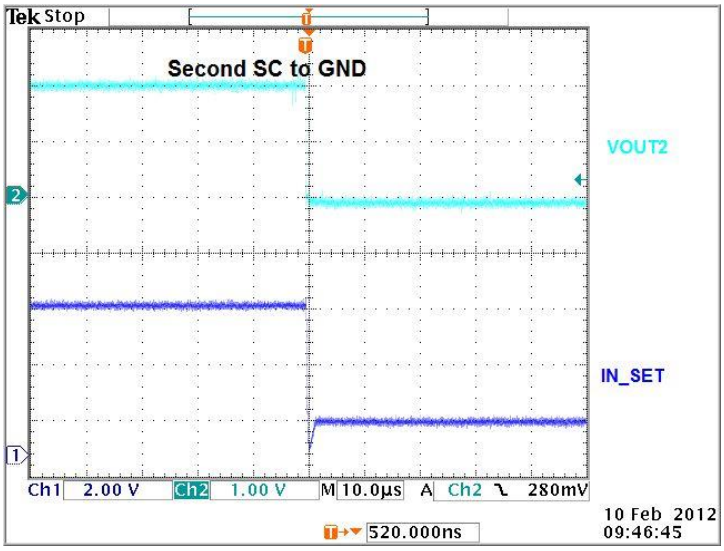
**Figure 45 Double Fault Detection – IN_SET diagnostics disabled (Open Load example)**

**Double Fault Detection (Short Circuit to Ground example)**

- The scope shots below as Figure 46 shows the case where the LITIX™ Basic will disable the diagnosis functions of the IN_SET pins due to short circuit to ground as a double fault.




CH1 SC to ground occurs, IN_SET diagnosis by rising to $V_{IN\_SET(OL/SC)}$




CH2 SC to ground occurs which is a Double Fault, diagnostics are disabled

**Figure 46 Double Fault Detection – IN_SET diagnostics disabled (Short Circuit to Ground example)**

- **Reflect the fault at the respective IN_SET pin**. The second way that the LITIX™ Basic can respond to more than 1 channel being faulted in a single device, is that the diagnosis is reflected at the respective IN_SET pin. This is done on the 3 IN_SET input devices (TLD2311, TLD2314 and TLD2326).

### 3.3.5 DC/DC control with FB pin

The LITIX™ Basic family of devices has variants containing a FB pin for external DC/DC converter control. This FB pin provides continuous output voltage feedback to an external DC/DC converter to ensure an optimal supply voltage to the LITIX™ Basic device.

- The purpose of the FB pin is to provide active control of the supply voltage provided by an external DC/DC converter to the LITIX™ Basic driver(s). This is to ensure the optimum amount of voltage overhead (voltage drop) between the supply pin of the LITIX™ Basic and the output voltage to the LEDs, which will vary with the number of LEDs, the drive current, temperature, etc. This ensures adequate overhead for proper current control of the LEDs, but at minimal power dissipation, improving overall system efficiency.
- The FB pin provides the maximum output voltage of the 3 outputs for the given LITIX™ Basic device. The block diagram for the FB pin is given in Figure 29.
- A possible application circuit using the FB pin for active voltage feedback in a boost to battery DC/DC configuration is shown in Figure 47. The calculation of the FB pin pulldown resistor $R_{FB(PD)}$ also follows.

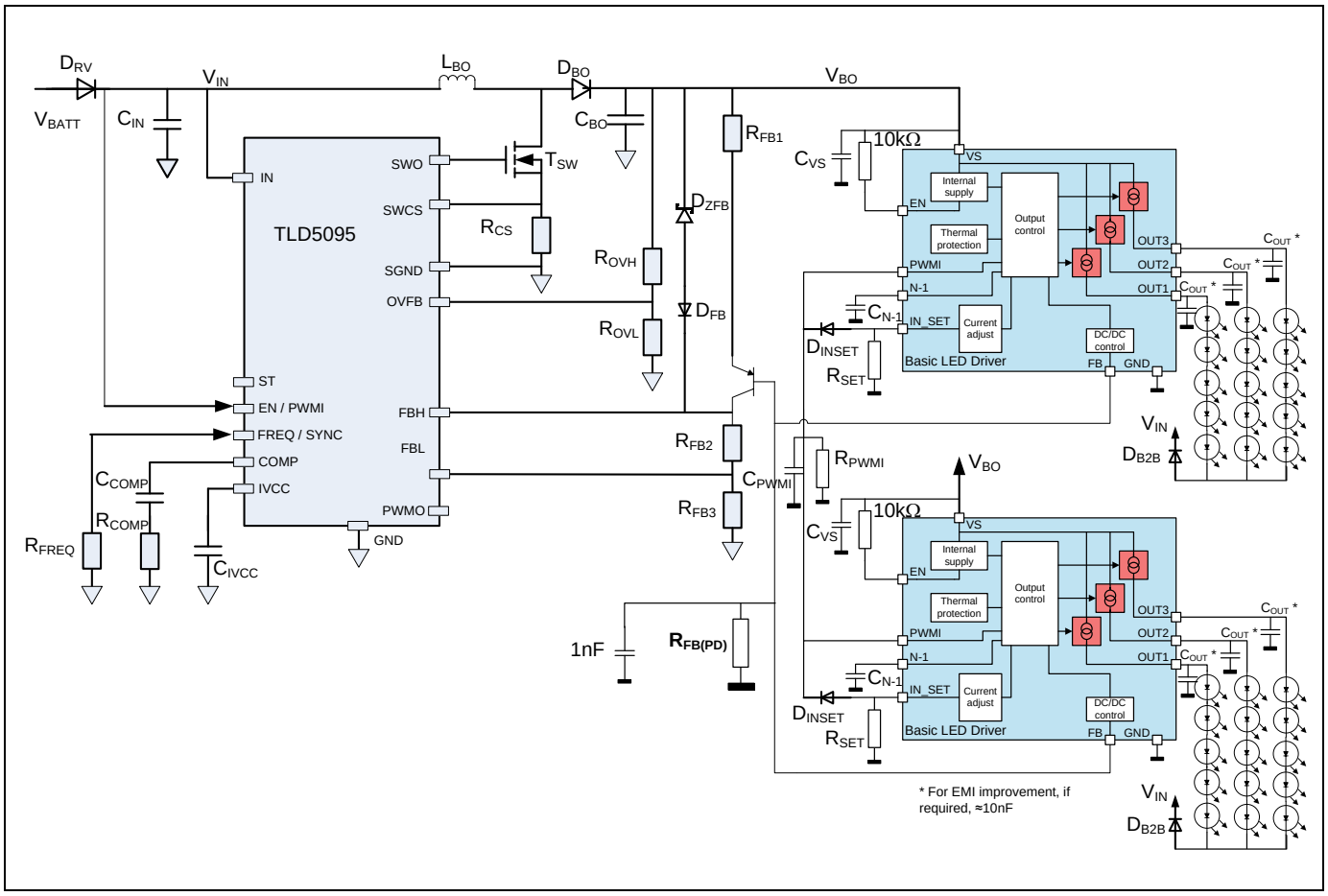



**Figure 47 DC/DC control using FB pin in Boost to Battery Application Circuit (TLD1326)**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

The resistor $R_{FB(PD)}$ connected from the FB pin to ground can be dimensioned by applying the equations below. The following parameters are required:

• $V_{OUT}$ - This represents the maximum LED load forward voltage, i.e. the number of LEDs multiplied by the maximum LED forward voltage. Temperature effects of the LED's forward voltage should be considered.
• $V_{BO}$ – This represents the DC/DC output voltage, which is defined by the feedback resistors ($R_{FB1}$, $R_{FB2}$, $R_{FB3}$). Please refer to the DC/DC device data sheet for the dimensioning of these resistors.
• $n_{len}$ – This represents the number of LITIX™ Basic Drivers using the longest LED-chains (e.g. if there are 3 devices connected to one DC/DC converter and two devices using LED chains with 7 LEDs and one device is used with LED chain length of 6 LEDs the according $n$len = 2.)
• $\beta$ represents the DC gain of the external bipolar transistor, which is connected to the DC/DC's feedback pins and is to be driven by the FB pins of the LITIX™ Basic devices.

$$R_{FB(PD,min)} = \min\left\{ \frac{V_{OUT} - 0.5\,V}{4 \cdot 10^{-5}\,A} \cdot \frac{1}{n_{len}}, \frac{V_{OUT} - 1.1\,V}{V_{BO} - V_{OUT} - 1.1\,V} \cdot \frac{1.7 \cdot 10^{5}\,\Omega}{n_{len}} \right\}$$

$$R_{FB(PD,max)} = \frac{V_{OUT} - 1.1\,V}{\frac{V_{BO} - V_{OUT}}{R_{FB1}} \cdot \frac{1}{\beta + 1}}$$

For example;

$V_{OUT}$ = 8 LEDs x 3.5V maximum forward voltage = 28V
$V_{BO}$ = 32V
$n_{len}$ = 3
$\beta$ = 100
$R_{FB1}$ = 4.7Kohm

$$R_{FB(PD,\,min)} = \min\left\{ \frac{28 - 0.5}{0.00004} \times \frac{1}{3}, \frac{28 - 1.1}{32 - 28 - 1.1} \times \frac{170000}{3} \right\} = \min\{ 229167, 525632 \} = 229.17\ k\Omega$$

$$R_{FB(PD,max)} = \frac{28 - 1.1}{\frac{(32 - 28)}{4700} \times \frac{1}{101}} = \frac{26.9}{8.426 \times 10^{-6}} = 3.19\ M\Omega$$

### 3.3.6 Internal PWM unit for brightness control

The LITIX™ Basic family of devices has members containing a PWMI pin and internal PWM unit. This internal PWM unit can be used to provide 2 level brightness control, with very little hardware or software overhead.

- The PWMI pin can be used as a discrete input where a logic signal from an external source (i.e. a microcontroller) controls the duty cycle of the outputs. The value and range of this output duty cycle is controlled by this external signal.
- By connecting the PWMI pin to an external parallel resistor and capacitor, the internal PWM unit is activated. See section 3.2.6 for an example calculation of the duty cycle and frequency.
- A possible application circuit using the PWMI pin for a 2 level brightness control application is shown in Figure 48. This particular example is for a brake and tail light application.

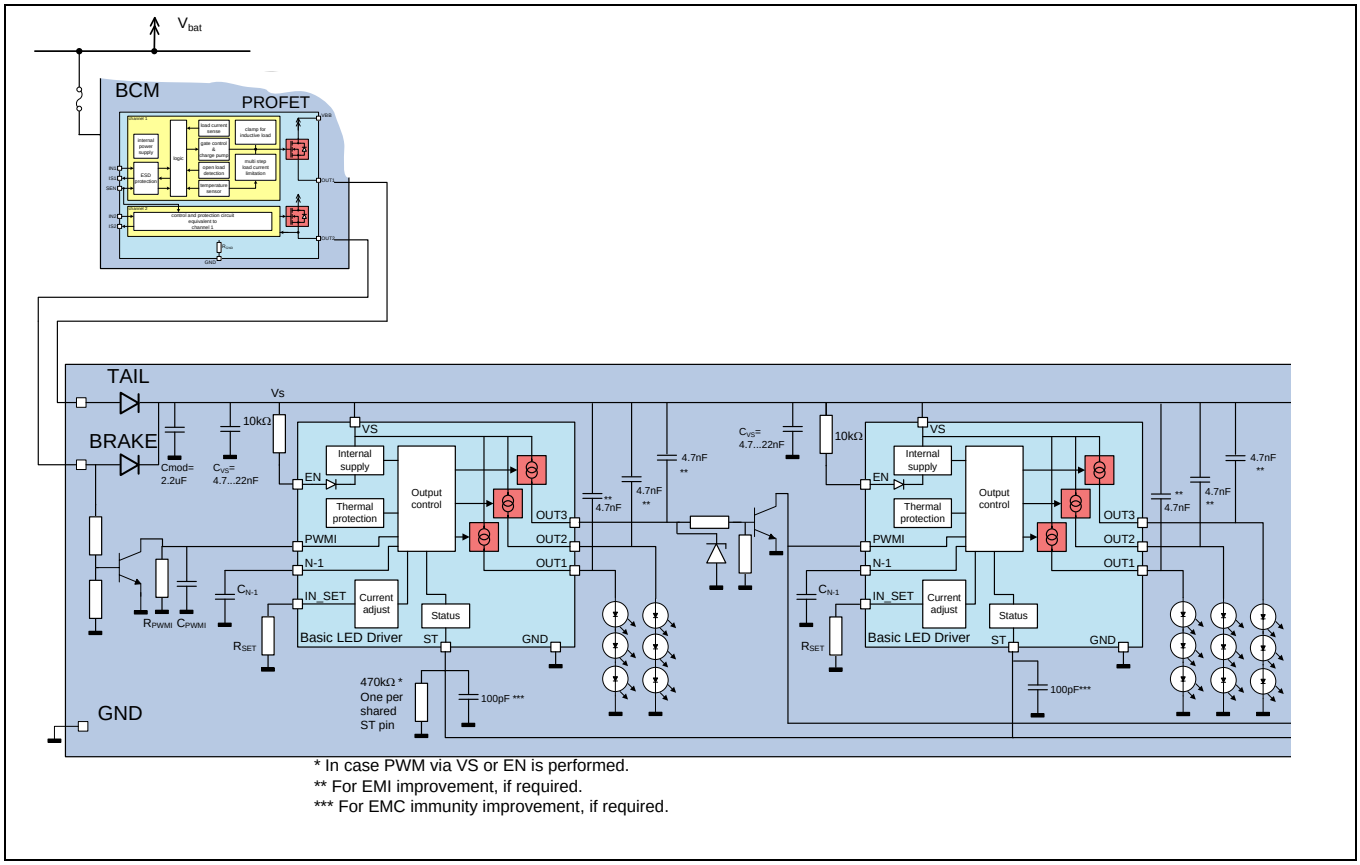



**Figure 48 Application Circuit using internal PWM unit to provide 2 level brightness control (TLD1315)**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

Explanation of application circuit operation using internal PWM unit to provide 2 level brightness control

- See Figure 49 for a diagram of the PWM unit external control circuitry.
- R1, R2: Provide bias point and ensures turn off of transistor T1 at Brake input signal.
- T1: Transistor to drive PWMI low (active) when Brake (100% duty cycle) is activated
- $R_{PWMI}$, $C_{PWMI}$ : Sets the duty cycle and frequency for internal PWM unit (see section 3.2.6 for example calculation)
- R3, R4: Provides bias point and ensures turn off of transistor T2 at OUT3.
- T2: Transistor to drive additional LITIX™ Basic PWMI pin(s) on additional devices.
- Brake off (duty cycle set by PWM unit)
  - Brake signal is 0V, so T1 is off. The LITIX™ Basic uses the internal PWM unit to generate a PWM signal on the outputs of a frequency and duty cycle determined by $R_{PWMI}$ and $C_{PWMI}$.
  - OUT3 drives base of T2, switching it on and off according to the signal at the PWMI signal described above.
- Brake on (duty cycle set to 100%)
  - Brake signal is at Vbat level, so T1 is on. This drives PWMI pin to low level, turning the outputs on at 100% duty cycle.
  - OUT3 is at 100% duty cycle, so T2 is on. This drives PWMI pin of the next LITIX™ Basic device(s) low, turning their outputs on at 100% duty cycle.

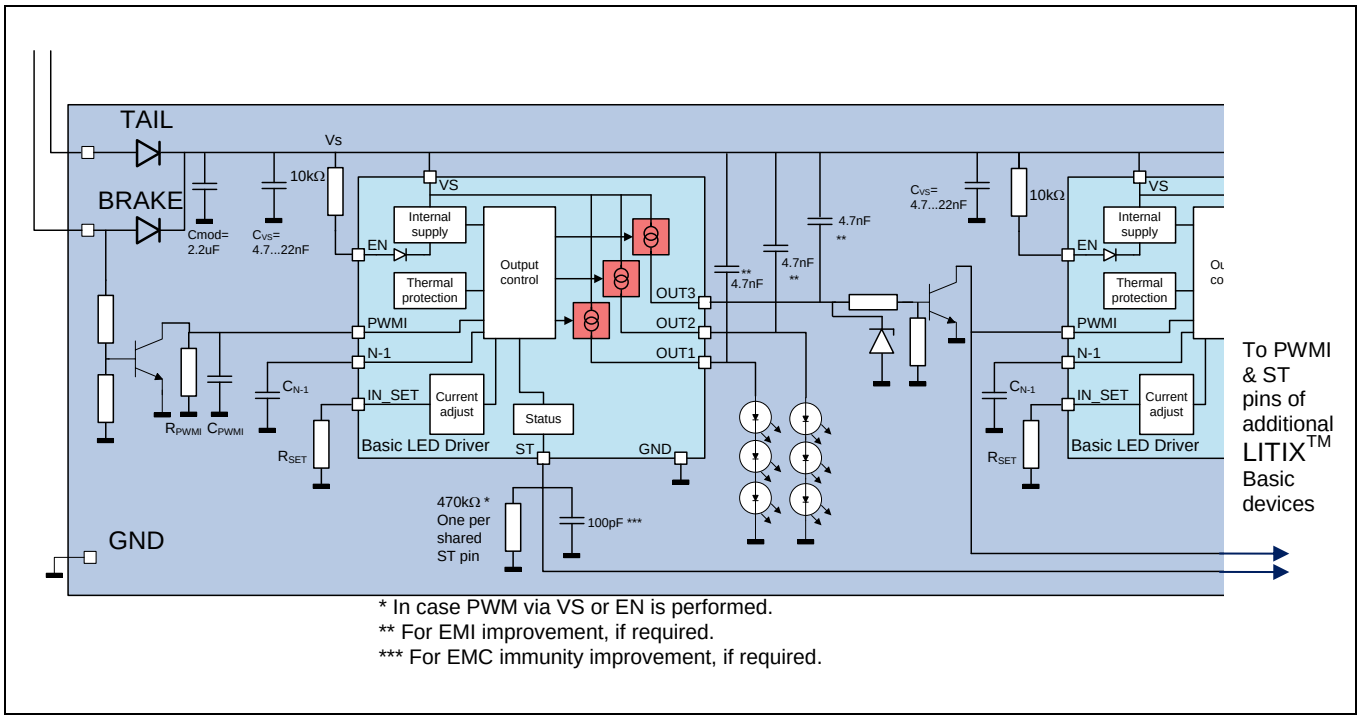



**Figure 49 Application Circuit – detail of PWM unit external circuitry (TLD1315)**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

### 3.3.7 Diagnostic Enable (DEN) pin application (TLD1124, 1314 and 2314)

The LITIX™ Basic family of devices has 3 members which have the DEN pin. The DEN pin in conjunction with a zener diode, can be used to disable the diagnosis output function below a specific supply voltage, during transients on the Vs supply or during Vs rampup.

When the supply voltage is near the output voltage (forward voltage drop of the LEDs, based on datasheet parameter $V_{PS(OL)}$ which is typically 300mV), an open load can be indicated if the supply voltage remains in this range beyond the OL detection filter time (parameter $t_{OL}$, min. of 10usec.). The DEN feature allows the disabling of the diagnosis to avoid false indications during these scenarios. Also see section 3.3.3.

A possible application circuit is shown in Figure 50. Since the sum of the zener voltage ($V_Z$) and the thresholds of the DEN pin ($V_{DEN(act)}$, $V_{DEN(dis)}$) determine the diagnosis range, the zener diode voltage can be adjusted to fit the specific application range of operation requirements.

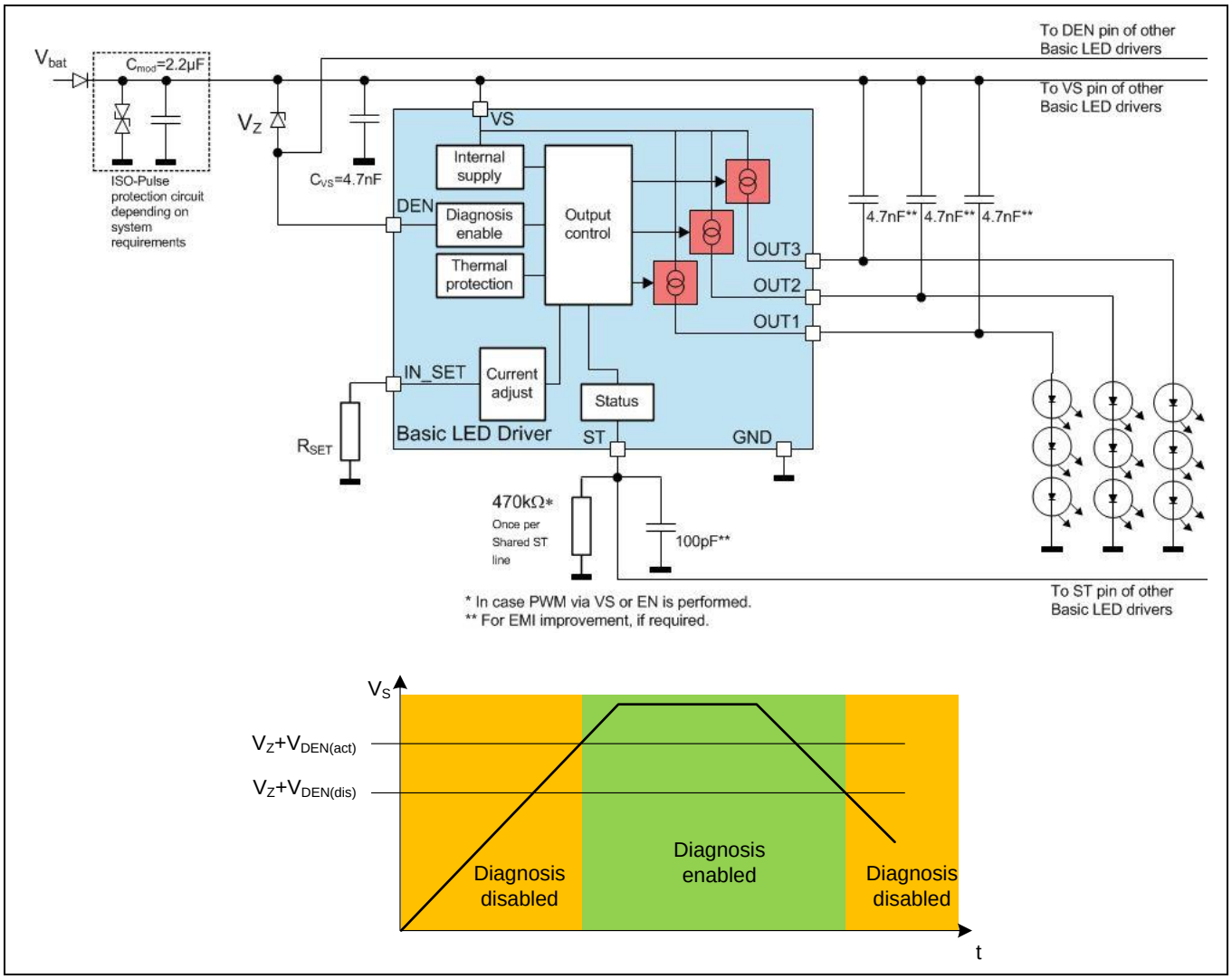



**Figure 50 Application Circuit using zener diode and diagnosis enable (DEN) feature, resulting diagnosis voltage range (TLD1314)**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

The DEN pin can also be activated directly by a microcontroller, by providing a voltage above $V_{DEN(act)}$ to enable diagnosis and a voltage below $V_{DEN(dis)}$ to disable diagnosis.

# 4 Design recommendations

## 4.1 Introduction

The following recommendations are based on observed and predicted behavior based on experiences in testing and customer applications. Every application is different. These recommendations should apply in the vast majority of cases.

### 4.1.1 PCB (Printed Circuit Board) Recommendations

#### 4.1.1.1 IN_SET pin(s)

Capacitance at the IN_SET pin(s) should be minimized in order to maintain good phase margin; and therefore stability of the control loop. So capacitors should not be placed on the IN_SET pins. In general, applications with higher output currents (lower IN_SET resistor values) can tolerate more stray capacitance, but the maximum capacitance below should not be exceeded to ensure adequate margin:

- 120mA channel output current: 70pF
- 60mA channel output current: 40pF
- 30mA channel output current: 20pF

In order to reduce excessive parasitic capacitance at the IN_SET pin(s), the following recommendations are given:

- Place the IN_SET resistor(s) as close as possible to their respective IN_SET pin(s).
- Keep ground connection of IN_SET resistors as short as possible back to the PCB ground plane.

Both of the recommendations above help reduce parasitic capacitance at the IN_SET pins.

Excessive parasitic capacitance at the IN_SET pin can reduce the phase margin of the control loop and lead to instability and oscillation.

In order to reduce crosstalk and noise coupling between the Vs/EN and IN_SET pin(s), the following recommendations are given:

- Isolate the traces of the Vs/EN pins relative to the IN_SET pin traces. Avoid running the traces for Vs/EN close to the IN_SET traces, either side by side or adjacent on opposite sides of the PCB.

This is to avoid potential crosstalk of noise which could affect the current setting of the control loop. Often the Vs/EN signals are pulse width modulated, so noise could be coupled to the IN_SET pins if the traces are not isolated. The Vs pin is also subject to significant externally generated transient pulses.

**Background**:

Noise can be coupled either through capacitive (electric field mechanism) or inductive (magnetic field mechanism) means, although capacitive coupling is more common on PCBs. Either mechanism can be activated if the noise producing and victim traces are in close proximity (either side by side on the PCB or on top of each other on opposite sides of the PCB). To reduce the chance of this coupling, if traces are kept as short as possible and known noise producing and victim traces separated as much as possible or crossed only at right angles to each other, coupled noise problems can be avoided. See figure 51.

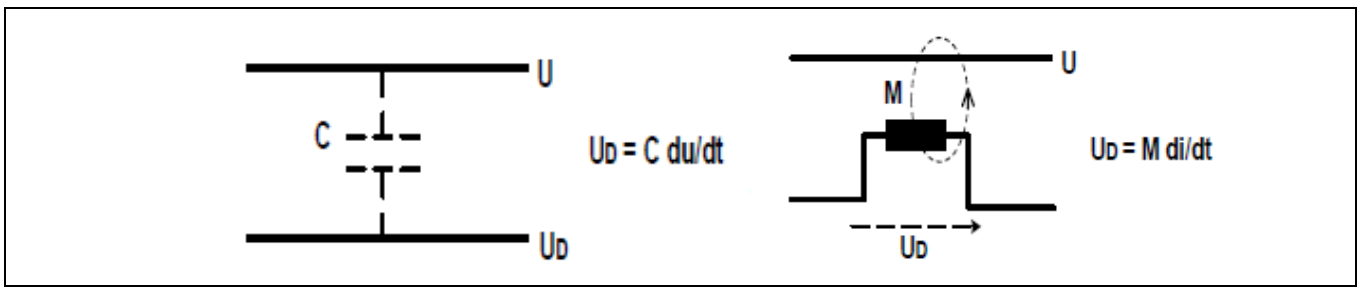



**Figure 51 Capacitive (Electric Field) and Inductive (Magnetic Field) Noise Coupling (Figures courtesy of Infineon® Application Note V 2.0, April 2001, AP 2426 "EMC Design Guideline for Microcontroller Board Layout")**

### 4.1.1.2 Vs pin (Supply pin)

A local decoupling capacitor to ground in the range 4.7nF to 22nF should be placed as close as possible to the Vs pins of the IC (a capacitor at each ICs Vs pin in case multiple ICs are used on the same PCB). See $C_{vs}$ below in figure 52.

The decoupling capacitor is needed to avoid disruption of the control loop due to noise and inductivity from wiring on either the supply or output side of the power stages. Both the connection to the IC pin and the connection to the ground plane should be as short as possible. See figure 32 for a measurement example of an application without a decoupling capacitor on the Vs pins.

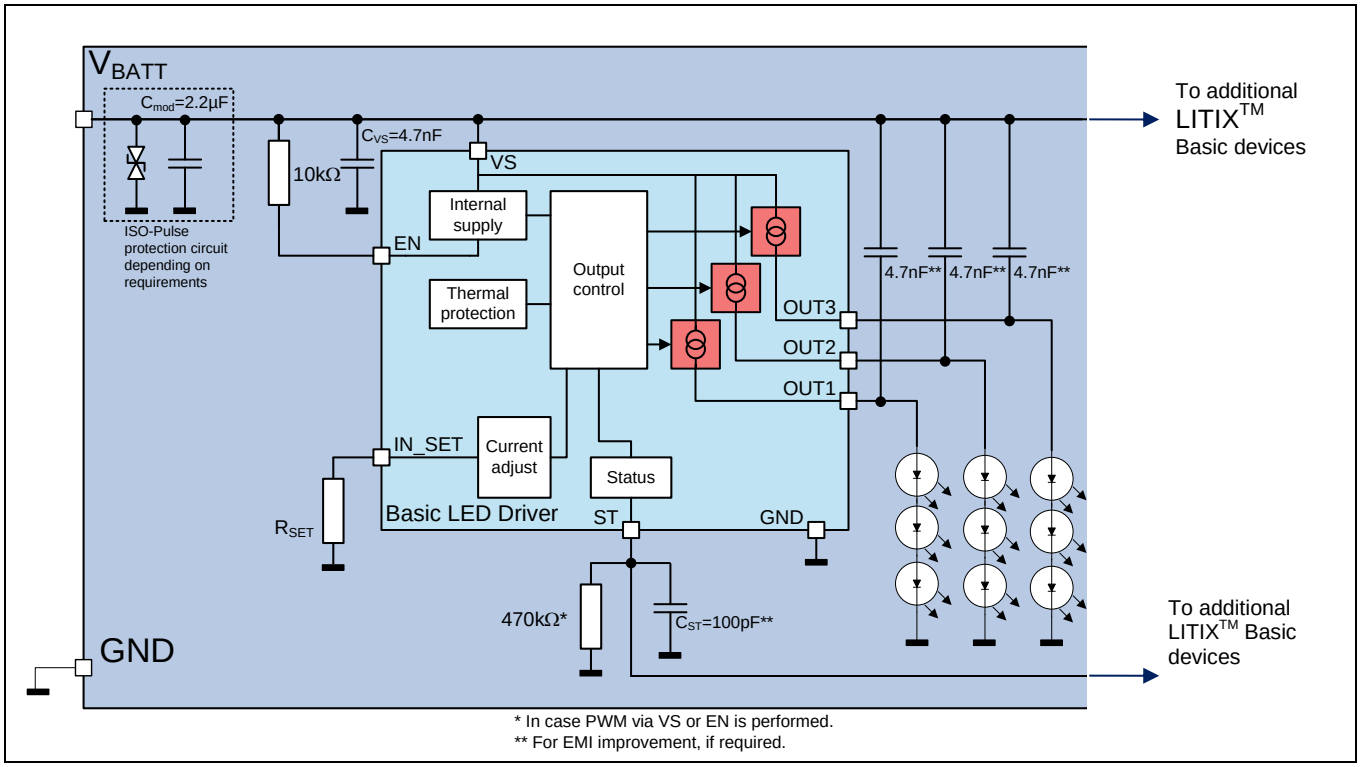



**Figure 52 Application diagram showing optional EMC output capacitors, local supply decoupling capacitor near device Vs pin and module bulk storage capacitor**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

In addition, near the supply input pin of the module, it is also recommended to have a larger, ceramic storage capacitor, $C_{mod}$. The minimum recommended value depends mainly on the length of the supply wiring to the module and the total output current (through the same Vs input) of the connected LITIX™ Basic devices sharing the ST pin diagnosis. 2.2uF is a good starting value for two devices sharing a common Vbat line.

The reason for this larger supply capacitor $C_{mod}$ is to reduce dv/dt during ISO pulses and transients on the supply. The $C_{VS2OUT}$ capacitors are recommended to reduce possible unstable open load detection when noise or supply ripple is encountered on Vs. Since the open load diagnosis is based on the voltage difference between the supply pin and output pins, Vs ripple could be sufficient to cause intermittent open load detection, during a valid open load condition. The $C_{VS2OUT}$ capacitors allow the outputs to follow the Vs level more closely during these events, avoiding a toggling or interemittent open load detection.

There could also be a case when an open load can cause ringing at the supply pin due to L*dI/dT of the supply wiring. If the optional $C_{out2gnd}$ capacitors are present at the outputs, these capacitors tend to hold the output voltages steady. The ringing at the supply pin can causing a toggling behavior of the ST pin as the voltage difference between the supply pin and outputs cross in and out of the open load detection range. Figure 53 illustrates this scenario.

The value of the $C_{out2gnd}$ capacitors should be less than one tenth the value of the $C_{VS2OUT}$ capacitors in order to reduce the capacitive divider impact during transient events on Vs.

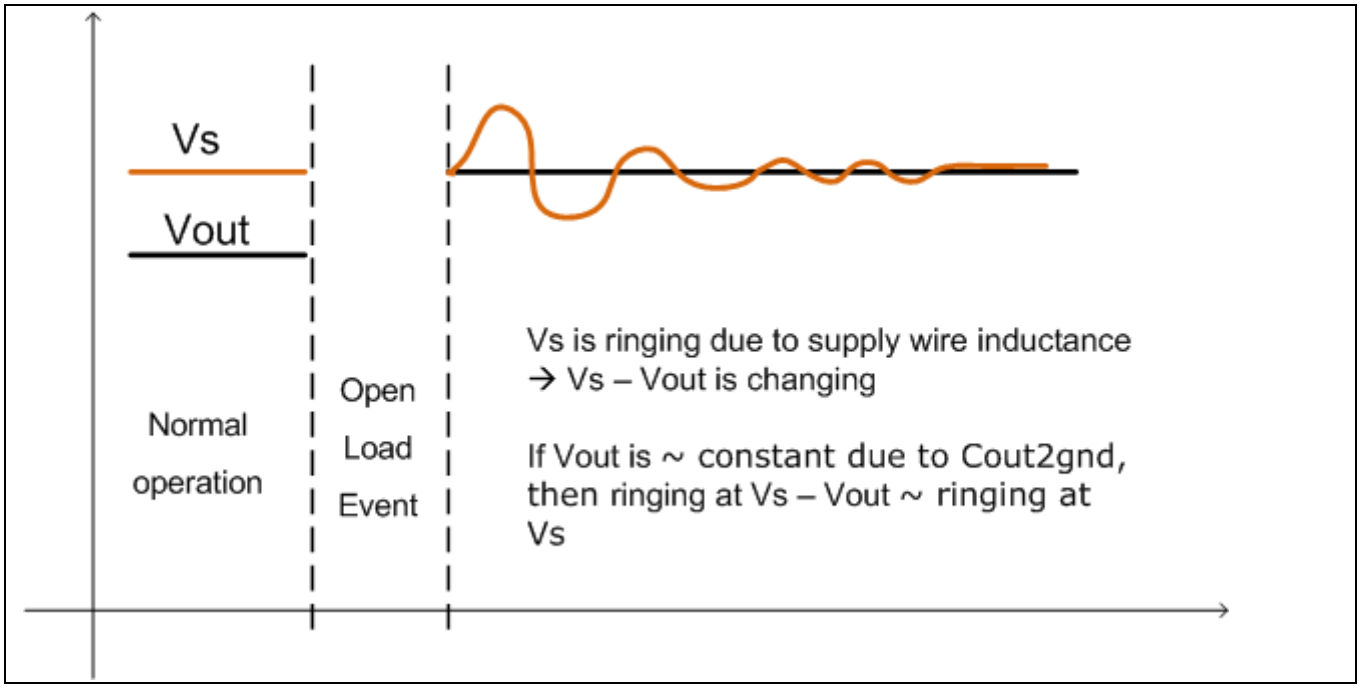



**Figure 53 Ringing at Vs while output voltage is stable**

### 4.1.1.3 Reverse Polarity, ISO pulse and supply noise protection

The LITIX™ Basic driver also offers an integrated reverse polarity protection. Only leakage currents may flow through the power stage during reverse battery condition (<5µA). Therefore, a reverse polarity diode for the light function may not be necessary. Depending on the ISO-pulse requirements and external components like capacitors on the light module and/or on the BCM, the reverse polarity diode may be recommended to avoid damage in case of negative ISO-pulses. Verification of each specific application is recommended to ensure if a reverse polarity diode is required or not.

The OEM specific requirements need to be considered when developing the proper ISO pulse protection circuit for the application. Figure 54 shows a possible configuration. Note that the value of Cmod, the clamping voltage of the suppressor, and the necessity of the reverse polarity diode should be adjusted to the application's requirements.

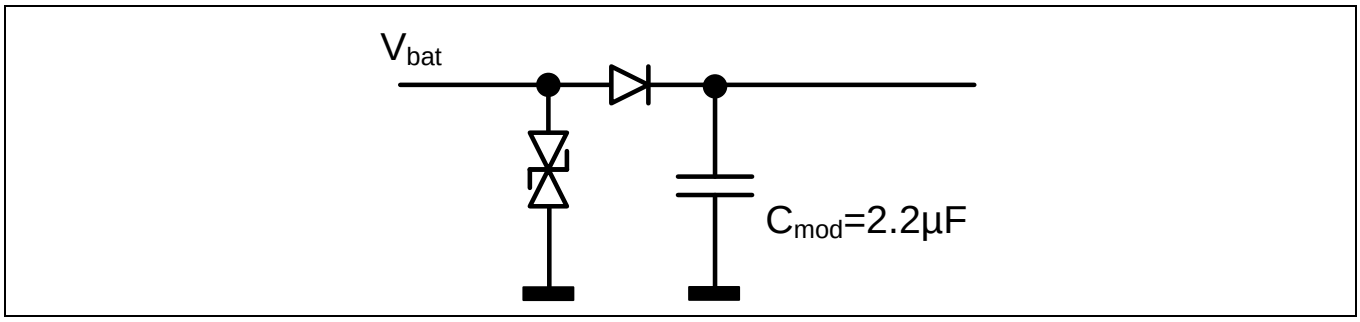



**Figure 54 Possible ISO pulse protection circuit**

#### 4.1.1.4 EN (Enable) pin

If the EN pin is controlled independently of the Vs pin, it is important to also isolate the EN pin PCB trace from the Vs and IN_SET pin traces. This is to prevent noise from capacitively coupling from the Vs pin to the EN or IN_SET pin(s) and either turning the device on or off erroneously or causing increased current leakage at the output(s).

#### 4.1.1.5 Output pins

The length of PCB traces and wiring from the output pins of the IC to the LED load must be limited. The output impedance connected to the output pins can affect the stability of the control loop and lead to oscillations if the wiring length is excessive.

Generally, up to 0.5uH of output wiring inductance (approx.40cm) between the output and LED load is tolerated without significant impact to phase margin and stability. A small (1-22nF) capacitor placed near the output pin(s) will minimize this impact.

In case of long wiring between IC and LED load it is recommended to place a 10nF capacitor close to the output to increase RF immunity. In parallel to this capacitor a 1nF capacitor should be placed with a PCB trace length of 1.5cm to realize a simple π-filter.

Unused outputs: If one of the output pins is not used in the application for devices with a single IN_SET-pin and diagnosis two different implementations are considered (also see section 3.1.1):

- Devices with N-1 diagnosis (only open load diagnosis, no short circuit to GND diagnosis, i.e. TLD1311, TLD1315, TLD1326) the unused output can be shorted to GND. The channel will be deactivated internally. Only a minor diagnosis current will flow through this deactivated channel.
- Devices with open load and short circuit to GND detection (TLD1313,TLD1314): An unused channel needs to be connected with a Zener diode to GND. The zener voltage should be in the range of the LED’s forward voltage. Please verify the EMC behavior of the Zener diode in the application.

Additionally, ground plane beneath the LEDs on the opposite side of the PCB should increase EMC robustness.

### 4.1.1.6 ST pin

If the ST pin is used in the application with PWM applied on the Vs and/or the EN pin, a pull down resistor to ground of 470kΩ should be connected once at the ST-pin or the connection wire/trace between multiple LITIX™ Basic drivers.
In case of EMC immunity issues on the ST-line, a small capacitor (10-100pF) can be connected at each device's ST pin, which filters EMC radiation. The size of the capacitor depends on the application, layout and length of PCB-trace. Please note that the capacitor will delay the diagnosis function, because the ST pin needs time to charge the capacitor and reach an active high level.

#### 4.1.1.6.1 Sharing a common ST pin between multiple devices

The ST pin can be connected together on multiple devices, to provide the function of a single device fault disabling all the connected devices. When connecting the ST pins of multiple devices together, only a single 470kΩ pull down resistor to ground is needed.

The number of devices sharing a common ST pin must be limited. Since a single device can have a fault while the other connected devices do not, the maximum number of connected devices is limited by the pull up current source of the device with a fault. Each connected device has a pull down current as well, which is active when the device does not have a fault.

The ST pin pull up current source ($I_{ST(OL/SC)}$ ) of the device with a fault must be able to supply more current than the sum of the pull down current sources ($I_{ST(PD)}$) of each device in order to ensure the needed voltage level of 2.5V ($V_{ST(H)}$) is reached to indicate a valid fault signal.

The calculation is given below:

Current through 470kΩ resistor to ground: 2.5V / 470kΩ = 5.3µA

Pull up current during a fault $I_{ST(OL/SC)}$ = 100µA minimum → 100µA – 5.3µA = 94.7µA pull up current available

94.7µA / 20µA = 4.73 → a single pull up current source can support a total of 4 pull down current sources;

So if each unfaulted device has a pull down current $I_{ST(PD)}$ of 20µA, then 4 additional devices can be connected to the ST pin of the faulted device, for a total of 5 devices sharing a single ST pin.

This is a worst case scenario, based on a fault on a single device, minimum pull up current $I_{ST(OL/SC)}$, maximum pull down current $I_{ST(PD)}$ and maximum ST turn off threshold voltage $V_{ST(H)}$.

Figure 55 is given below to illustrate this calculation. Each block represents only the ST pin current source portion of each LITIX™ Basic device.

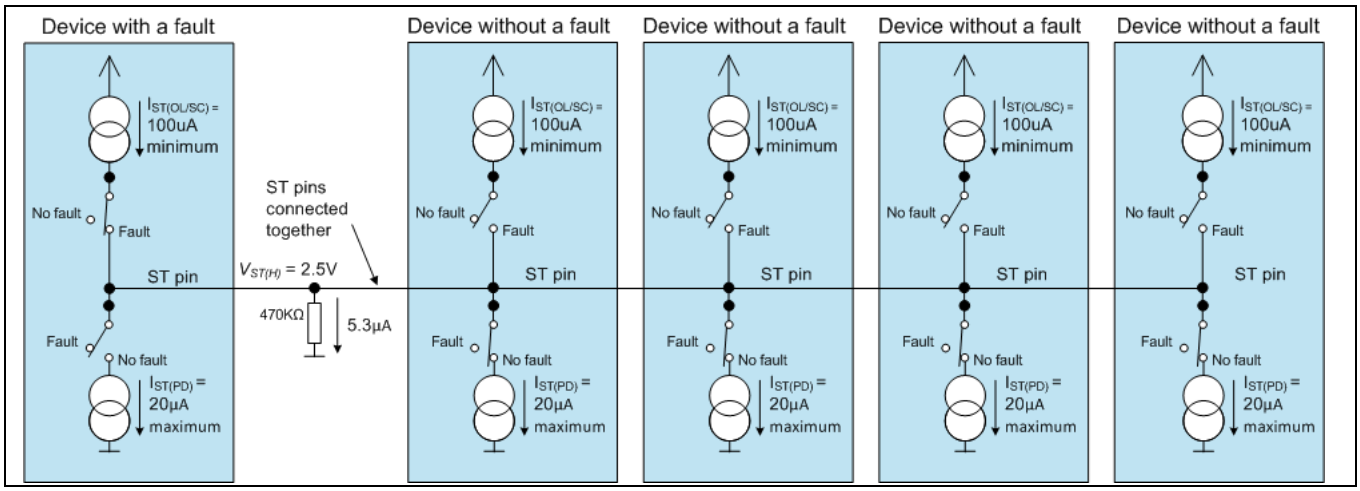



**Figure 55 Sharing an ST diagnostic pin between multiple devices**

### 4.1.1.6.2 Connecting the ST pin between groups of devices

When the application requires that more than 5 devices share an ST pin (i.e. to reduce the I/O requirements of the ECU microcontroller), it is possible to implement a simple level shifter interface circuit to overcome the limitations of the pull up current source described in 4.1.1.6.1. This is done by connecting 2 or more groups of 5 or less devices.

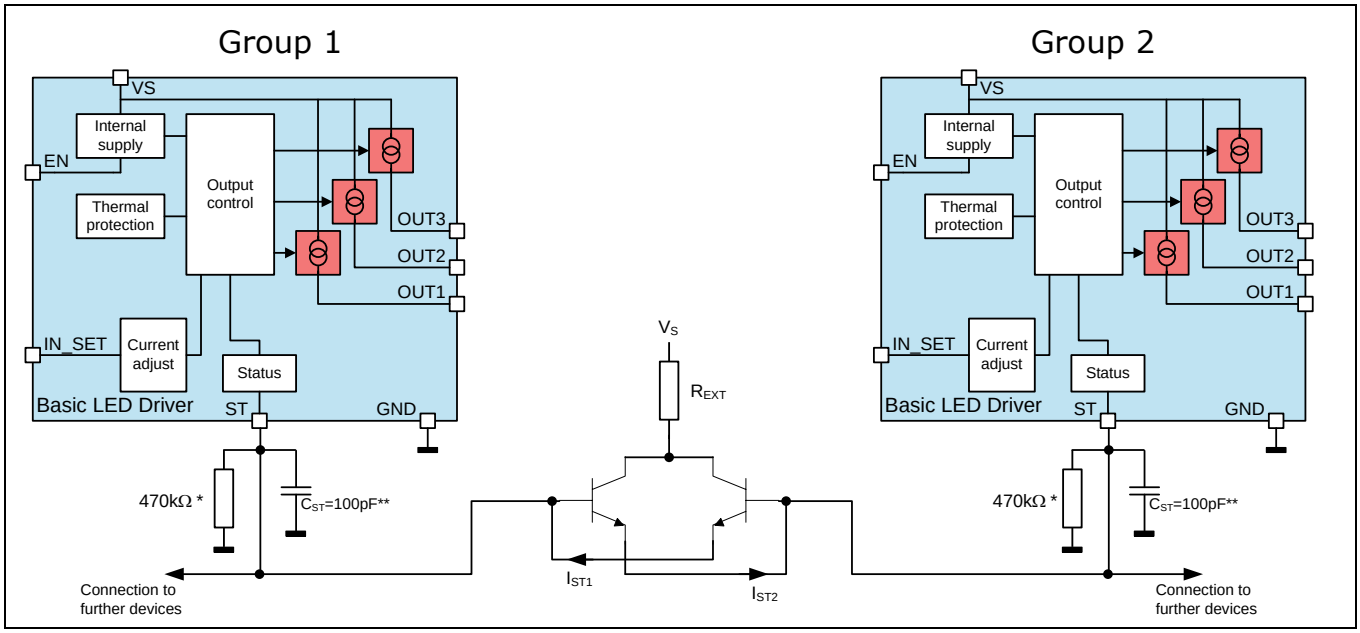



**Figure 56 Application circuit example with interface circuit**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

The interface circuit consists of 2 bipolar transistors, connected to Vs via a pullup resistor as shown in Figure 56. Since each transistor's base is connected to both an ST pin or the emitter of the opposite transistor, either the ST pin or the opposite transistor can supply the base current. In this way, the first transistor that is supplied base current (via the connected ST pin of the corresponding group) will act to supply the other transistor's base current and raise the other group's ST pin to a high level.

Since applying a high signal to the ST pin deactivates the device, this circuit will allow Group 1 to deactivate Group 2 when it encounters a fault and vice versa.

The base current into the bipolar transistor needs to be considered since this is additional current is not considered in the calculation discussed in section 4.1.1.6.1. It is recommended to select bipolar transistors with a current gain of 100 or more to minimize this base current, which is drawn from the pullup current source of the ST pin.

The basic equations for this circuit are shown below.

$$I_{ST2} = \frac{V_{ST(OL/SC,\max)} - V_{BE(\min)}}{R_{ST2}} + n \cdot I_{ST(PD,\max)}$$

$$R_{EXT} \leq \frac{V_{S(\min)} - V_{ST(OL/SC,\max)}}{I_{EXT}}$$

Where;
$I_{ST2}$ is the current flowing to the connected ST pins of Group 2 as a result of a fault on Group 1
$I_{EXT}$ is the current flowing through $R_{EXT}$ which is approximately equal to $I_{ST2}$
$R_{EXT}$ is the external pullup resistor to $V_S$
$V_{ST(OL/SC,max)}$ is the maximum voltage on the ST pin during an open load or short circuit (specified in the device datasheets)
$V_{BE(min)}$ is the minimum base to emitter voltage for the external transistor
$V_{S(min)}$ is the minimum operating supply voltage at the pullup resistor of the external transistors
$R_{ST2}$ is the pull down resistor at the ST pin of Group 2
$n$ is the number of devices in Group 2
$I_{ST(PD,max)}$ is the maximum pull down current for the ST pin (specified in the device datasheets)

Please consider the transistor's base current $I_{BE}$ for the maximum number $n_{max}$ of devices within one group:

$$n_{\max} = \frac{I_{ST(OL/SC,\max)} - \frac{V_{ST(OL/SC,\max)}}{R_{ST}} - I_{BE}}{I_{ST(pd,\max)}} \quad \text{With} \quad I_{BE} = \frac{I_{ST2}}{\beta} \quad ; \quad \beta \text{ is DC current gain}$$

An example calculation follows:
Where;
$V_{ST(OL/SC,max)}$ is 5.5V
$V_{BE(min)}$ is 0.4V
$V_{S(min)}$ is 9V
$R_{ST2}$ is 470KΩ
$n$ is 4
$I_{ST(PD,max)}$ is 20µA

$$I_{ST2} = \frac{V_{ST(OL/SC,\max)} - V_{BE(\min)}}{R_{ST2}} + n \cdot I_{ST(PD,\max)} = \frac{5.5V - 0.4V}{470k\Omega} + 4 \cdot 20\mu A = 91\mu A \approx I_{EXT}$$

$$R_{EXT} \le \frac{V_{S(\min)} - V_{ST(OL/SC,\max)}}{I_{EXT}} = \frac{9V - 5.5V}{91\mu A} = 39k\Omega$$

#### 4.1.1.7 GND-connections

The device GND-pin, GNDS-pin and exposed pad should be connected with a low ohmic connection to the PCB GND (i.e.a solid GND-plane is recommended on the backside of the PCB). The LED-GND-potential should be fed back to the PCB-GND (LEDs and LITIX™ Basic driver should use the same GND-connection).

#### 4.1.1.8 Power dissipation and cooling area of the PCB

The layout and design of the PCB must consider the thermal dissipation of the LITIX™ Basic driver, taking into account maximum ambient temperature seen in the application, the expected maximum device power dissipation and the maximum allowed PCB temperature.

The thermal resistance ratings (as listed in the device datasheets) of the LITIX™ Basic devices consider 2 cases based on the JESD51 natural convection standard:

- Junction to Ambient 1s0p: See Figure 57. This is the case where the PCB consists of a single layer of 70um copper, and the device exposed pad is thermally connected to 300mm$^2$ of cooling area.

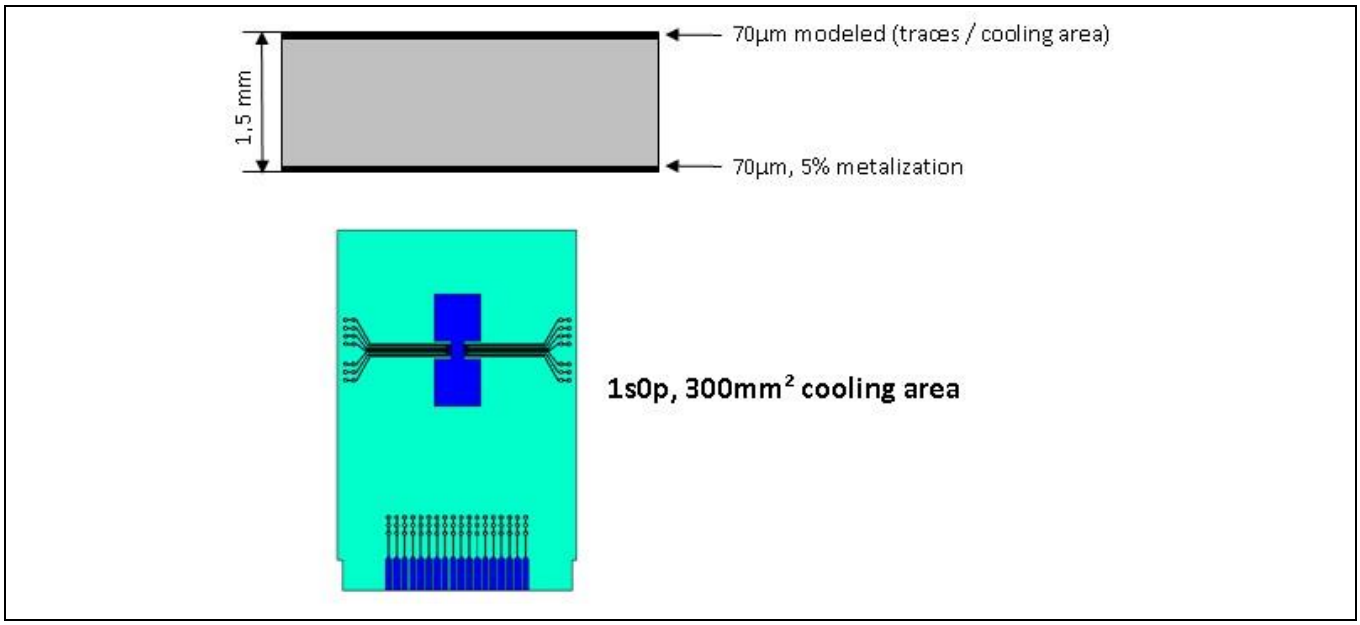



**Figure 57 JESD51 1s0p PCB configuration**

- Junction to Ambient 2s2p: See Figure 58. This is the case where the PCB consists of a top and bottom layer of 70um copper, 2 inner layers of 35um copper and a matrix of thermal vias connecting the exposed pad of the device to the first inner layer.

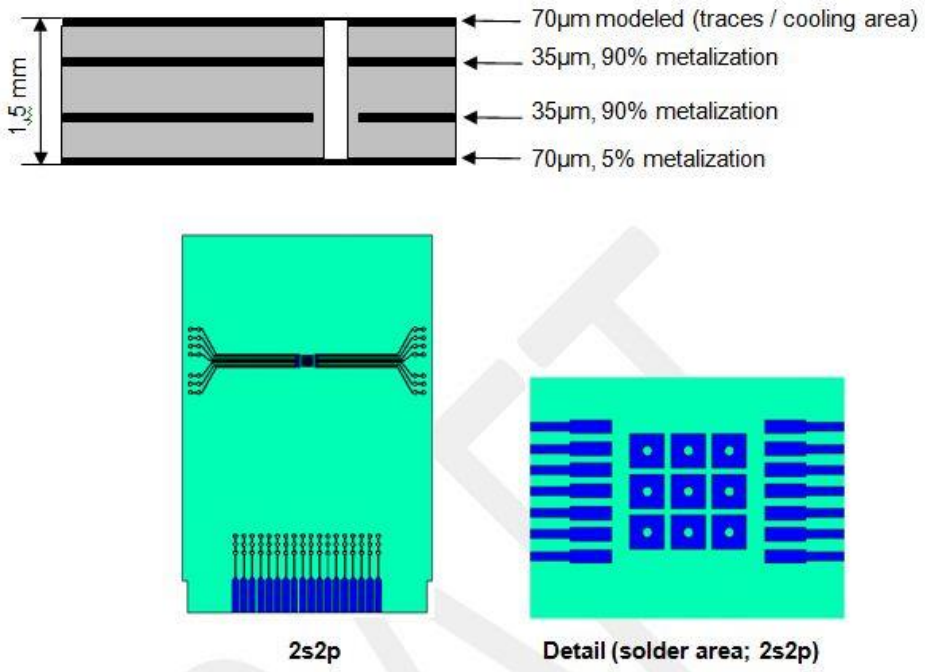



**Figure 58 JESD51 2s2p PCB configuration**

The thermal resistance values are based on simulations using the JESD51 standard for PCB definition.

In general, for the 1s0p configuration, cooling area greater than 300mm$^2$ will lower the junction to ambient thermal resistance; but a point of diminishing returns occurs at about 600mm$^2$. This would need to be evaluated for each application.

For the 2s2p configuration, a larger area connected to the thermal vias will provide a lower junction to ambient thermal resistance, but again with a limit.

Figure 59 shows the typical thermal resistance information included in the device datasheets.

**4.3 Thermal Resistance**

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 4.3.1 | Junction to Case | $R_{thJC}$ | – | 8 | 10 | K/W | 1) 2) |
| 4.3.2 | Junction to Ambient 1s0p board | $R_{thJA1}$ | | | | K/W | 1) 3) |
| | | | – | 61 | – | | $T_a$ = 85 °C |
| | | | – | 56 | – | | $T_a$ = 135 °C |
| 4.3.3 | Junction to Ambient 2s2p board | $R_{thJA2}$ | | | | K/W | 1) 4) |
| | | | – | 45 | – | | $T_a$ = 85 °C |
| | | | – | 43 | – | | $T_a$ = 135 °C |

**Figure 59 Typical thermal resistance values**

For exposed pad devices, in many cases the maximum board temperature can be the limiting factor. This is because the thermal resistance from the junction to the exposed pad is low, meaning that the temperature of the exposed pad is quite close to the junction temperature.

For example, with 1 watt of power dissipation, if the junction temperature is 145° C, then the exposed pad will be approximately (using the Rth(j-case) value of 8° C per watt):

Temperature of exposed pad = Junction temperature – (Power dissipation x Rth (junction-case))
= 145° C – (1 watt x 8° C per watt) = 137° C

So if the glass transition temperature of the PCB material (maximum rated temperature) is 135° C, then this scenario would exceed the PCB temperature rating, while the junction temperature of the device is within the maximum rating.

Figure 60 shows the LITIX™ LITIX™ Basic Zth diagram (junction to case and junction to ambient) based on typical simulation parameters.

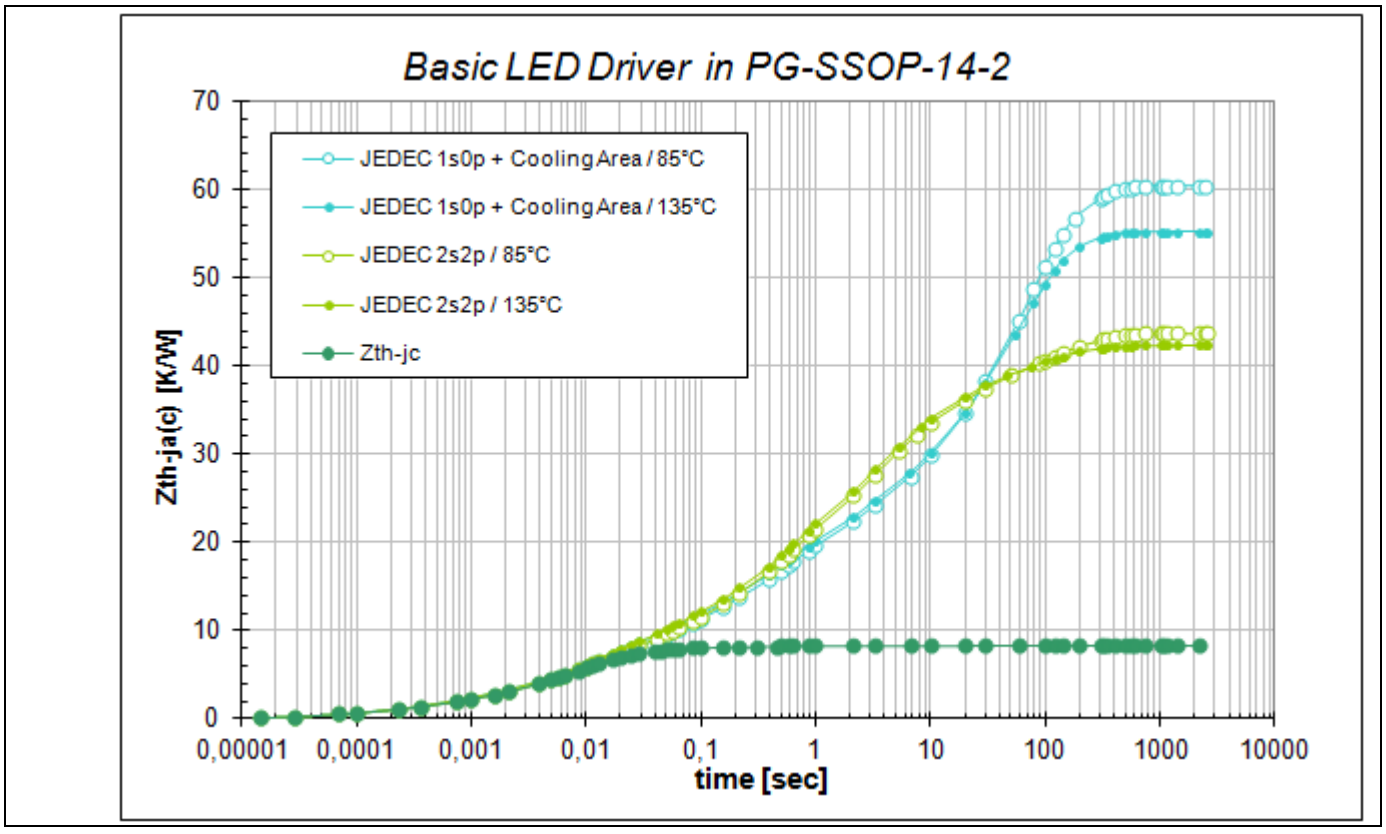



**Figure 60 Typical Zth(j-c) and Zth(j-a) based on thermal simulation for JEDEC 1s0p and 2s2p PCB configurations**

# 5 Additional Information

- Please contact us to get the Pin FMEA
- For further information you may contact http://www.infineon.com/automotive-leddrivers

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