MR+ SBC Family

User's Guide

About this document

Scope and purpose

The intention of this User's Guide is to provide relevant design-in information for automotive applications with the Infineon Mid-Range+ SBC family. The explanations of the hardware and of software aspects are always based on the superset device TLE9263-3BQX, in which all device features are present.

This document covers in addition the following products of the Mid-Range+ SBC device family (with and without CAN Partial Networking and for VCC1 = 5.0 V and 3.3 V output voltage):

- TLE9261BQX
- TLE9261BQXV33
- TLE9261-3BQX
- TLE9261-3BQXV33
- TLE9262BQX
- TLE9262BQXV33
- TLE9262-3BQX
- TLE9262-3BQXV33
- TLE9263BQX
- TLE9263BQXV33
- TLE9263-3BQX
- TLE9263-3BQXV33

Note: This User's Guide is also applicable for devices of the Mid-Range SBC family with the exception of the CAN FD feature.

Intended audience

This document is aimed at hardware and software engineers integrating MR+ SBC family devices into their designs.

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1 Hardware aspects

1.1 Introduction

This chapter describes consideration regarding:

- Pin input- and output structures.
- The device behavior regarding certain failures on system level.
- The device behavior regarding watchdog trigger failure and VCC1 overvoltage conditions, depending on the device configuration (see ***Behavior in case of VCC1 overvoltage condition*** on page 15).

The device configuration is selected by setting the voltage level at the INT pin (CFGP) during the power-on phase in combination with setting the SPI bit CFG in the HW_CTRL register.

1.2 Pin structures

Table 1 Pin overview

Pin	Symbol	Input / output structure
1	GND	
2	n.c.	not connected; internally not bonded
3	VCC3REF	Active pull-down (~2.5 mA) to GND when VCC3 = OFF
4	VCC3B	150 kΩ pull-up to VS
5	VCC3SH	5 kΩ pull-up to VS
6	n.c.	not connected; internally not bonded
7	n.c.	not connected; internally not bonded
8	HS1	High-side switch
9	HS2	High-side switch
10	HS3	High-side switch
11	HS4	High-side switch
12	n.c	not connected; internally not bonded
13	VSHS	
14	VS	
15	VS	
16	n.c.	not connected; internally not bonded
17	VCC1	Active pull-down to GND when VCC1 = OFF (~1 mA)
18	VCC2	Active pull-down to GND when VCC2 = OFF (~1 mA)
19	n.c.	not connected; internally not bonded
20	GND	
21	FO1	Low-side switch
22	WK1	High-ohmic after POR, configurable 10 µA pull-up/pull-down to internal 5 V/GND
23	WK2	High-ohmic after POR, configurable 10 µA pull-up/pull-down to internal 5 V/GND
24	WK3	High-ohmic after POR, configurable 10 µA pull-up/pull-down to internal 5 V/GND
25	TXDLIN2	40 kΩ pull-up to VCC1
26	RXDLIN2	Push-pull output stage
27	CLK	40 kΩ pull-down to GND
28	SDI	40 kΩ pull-down to GND
29	SDO	Push-pull output stage
30	CSN	40 kΩ pull-up to VCC1
31	INT	250 kΩ pull-down to GND during reset delay time and Init, push-pull output stage afterwards
32	RO	20 kΩ pull-up to VCC1, open-drain output stage

Table 1 Pin overview (continued)

Pin	Symbol	Input / output structure
33	TXDLIN1	40 kΩ pull-up to VCC1
34	RXDLIN1	Push-pull output stage
35	TXDCAN	40 kΩ pull-up to VCC1
36	RXDCAN	Push-pull output stage
37	VCAN	
38	GND	
39	CANL	Low-side switch
40	CANH	High-side switch
41	n.c.	not connected; internally not bonded
42	LIN1	Low-side switch, internal 30 kΩ pull-up
43	GND	
44	LIN2	Low-side switch, internal 30 kΩ pull-up
45	n.c.	not connected; internally not bonded
46	n.c.	not connected; internally not bonded
47	FO2	Default is low-side switch, configurable to high-side switch or to input with 5 kΩ pull-up to internal 5 V
48	FO3/TEST	5 kΩ pull-up to internal 5 V during POR and Init. Configurable to low-side or high-side switch or to input with 5 kΩ pull-up to internal 5 V

1.3 Failure behavior

1.3.1 Loss of GND and HS short circuit aspects

Loss of module GND is a state-of-the-art module test in automotive applications.

It is important to know and to understand the behavior of the ECU in this case, specifically the SBC.

Certain scenarios are possible for a loss-of-GND of the module:

- ***Scenario 1: Loss of module GND and no connections to external GND*** on page 8
- ***Scenario 2: Loss of module GND and connections to external GND, with external ESD diode*** on page 9
- ***Scenario 3: Loss of module GND and connections to external GND, with internal ESD diode*** on page 10

Short circuit scenarios for the HS switches are discussed in:

- ***HS switches: Short-circuit scenarios*** on page 11

1.3.1.1 Scenario 1: Loss of module GND and no connections to external GND

Behavior description:

- All SBC GND connections should be connected together.
- All loads of the ECU are on-board, i.e., no external GND connection is present.
- A loss of module (ECU) GND allows the module GND to float towards VS (or Vbat) level. Only if internal GND structures are floating.
- The SBC then has no voltage across VS and GND and is therefore disabled, i.e., there is no current flow or activity.

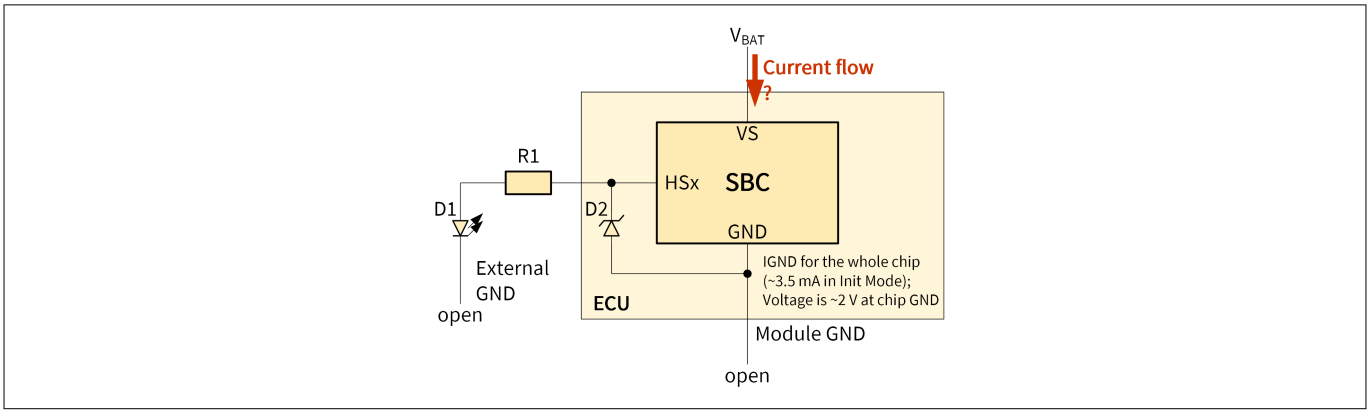

Figure 1 Scenario 1: Loss of module GND, no connections to external GND

1.3.1.2 Scenario 2: Loss of module GND and connections to external GND, with external ESD diode

Behavior description:

- Depending on the external circuitry, an external load (with an external GND connection) could lead to a current flow through the SBC.
- The example below shows an on-board protection diode for the high-side switch and an off-board load, e.g. LED.
- Other scenarios with similar configurations are possible.
- In such a case, a current flow is possible even with a loss of GND of the module.
- The SBC and module current (loads, etc.) flows through the on-board protection diode into the load. The amount of current that flows is determined by the amount of loads that are connected, as long as the current capability of the ESD diode(s) is not exceeded.
- Example: If the SBC is in Sleep Mode and no other loads are activated, then the current flow will be typ. only ~20 µA.
- The SBC is functional as long as there is sufficient voltage drop across the SBC, i.e. as long as $V_{por,f}$ is not triggered.
- No destruction of the SBC occurs – possibly the on-board protection diode might be damaged.
- In case there is no active path to the external GND, no current flow occurs, and the SBC is off.

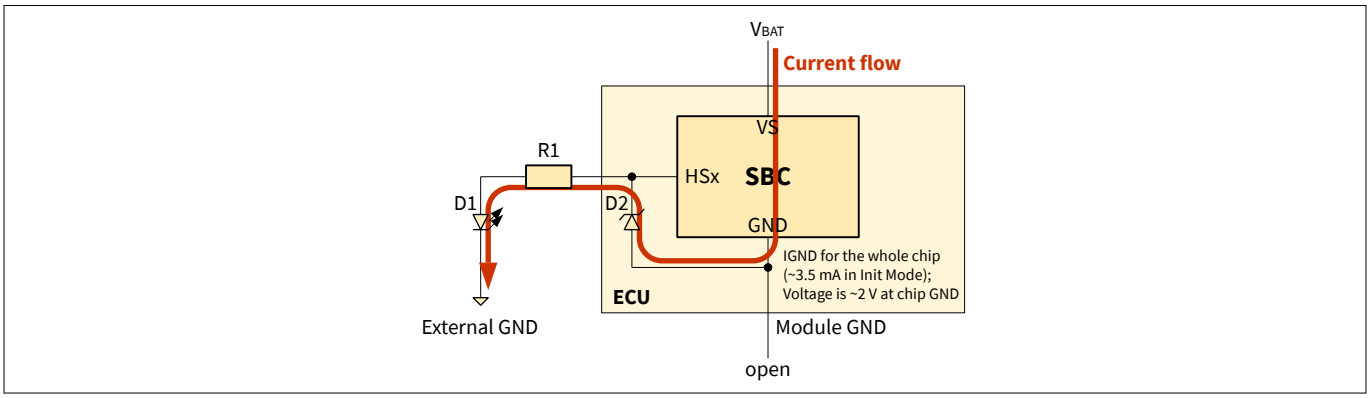

Figure 2 Scenario 2: Loss of module GND, connections to external GND, external ESD diode

1.3.1.3 Scenario 3: Loss of module GND and connections to external GND, with internal ESD diode

Behavior description:

- External GND is now the reference GND for the SBC (module GND is floating).
- The ESD protection diode from VCC2 is now forward biased due to the loss of module GND and, e.g., VCC2 is shorted to external GND.
- As long as the module GND potential is ~0.7 V higher than the ext. GND, and the ESD diodes current capability is not exceeded, the SBC works as expected.
- The whole SBC current, which is normally flowing through the device from VS to GND (assumed all GND pins are connected), and all the load current (e.g. I_VCC1) is now flowing through the VCC2 ESD diode biased in forward direction.
- However, the ESD diode is not designed for permanent current flow in forward direction → life time issue & potential destruction possible.

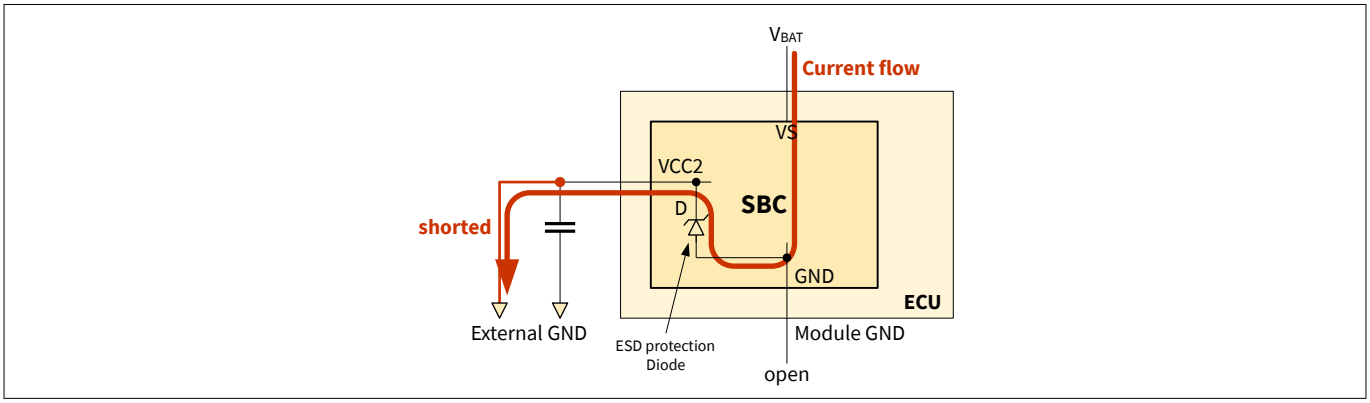

Figure 3 Scenario 3: Loss of module GND, connections to external GND, internal ESD diode

1.3.1.4 HS switches: Short-circuit scenarios

The following test scenarios are analyzed:

- KL30 (permanent battery connection) connected, KL31 (= GND) NOT connected, short circuit of one or more HS outputs to V_{bat}, see ***Chapter 1.3.1.4.1***
- KL30 (permanent battery connection) connected, KL31 (= GND) NOT connected, short circuit of one or more HS outputs to GND, see ***Chapter 1.3.1.4.2***
- KL30 (permanent battery connection) NOT connected, KL31 (= GND) connected, short circuit of one or more HS outputs to V_{bat}, see ***Chapter 1.3.1.4.3***
- KL30 (permanent battery connection) NOT connected, KL31 (= GND) connected, short circuit of one or more HS outputs to GND, see ***Chapter 1.3.1.4.4***

Note: In case of complete GND connection (module GND and output GND), the device completely shuts down, i.e. no unintended current flow.

1.3.1.4.1 Scenario 1: KL30 connected, KL31 open, short circuit of one or more HS outputs to V_{bat}

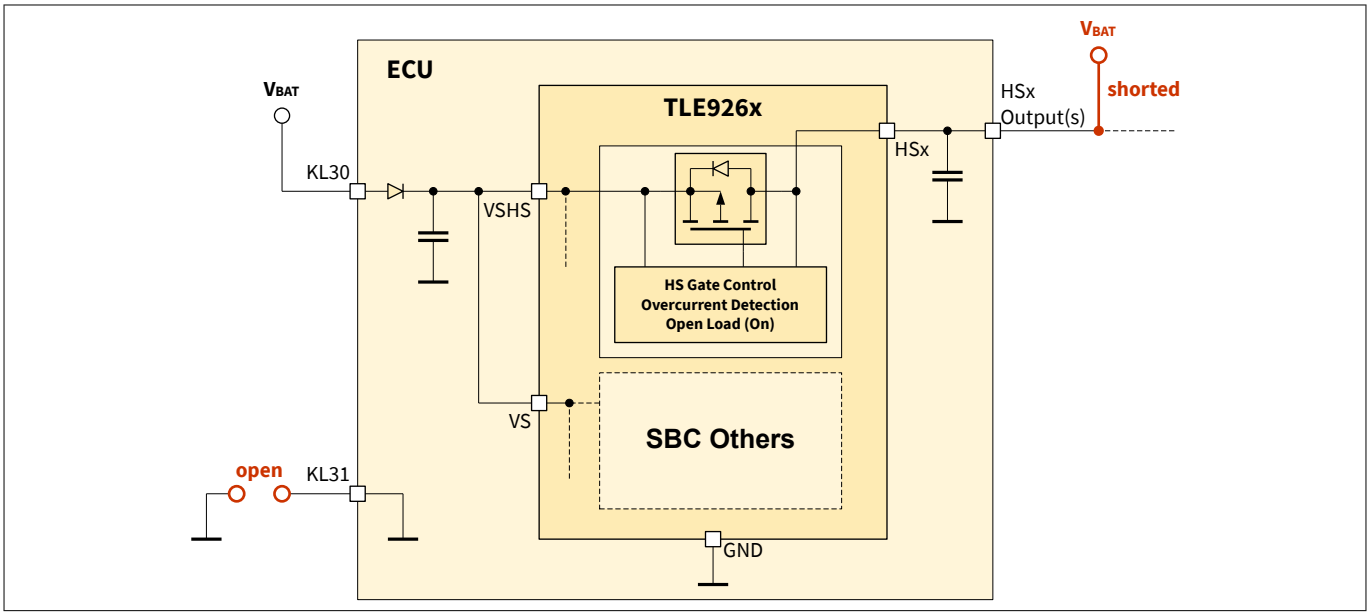

Figure 4 Simplified circuitry for scenario 1

SBC device behavior:

- Device stays disabled, because GND potential floats toward VS.
- This behavior is true as long as:
  - No other loads are shorted to GND with a possible path from V_{bat} to GND.
  - V_{bat} (shorted at HSx) is not >> V_{bat} of ECU supply → inverse current flow.

1.3.1.4.2 Scenario 2: KL30 connected, KL31 open, short circuit of one or more HS outputs to GND

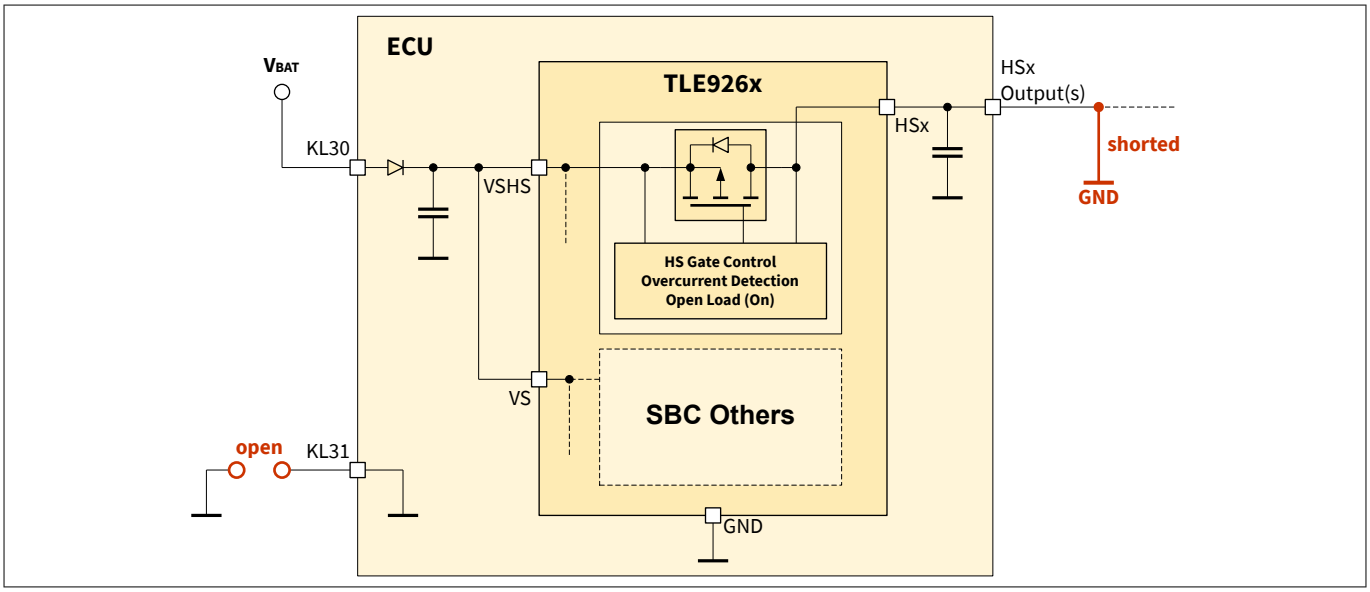

Figure 5 Simplified circuitry for scenario 2

SBC device behavior:

- An external load could lead to a current flow through the SBC.
- The example below shows an on-board protection diode for the high-side switch and an off-board load, e.g. LED.
- Other scenarios with similar configurations are possible.
- In such a case, a current flow is possible even with a loss of module GND.
- The SBC and module current (loads, etc) flows through the on-board protection diode into the load. The amount of current that flows is determined by the amount of loads that are connected, as long as the current capability of the ESD diode(s) is not exceeded.
- The SBC is functional as long as there is sufficient voltage drop across the SBC, i.e. as long as $V_{por,f}$ is not triggered.
- No destruction of the SBC occurs – possibly the on-board protection diode might be damaged.
- In case there is no active path to the external GND, no current flow occurs, and the SBC is off.

Note: Also VCC2 could be an off-board output.

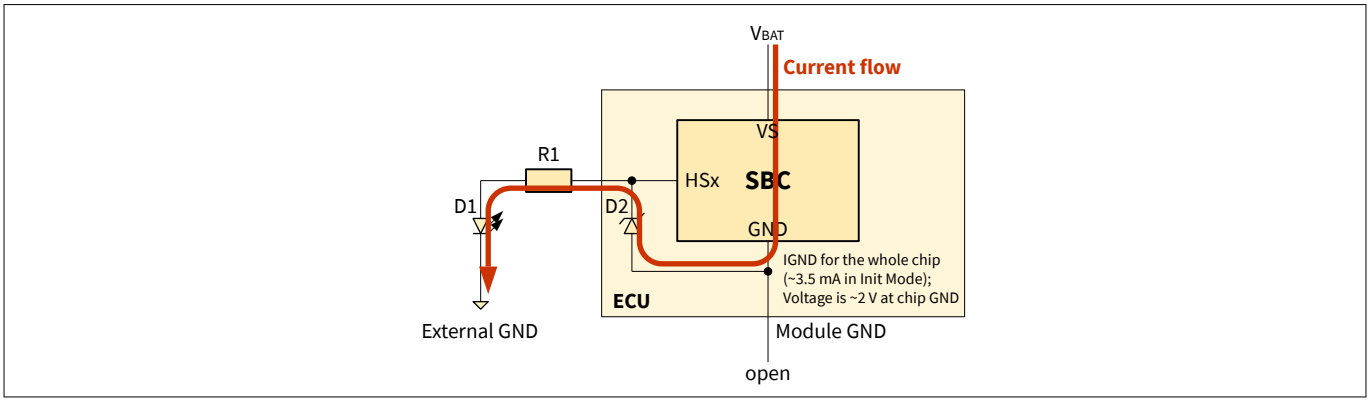

Figure 6 Example for a potential fault case

1.3.1.4.3 Scenario 3: KL30 open, KL31 connected, short circuit of one or more HS outputs to V_{bat}

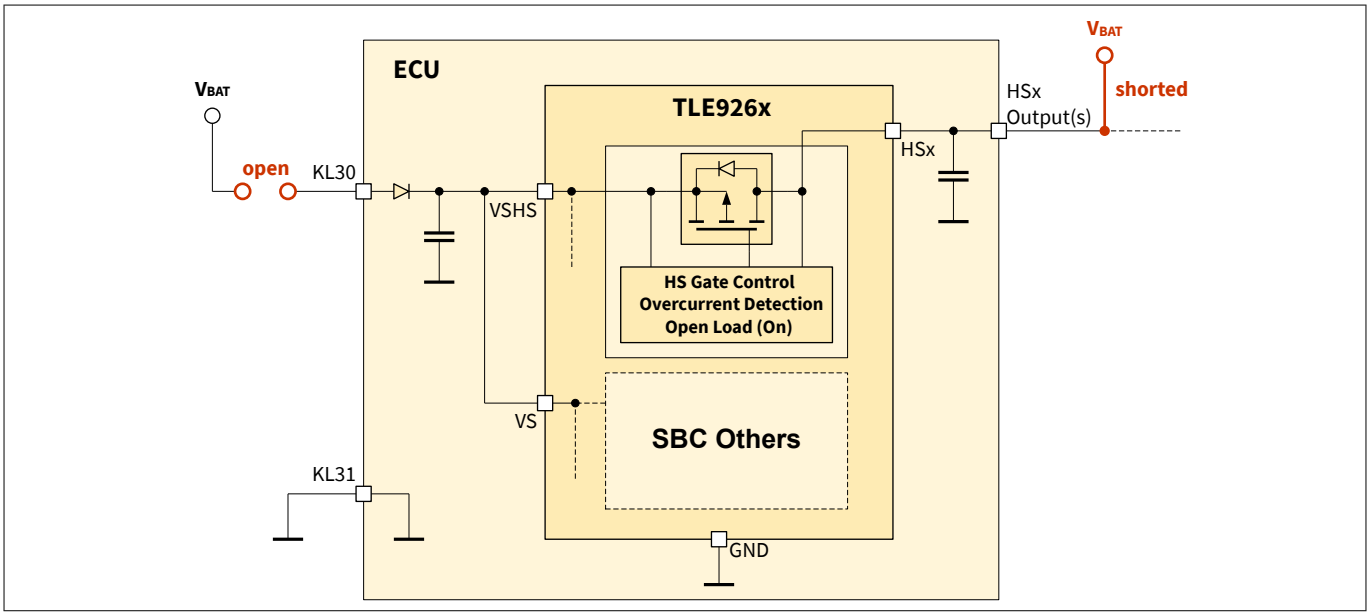

Figure 7 Simplified circuitry for scenario 3

SBC device behavior:

- Device is off, because KL30 is open.
- However, the SBC can be supplied through an HSx pin, enabling a reverse current flow.
- Depending on the VS/VSHS configuration, different scenarios are possible.
- In case such behavior is not acceptable, an external diode or series resistor could be placed.

1.3.1.4.4 Scenario 4: KL30 open, KL31 connected, short circuit of one or more HS outputs to GND

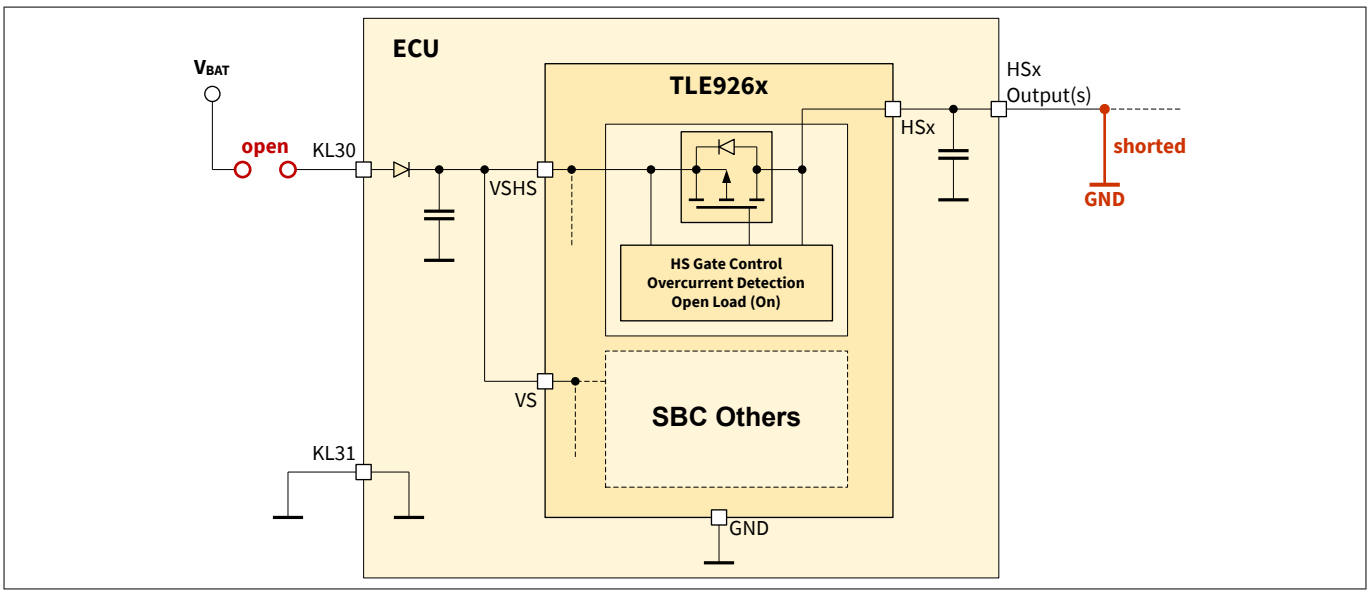

Figure 8 Simplified circuitry for scenario 4

SBC device behavior:

- Device is off, because KL30 is open and HSx is shorted to GND.
- No back supply via HSx as long as potential GND shift is < diode drop of HSx body diode.

1.3.1.4.5 Conclusion

In general, a loss of module GND and a short of an output is considered as a double failure, and therefore not covered by the SBC by default.

Depending on the failure case, there could be an unintended behavior of the SBC with a worst-case scenario, leading to destruction of external components or the device itself.

A case by case analysis is required in the actual application to determine (because not all possible cases can be considered):

- The device behavior.
- Whether external components can protect the ECU / device.

1.3.2 Behavior in case of VCC1 overvoltage condition

The behavior due to VCC1 overvoltage is different compared to watchdog trigger failures.

Strategy of VCC1 overvoltage signalization:

- Level 1: SPI flag (VCC1_OV) activation only.
- Level 2: SPI flag (VCC1_OV) + Restart Mode entry (reset).
- Level 3: SPI flag (VCC1_OV) + SBC Fail-Safe Mode entry and thus FOx activation.

Additional selection via SPI bit VCC1_OV_RST in M_S_CTRL:

(default value after POR/SOFT Reset & Restart = 0).

- If VCC1_OV_RST = 0 (default), then a VCC1 overvoltage condition is only flagged with the SPI status bit VCC1_OV (SUP_STAT_2).
- If VCC1_OV_RST = 1, then a VCC1 overvoltage condition sets the VCC1_OV bit and in addition, depending on the hardware configuration, below listed action is triggered:
  - If CFGP = 1, the SBC Restart Mode is entered in case of VCC1_ OV.
    Fail-outputs are activated. VCC1_OV_RST is cleared if SBC enters the Restart Mode.
  - If CFGP = 0, the SBC Fail-Safe Mode is entered in case of VCC1_ OV.
    Fail-outputs are activated. A Wake event exits Fail-Safe Mode.
    VCC1_OV_RST is cleared if SBC enters the Restart Mode.

1.3.2.1 Device behavior due to VCC1 overvoltage for Config1/3 configuration (CFGP = 1, CFG = 0/1)

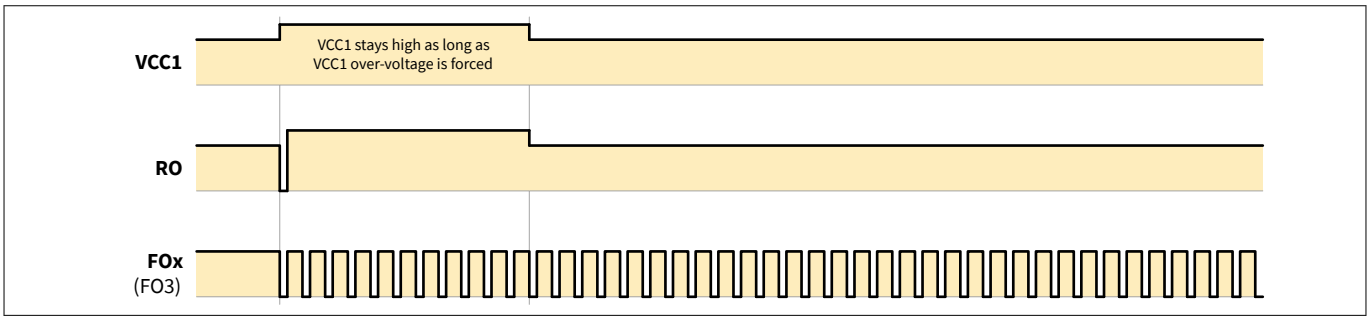

Figure 9 SBC Restart Mode entry due to VCC1 overvoltage

1.3.2.2 Device behavior due to VCC1 overvoltage for Config2/4 configuration (CFGP = 0, CFG = 0/1)

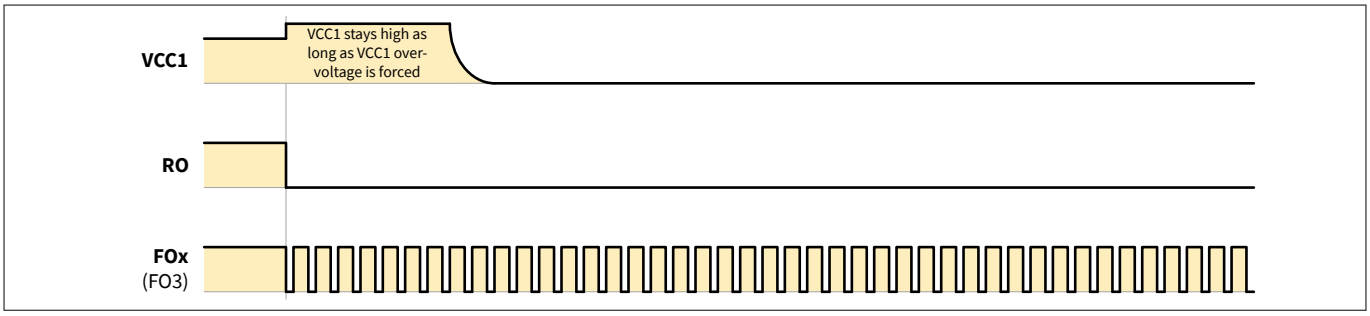

Figure 10 Fail-safe mode entry due to VCC1 OV

1.3.3 Behavior in case of watchdog trigger failure

The device behavior in case of a watchdog trigger failure with the respective configuration is described in the table below.

Table 2 Watchdog trigger failure configuration

Config	INT pin (CFGP)	SPI bit CFG	Event	FOx activation	SBC mode entry
1	External pull-up	1	1 x watchdog failure	after 1st WD failure	SBC Restart Mode
2	No ext. pull-up	1	1 x watchdog failure	after 1st WD failure	SBC Fail-Safe Mode
3	External pull-up	0	2 x watchdog failure	after 2nd WD failure	SBC Restart Mode
4	No ext. pull-up	0	2 x watchdog failure	after 2nd WD failure	SBC Fail-Safe Mode

The respective configuration is stored for all conditions, and can only be changed by powering down the device ($V_S < V_{POR,f}$).
Timing diagrams on the next pages show the behavior described in the table above.

1.3.3.1 Device behavior due to WD trigger failure when Config1 is selected

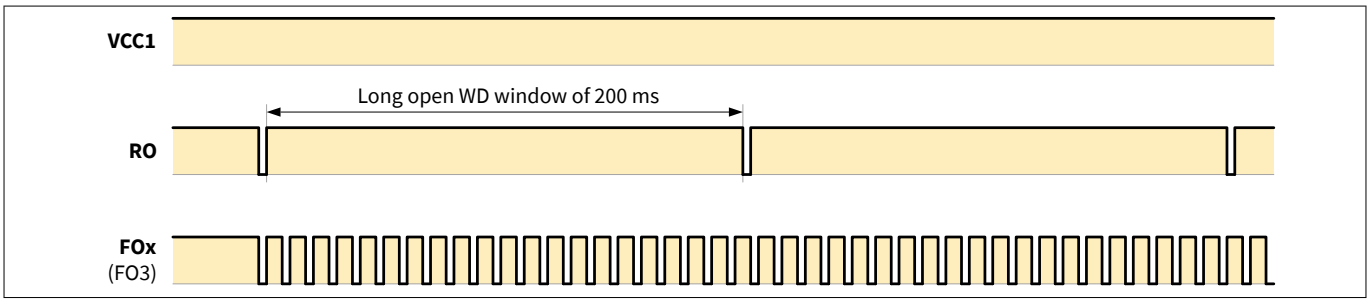

Figure 11 SBC Restart Mode entry and FOx activation after 1st WD trigger failure

1.3.3.2 Device behavior due to WD trigger failure when Config3 is selected

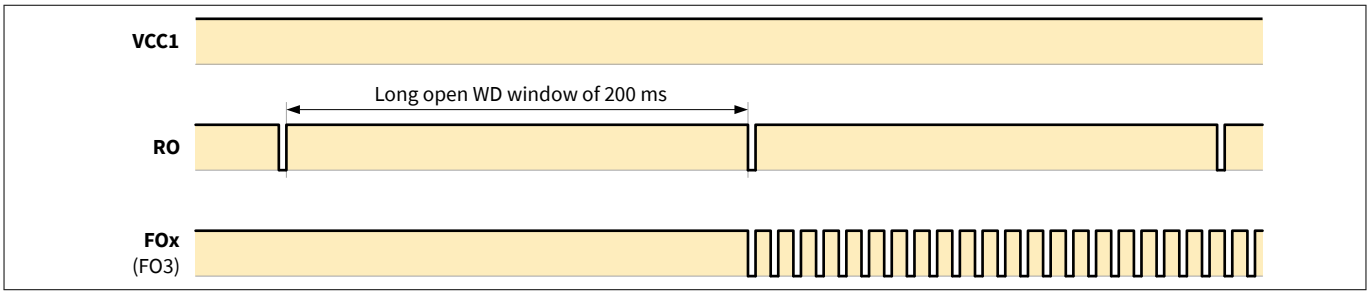

Figure 12 SBC Restart Mode entry due to WD failure and FO activation after 2nd WD trigger failure

1.3.3.3 Device behavior due to WD trigger failure when Config2 is selected

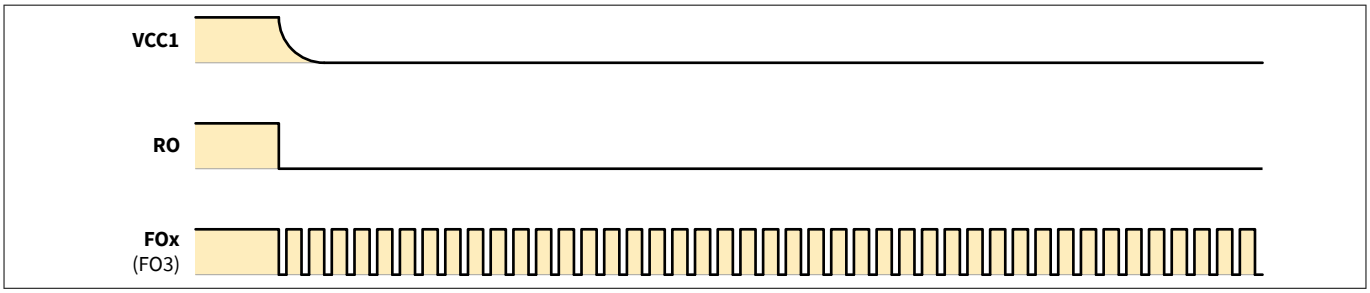

Figure 13 SBC Fail-Safe Mode entry and FOx activation after 1st WD trigger failure

1.3.3.4 Device behavior due to WD trigger failure when Config4 is selected

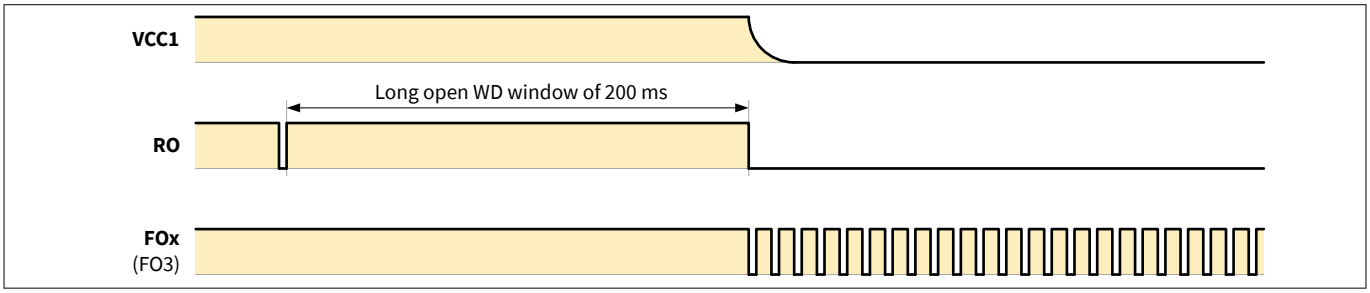

Figure 14 SBC Fail-Safe Mode entry and FOx activation after 2nd WD trigger failure

2 Layout guidelines

2.1 Thermal layout considerations

- For optimum thermal performance, a 4-layer PCB is recommended.
- Cu thickness (35 µm/70 µm; the thicker the better).
- Place as many thermal vias as possible.
- Consider cooling areas:
  - Connect inner GND layers with thermal vias and use for cooling.
  - Try to form a quadratic cooling area ≥ 300 mm^2 underneath the SBC and connect it to the power pad (routing should not go through cooling area).
  - In case the PNP is used for VCC3, then also try to form a cooling area (Note: Connect to VS).
- If possible, do not place the SBC at the edge of the PCB to minimize thermo-mechanical stress.

2.2 EMC layout considerations

- It is recommended to connect all GND pins / tabs together (star GND).
- Route CAN and LIN bus lines separated or even shielded.
- Place SBC and microcontroller (focus on digital I/Os) side by side as close together as possible.
- Place a capacitor (100 nF) for CAN supply close to VCAN and CAN GND (pin 38). Hint: Place a footprint for a 1 µF capacitor in case more than 100 nF would be required.
- Connect CAN GND (pin 38) to GND plane and not to ePad.
- Place ceramic capacitors for VCC1/VCC2 as close as possible to the respective pin.
- For VCC3 stand-alone operation: Place the capacitor for VCC3 (VCC3REF) close to the collector of PNP, and also close to the VCC3REF pin (min. 4.7 µF – regulation point).
- For VCC3 load-sharing operation: Place the capacitor for VCC1/VCC3 (min. 10 µF in this case) close to the VCC1 pin (regulation point).

2.3 ESD layout considerations

- It is recommended to connect all GND pins / tabs together (star GND).
- Route CAN and LIN bus lines separated or even shielded.
- Place SBC and microcontroller (focus on digital I/Os) side by side as close as possible (also to ensure common GND connection).
- In case of off-board usage for e.g. HSx, WKx, place first the serial resistor and then the capacitor directly at the pin (besides the blocking capacitor directly at the connector).

3 Power dissipation and thermal measurements

3.1 Junction temperature measurement

3.1.1 Background

In order to verify the System Basis Chip (SBC) in the application properly, the maximum junction temperature must be determined to derive max. operating conditions and to ensure proper operation.

However, the device junction temperature cannot be directly determined for the SBC family in the application.

The solution is to measure the device temperature on the top of the package, and then to calculate the junction temperature by using the thermal correlation factor Ψ_{JT} (Psi).

The following pages show the boundary conditions and the results with an example.

3.1.2 Boundary conditions for Ψ value calculation

Ψ calculation was done with following conditions/variations:

- 2 different PCB designs with 16 thermal vias each.
- Cooling area on bottom of PCB with 0 mm^2 / 300 mm^2 / 600 mm^2.
- Ambient temperature: 85 °C / 105 °C.

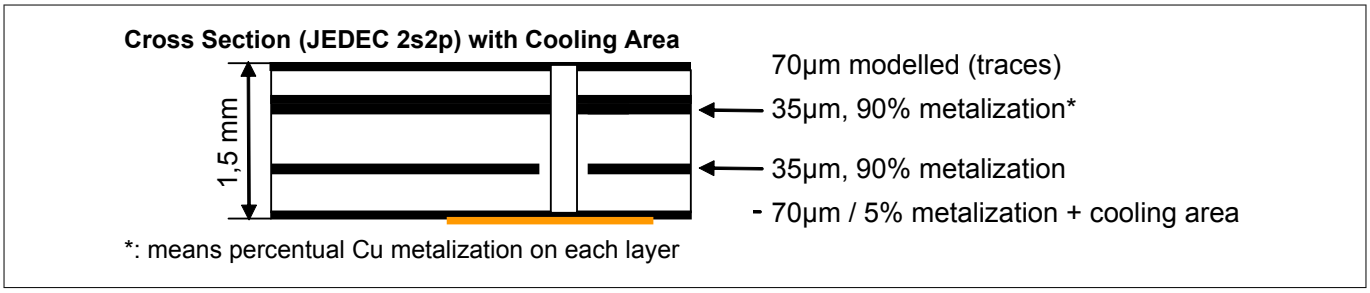

Figure 15 PCB stackup (JEDEC 2s2p) with cooling area

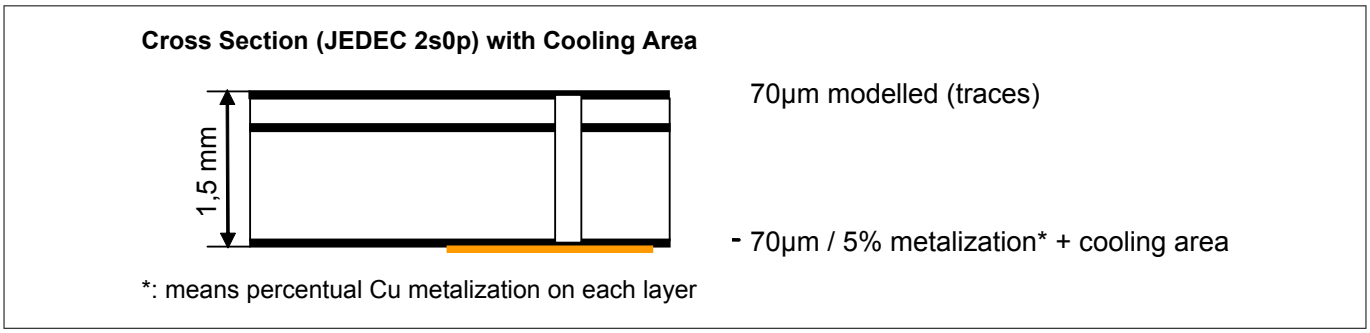

Figure 16 PCB stackup (JEDEC 2s0p) with cooling area

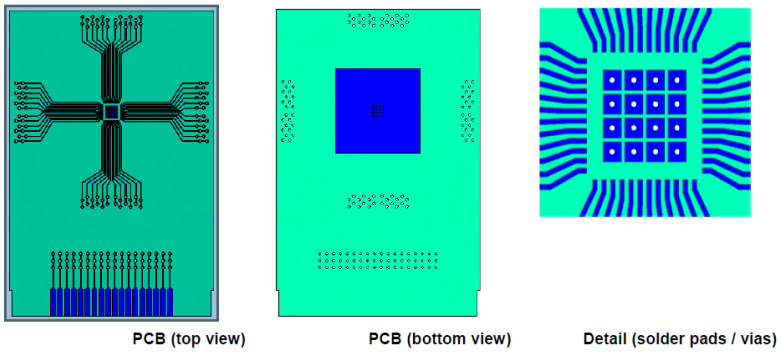

Figure 17 JEDEC PCB Layout

Table 3 Assumption for a nominal power dissipation per power module

Power module	Nominal power dissipation (W)
Chip	0.50
VCC1	0.85
VCC2	0.26
VCC3	0.01
Preregulator	0.07
HS1..4	0.14
Total	**1.83**

3.1.3 Ψ calculation results

The following figure shows the R_{thJA} results with the equivalent Ψ_{JT} values. From these Ψ_{JT} results, the chip temperature can be calculated if the package top temperature and the applied power is known (see ***Chapter 3.1.4***).

2s0p	Cooling [mm²]	600	300	0
	Rth- ja [K/W]	48.2	54.6	73.2
	Psi- jt [K/W]	7.51	7.78	8.59
2s2p	Cooling [mm²]	600	300	0
	Rth- ja [K/W]	31.0	31.7	34.8
	Psi- jt [K/W]	6.87	6.90	7.03

Rth-ja / Psi- jt for Tamb = 85°C

2s0p	Cooling [mm²]	600	300	0
	Rth- ja [K/W]	46.93	53.17	71.63
	Psi- jt [K/W]	7.79	8.05	8.89
2s2p	Cooling [mm²]	600	300	0
	Rth- ja [K/W]	30.63	31.31	34.42
	Psi- jt [K/W]	7.15	7.17	7.31

Rth-ja / Psi- jt for Tamb = 105°C

Figure 18 R_{thJA}/Ψ_{JT} results for both PCB designs

3.1.4 Calculation of the device junction temperature

Natural convection thermal resistance R_{thJA} was determined in accordance with JEDEC JESD51-1 specifications and is calculated with the formula:

$$R_{thJA} = \frac{T_{junction} - T_{ambient}}{P_{dissipation}}$$

Ψ_{JT} is derived under natural convection conditions and provides a correlation between the junction temperature and the temperature on the package's top surface. Because temperature differences are driven by heat flow, the package's top temperature is close to the junction temperature. Ψ_{JT} is calculated with the formula:

$$\Psi_{JT} = \frac{T_{junction} - T_{top}}{P_{dissipation}}$$

The device junction temperature can be calculated by rearranging the formula accordingly:

$$T_{junction} = \left(\Psi_{JT} \cdot P_{dissipation}\right) + T_{top}$$

Example calculation

- Conditions
  - T_{top} = 110 °C
  - $P_{dissipation}$ = 1.83 W
  - PCB type: 2s2p
  - Cooling Area = 300 mm²
  - T_a = 85 °C
  - resulting: R_{thJA} = 31.7 K/W, Ψ_{JT} = 6.9 K/W
- $T_{junction}$ = (6.9 K/W * 1.83 W) + 110 °C = 122.6 °C

4 VCC3 application hints

4.1 Increasing the VCC3 output voltage with external components

VCC3 can be set internally to a nominal voltage of 3.3 V or 1.8 V via SPI. It is not possible to configure VCC3 to a higher voltage (e.g. 5 V). This can be done with an external voltage divider. The example below shows a 5 V output voltage generation for a 3.3 V type.

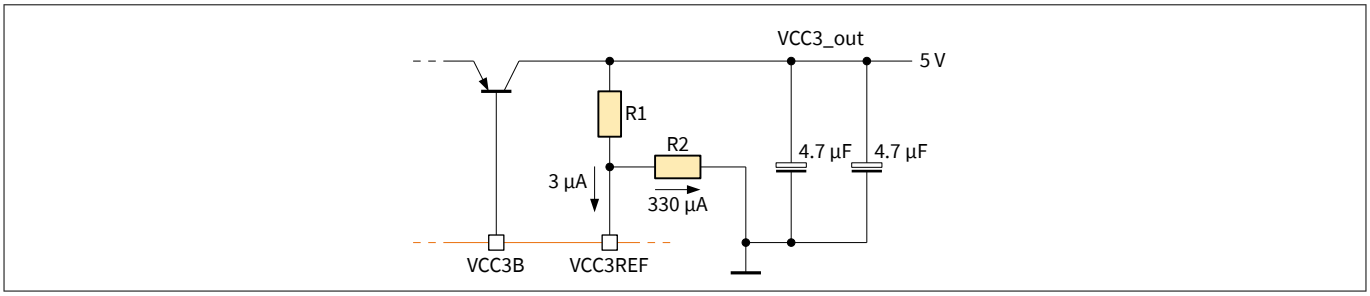

Figure 19 Increasing the VCC3 output voltage

Calculation

Input current on VCC3REF:

$$R1 = \frac{VCC3_{out} - VCC3_{ref}}{I_{R2} + I_{VCC3\_ref}} = \frac{5\,V - 3.3V}{330\mu A + 3\mu A} = 5.11\,k\Omega$$

assuming a typical base current of 3 µA at ambient temperature.

The resulting 330 µA are an optimum choice between circuit robustness and current consumption (see also next page):

$$R2 = \frac{VCC3_{ref}}{I_{R2}} = \frac{3.3\,V}{330\,\mu A\,\cdot} = 10\,k\Omega$$

For a VCC1 = 3.3 V device, VCC3 can be set to 3.3 V or 1.8 V via SPI. But it is not possible to configure VCC3 to 5 V.

The following recommendations should be considered:

- Use 1% (or better) SMD resistors placed very close to the VCC3REF pin.
- Use in parallel 2 x 4.7 µF ceramic, low ESR capacitors (or 1 x 10 µF) to achieve a good regulation performance and place it close to the collector of the PNP.
- Recommended current through R2: 330 µA (optimum choice between current consumption vs. circuit robustness).
- Additional tests are required in the real application board to verify the circuit performance for all boundary conditions of the application.

Regarding the tolerance of the VCC3 output voltage:

- It is estimated as max. additional +/-2% error to the specified output voltage tolerance.
- Assumptions for the error stated above are as follows:
  - The two additional external resistors must be of the same type and from same lot to avoid additional temperature effects.
  - The tolerance can be improved by using 0.1% tolerance resistors.

The same topics apply, of course, also for a 5 V device type.

4.2 VCC3 robustness hints - short circuit of VCC3 against GND for ext. supplies

VCC3 can be used in the stand-alone configuration to supply external loads. In the event of a short circuit to GND, negative voltage undershoot can occur due to resonance of the output capacitor/wire inductance combination. The absolute maximum ratings of the device (e.g. VCC3REF pin) can be exceeded. In order to limit such effect, the load should be connected close or a resistor R_{Lim} of about 100 Ohm can be inserted (see ***Figure 20***). The electrical functionality of the regulator remains unchanged.

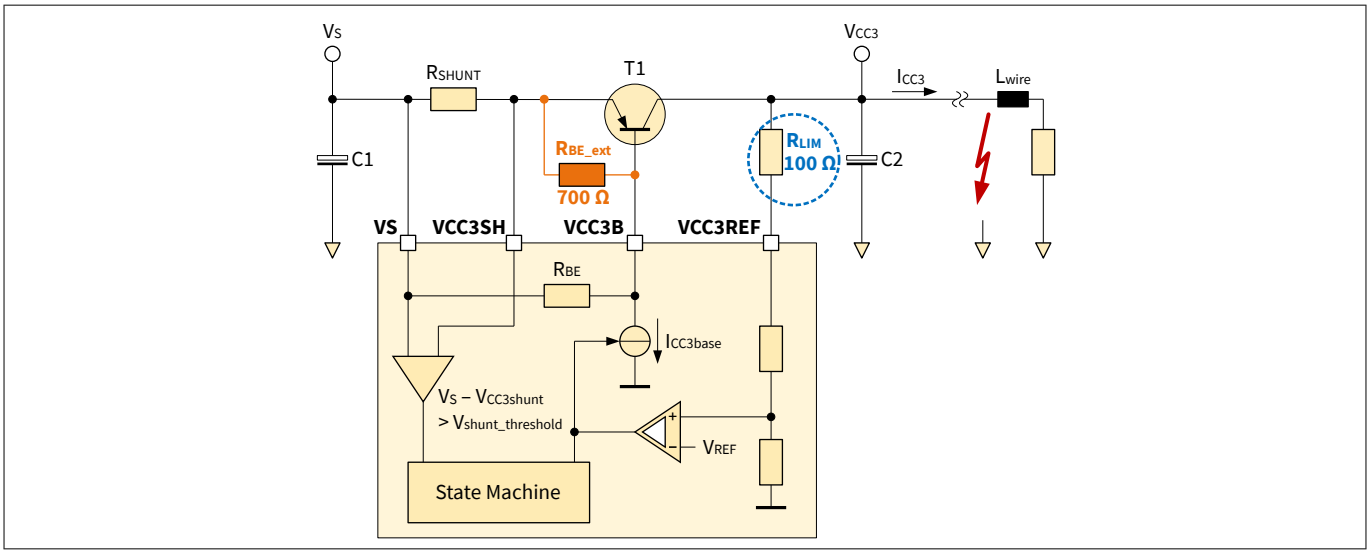

Figure 20 VCC3 external supply with robustness for short circuit against GND

4.3 VCC3 robustness hints - protection against increased VCC3 output voltage

Under worst case conditions (dirt, humidity, icing, …), an external leakage path from the base of the PNP (VCC3B) to GND can occur. A respective leakage current causes an increased output voltage when VCC3 is on, which could violate the max. ratings of VCC3. In addition, the output voltage could rise when VCC3 is OFF. The device has an internal protection circuitry which prevents the above mentioned behavior. The protection circuitry can compensate a leakage current of ~200 µA on VCC3B, and can sink 2.5 mA on VCC3REF (see ***Figure 20***).

If the leakage current on VCC3B exceed the value stated above, an external resistor R_{BE_EXT} of about 700 Ohm can be inserted to further compensate excessive leakage currents. This applies to VCC3 stand-alone as well as load sharing configuration. The functionality of the regulator remains unchanged. However, additional currents contribute to the SBC overall current consumption.

4.4 Increasing the power dissipation capability of VCC3

The VCC3 load sharing feature is intended to increase the current capability of the SBC power supply by distributing the power dissipation (see also Chapter 8.2.2 "External Voltage Regulator in Load Sharing Mode" in the product datasheet). This can be further distributed by using the load sharing feature with multiple PNP devices (e.g. 2 instead of only 1). The topics below should be considered and carefully analyzed.

VCC3 application hints

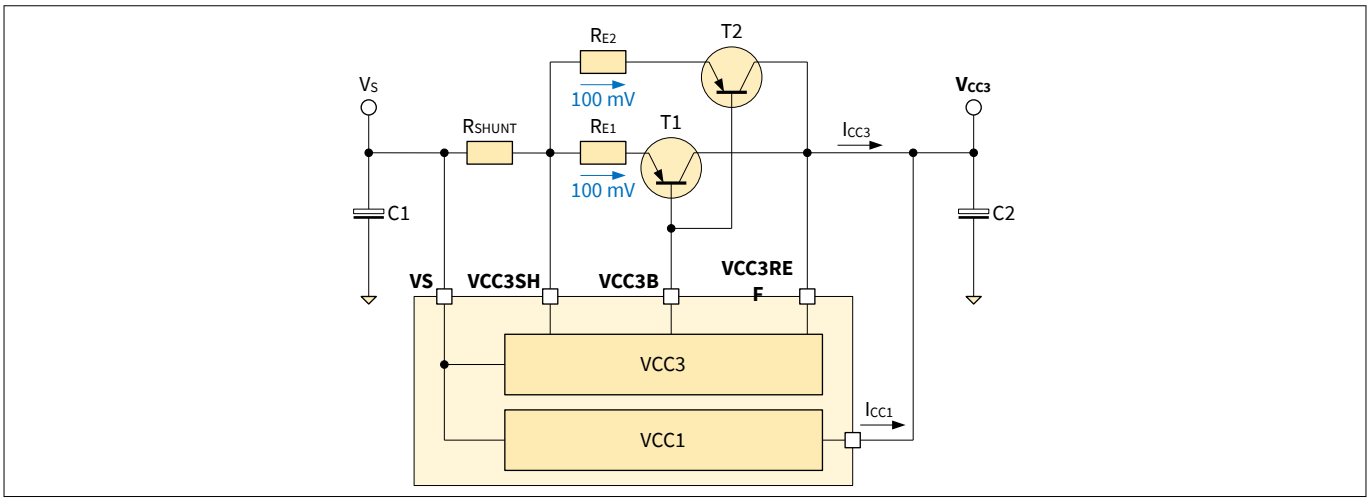

Figure 21 Increasing the power dissipation capability of VCC3

- The base current capability of VCC3B (P_8.6.1) must not be exceeded.
- The layout must be done carefully to avoid an instable regulation loop.
- This applies also to stand-alone configuration of VCC3.
- The current gains of the PNP vary and one device could take over all the current. To prevent this situation, the insertion of emitter resistors is recommended to achieve a negative current feedback. The voltage drop across the resistors shall be approx. 100 mV.

5 High-side outputs

5.1 Parallel switching

5.1.1 Background

- Certain loads require more current (peak or permanent load) or lower R_{on} than one HS switch (integrated in the MR+ SBC Family) can provide.
- To double the HS switch current capability or lower the R_{on}, it is possible to combine two HS switches and enable/disable them at the same time. The switches must be in the same register to ensure same switching timing, i.e. combine HS1 & HS2 (in register HS_CTRL_1) and/or HS3 & HS4 (in register HS_CTRL_2).
- There are certain aspects which need to be considered in order to ensure a proper operation:
  - Total current not exceeding 2x overcurrent threshold.
  - Total chip power dissipation not leading to overtemperature.
  - Temperature gradients between two HS switches not too high.
  - Process variation of HS switch parameters.

5.1.2 Statistical data of R_{on} vs. temperature

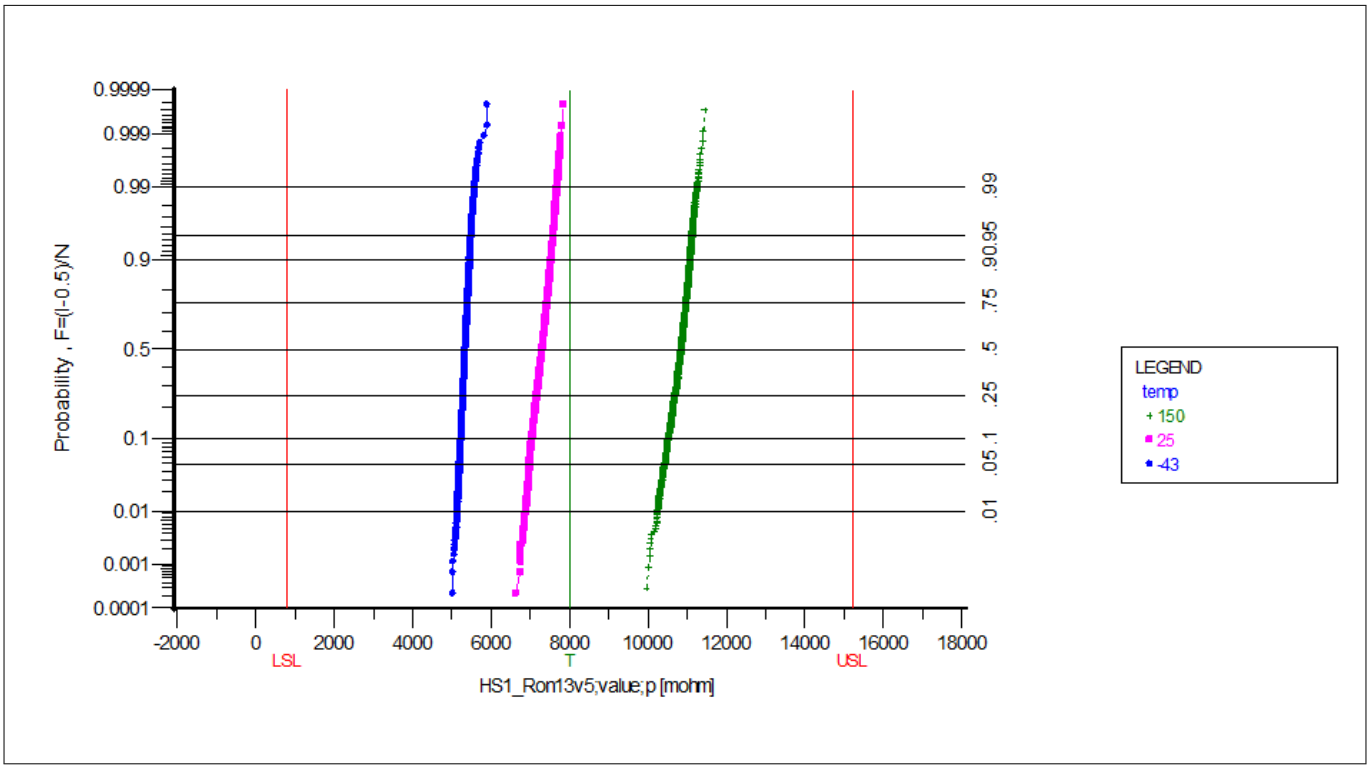

Figure 22 R_{on} of HS1 at V_S = 13.5 V

R_{on} is strongly depending on temperature, but same statistical behavior applies to all switches an VS voltages → same power dissipation within two parallel switches.

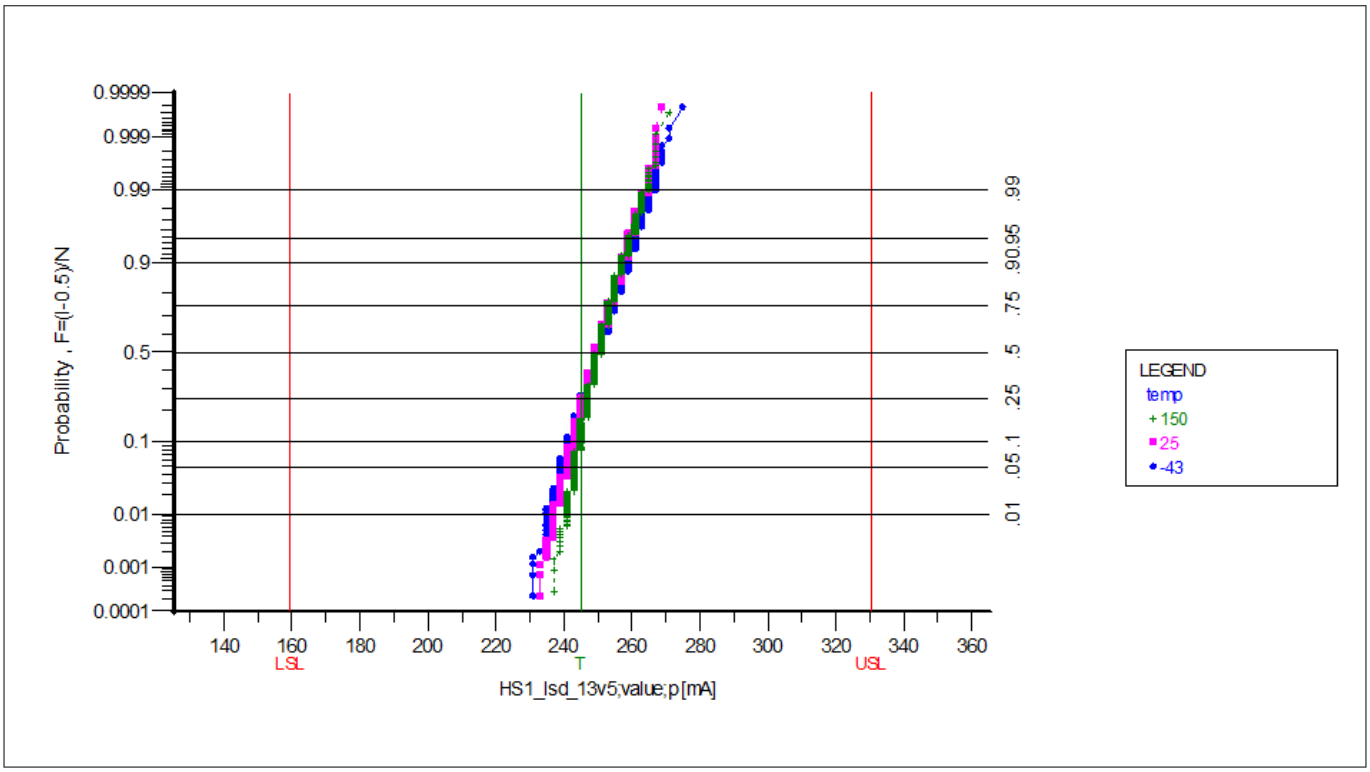

Figure 23 HS1 at V_S = 13.5 V

The overcurrent threshold is nearly independent from temperature and VS voltage variation, and shows the same behavior for all switches → switches have same overcurrent shutdown threshold.

5.1.3 Total chip power dissipation with two HS switches enabled in parallel

- The total chip power dissipation must always be considered including PCB properties, layout, etc.
- This is especially true when high loads are driven from the HS switches, e.g. parallel switching of HS1/2.
- Depending on the current, the HS switches can be a big contributor to the power dissipation.
- To limit the internal HS switch current, the load-sharing configuration of VCC1 & VCC3 should be considered.
- The Power Dissipation Tool (www.infineon.com/sbc) can be used to estimate the total power dissipation of the device per module.

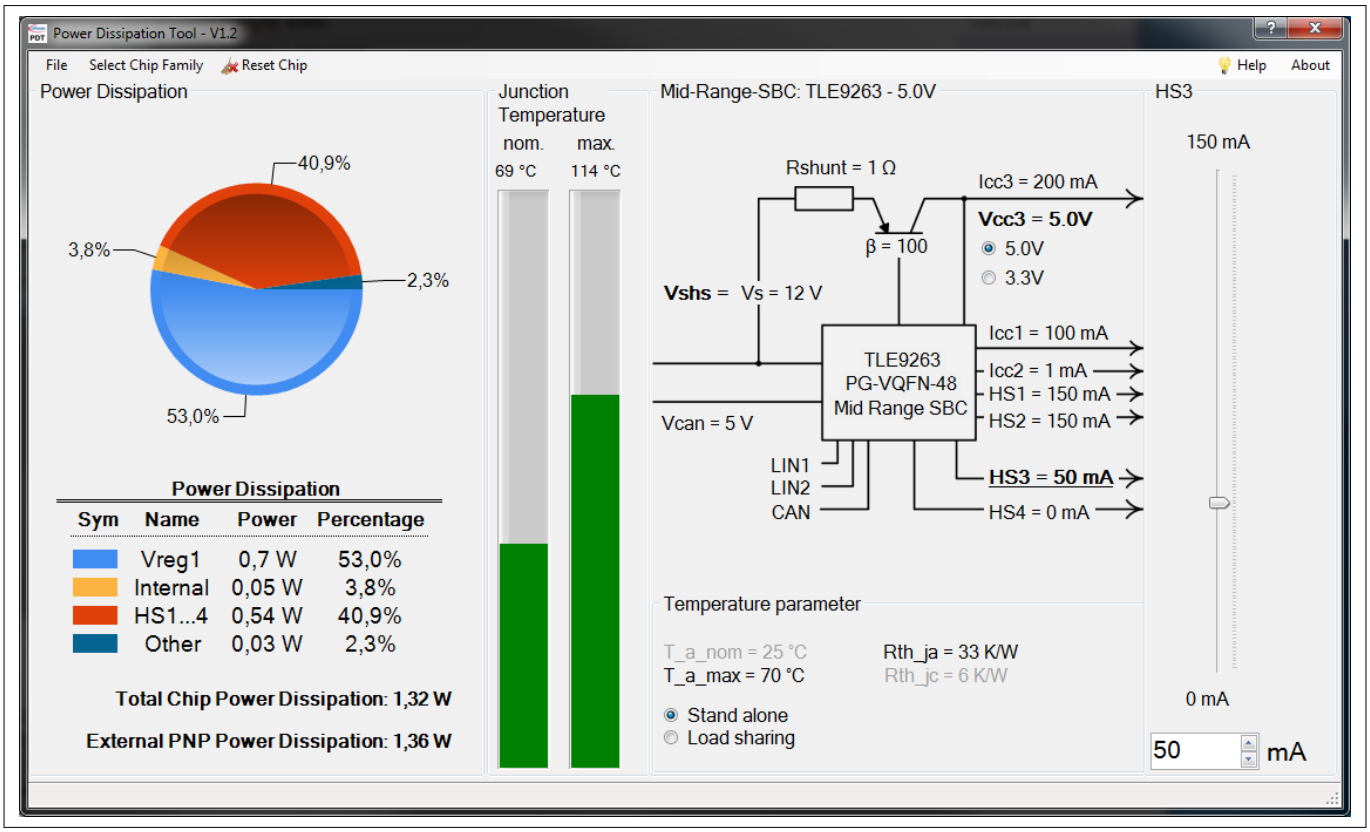

Figure 24 Power Dissipation Tool GUI

5.1.4 Temperature gradients between two neighboring HS switches

- The HS switches are thermally coupled on the silicon (see ***Figure 25*** with simulation results of layout).
- Even if only one HS switch is conducting 250 mA (here HS4), the temperature difference to the neighboring HS switch is ~20 °C.
- If two HS switches are enabled at the same time, it can be assumed that both switches have nearly the same junction temperature, and thus the same R_{on}.

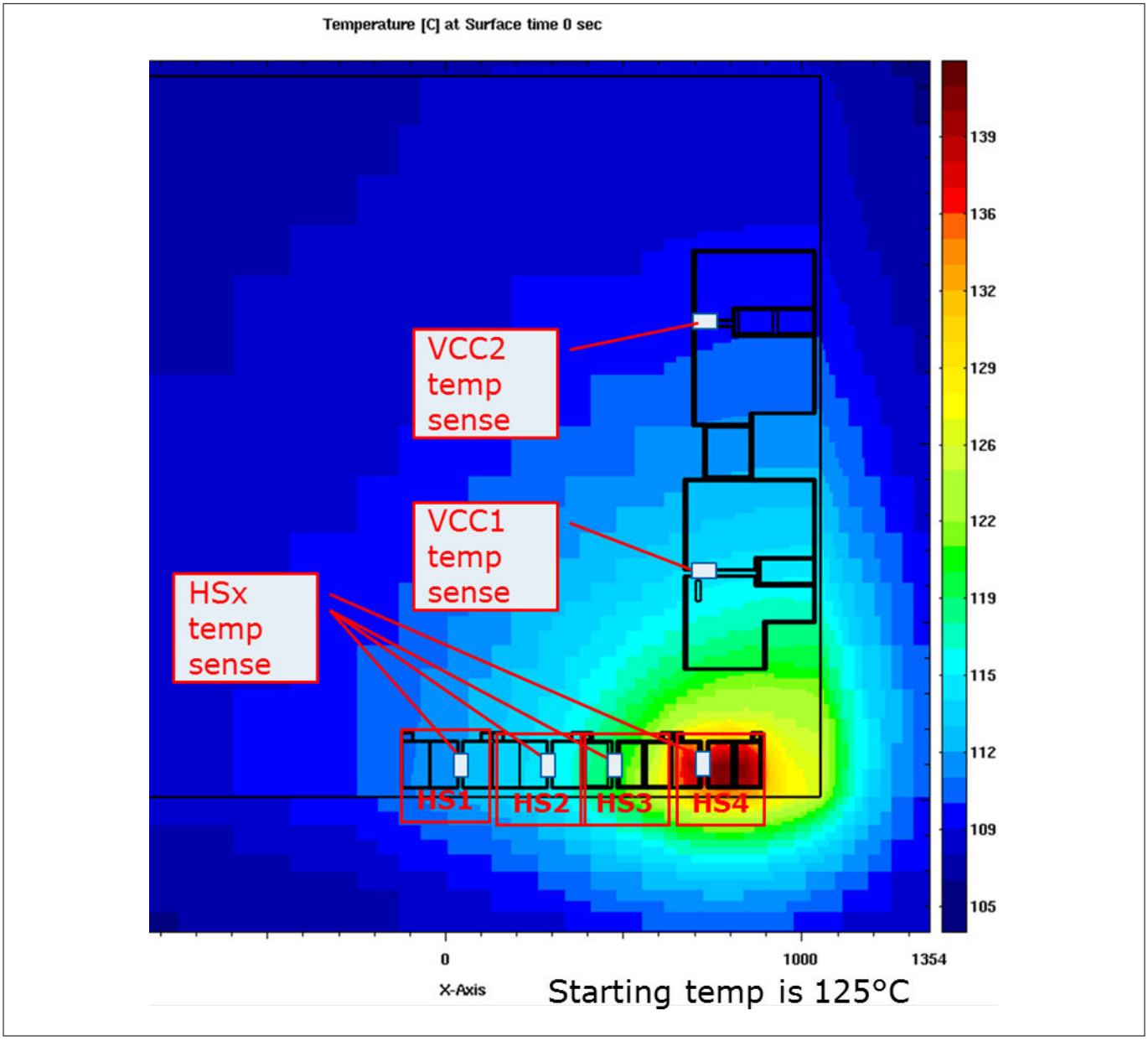

Figure 25 Heat distribution around HS switches

5.1.5 Process variation of HS switch parameters

- The HS switches are physically located very close to each other.
- All HS switches have identical circuitry and layout.
- It can be assumed that process variation is negligible in a first approximation.
- Due to this fact, life time effects can also be neglected.

5.1.6 Conclusions

- Parallel operation of two HS switches, which are located in the same SPI register, is possible to increase the output current.
- To ensure a proper operation, the application must ensure the topics listed below:
  - The total current is not more than 2x the min. current limit of both HS switches.
  - The overall power dissipation within the chip does not trigger a thermal shutdown.
  - The temperature gradient within High-Side switches and the process variation can be neglected in this case.
- In case the R_{on} must be lowered, the same method is possible to connect two HS switches in parallel. If the total load current does not exceed the min. overcurrent limit of one HS switch, it is also possible to connect 3 or 4 switches together. The open load threshold must be considered for each switch.

5.2 High-side inverse current behavior

5.2.1 Definition of inverse current

- An HSx is operating in inverse current mode (current flow from source to drain) if the voltage condition $V_{HSx} > V_{VSHS} > 0$ V applies (see ***VSHS back supply*** on page 32).
  - Such a condition could occur if an HSx is shorted to $V_{bat} > V_{VSHS}$ due to the reverse battery protection diode at VSHS and/or a voltage shift between different battery feats.
- An inverse current I_{HS_Inv} flows immediately if the shorted HSx output (HSx_SC) is in ON state and $V_{HS,max} > V_{VSHS}$. In OFF state, I_{HS_Inv} flows over the body diode earliest when the specified max. rating $V_{HS,max} > V_{VSHS} + 0.3$ V is exceeded.

Note: No protection mechanism like temperature protection or overload protection is active during applied inverse currents. Inverse currents cause power losses inside the DMOS, which increase the overall device temperature. An HSx output short to battery diagnostic is not specified, and there is no dedicated diagnostic bit available.

5.2.2 Possible inverse current flow scenarios

Assuming a separate reverse battery protection diode at VSHS, the following inverse current flow scenarios are considered (see ***Internal back supply scenarios***):

- Scenario 1: Back supply of integrated LIN-transceiver(s), HSx and GPIOx configured as HS in ON state (see also ***VSHS back supply***).
  - Typ. inverse current flow of 15 mA per LIN transceiver + load current of enabled HSx (switched ON) + GPIOx.
- Scenario 2: As scenario 1 + external load sharing same reverse battery protection VSHS diode.
  - Typ. inverse current flow of 15 mA per LIN transceiver + load current of enabled HSx + GPIOx + current of external load.
- Scenario 3: VS and VSHS share the same reverse battery protection diode.
  - In addition to the back supplied blocks (LINx + HSx + GPIOx), the current of VCC1, VCC2 and internal consumption (typ. 3.5 mA) has to be considered as total inverse current.
  - External loads sharing the same reverse battery protection have to be considered as well.

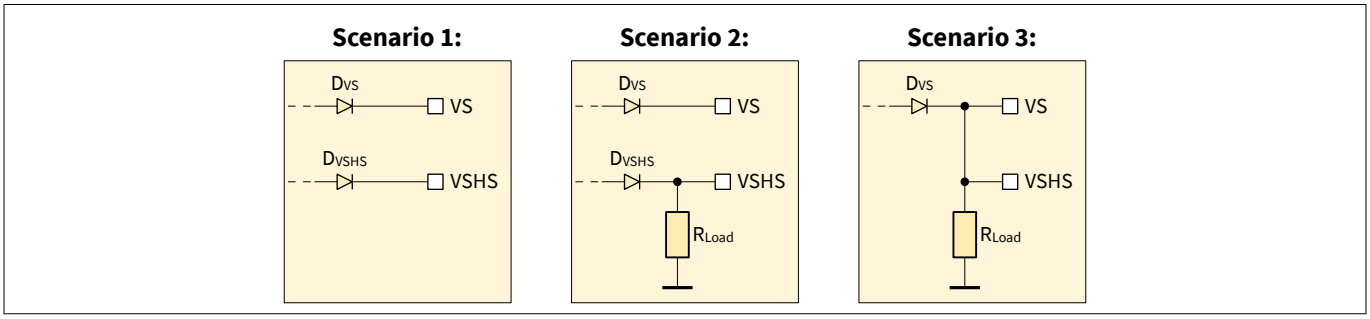

Figure 26 Internal back supply scenarios

5.2.3 Block Diagram

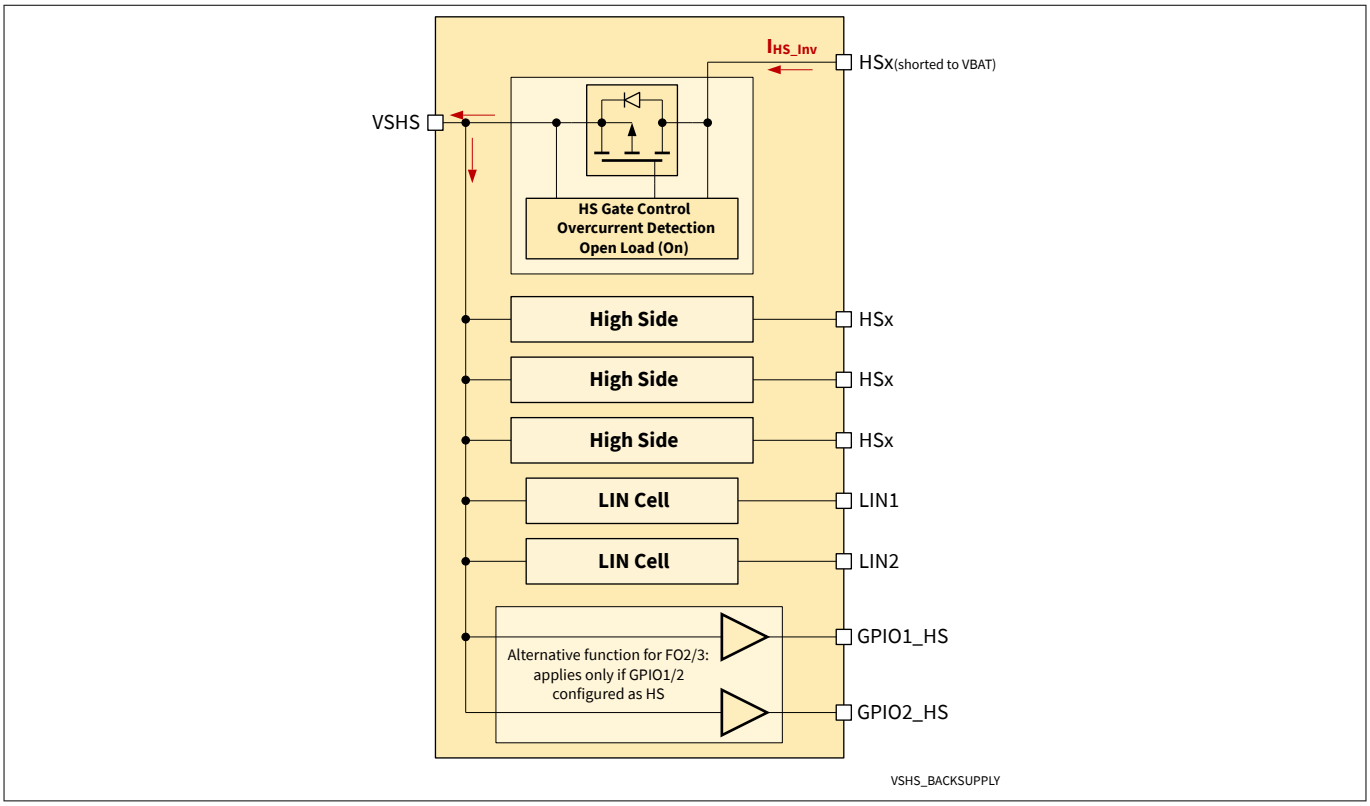

Figure 27 VSHS back supply

5.2.4 Product behavior in case of inverse current

The following inverse current behavior ($V_{HSx} > V_{VSHS}$) can be observed due to parasitic effects:

- $HSx_{(shorted\ to\ VBAT)}$ in ON-state:

  Note: The open-load bit is set as expected for inverse currents $I_{HS\_Inv} > 0$ mA, but only if the respective HSx is longer enabled than the open-load filter time (t_{OL_HS}).

  - $HSx_{(shorted\ to\ VBAT)}$ is switched OFF if the $I_{HS\_Inv\_1}$ ~90 mA.
  - Open-load (OL) and overcurrent (OC) bit of respective shorted $HSx_{(shorted\ to\ VBAT)}$ are set. OC is set for HSx, which were enabled.
  - Other enabled HSx are switched OFF (in addition to $HSx_{(shorted\ to\ VBAT)}$).
- $HSx_{(shorted\ to\ VBAT)}$ in OFF-state:

  Note: The value of $I_{HS\_Inv\_2}$ depends on the number of HSx switched ON and on the total HSx load current.

  - Enabled HSx is switched OFF if the $I_{HS\_Inv\_2}$ ~380 mA.
  - OC bit of respective enabled HSx switching OFF will be set.
- $HSx_{(shorted\ to\ VBAT)}$ and HSx in OFF-state:
  - If $I_{HS\_Inv\_3} > 1$ A, the overtemperature bit (TSD1) is set.
  - Can only occur for scenario 2 or 3 (see ***Possible inverse current flow scenarios*** on page 31).

5.2.5 Possible software strategy

The failure signatures listed below can be used as an inverse current failure indication ($V_{HSx} > V_{VSHS}$).

- Simultaneous shutdown of all activated switches and no TSD signalized (i.e. TSD1 bit is not set).

  Note: Also unused HSx switches can be turned on for this diagnosis (consider additional device current consumption).

- Both OL (open load) & OC (overcurrent) bits are set simultaneously if a certain inverse current flows (and the respective switch was ON for longer than the open-load filter time).

This failure signature shall be used to avoid continuous or repetitive inverse current mode.

5.2.6 Application recommendation

- An HSx short to battery is an unlikely, but not avoidable failure case.
- Therefore, the following needs to be considered in case of an inverse current failure occurrence:
  - Such inverse current mode can be detected once the inverse current exceeds the mentioned currents $I_{HS\_Inv\_1} > 90$ mA or $I_{HS\_Inv\_2} > 380$ mA.
  - To avoid a reliability or life time issue, Infineon strongly recommends not to exceed an inverse-current of maximum 500 mA. This has to be ensured by the application design.
  - A series diode should be placed on an HSx output if a short to Vbat can occur and an open load has to be detected under all conditions, or if the inverse current might exceed > 500 mA.

5.3 PWM hints with high-side switches

5.3.1 Background: PWM generation

- The MR+ SBC family offers the possibility to control the high-side switches with PWM.
- Two 8-bit PWM generators can be assigned to any of the four high-side switches. The frequency of the PWM generators can be configured with 200 Hz or 400 Hz.
- The PWM generators can be set between 0% and 100% duty cycle. The high-side switches have an integrated slew rate control to optimize the emission behavior. Therefore, the actual minimum duty cycle for a frequency of 200 Hz/400 Hz is 2 resp. 4 digits.
- The PWM operation is controlled by the SBC once the configuration is completed.
- In case the automatic PWM generation is not possible, it can also be generated via SPI.

5.3.2 Automatic PWM generation by the SBC

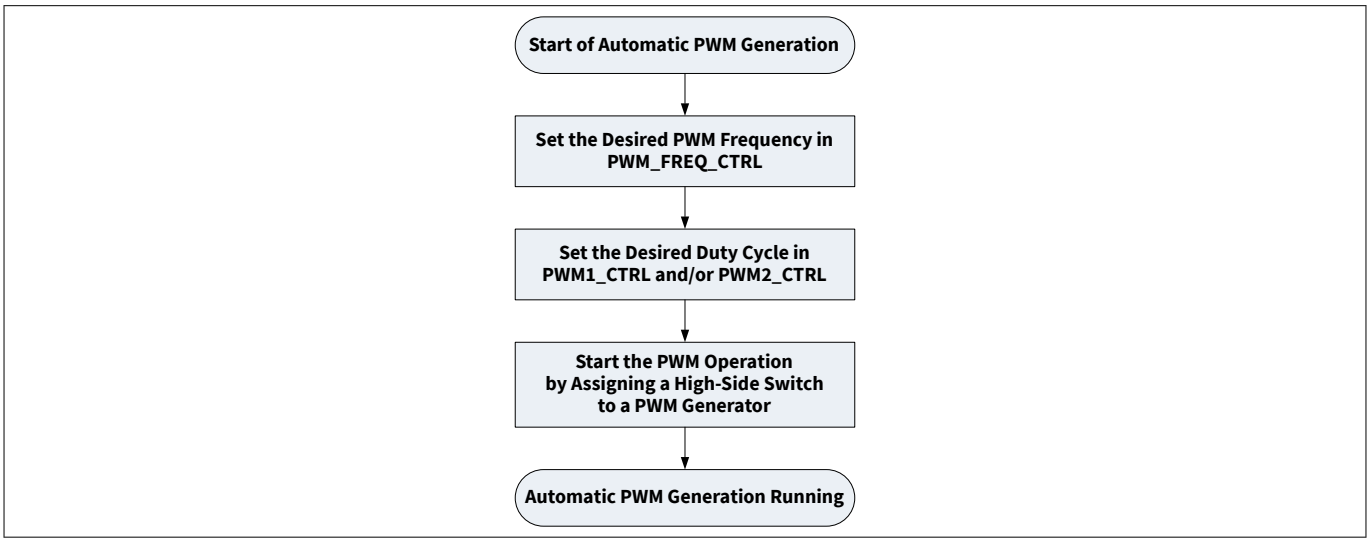

Figure 28 Configuration of the PWM generation

Remarks

- The PWM generation starts with the assignment of the PWM generator high-side.
- It takes ~10 µs after the CSN goes High, until the respective high-side switch is enabled (see ***Delay after SPI command is sent*** on page 35).
- The PWM generation always starts with the on-time (see ***HS1 with PWM generator 1, frequency 200 Hz, 10% duty cycle*** on page 35).
- The duty cycle can be changed any time during the operation without any spikes. The new duty cycle starts once the SPI command is sent (see ***HS1 with PWM generator 1, frequency 200 Hz, 10% duty cycle*** on page 35 and ***HS1 with PWM1, frequency 200 Hz*** on page 36).

5.3.2.1 Start of PWM generation

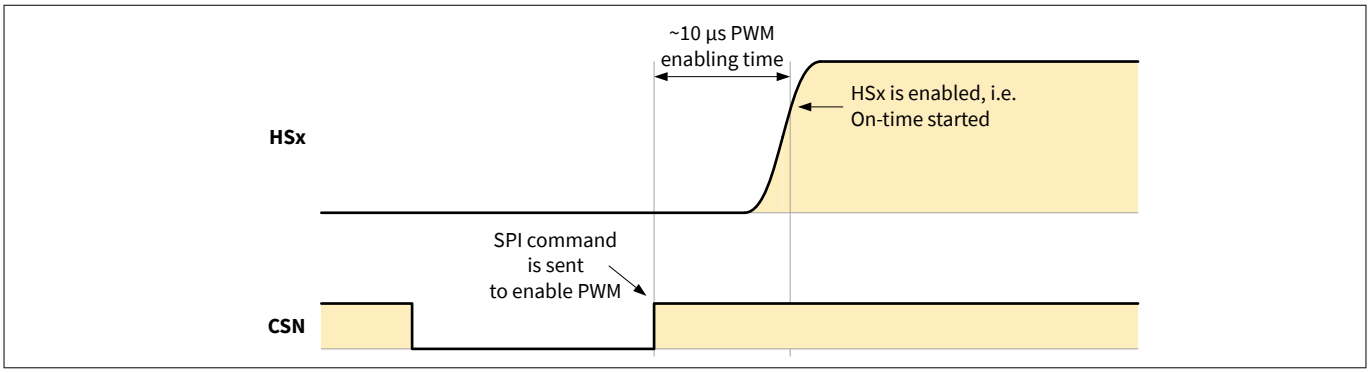

Figure 29 Delay after SPI command is sent

5.3.2.2 Example for PWM generation

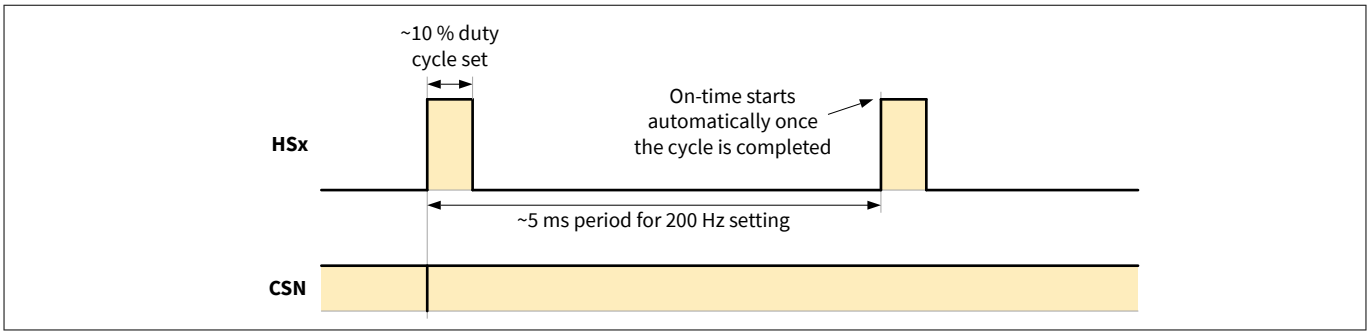

Figure 30 HS1 with PWM generator 1, frequency 200 Hz, 10% duty cycle

5.3.2.3 Example for duty cycle interruption

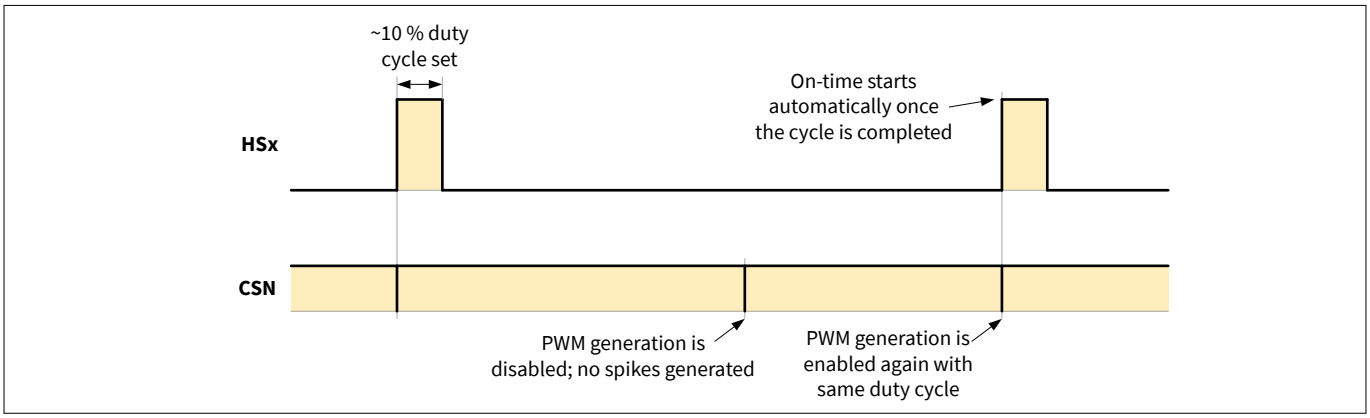

Figure 31 HS1 with PWM generator 1, frequency 200 Hz, 10% duty cycle

5.3.2.4 Example for changing duty cycle

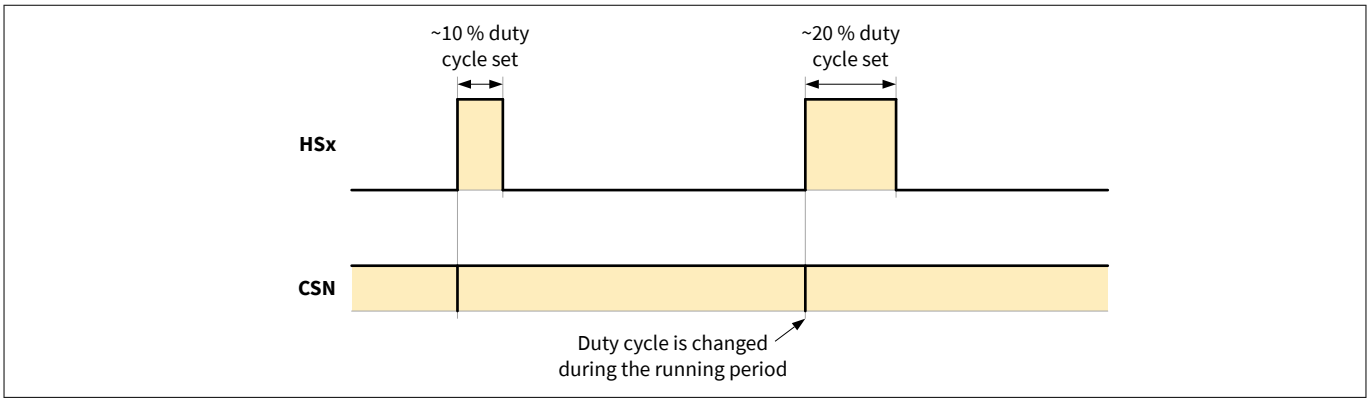

Figure 32 HS1 with PWM1, frequency 200 Hz

5.3.3 Manual PWM generation

Manual PWM generation via SPI - in case the automatic PWM generation needs to be controlled by an external event:

- Use case: The HS on-time is triggering an ADC conversion.
- Sequence as shown below – the ADC conversion should only start with an external trigger – therefore, the SBC internal PWM logic cannot be used, but the PWM is generated via SPI.

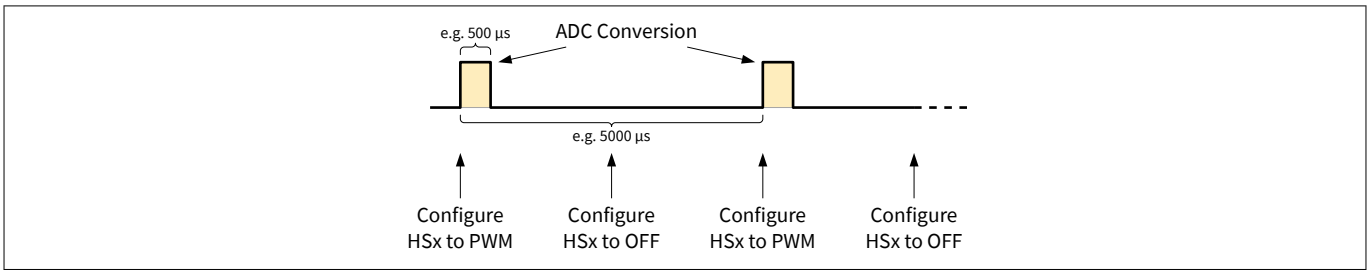

Figure 33 PWM generation via SPI

5.3.3.1 Possible SPI sequences

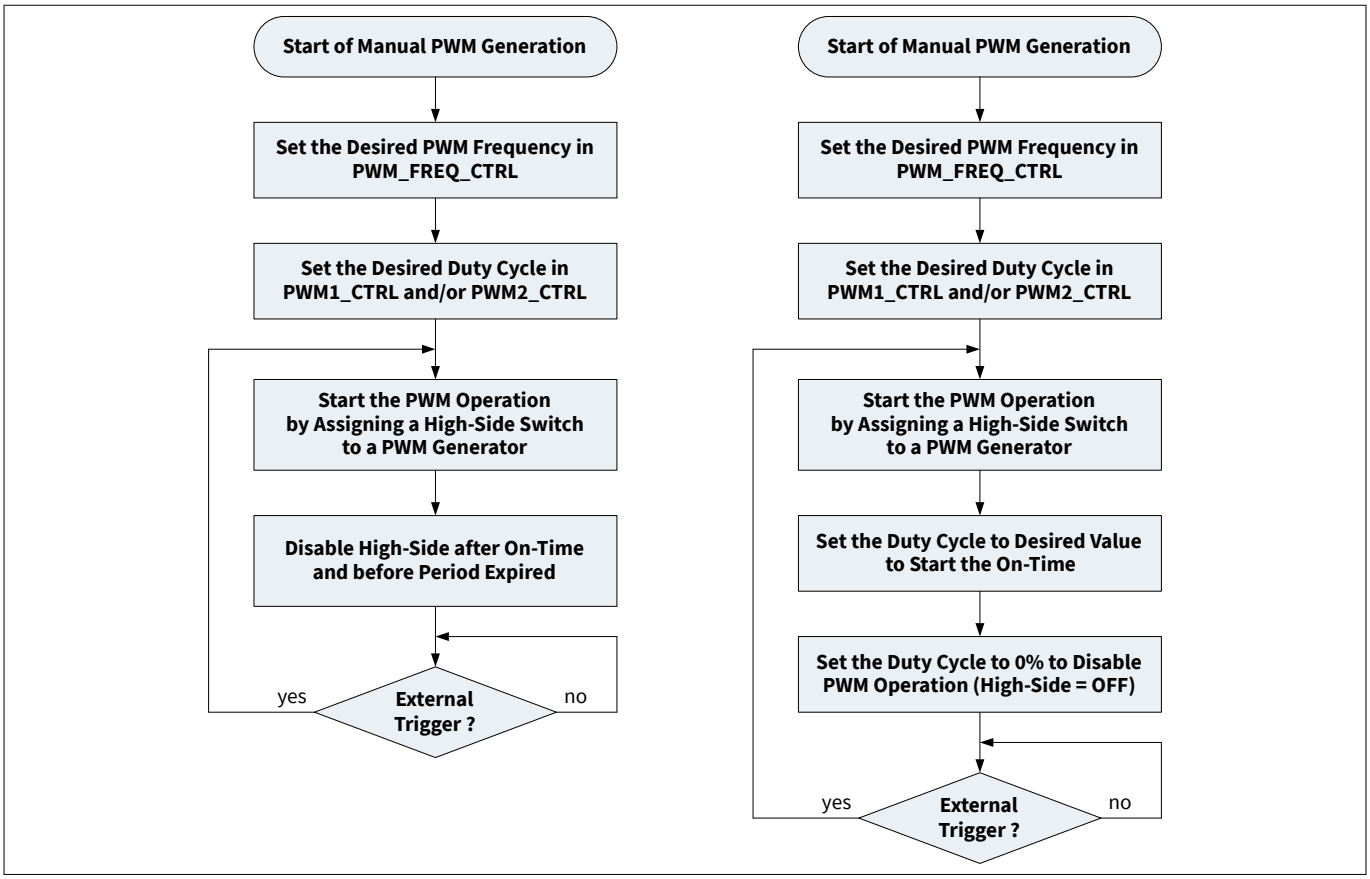

Figure 34 Manual PWM generation via SPI

Remarks

- A manual PWM operation can be achieved by:
  - Enabling and disabling the respective high-side switch.
  - Setting and clearing the respective duty cycle.
- The duty cycle can be changed any time during the operation without any spike generation on the respective high-side switch.

5.3.3.2 Example: PWM generation

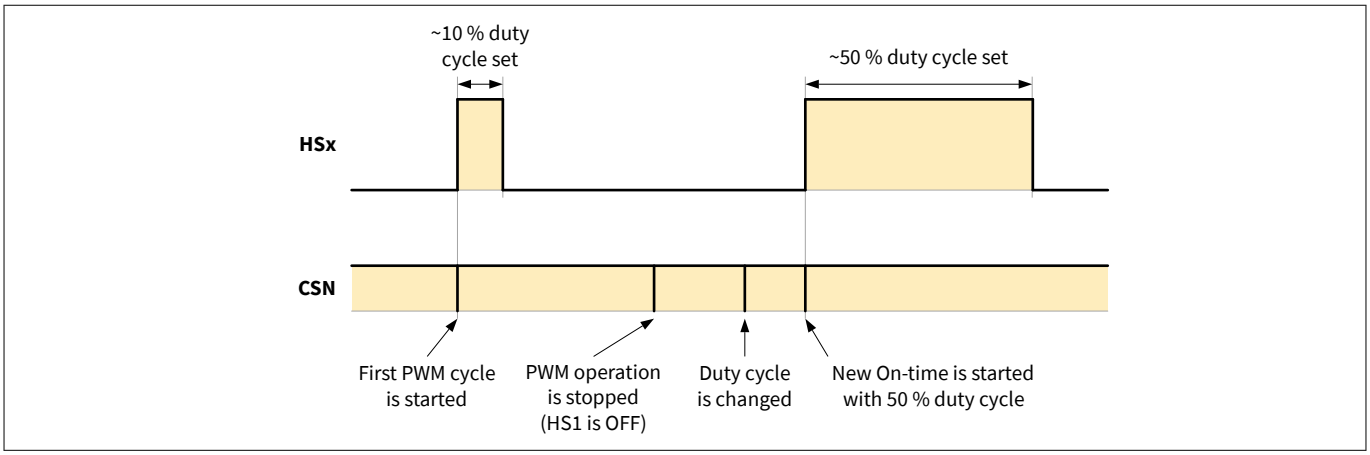

Figure 35 HS1 with PWM1, frequency 200 Hz

5.3.3.3 SPI command example for PWM generation

- Example shows a manual PWM generation via SPI (corresponds to example above).
- PWM is generated manually by setting and clearing the PWM_CTRL register.
- The duty cycle can be modified at any time.

Table 4 SPI commands and responses

Step	Command	To SBC		From SBC	
0	PWM1_CTRL to 10%	0x1998	0001 1001 1001 1000	0x0080	0000 0000 1000 0000
1	PWM1_Freq_200Hz	0x009C	0000 0000 1001 1100	0x0080	0000 0000 1000 0000
2	HS1_2_PWM1	0x0494	0000 0100 1001 0100	0x0080	0000 0000 1000 0000
3	Delay of 1 ms				
4	PWM1_CTRL to 50%	0x8098	1000 0000 1001 1000	0x1980	0001 1001 1000 0000
5	PWM1_CTRL to 0%	0x0098	0000 0000 1001 1000	0x8080	1000 0000 1000 0000

6 CAN partial networking hints - SWK configuration & activation

6.1 Background

The CAN partial networking feature allows to reduce the current consumption of ECUs on the CAN network by selectively enabling/disabling ECUs (if needed or not).

The MR+ SBC family includes variants featuring the CAN partial networking function according to ISO11898-6 (will be integrated in the revised ISO11898-2).

This document describes all necessary configuration and activations tasks needed to properly use the CAN partial networking (= SWK) feature.

Reference is the TLE9263-3BQX Rev 1.1 datasheet.

6.2 Overall SWK configuration & activation sequence

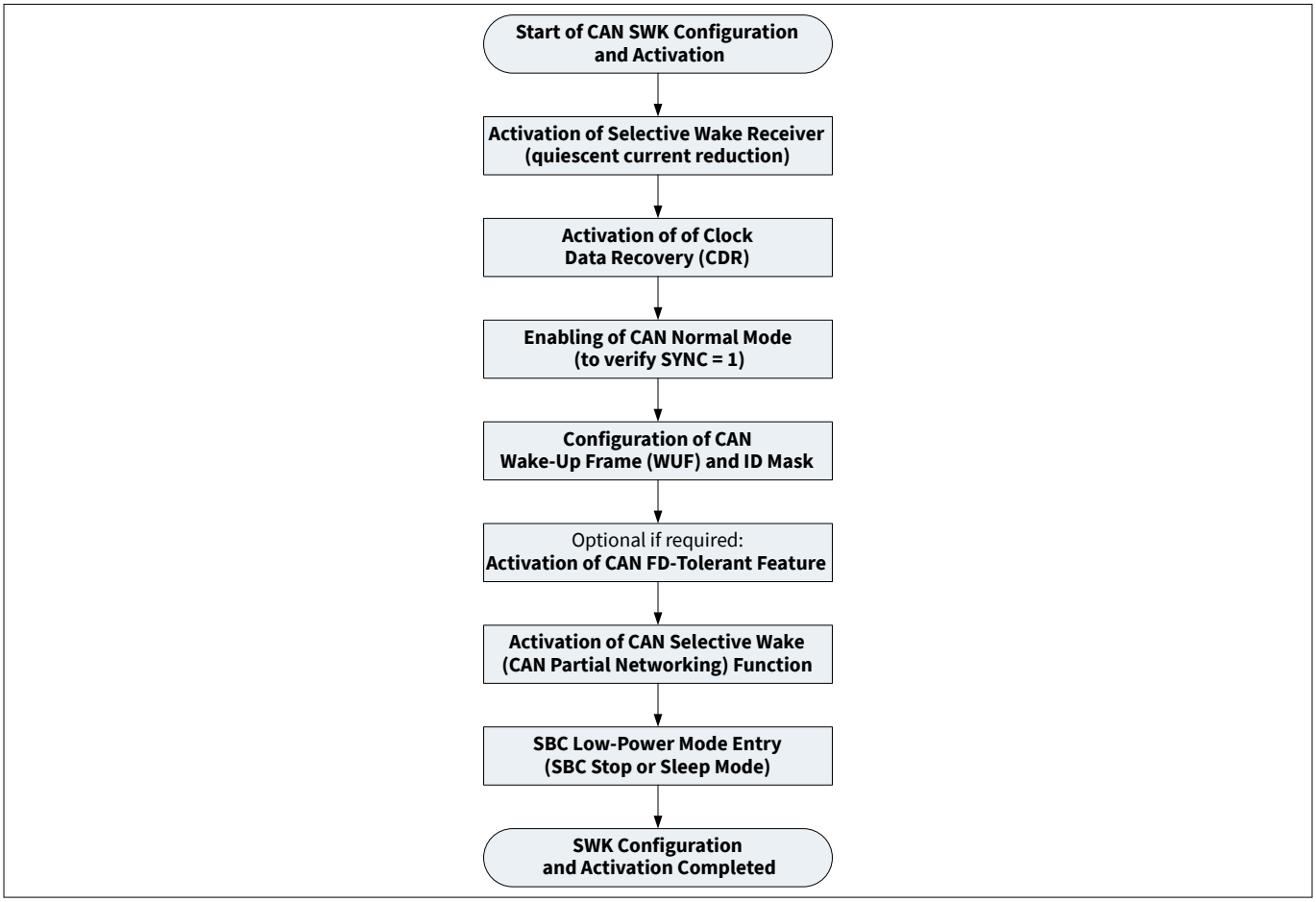

Figure 36 Overall SWK configuration & activation sequence

For a detailed explanation of the different sequence steps, see below:

- Activation of Selective Wake Receiver, see ***Chapter 6.3***.
- Activation of Clock Data Recovery (CDR), see ***Chapter 6.4***.
- Configuration of CAN Wake-Up Frame (WUF), see ***Chapter 6.5***.
- Activation of CAN FD tolerant feature, see ***Chapter 6.6***.

CAN partial networking hints - SWK configuration & activation

- Activation of CAN Selective Wake Function, see ***Chapter 6.7***.
- SBC low-power mode entry, see ***Chapter 6.8***.

6.3 Activation of the Selective Wake Receiver

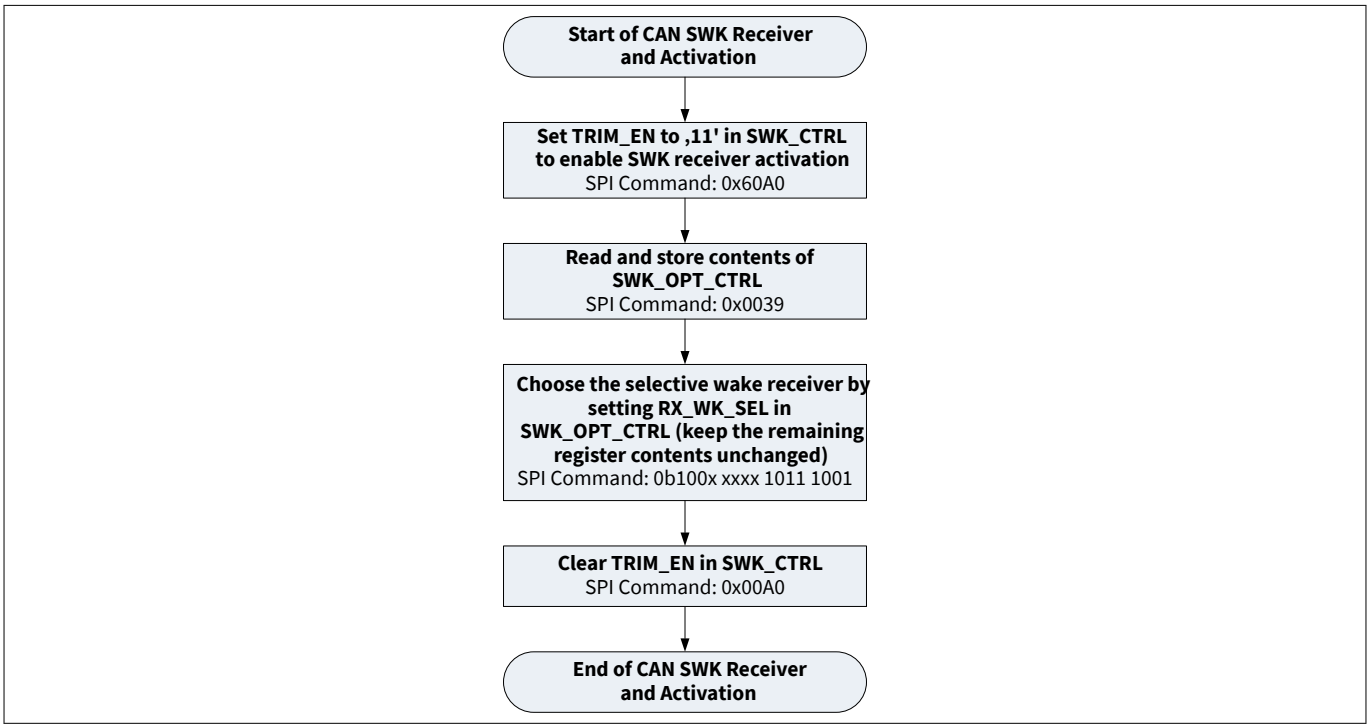

Figure 37 Activation of the Selective Wake Receiver

The activation of the selective wake receiver reduces the quiescent current consumption by around 500 µA.

Once partial networking is deactivated and the regular CAN communication is resumed, the Normal Mode receiver is activated again or needs to be activated again.

6.4 Activation of the Clock Data Recovery (CDR)

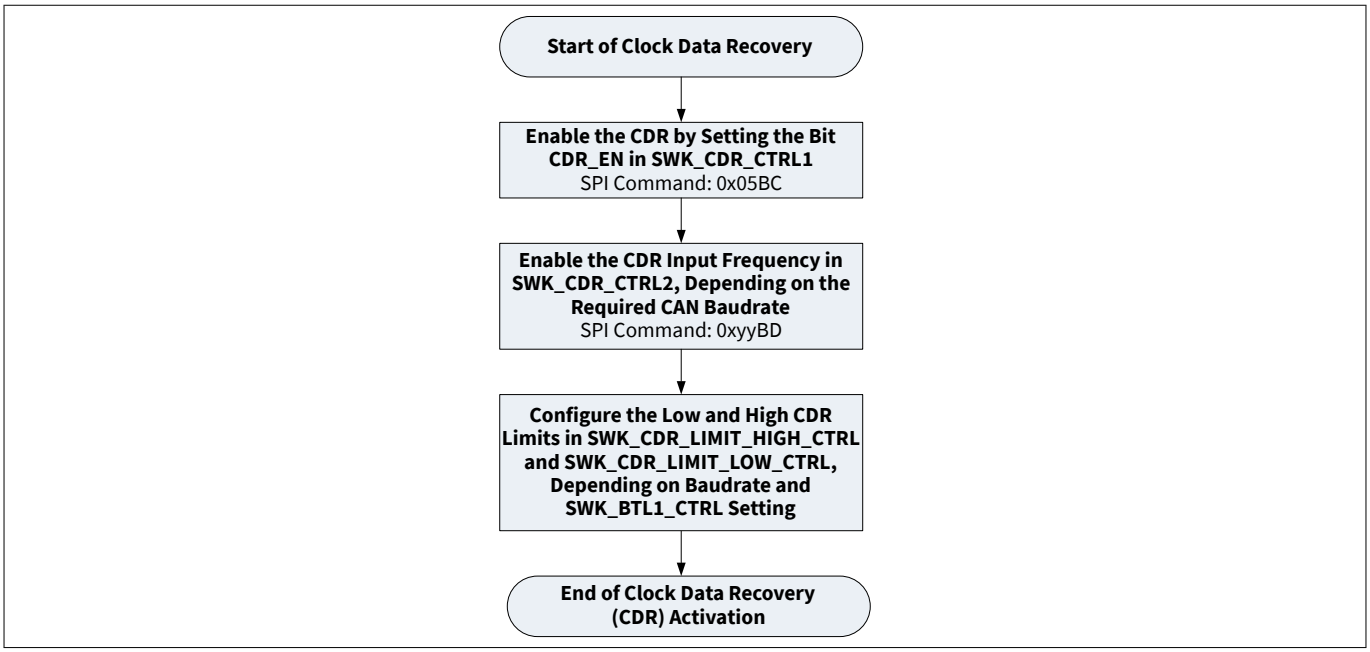

Figure 38 Activation of the Clock Data Recovery (CDR)

Enabling of the Clock Data Recovery (CDR) is strongly recommended to compensate drift effects (lifetime, temperature, etc.).

The CDR settings for the registers SWK_CDR_CTRL2, SWK_BTL1_CTRL, SWK_CDR_LIMIT_HIGH_CTRL, SWK_CDR_LIMIT_LOW_CTRL need to be chosen depending on the CAN baud rate.

Please also refer to tables 36 and 37 in the data sheet.

6.5 Configuration of the CAN Wake-Up Frame (WUF) and ID mask

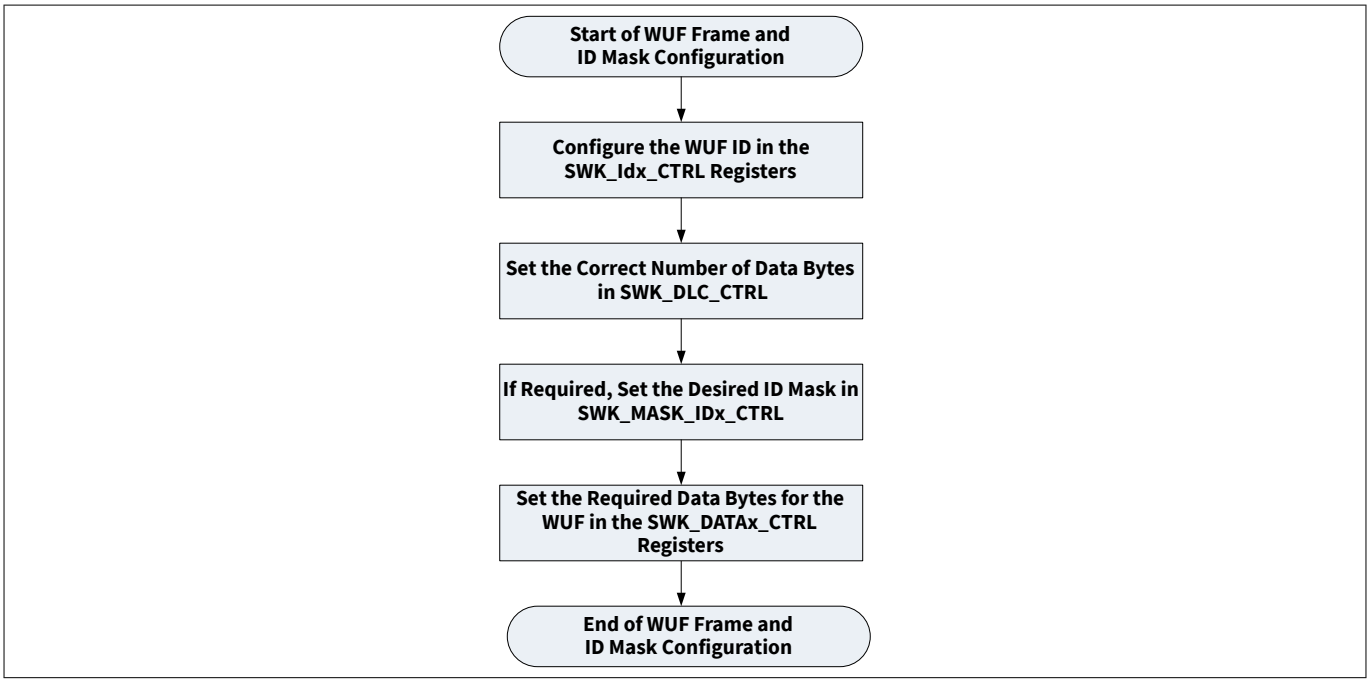

Figure 39 Configuration of the CAN Wake-Up Frame (WUF) and ID mask

CAN partial networking hints - SWK configuration & activation

The ID configuration depends on standard or extended frame format. In both cases, the configuration is done from the end of the registers, e.g. in SWK_ID3_CTRL and SWK_ID2_CTRL.

The DLC content must match exactly the number of data bytes.

It is not possible to mask the IDE bit.

The data bytes start from SWK_DATA7_CTRL, e.g., if two data bytes are sent, they have to be configured in SWK_DATA7_CTRL and SWK_DATA6_CTRL.

6.6 Activation of the CAN FD tolerant feature (optional)

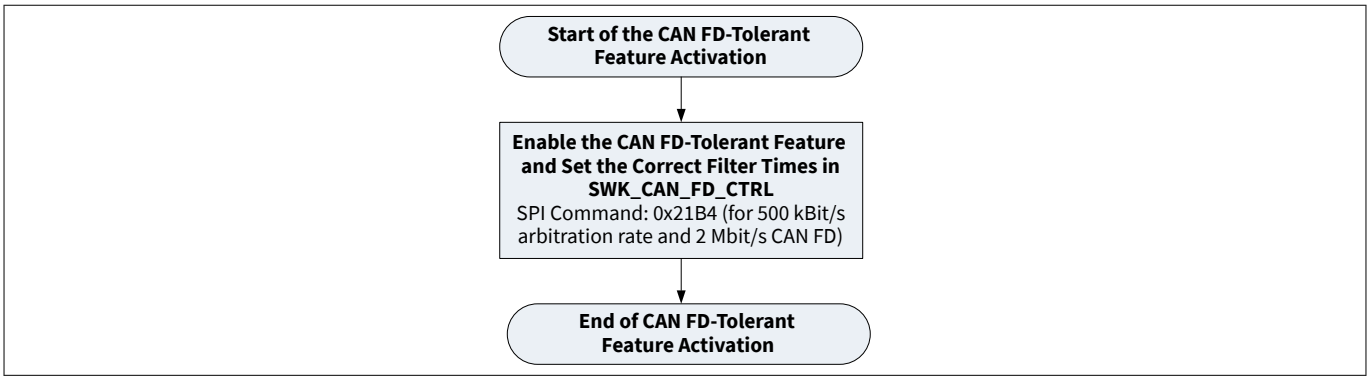

Figure 40 Activation of the CAN FD tolerant feature

This is an optional feature and should only be used if the CAN FD tolerance is needed for the respective ECU (mixed classical and CAN FD networks).

The recommended settings apply for an arbitration rate of 500 kBit/s and a 2 MBit/s CAN FD communication.

For more information, please refer to chapter 5.4.7 and the SPI register SWK_CAN_FD_CTRL.

SWK_CAN_FD_CTRL
CAN FD Configuration Control Register (Address 011 0100$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 00xx xxxx$_B$

7	6	5	4	3	2	1	0
Reserved	Reserved	DIS_ERR_CNT	RX_FILT_BYP	FD_FILTER_2	FD_FILTER_1	FD_FILTER_0	CAN_FD_EN
r	r	rwh	rw	rw	rw	rw	rw

Figure 41 SWK_CAN_FD_CTRL register

6.7 Activation of the CAN Selective Wake (SWK) function

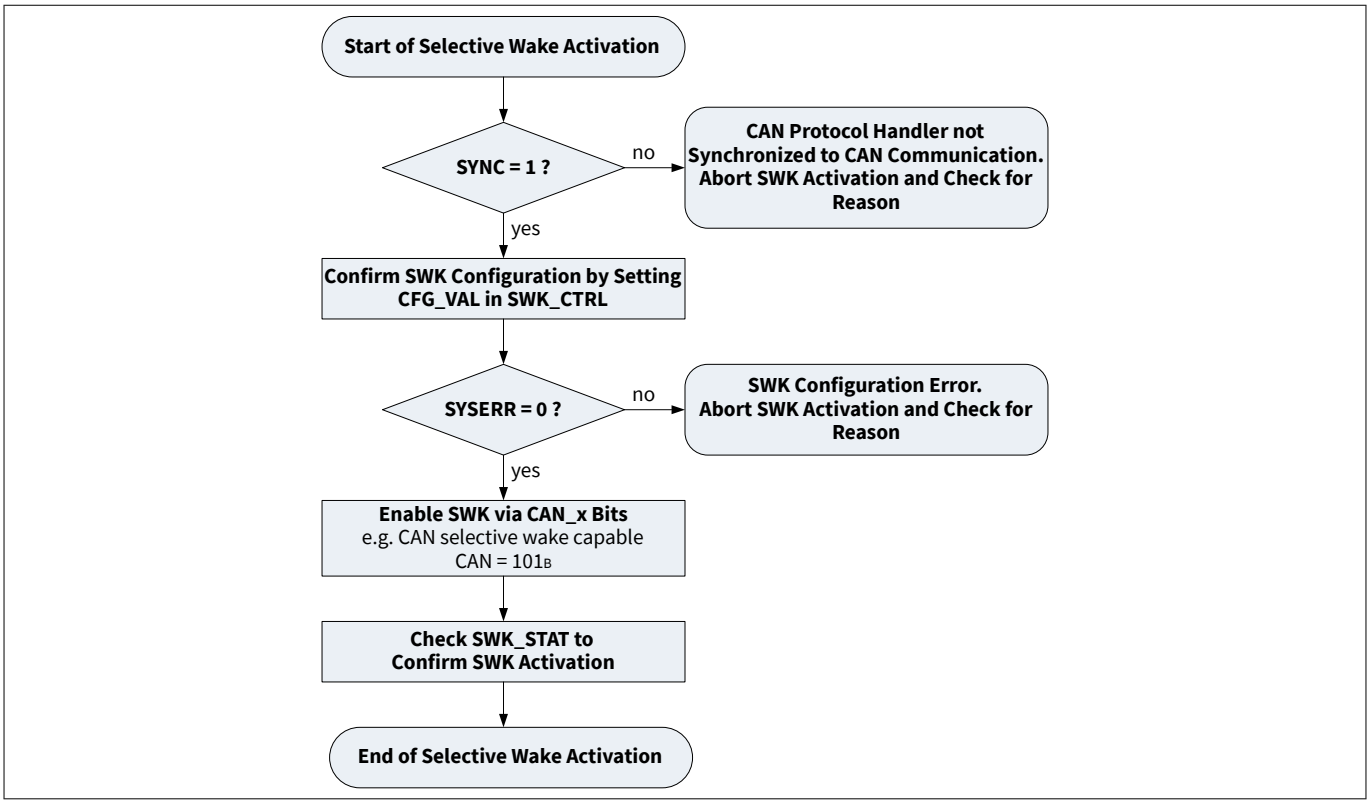

Figure 42 Activation of the CAN Selective Wake (SWK = CAN partial networking) function

The synchronization of the protocol handler must be ensured for the selective wake operation, to ensure a wake-up via WUF.

The CFG_VAL bit is cleared by the SBC in case the SWK configuration is changed, or in case of a configuration error.

SWK_STAT content should be: SWK_SET = 1, SYNC = 1, WUP = 0, WUF = 0.

6.8 SBC Low-Power Mode (SBC Stop or Sleep Mode) entry

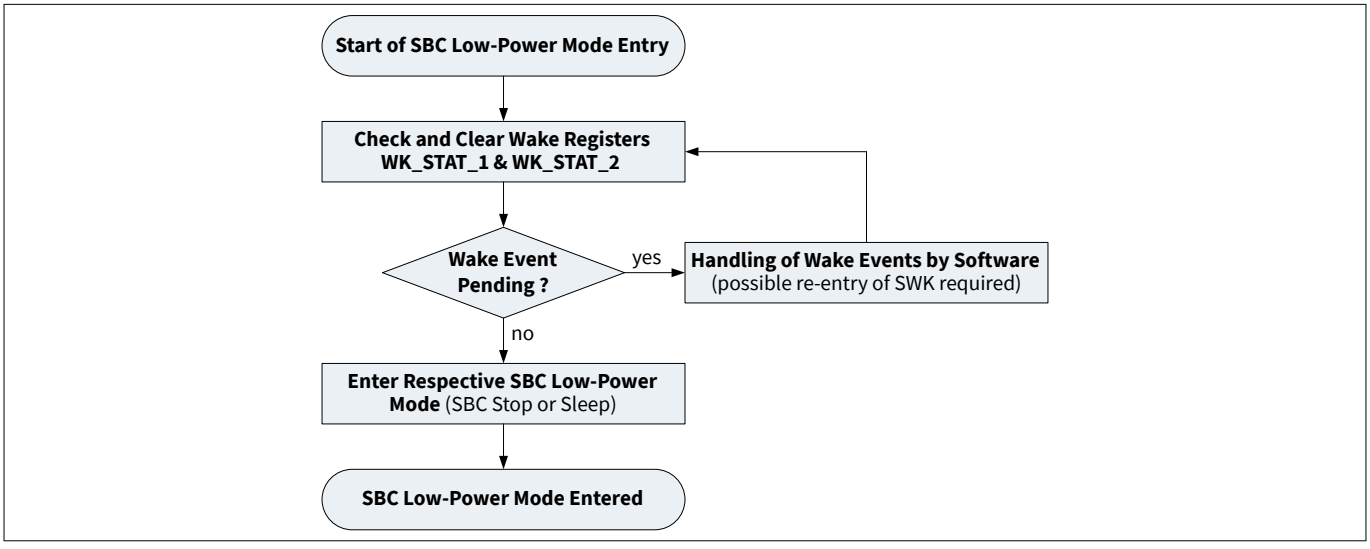

Figure 43 SBC Low-Power Mode entry

CAN partial networking hints - SWK configuration & activation

Right after enabling SWK, this sequence should be executed.

Before entering SBC Sleep Mode, it is mandatory to check pending wake events and to clear the wake status register.

Wake events lead to disabling the SWK function.

7 General-purpose IOs/fail-output behavior

7.1 Overview

This addendum describes the following behavior of the fail-output pins in addition to the datasheet:

- the default function as fail-outputs.
- their alternate function as general-purpose IOs (GPIOs).
- the behavior of the FO_ON bit.
- the current consumption adders for the respective GPIO functions.

7.2 Introduction to fail-outputs and GPIOs

All variants of the MR+ SBC family include three fail-output pins (FO, FO2, FO3/TEST) to support fail-safe functions. Each fail-output pin has a different behavior, as described in the data sheet.

In case FO2 and FO3/TEST are not used for fail-safe functionality, they can be re-configured as GPIOs (GPIO1, GPIO2) to either realize a wake-input, or a low-side or high-side function for on-board purposes.

The product datasheet describes the specified functionality of the fail outputs and GPIOs in the following chapters:

- "Chapter 5, System Features"
- "Chapter 14, Fail Outputs"
- "Chapter 15, Supervision Functions"
- "Chapter 16, Serial Peripheral Interface"

This section describes in addition the functions and behavior of the fail-outputs and GPIOs in more detail.

7.3 Fail-output and GPIO behavior

This section is an addendum to the data sheet chapter "14.1.1 General Purpose I/O Functionality of FO2 and FO3 as Alternate Function".

The FO1 pin is a dedicated fail-output pin without configuration possibilities.

The pins FO2 (= GPIO1) and FO3/TEST (= GPIO2) can be reconfigured in SBC Normal Mode for the following functions:

- FO functionality (default state) when configured as GPIOx ='000'...'011'
- OFF (also disabled in case FO1 is activated) when configured as GPIOx ='100'
- Wake input when configured as GPIOx ='101'
- Low-side when configured as GPIOx ='110'
- High-side when configured as GPIOx ='111'

The behavior for the respective configurations and SBC modes is listed in the table below:

Table 5 Fail-output and GPIO configuration behavior during the respective SBC Modes

FOx configuration	SBC Normal Mode	SBC Stop Mode	SBC Sleep Mode	SBC Restart Mode	SBC Fail-Safe Mode
FOx (default)	configurable	fixed	fixed	active / fixed	active
OFF		OFF	OFF	OFF	OFF
Wake input		wake-capable	wake-capable	wake-capable	OFF
Low-side		fixed	fixed	OFF	OFF
High-side		fixed	fixed	OFF	OFF

Explanation of GPIO states:

- configurable: Settings can be changed in this SBC mode.
- fixed: Settings stay as configured in SBC Normal Mode.
- active: FOx is activated due to a failure (leads to SBC Restart or Fail-Safe Mode).

Restart behavior:

The behavior during SBC Restart and Fail-Safe Mode as well as the transition to SBC Normal Mode is as follows:

- If configured as wake input: Stays wake-capable during SBC Restart Mode, and OFF while in SBC Fail-Safe Mode. Resumes wake-capability when leaving SBC Restart Mode (SPI register is not modified).
- If configured as low-side or high-side: Is disabled during SBC Restart and Fail-Safe Mode. After leaving SBC Restart Mode, the previously configured function is resumed (SPI register is not modified).
- If configured as FO and activated due to a failure: FO stays activated during SBC Restart Mode and when entering SBC Normal Mode (SPI register is not modified).

Signalization of wake events in case of wake input configuration:

- The behavior of the wake-input function is the same as for the WK1...3 inputs:
  - SBC Normal & Stop Mode: The input level is shown in the WK_LVL_STAT register, and INT is triggered.
  - SBC Restart Mode: The SPI is blocked and cannot be read; INT is not triggered.
  - SBC Sleep Mode: The device is woken up, i.e. VCC1 is enabled.
  - For all cases, the wake event is flagged in the respective SPI wake bit in the WK_STAT_2 register.
- Internal pull-up or pull-down structures are not implemented

7.4 Fail-output behavior in case of activation via the FO_ON bit

This section is an addendum to the data sheet chapters "14.1.1 General Purpose I/O Functionality of FO2 and FO3 as Alternate Function" and "16.5. SPI Control Registers".

As described in the datasheet, the fail outputs can be activated for testing purposes in SBC Normal Mode via the SPI bit FO_ON. This bit is an OR combination with the failure bit that activates the FOx outputs. In case there is no failure condition, the FO outputs can be turned off again by clearing the FO_ON bit. FO2 and FO3/TEST is controlled only by the FO_ON bit (if they are configured as fail outputs).

The behavior of the FOx outputs, when activated via the FO_ON bit and no failure has occurred, is as follows:

Table 6 Fail-output behavior for FO_ON = 1

FOx configuration	SBC Normal Mode	SBC Stop Mode	SBC Sleep Mode	SBC Restart Mode	SBC Fail-Safe Mode
FO_ON = 1	ON	ON	ON	OFF	active

In case the fail outputs were activated with the FO_ON bit, they stay activated also in SBC Stop and Sleep Mode. When SBC Restart Mode is entered (e.g. also coming from SBC Sleep Mode), the FOx outputs are disabled and stay disabled, because the restart value of the FO_ON bit is 0 (see also the HW_CTRL register overview below). As stated in ***Table 5***, the FOx output will be activated and also stay activated in SBC Restart Mode in case of a failure.

HW_CTRL
Mode- and Supply Control (Address 000 0010$_B$)
POR / Soft Reset Value: y000 y000$_B$; Restart Value: xx0x x00x$_B$

7	6	5	4	3	2	1	0
VCC3_V_CFG	SOFT_RESET_RO	FO_ON	VCC3_VS_UV_OFF	VCC3_LS	Reserved	VCC3_LS_STP_ON	CFG
rw	rw	rwh	rw	rw	r	rw	rw

Figure 44 Overview of HW_CTRL register

7.5 Current consumption for GPIO functions

This section is an addendum to the datasheet chapter "4.4 Current Consumption", which lists the current consumptions for the respective GPIO configurations:

- FOx configuration: The current consumption is specified in P_4.4.24. The parameter applies if all three FO pins are activated. In case FO2 and/or FO3/TEST are not configured as fail-output, the current consumption is reduced accordingly by 1/3 or 2/3.
- OFF configuration: No additional current consumption.
- Wake-input configuration: The parameters P_4.4.13 and P_4.4.14 apply also to GPIO1 and GPIO2.
- Low-side/high-side configuration: The current consumption adders are listed below in ***Table 7*** and apply to each GPIO.

Table 7 Current consumption

Current consumption values are specified at Tj = 25 °C, VS = 13.5 V, all outputs open (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or test condition	Number
		Min.	Typ.	Max.			
Feature incremental current consumption: GPIOx							
Current consumption for GPIOx if configured as low-side/high-side for SBC Stop or Sleep Mode	$I_{Stop,GPIOx,LS/HS}$	–	450	550	µA	SBC Stop/Sleep Mode; GPIO configured as LS/HS (no load);	P_4.4.37
Current consumption for GPIOx if configured as low-side/high-side for SBC Stop or Sleep Mode	$I_{Stop,GPIOx,LS/HS}$	–	450	600	µA	SBC Stop/Sleep Mode; T_j = -40..150°C; GPIO configured as LS/HS (no load);	P_4.4.38

Note: These parameters are not subject to production test, specified by design.

8 SPI diagnosis

8.1 Mid-range+ system basis chip (MR+ SBC) family

- The mid-range SBC family features an in-depth diagnosis and failure signalization in the SPI registers (status registers).
- These diagnosis and failure bits are intended to support a system and failure diagnosis of the ECU, which is required by the system and by functional safety.
- Those diagnosis functions are in general required by OEMs and vary in detail from OEM to OEM, depending on the partitioning and implementation.
- There are also pre-warning bits, e.g. thermal prewarning or VCC1 undervoltage prewarning, which can be used to react early enough to perform any emergency savings, to disregard any incorrect measurements, or to shut down functions, avoiding a thermal shutdown.

8.2 SPI configuration

8.2.1 SPI interface - timing

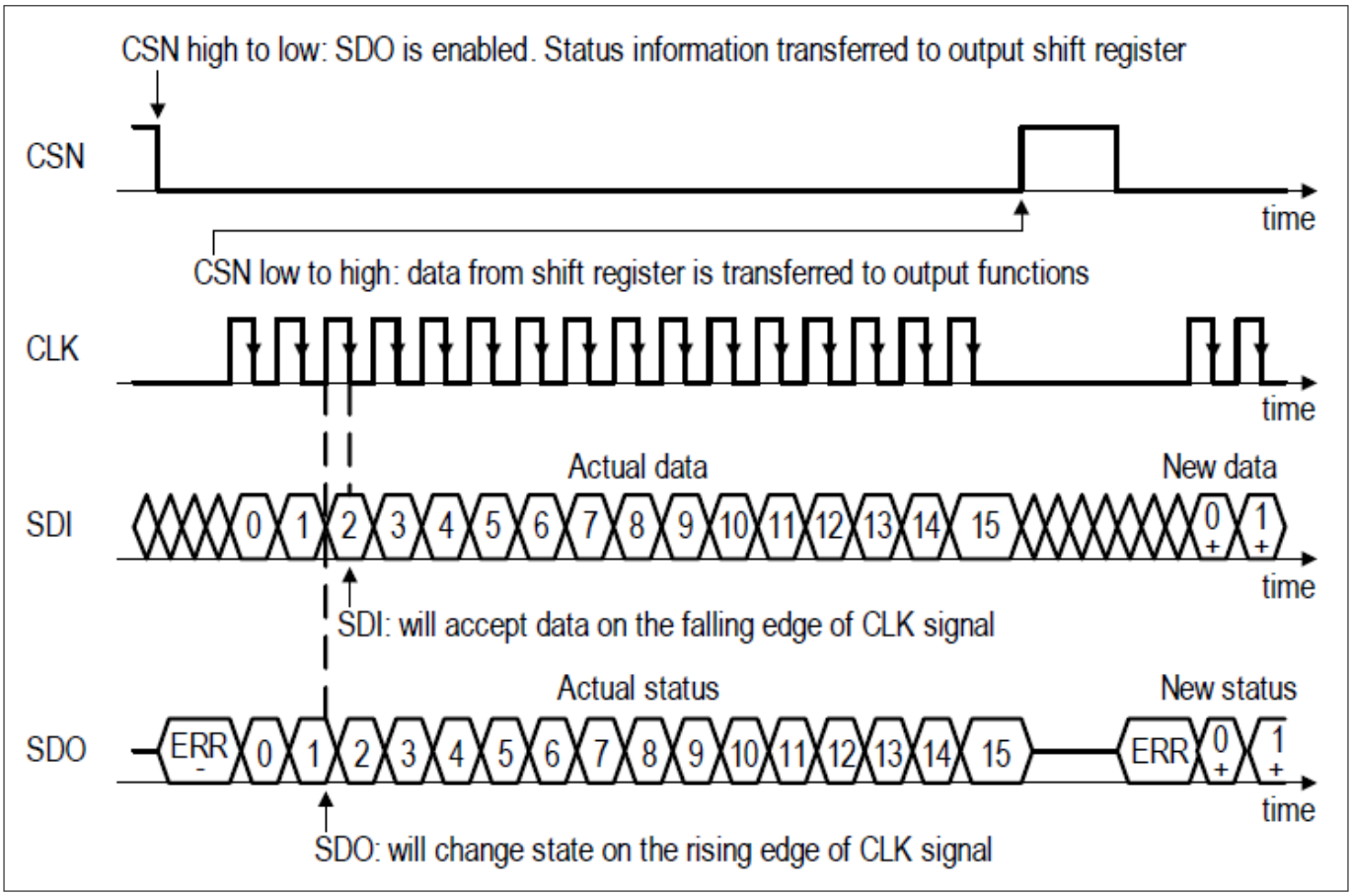

Figure 45 SPI timing diagram

The SPI command is executed, at the latest, 5 µs after the CSN is set to HIGH.

- Take care about the minimum CSN high time.
- The time between two SPI commands must be longer than 3 µs (P_16.7.24 in product datasheet).

8.2.2 SPI interface – status information field

The status information field shows immediately, whether there was a change in status flags → avoids unnecessary polling. The bit in the status information field is set, if any bit in the respective register is set.

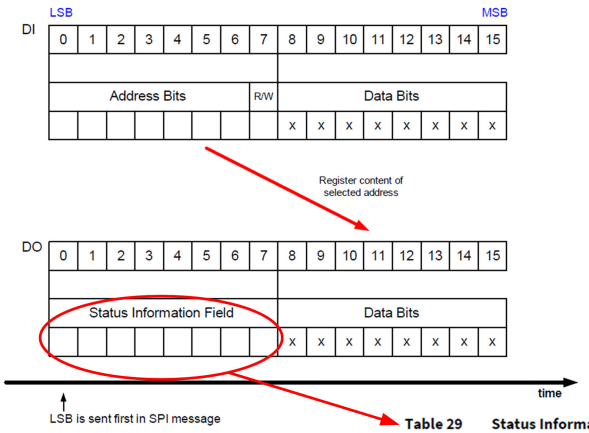

Table 29 Status Information Field

Bit in Status Information Field	CorrespondingAddress Bit	Status Register Description
0	100 0001	SUP_STAT_1: Supply Status -VSHS fail, VCCx fail, POR
1	100 0010	THERM_STAT: Thermal Protection Status
2	100 0011	DEV_STAT: Device Status - Mode before Wake, WD Fail, SPI Fail, Failure
3	100 0100	BUS_STAT: Bus Failure Status: CAN, LINx; BUS_STAT_1 & BUS_STAT_2 are a combinational OR
4	100 0110	WK_STAT_1, WK_STAT_2: Wake Source Status; Status bit is set as combinational OR of both registers
5	100 0000	SUP_STAT_2: VCC1_WARN/OV, VCC3 Status
6	101 0100	HS_OC_OT_STAT: High-Side Over Load Status
7	101 0101	HS_OL_STAT: High-Side Open Load Status

Figure 46 SPI Interface – status information field

8.2.3 SPI register mapping structure

	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0	
	8 Data Bits [bits 8...15] for Configuration & Status Information								Reg. Type	7 Address Bits [bits 0...6] for Register Selection							
Control Registers	M_S_CTRL								rw	0	0	0	0	0	0	1	
	HW_CTRL								rw	0	0	0	0	0	1	0	
	WD_CTRL								rw	0	0	0	0	0	1	1	
	BUS_CTRL_1								rw	0	0	0	0	1	0	0	
	BUS_CTRL_2								rw	0	0	0	0	1	0	1	
	WK_CTRL_1								rw	0	0	0	0	1	1	0	
	WK_CTRL_2								rw	0	0	0	0	1	1	1	
	WK_PUPD_CTRL								rw	0	0	0	1	0	0	0	
	WK_FLT_CTRL								rw	0	0	0	1	0	0	1	
	TIMER1_CTRL								rw	0	0	0	1	1	0	0	
	TIMER2_CTRL								rw	0	0	0	1	1	0	1	
	SW_SD_CTRL								rw	0	0	1	0	0	0	0	
	HS_CTRL_1								rw	0	0	1	0	1	0	0	
	HS_CTRL_2								rw	0	0	1	0	1	0	1	
	GPIO_CTRL								rw	0	0	1	0	1	1	1	
	PWM1_CTRL								rw	0	0	1	1	0	0	0	
	PWM2_CTRL								rw	0	0	1	1	0	0	1	
	PWM_FREQ_CTRL								rw	0	0	1	1	1	0	0	
	SYS_STAT_CTRL								rw	0	0	1	1	1	1	0	
Selective Wake Control Registers	SWK_CTRL								rw	0	1	0	0	0	0	0	
	SWK_BTL1_CTRL								rw	0	1	0	0	0	0	1	
	SWK_BTL2_CTRL								rw	0	1	0	0	0	1	0	
	SWK_ID3_CTRL								rw	0	1	0	0	0	1	1	
	SWK_ID2_CTRL								rw	0	1	0	0	1	0	0	
	SWK_ID1_CTRL								rw	0	1	0	0	1	0	1	
	SWK_ID0_CTRL								rw	0	1	0	0	1	1	0	
	SWK_MASK_ID3_CTRL								rw	0	1	0	0	1	1	1	
	SWK_MASK_ID2_CTRL								rw	0	1	0	1	0	0	0	
	SWK_MASK_ID1_CTRL								rw	0	1	0	1	0	0	1	
	SWK_MASK_ID0_CTRL								rw	0	1	0	1	0	1	0	
	SWK_DLC_CTRL								rw	0	1	0	1	0	1	1	
	SWK_DATA7_CTRL								rw	0	1	0	1	1	0	0	
	SWK_DATA6_CTRL								rw	0	1	0	1	1	0	1	
	SWK_DATA5_CTRL								rw	0	1	0	1	1	1	0	
	SWK_DATA4_CTRL								rw	0	1	0	1	1	1	1	
	SWK_DATA3_CTRL								rw	0	1	1	0	0	0	0	
	SWK_DATA2_CTRL								rw	0	1	1	0	0	0	1	
	SWK_DATA1_CTRL								rw	0	1	1	0	0	1	0	
	SWK_DATA0_CTRL								rw	0	1	1	0	0	1	1	
	SWK_CAN_FD_CTRL								rw	0	1	1	0	1	0	0	
	SWK_OSC_TRIM_CTRL								rw	0	1	1	1	0	0	0	
	SWK_OPT_CTRL								rw	0	1	1	1	0	0	1	
	SWK_OSC_CAL_H_STAT								r	0	1	1	1	0	1	0	
	SWK_OSC_CAL_L_STAT								r	0	1	1	1	0	1	1	
	SWK_CDR_CTRL1								rw	0	1	1	1	1	0	0	
	SWK_CDR_CTRL2								rw	0	1	1	1	1	0	1	
	SWK_CDR_LIMIT_H_CTRL								rw	0	1	1	1	1	1	0	
	SWK_CDR_LIMIT_L_CTRL								rw	0	1	1	1	1	1	1	
Status Registers	SUP_STAT_2								rc	1	0	0	0	0	0	0	5
	SUP_STAT_1								rc	1	0	0	0	0	0	1	0
	THERM_STAT								rc	1	0	0	0	0	1	0	1
	DEV_STAT								rc	1	0	0	0	0	1	1	2
	BUS_STAT_1								rc	1	0	0	0	1	0	0	3
	BUS_STAT_2								rc	1	0	0	0	1	0	1	3
	WK_STAT_1								rc	1	0	0	0	1	1	0	4
	WK_STAT_2								rc	1	0	0	0	1	1	1	4
	WK_LVL_STAT								r	1	0	0	1	0	0	0	-
	HS_OC_OT_STAT								rc	1	0	1	0	1	0	0	6
	HS_OL_STAT								rc	1	0	1	0	1	0	1	7
	SWK_STAT								r	1	1	1	0	0	0	0	
	SWK_ECNT_STAT								r	1	1	1	0	0	0	1	
	SWK_CDR_STAT1								r	1	1	1	0	0	1	0	
	SWK_CDR_STAT2								r	1	1	1	0	0	1	1	
	FAM_PROD_STAT								r	1	1	1	1	1	1	0	

Status Information Field Bit

Figure 47 SPI Register Mapping Overview

- Control registers to configure all SBC functionalities in SBC Normal Mode.
- SYS_CTRL is a freely usable 8-bit RAM register – not changed by SBC.
- Selective wake registers only visible in -3BQX variants.
- Status registers for wake & failure signalization and diagnosis keep content until cleared (except WD_FAIL bits).

8.3 SPI diagnosis – prewarning examples

- Thermal prewarning

TPW	0	rc	**Thermal Pre Warning** 0B , No Thermal Pre warning 1B , Thermal Pre warning detected

  - Intended to provide early warning that the SBC is close to the critical junction temperature.
  - Possible use cases: Emergency saving of RAM data, storing of error events, shutting down non-critical functions to reduce the power dissipation in order to reduce the junction temperature.
- VCC1 undervoltage prewarning

VCC1_ WARN	0	rc	**VCC1 Undervoltage Prewarning ($V_{PW,f}$)** 0B , No VCC1 undervoltage prewarning 1B , VCC1 undervoltage prewarning detected

  - Give early warning in case the VCC1 UV threshold is set to a lower level, and that the VCC1 voltage is not qualified anymore.
  - Possible actions from software: emergency saving of RAM data, ignoring ADC measurements, disabling communication.

8.4 Determining source of restart/reset

Description
Power-On Reset Detection
0B , No POR
1B , POR occurred
VSHS Undervoltage Detection ($V_{SHS,UVD}$)
0B , No VSHS-UV
1B , VSHS-UV detected
VSHS Overvoltage Detection ($V_{SHS,OVD}$)
0B , No VSHS-OV
1B , VSHS-OV detected
VCC2 Overtemperature Detection
0B , No overtemperature
1B , VCC2 overtemperature detected
VCC2 Undervoltage Detection ($V_{CC2,UV,f}$)
0B , No VCC2 undervoltage
1B , VCC2 undervoltage detected
VCC1 Short to GND Detection (<Vrtx for t>4ms after switch on)
0B , No short
1B , VCC1 short to GND detected
VCC1 UV-Detection (due to Vrtx reset)
0B , No Fail-Safe Mode entry due to 4th consecutive VCC1_UV
1B , Fail-Safe Mode entry due to 4th consecutive VCC1_UV
VCC1 UV-Detection (due to Vrtx reset)
0B , No VCC1_UV detection
1B , VCC1 UV-Fail detected

Description
Wake up via TimerX
0B , No Wake up
1B , Wake up
Reserved, always reads as 0
Wake up via WK3
0B , No Wake up
1B , Wake up
Wake up via WK2
0B , No Wake up
1B , Wake up
Wake up via WK1
0B , No Wake up
1B , Wake up

Description
Reserved, always reads as 0
TSD2 Thermal Shut-Down Detection
0B , No TSD2 event
1B , TSD2 OT detected - leading to SBC Fail-Safe Mode
TSD1 Thermal Shut-Down Detection
0B , No TSD1 fail
1B , TSD1 OT detected
Thermal Pre Warning
0B , No Thermal Pre warning
1B , Thermal Pre warning detected

Description
Device Status before Restart Mode
00B , Cleared (Register must be actively cleared)
01B , Restart due to failure (WD fail, TSD2, VCC1_UV); also after a wake from Fail-Safe Mode
10B , Sleep Mode
11B , Reserved
Reserved, always reads as 0
Number of WD-Failure Events (1/2 WD failures depending on CFG)
00B , No WD Fail
01B , 1x WD Fail, FOx activation - Config 2 selected
10B , 2x WD Fail, FOx activation - Config 1 / 3 / 4 selected
11B , Reserved (never reached)
SPI Fail Information
0B , No SPI fail
1B , Invalid SPI command detected
Activation of Fail Output FO
0B , No Failure
1B , Failure occurred

Figure 48 Status registers signalize source of wake-up and failure events

9 Reset behavior during power-up/down

9.1 Possible VCC1 undervoltage reset toggling due to dynamic load changes

If V_S is close to the VCC1 undervoltage threshold (VRTx), and a dynamic variation of the output current of VCC1 and/or VCC2 occurs, a VCC1 undervoltage reset toggling could be generated.

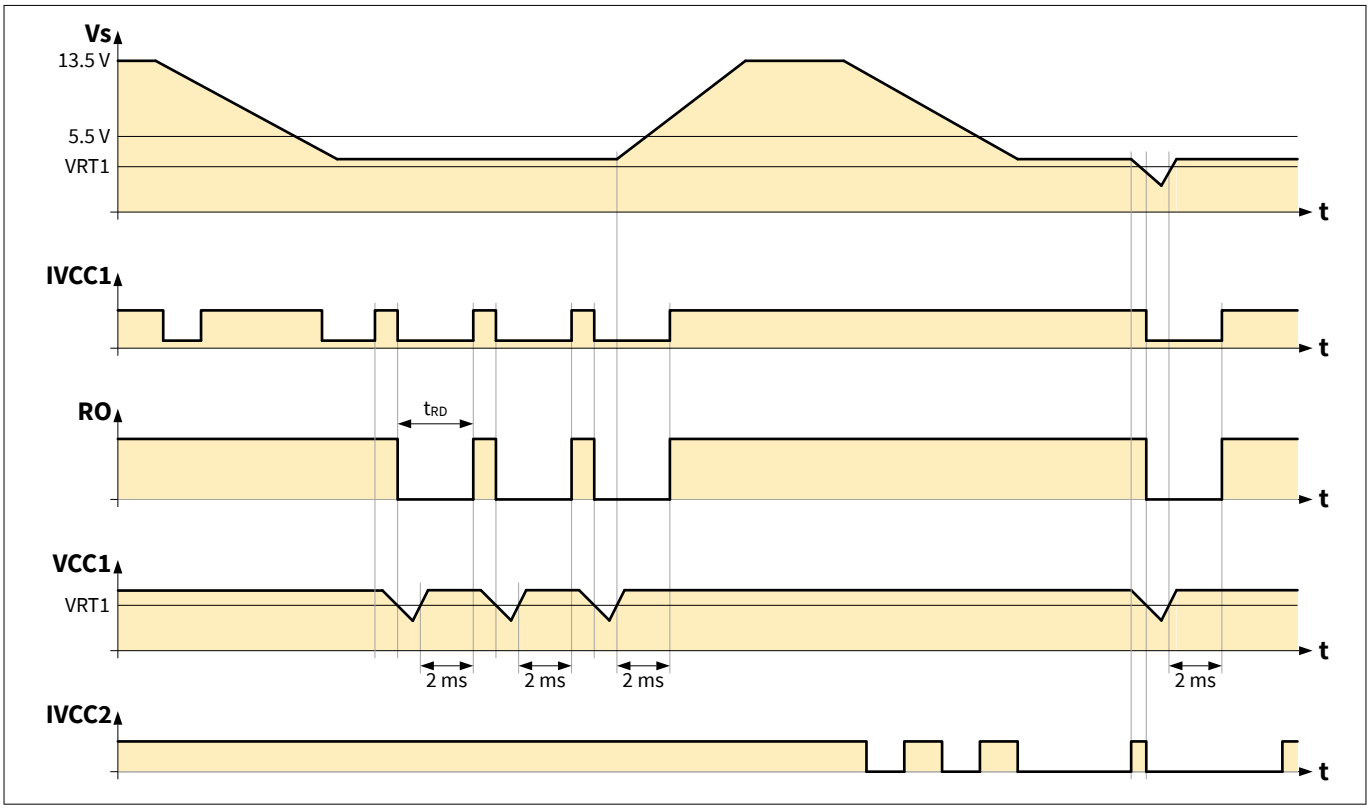

Figure 49 Simplified timing diagram of reset behavior at low supply voltage

- When V_S is close to the VCC1 undervoltage threshold, the regulator is in linear (R_{ON}) operation, i.e. the voltage drop across the voltage regulator is defined as: $V_{drop} = R_{on} * I_{load}$.
- A VCC1 undervoltage reset forces the microcontroller into reset state (assuming the reset lines are connected) .

  → the load current on VCC1 drops immediately, causing the voltage on VCC1 to rise again.
- VCC1 could rise again above the undervoltage threshold, and the reset would be released again.
- This would cause the microcontroller to start up again applying, a load on VCC1.

  → the increased voltage drop would cause again a VCC1 undervoltage reset.
- The behavior is repeated as long as VS is close to the VCC1 undervoltage threshold.
- Also a load jump on VCC2 could cause that the VS voltage would drop temporarily, causing a VCC1 undervoltage reset.

9.2 Use case: Reset toggling at low V_S, slow ramp-down, slow ramp-up (LV124-E07)

Operating modes of the DUT	**Test 1:** KL 30 ON and KL 15 ON **Test 2:** KL 30 ON
Initial voltage	U_{Bmax}
Rate of voltage ramp-down/ramp-up	0.5 V/min
Hold time at U_{Bmax}	Until error memory completely read out
Minimum voltage	0 V
Final voltage	U_{Bmax}
Number of cycles	1 cycle in operating mode II.c 1 cycle in operating mode II.a
Number of DUT	minimum 6

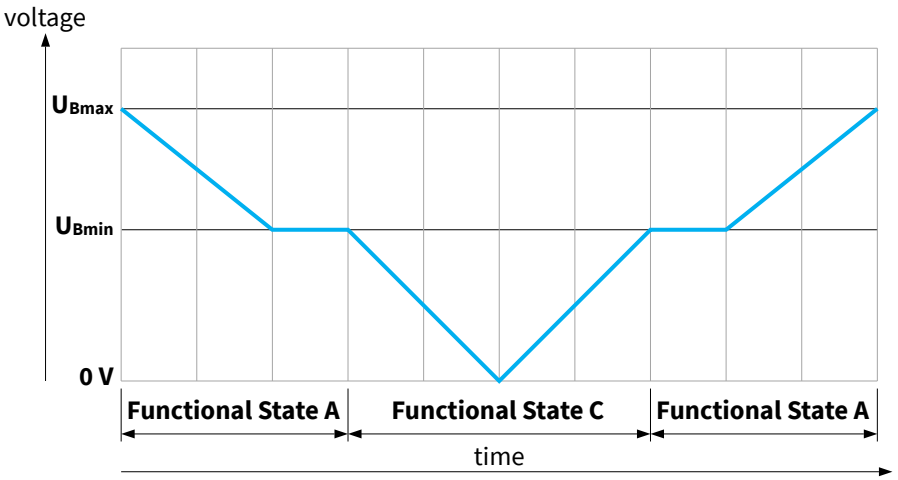

Figure 50 Voltage ramp for testing low supply voltage according to LV124

9.3 VCC1 undervoltage reset toggling at low V_S, expected system behavior

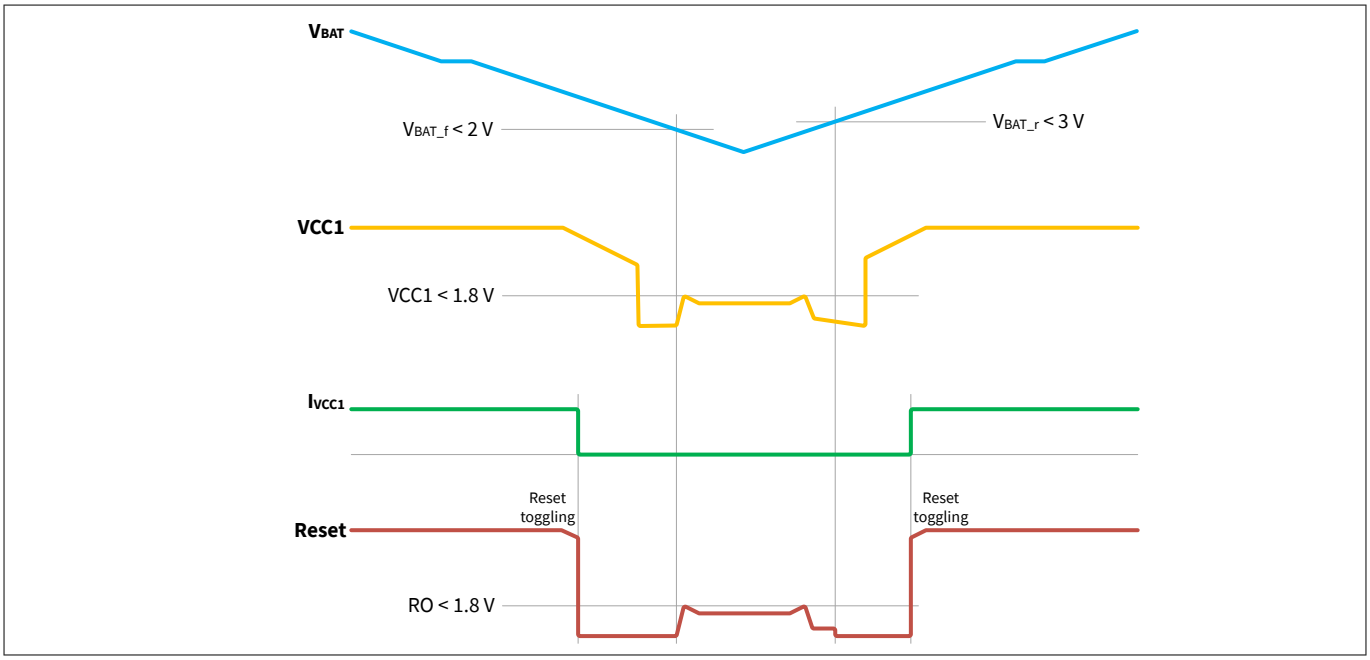

Figure 51 Expected system behaviour at low supply voltages according LV124

10 Pin FMEA

10.1 Abstract

Note: The following information is given as a hint for the implementation of the device only, and shall not be regarded as a description or warranty of a certain functionality, condition, or quality of the device.

This Application Note is intended to provide a basis for an FMEA on application level.

The Application Note shows the considerations that have been taken during the Pin FMEA.

The information provided in the FMEA is intended for FMEA evaluation of the TLE9260…63(-3)QX(V33) and other devices of this family.

10.2 Introduction

10.2.1 General Information about FMEA

A failure modes and effects analysis (FMEA) is a procedure in operations management for the analysis of potential

failure modes within a system, for classification by severity or determination of the effect of failures on the system.

Failure modes are any errors or defects in a process, design, or item, especially those that affect the customer, and can be potential or actual. Effects analysis refers to studying the consequences of those failures.

10.2.2 Implementation

In FMEA, failures are prioritized according to how serious their consequences are, how frequently they occur, and how easily they can be detected. An FMEA also documents current knowledge and actions about the risks of failures for use in continuous improvement.

The purpose of the FMEA is to take actions to eliminate or reduce failures, starting with the highest-priority ones. It may be used to evaluate risk management priorities to mitigate known vulnerabilities.

10.3 Classification of Failure Effects

Table 8 Classes of Failure Effects

Class	Failure Effects
A	Damage to device affects application functionality
B	No damage to device but thermal damage must be considered
C	No damage to device but can affect application functionality
D	No damage to device and no affect to application functionality

10.4 Pin FMEA Table

Table 9 Potential Failure Mode and Effects Analysis

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FOx) function	Class
1	GND	Pin open	Digital ground current distributes to the other GND pins, EMC disturbance possible	FO unchanged	D
		Pin shorted to VS	Application not supplied, very large current flowing on PCB	Application doesn't work, no FO function	B
		Pin shorted to VCC1	VCC1 load not supplied, application not working, large current flowing (limited internally), Fail-Safe mode entered after 4 ms	FO switched on after 4 ms	C
3	VCC3REF	Pin open	VCC3 regulator forces output voltage near to VS, components supplied by VCC3 may be damaged by high voltage, SPI status bit VCC3_UV set	FO unchanged	A
		Pin shorted to GND	VCC3 load not supplied, large current flowing (limited), SPI status bit VCC3_UV set	FO unchanged	C
		Pin shorted to VS, PNP emitter and collector shorted	Components supplied by VCC3 may be damaged by high voltage	FO unchanged	C
		Pin shorted to VCC1	In stand-alone regulator configuration an oscillation may occur due to two-point regulation; normal application case in load sharing configuration	FO unchanged	C
		Pin shorted to next pin (VCC3B), PNP base and collector shorted	Components supplied by VCC3 may be damaged by high voltage	FO unchanged	B
		Pin leakage to next pin (VCC3B)	Regulation loop bypassed, output voltage not predictable	FO unchanged	B

Table 9 Potential Failure Mode and Effects Analysis (continued)

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FOx) function	Class
4	VCC3B	Pin open	VCC3 load not supplied, SPI status bit VCC3_UV set	FO unchanged	C
		Pin shorted to GND	VCC3 load not supplied, large current flowing through PNP emitter-base junction (not limited), SPI status bit VCC3_UV set	FO unchanged	B
		Pin shorted to VS	VCC3 load not supplied, large current flowing into pin, SPI status bit VCC3_UV set	FO unchanged	B
		Pin shorted to VCC1	Pin VCC1 including load may be damaged due too large voltage, large current flowing through PNP emitter-base junction (not limited)	EOS - FO not functional	A
		Pin shorted to next pin(VCC3SH), PNP base and emitter shorted	VCC3 load not supplied, large current flowing into pin, SPI status bit VCC3_UV set	FO unchanged	B
		Pin leakage to next pin (VCC3SH)	Reduced maximum output current of VCC3 possible depending on PNP base driver strength	FO unchanged	C
5	VCC3SH	Pin open	VCC3 current limitation always active, VCC3 load not supplied, SPI status bits VCC3_OC and VCC3_UV set	FO unchanged	B
		Pin shorted to GND	VCC3 load not supplied, large current flowing (not limited), SPI status bit VCC3_UV set	FO unchanged	A
		Pin shorted to VS, external shunt resistor shorted	VCC3 current limitation not working, external PNP not protected	FO unchanged	A
		Pin shorted to VCC1	Pin VCC1 including load may be damaged due to large voltage	EOS - FO not functional	A

Table 9 Potential Failure Mode and Effects Analysis (continued)

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FOx) function	Class
8...11	HS1...4	Pin open	Load not supplied, SPI status bit HSx_OL set	FO unchanged	C
		Pin shorted to GND	Load not supplied, HS switched off due to overcurrent, SPI status bit HSx_OC_OT set	FO unchanged	B
		Pin shorted to VS	Load always supplied, SPI status bit HSx_OL set	FO unchanged	C
		Pin shorted to VCC1	Pin VCC1 including load may be damaged due to large voltage	EOS - FO not functional	A
		Pin shorted to next pin (HS2...4)	All loads switched by any of the shorted HS	FO unchanged	C
		Pin leakage to next pin (HS2...4)	Other load may be supplied by leakage current when HS is switched on	FO unchanged	C
13	VSHS	Pin open	HS switches and LIN not supplied	FO unchanged	C
		Pin shorted to GND	HS switches and LIN not supplied, very large current flowing on PCB	FO unchanged	B
		Pin shorted to VS	Normal operation	FO unchanged	D
		Pin shorted to VCC1	Pin VCC1 including load may be damaged due to large voltage	EOS - FO not functional	A
		Pin shorted to next pin (VS)	Normal operation	FO unchanged	D
		Pin leakage to next pin (VS)	Normal operation	FO unchanged	D
14	VS	Pin open	VCC3 current limitation not working, external PNP not protected	FO unchanged	B
14...15	VS	Pin shorted to GND	Application not supplied, very large current flowing on PCB	Application doesn't work, no FO function	B
		Pin shorted to VCC1	Pin VCC1 including load may be damaged due to large voltage	EOS - FO not functional	A

Table 9 Potential Failure Mode and Effects Analysis (continued)

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FOx) function	Class
17	VCC1	Pin open	VCC1 load not supplied, application not working, Fail-Safe mode is entered after 400 ms (two watchdog long open windows)	FO switched on after 400 ms	C
		Pin shorted to GND	VCC1 load not supplied, application not working, large current flowing (limited internally), Fail-Safe mode entered after 4 ms	FO switched on after 4 ms	C
		Pin shorted to VS	Pin VCC1 including load may be damaged due to large voltage	EOS - FO not functional	A
		Pin shorted to next pin (VCC2)	Voltage regulators may oscillate due to two-point regulation, if one regulator is off, its load is supplied from the other regulator (potential overload)	FO unchanged	B
		Pin leakage to next pin (VCC2)	If one regulator is off, that load is supplied by the leakage current	FO unchanged	C
18	VCC2	Pin open	VCC2 load not supplied	FO unchanged	C
		Pin shorted to GND	VCC2 load not supplied, SPI status bit VCC2_UV set	FO unchanged	C
		Pin shorted to VS	VCC2 load may be damaged due to large voltage	FO unchanged	B
		Pin shorted to VCC1	Voltage regulators may oscillate due to two-point regulation, if one regulator is off, its load is supplied from the other regulator (potential overload)	FO unchanged	B

Table 9 Potential Failure Mode and Effects Analysis (continued)

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FOx) function	Class
20	GND	Pin open	Disturbance or parameter shifts possible due to parasitic metal resistance	FO unchanged	C
		Pin shorted to VS	Application not supplied, very large current flowing on PCB	Application doesn't work, no FO-function	B
		Pin shorted to VCC1	VCC1 load not supplied, application not working, large current flowing (limited internally), Fail-Safe mode entered after 4 ms	FO switched on after 4 ms	C
		Pin shorted to next pin (FO1)	FO load always on	Pin directly affected	C
		Pin leakage to next pin (FO1)	FO load supplied by leakage current	Pin directly affected	C
21	FO1	Pin open	FO load not supplied in case of failure	Pin directly affected; other FO pins not affected	C
		Pin shorted to GND	FO load always on	Pin directly affected; other FO pins not affected	C
		Pin shorted to VS	FO load not supplied in case of failure, current flowing in case of FO activation	Pin directly affected; other FO pins not affected	B
		Pin shorted to VCC1	FO load pulls up VCC1 (depends on external circuitry on FO and load), current flowing in case of FO activation	EOS - FO not functional (depending on external circuitry)	C
		Pin shorted to next pin (WK1)	FO1 load activated when WK1 input is low (e.g. with external switch to GND), no wake-up possible on WK1 when FO is active	Pin directly affected; other FO pins not affected	C
		Pin leakage to next pin (WK1)	FO1 load supplied by leakage current when WK1 input is low (e.g. with external switch to GND), wake- up endangered on WK1 when FO is active	Pin directly affected; other FO pins not affected	C

Table 9 Potential Failure Mode and Effects Analysis (continued)

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FOx) function	Class
22...24	WK1...3	Pin open	No wake-up possible	FO unchanged	C
		Pin shorted to GND	No wake-up possible	FO unchanged	C
		Pin shorted to VS	No wake-up possible	FO unchanged	C
		Pin shorted to VCC1	No wake-up possible	EOS - FO not functional (depending on external switch configuration)	C
22...23	WK1...2	Pin shorted to next pin (WK2...3)	Wake-up on one input wakes both inputs	FO unchanged	C
		Pin leakage to next pin (WK2...3)	Wake-up on one input may wake both inputs	FO unchanged	C
24	WK3	Pin shorted to next pin (TXDLIN2), pins are no real neighbors	TXDLIN2 pin may be destroyed due to large voltage at WK3 pin, additional failures possible	EOS - FO not functional (depending on external switch configuration)	A
		Pin leakage to next pin (TXDLIN2), pins are no real neighbors	TXDLIN2 pin may be destroyed due to large voltage at WK3 pin, additional failures possible	EOS - FO not functional (depending on external switch configuration)	A
25	TXDLIN2	Pin open	No LIN communication possible	FO unchanged	C
		Pin shorted to GND	No LIN communication possible, SPI status bit LIN2_FAIL set	FO unchanged	C
		Pin shorted to VS	Destruction of pin, possible additional failures	EOS - FO not functional	A
		Pin shorted to VCC1	No LIN communication possible	FO unchanged	C
		Pin shorted to next pin (RXDLIN2)	No LIN communication possible	FO unchanged	C
		Pin leakage to next pin (RXDLIN2)	Cross-current of digital I/O drivers due to leakage, no functional deviation	FO unchanged	D

Table 9 Potential Failure Mode and Effects Analysis (continued)

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FOx) function	Class
26	RXDLIN2	Pin open	No LIN communication possible	FO unchanged	C
		Pin shorted to GND	No LIN communication possible, large pin current	FO unchanged	A
		Pin shorted to VS	Destruction of pin, possible additional failures	EOS - FO not functional	A
		Pin shorted to VCC1	No LIN communication possible	FO unchanged	C
		Pin shorted to next pin (CLK)	SPI failure, no LIN communication possible	FO switched on after 400 ms	C
		Pin leakage to next pin (CLK)	Cross-current of digital I/O drivers due to leakage, no functional deviation, increased current consumption	FO unchanged	D
27	CLK	Pin open	SPI failure	FO switched on after 400 ms	C
		Pin shorted to GND	SPI failure	FO switched on after 400 ms	C
		Pin shorted to VS	Destruction of pin, possible additional failures	EOS - FO not functional	A
		Pin shorted to VCC1	SPI failure, shown by first bit of following SPI frame	FO switched on after 400 ms	C
		Pin shorted to next pin (SDI)	SPI failure	FO switched on after 400 ms	C
		Pin leakage to next pin (SDI)	Cross-current of digital I/O drivers due to leakage, no functional deviation	FO unchanged	D

Table 9 Potential Failure Mode and Effects Analysis (continued)

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FOx) function	Class
28	SDI	Pin open	SPI failure	FO switched on after 400 ms	C
		Pin shorted to GND	SPI failure	FO switched on after 400 ms	C
		Pin shorted to VS	Destruction of pin, possible additional failures	EOS - FO not functional	A
		Pin shorted to VCC1	SPI failure	FO switched on after 400 ms	C
		Pin shorted to next pin (SDO)	SPI failure or wrong SPI output	FO unchanged	C
		Pin leakage to next pin (SDO)	Cross-current of digital I/O drivers due to leakage, no functional deviation	FO unchanged	D
29	SDO	Pin open	Wrong SPI output to µC	FO unchanged	C
		Pin shorted to GND	Wrong SPI output to µC	FO unchanged	C
		Pin shorted to VS	Destruction of pin, possible additional failures	EOS - FO not functional	A
		Pin shorted to VCC1	Wrong SPI output to µC	FO unchanged	C
		Pin shorted to next pin (CSN)	SPI failure or wrong SPI output to µC	FO unchanged	C
		Pin leakage to next pin (CSN)	Cross-current of digital I/O drivers due to leakage, no functional deviation	FO unchanged	D
30	CSN	Pin open	SPI failure	FO switched on after 400 ms	C
		Pin shorted to GND	SPI failure	FO switched on after 400 ms	C
		Pin shorted to VS	Destruction of pin, possible additional failures	EOS - FO not functional	A
		Pin shorted to VCC1	SPI failure	FO switched on after 400 ms	C
		Pin shorted to next pin (INT)	Wake-up is shown with each SPI command, and maybe SPI failure	FO unchanged	C
		Pin leakage to next pin (INT)	Cross-current of digital I/O drivers due to leakage, no functional deviation	FO unchanged	D

Table 9 Potential Failure Mode and Effects Analysis (continued)

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FOx) function	Class
31	INT	Pin open	No wake-up is shown	FO unchanged	C
		Pin shorted to GND	No wake-up is shown, large pin current	FO unchanged	B
		Pin shorted to VS	Destruction of pin, possible additional failures	EOS - FO not functional	A
		Pin shorted to VCC1	No wake-up is shown	FO unchanged	C
		Pin shorted to next pin (RO)	Each wake-up generates µC reset	FO unchanged	C
		Pin leakage to next pin (RO)	Each wake-up generates µC reset	FO unchanged	C
32	RO	Pin open	No reset is generated, behavior depends on µC input configuration	FO unchanged	C
		Pin shorted to GND	Always reset for µC, application not working	FO unchanged	C
		Pin shorted to VS	Destruction of pin, possible additional failures	EOS - FO not functional	A
		Pin shorted to VCC1	No reset is generated, large pin current	FO unchanged	B
		Pin shorted to next pin (TXDLIN1)	Reset with each LIN communication	FO unchanged	C
		Pin leakage to next pin (TXDLIN1)	Reset with each LIN communication	FO unchanged	C
33	TXDLIN1	Pin open	No LIN communication possible	FO unchanged	C
		Pin shorted to GND	No LIN communication possible, SPI status bit LIN1_FAIL set	FO unchanged	C
		Pin shorted to VS	Destruction of pin, possible additional failures	EOS - FO not functional	A
		Pin shorted to VCC1	No LIN communication possible	FO unchanged	C
		Pin shorted to next pin (RXDLIN1)	No LIN communication possible	FO unchanged	C
		Pin leakage to next pin (RXDLIN1)	Cross-current of digital I/O drivers due to leakage, no functional deviation	FO unchanged	D

Table 9 Potential Failure Mode and Effects Analysis (continued)

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FOx) function	Class
34	RXDLIN1	Pin open	No LIN communication possible	FO unchanged	C
		Pin shorted to GND	No LIN communication possible, large pin current	FO unchanged	A
		Pin shorted to VS	Destruction of pin, possible additional failures	EOS - FO not functional	A
		Pin shorted to VCC1	No LIN communication possible	FO unchanged	C
		Pin shorted to next pin (TXDCAN)	No CAN communication possible, LIN communication may be disturbed depending on strength of TXDCAN driver in µC	FO unchanged	C
		Pin leakage to next pin (TXDCAN)	Cross-current of digital I/O drivers due to leakage, no functional deviation	FO unchanged	D
35	TXDCAN	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	No CAN communication possible, SPI status bit CAN_FAIL set	FO unchanged	C
		Pin shorted to VS	Destruction of pin, possible additional failures	EOS - FO not functional	A
		Pin shorted to VCC1	No CAN communication possible	FO unchanged	C
		Pin shorted to next pin (RXDCAN)	No CAN communication possible	FO unchanged	C
		Pin leakage to next pin (RXDCAN)	Cross-current of digital I/O drivers due to leakage, no functional deviation	FO unchanged	D

Table 9 Potential Failure Mode and Effects Analysis (continued)

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FOx) function	Class
36	RXDCAN	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	No CAN communication possible, large pin current	FO unchanged	B
		Pin shorted to VS	Destruction of pin, possible additional failures	EOS - FO not functional	A
		Pin shorted to VCC1	No CAN communication possible	FO unchanged	C
		Pin shorted to next pin (VCAN), pins are no real neighbors	No CAN communication possible	FO unchanged	C
		Pin leakage to next pin (VCAN), pins are no real neighbors	Cross-current of digital I/O driver due to leakage, no functional deviation	FO unchanged	D
37	VCAN	Pin open	CAN is not supplied, no CAN communication possible	FO unchanged	C
		Pin shorted to GND	CAN is not supplied, no CAN communication possible, large current flowing on PCB until thermal shutdown	FO unchanged/FO activated if VCAN connected to VCC1 and short circuit or TSD2 is detected	C
		Pin shorted to VS	Destruction of pin, possible additional failures	EOS - FO not functional	A
		Pin shorted to VCC1	Usual application case	FO unchanged	D
		Pin shorted to next pin (GND)	CAN is not supplied, no CAN communication possible, large current flowing on PCB	FO unchanged	B
		Pin leakage to next pin (GND)	Current to GND due to leakage, no functional deviation, increased current consumption	FO unchanged	D

Table 9 Potential Failure Mode and Effects Analysis (continued)

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FOx) function	Class
38	GND	Pin open	No low ohmic ground for CAN. Ground connection over substrate contacts, increased EM emission and disturbance of other functions possible.	FO unchanged	C
		Pin shorted to VS	Application not supplied, very large current flowing on PCB	Application doesn't work, no FO-function	B
		Pin shorted to VCC1	VCC1 load not supplied, application not working, large current flowing (limited internally), Fail-Safe mode entered after 4 ms	FO switched on after 4 ms	C
		Pin shorted to next pin (CANL)	CAN communication disturbed and generates EMC	FO unchanged	C
		Pin leakage to next pin (CANL)	Bus not symmetrical, no functional deviation	FO unchanged	D
39	CANL	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	CAN communication disturbed and generates EMC	FO unchanged	C
		Pin shorted to VS	No CAN communication possible	FO unchanged	C
		Pin shorted to VCC1	No CAN communication possible	FO unchanged	C
		Pin shorted to next pin (CANH)	No CAN communication possible	FO unchanged	C
		Pin leakage to next pin (CANH)	Increased bus load, no functional deviation	FO unchanged	D
40	CANH	Pin open	No CAN communication possible	FO unchanged	C
		Pin shorted to GND	No CAN communication possible	FO unchanged	C
		Pin shorted to VS	CAN communication disturbed and generates EMC	FO unchanged	C
		Pin shorted to VCC1	CAN communication disturbed and generates EMC	FO unchanged	C

Table 9 Potential Failure Mode and Effects Analysis (continued)

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FOx) function	Class
42	LIN1	Pin open	No LIN communication possible	FO unchanged	C
		Pin shorted to GND	LIN bus blocked, no LIN communication possible	FO unchanged	C
		Pin shorted to VS	LIN bus blocked, no LIN communication possible	FO unchanged	C
		Pin shorted to VCC1	LIN communication disturbed (or not possible at all when VS <10V), pin VCC (and also µC) may be damaged by high voltage	EOS - FO not functional	A
		Pin shorted to next pin (GND)	LIN bus blocked, no LIN communication possible	FO unchanged	C
		Pin leakage to next pin (GND)	LIN communication disturbed	FO unchanged	C
43	GND	Pin open	No low ohmic ground for LIN. Ground connection over substrate contacts, increased EM emission and disturbance of other functions possible.	FO unchanged	C
		Pin shorted to VS	Application not supplied, very large current flowing on PCB	Application doesn't work, no FO function	B
		Pin shorted to VCC1	VCC1 load not supplied, application not working, large current flowing (limited internally), Fail-Safe mode entered after 4 ms	FO switched on after 4 ms	C
		Pin shorted to next pin (LIN2)	LIN bus blocked, no LIN communication possible	FO unchanged	C
		Pin leakage to next pin (LIN2)	LIN communication disturbed	FO unchanged	C

Table 9 Potential Failure Mode and Effects Analysis (continued)

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FOx) function	Class
44	LIN2	Pin open	No LIN communication possible	FO unchanged	C
		Pin shorted to GND	LIN bus blocked, no LIN communication possible	FO unchanged	C
		Pin shorted to VS	LIN bus blocked, no LIN communication possible	FO unchanged	C
		Pin shorted to VCC1	LIN communication disturbed (or not possible at all when VS <10V), pin VCC (and also µC) may be damaged by high voltage	EOS - FO not functional	A
47	FO2	Pin open	FO load not supplied in case of failure, GPIO load not supplied or no wake-up possible	Pin directly affected; other FO pins not affected	C
		Pin shorted to GND	FO load always on, GPIO load always on or never supplied (limited current flowing) or no wake-up possible	Pin directly affected; other FO pins not affected	C
		Pin shorted to VS	FO load not supplied in case of failure (limited current flowing), GPIO load always on or never supplied (limited current flowing) or no wake-up possible	Pin directly affected; other FO pins not affected	C
		Pin shorted to VCC1	FO/GPIO load pulls up VCC1 (probably damaging it and the connected load), limited current flowing in case of FO/ GPIO activation or no wake-up possible	EOS - FO not functional (depending on external circuitry)	A
		Pin shorted to next pin (FO3/TEST)	Both FO loads are switched on with a wrong duty cycle, limited cross-current in case of GPIO HS & LS configuration or wrong wake-up behavior	Pin directly affected; FO1 pin not affected	C
		Pin leakage to next pin (FO3/TEST)	Both FO loads are switched on with a wrong duty cycle	Pin directly affected; FO1 pin not affected	C

Table 9 Potential Failure Mode and Effects Analysis (continued)

Pin Number	Pin Name	Potential Failure Mode	Potential Effect(s) of Failure	Effect(s) of Failure on Fail Output (FOx) function	Class
48	FO3/TEST	Pin open	FO load not supplied in case of failure, GPIO load not supplied or no wake-up possible, no SBC Development mode possible	Pin directly affected; FO1 pin not affected	C
		Pin shorted to GND	FO load always on, GPIO load always on or never supplied (limited current flowing) or no wake-up possible, always SBC Development mode	Pin directly affected; other FO pins not affected	C
		Pin shorted to VS	FO load not supplied in case of failure (limited current flowing), GPIO load always on or never supplied (limited current flowing) or no wake-up possible, no SBC Development mode possible	Pin directly affected; other FO pins not affected	C
		Pin shorted to VCC1	FO/GPIO load pulls up VCC1 (probably damaging it and the connected load), limited current flowing in case of FO/ GPIO activation or no wake-up possible, no SBC Development possible	EOS - FO not functional (depending on external circuitry)	A
		Pin shorted to next pin (GND), pins are no real neighbors	FO load always on, GPIO load always on or never supplied (limited current flowing) or no wake-up possible, always SBC Development mode	Pin directly affected; other FO pins not affected	C
		Pin leakage to next pin (GND), pins are no real neighbors	FO/GPIO load supplied by leakage current or wrong wake-up behavior, always SBC Development mode	Pin directly affected; other FO pins not affected	C
EP	Exposed pad	Pin open	Worse thermal behavior, thermal shutdown with smaller dissipated power	FO unchanged	C
		Pin shorted to VS	Application not supplied, very large current flowing on PCB	Application doesn't work, no FO function	B
		Pin shorted to VCC1	VCC1 load not supplied, application not working, large current flowing (limited internally), Fail-Safe mode entered after 4 ms	FO switched on after 4 ms	C

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Revision	Date	Changes
1.0	2018-08-16	Initial release

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