45 W 19 V adapter reference board

using the 700 V CoolMOS™ P7 in SOT-223 package

DEMO_45W_19V_FLYB_P7

About this document

Scope and purpose

This application note describes a reference design board designed in a 45 W notebook adapter form factor using the 700 V CoolMOS™ P7 in a SOT-223 package (IPN70R600P7S) and a standard flyback PWM controller. The system solutions used for conducted emissions, radiated emissions and thermals will also be described. The reference adapter board in this application note is not only designed to meet efficiency and thermal specifications, but has also passed the necessary conducted and radiated emissions requirements. It is a reference design which meets the typical notebook adapter requirements and can be produced after verification tests.

Intended audience

This document is intended for power supply designers, application engineers, students and anyone who wants to quickly design a high-efficiency and low-cost AC-DC adapter using a Surface Mount Device (SMD) MOSFET package.

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Abstract

1 Abstract

The new 700 V CoolMOS™ P7 in a SOT-223 package combines the latest high-performance Superjunction (SJ) MOSFET technology with a small SMD package with devices available with a breakdown voltage of 600 V, 700 V and 800 V. The SOT-223 package can be used to achieve high power efficiency and high power density while reducing Bill of Materials costs, which in adapter products is a constant target for new designs. Obviously, automated manufacturing with SMD MOSFETs improves manufacturing performance and reliability issues caused by ESD from handling through-hole devices. However, there are two major concerns raised by engineers who are familiar with traditional through-hole packages when they consider transitioning to SMD MOSFETs: thermals and Electromagnetic Compatibility (EMC). The P7 technology helps to reduce the thermal issues of transitioning to SMD due to its improved switching performance, and this application note will address how to handle the EMI concerns.
In this application note, a standard form factor 45 W notebook adapter is implemented with a 700 V CoolMOS™ P7 in SOT-223 to demonstrate the device performance and that a SOT-223 is capable of meeting the requirements of a 45 W notebook adapter. All thermal and EMC solutions are described in this application note to help the reader utilize the benefits of the new 700 V CoolMOS™ P7 in a SOT-223 package .

2 Key features of the 700 V CoolMOS™ P7

Compared to the 650 V CoolMOS™ C6 and conventional non-SJ MOSFETs, the 700 V CoolMOS™ P7 technology, Infineon's latest-generation CoolMOS™, improves three important characteristics in notebook adapters. First, it reduces switching losses, which usually contribute to the greatest power losses of the MOSFET. Figure 1 shows the power loss distribution of various MOSFETs in two EMI-compliant notebook adapters. Even with higher gate resistances and additional external capacitance across the MOSFET drain and source pins, the IPN70R600P7S has lower power losses than the competition and performs with higher efficiency over the entire power range.

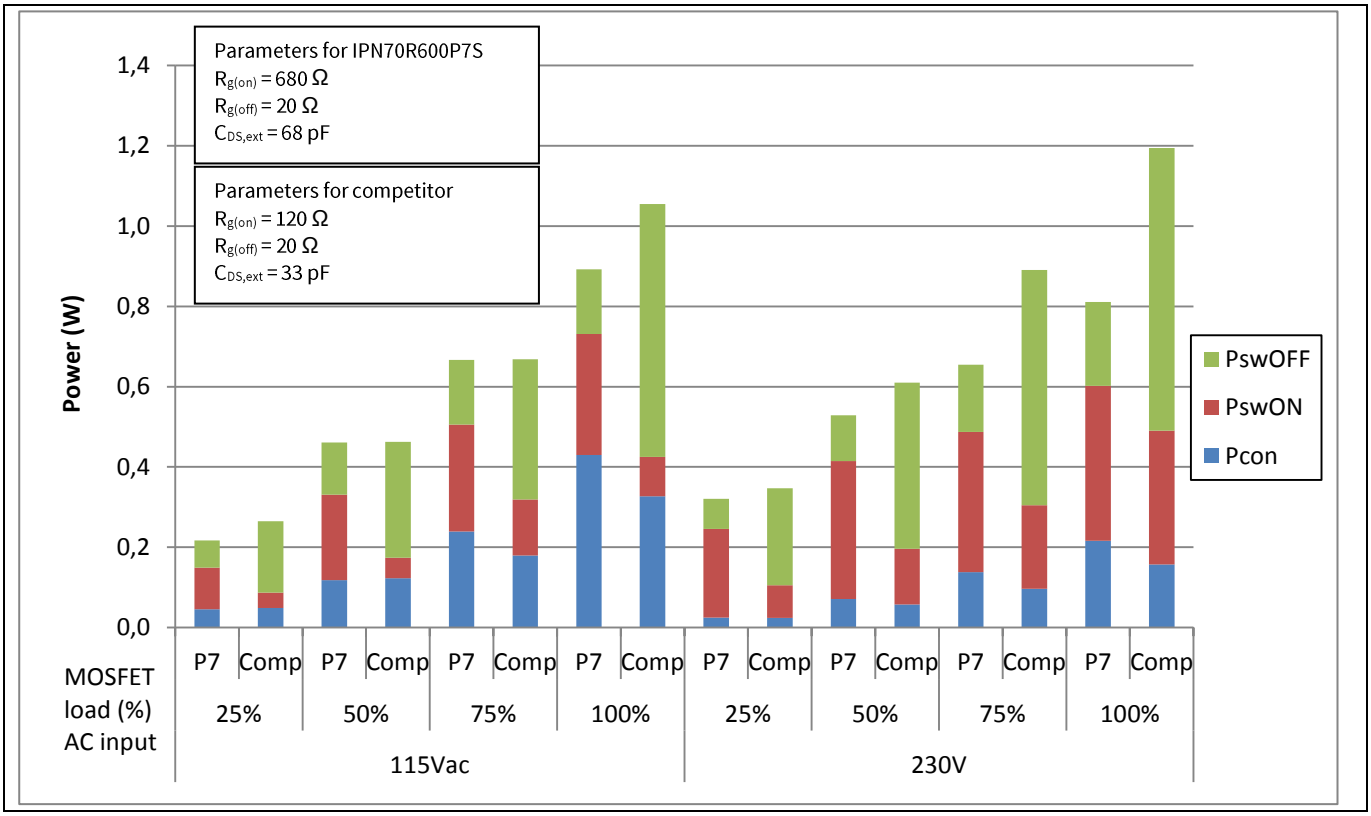


Figure 1 Power loss distribution of the adapter MOSFET with the IPN70R600P7S vs competition at low-line and high-line (at 115 V AC/ 230 V AC)

A smaller $R_{DS(on)}$ temperature dependency, as shown in Figure 2, is another key characteristic of the 700 V CoolMOS™ P7, generating lower conduction losses and therefore a lower temperature of the MOSFET. The worst-case operating condition for notebook adapters is at full load with a 90 V AC input, which is the condition used in thermal testing to obtain the temperature data of key components for reliability evaluation.

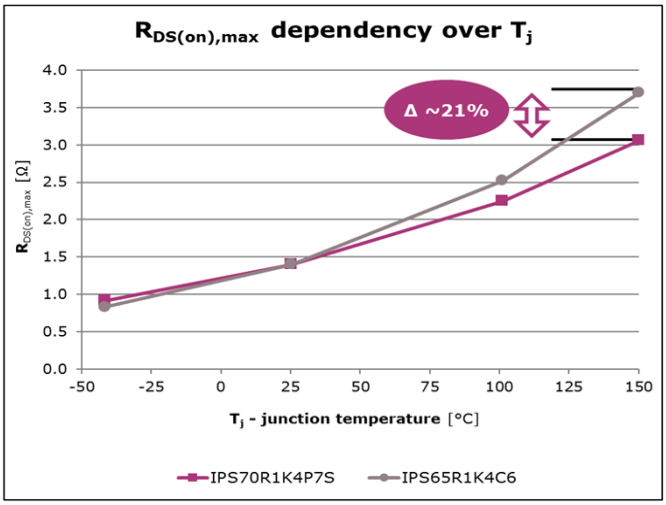


Figure 2 $R_{DS(on)}$ behavior over-junction temperature

By measuring the voltage and current waveform of the IPN70R600P7S in the adapter with a 90 V AC input and calculating the power loss distribution of the MOSFET, it is obvious that the conduction loss accounts for the greater part of the total power dissipation of the MOSFET, as shown in Figure 3. A higher $R_{DS(on)}$ causes higher conduction losses and therefore a higher junction temperature. This characteristic helps to prevent the MOSFET from possible thermal runaway in thermal testing.

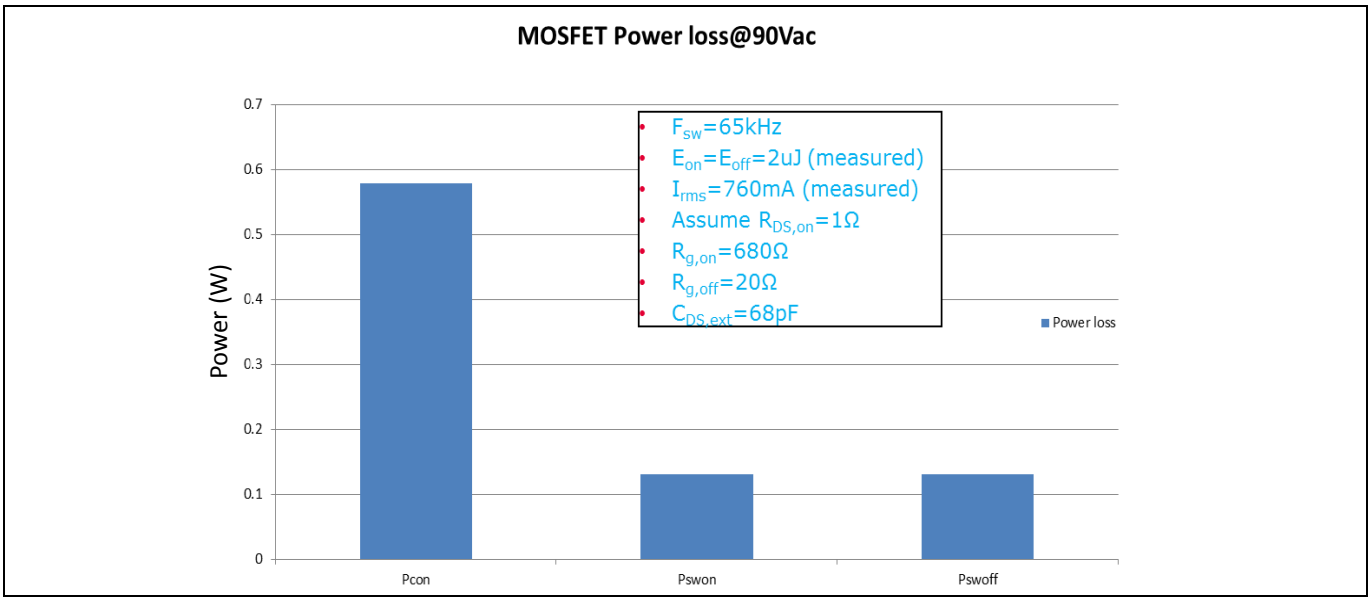


Figure 3 Power loss distribution of MOSFET at 90 V AC input

Finally, the mounting of the heatsink and lead bending of the through-hole package, such as the TO-220, unavoidably leads to physical damage from ESD or other unexpected forces. With the 700 V CoolMOS™ P7 in a SMD package, the device is suitable for automated assembly, making manufacturing more efficient. Improved built-in ESD protection from the gate-to-source of the device prevents damage to the MOSFET from ESD and improves the reliability of power supply products.

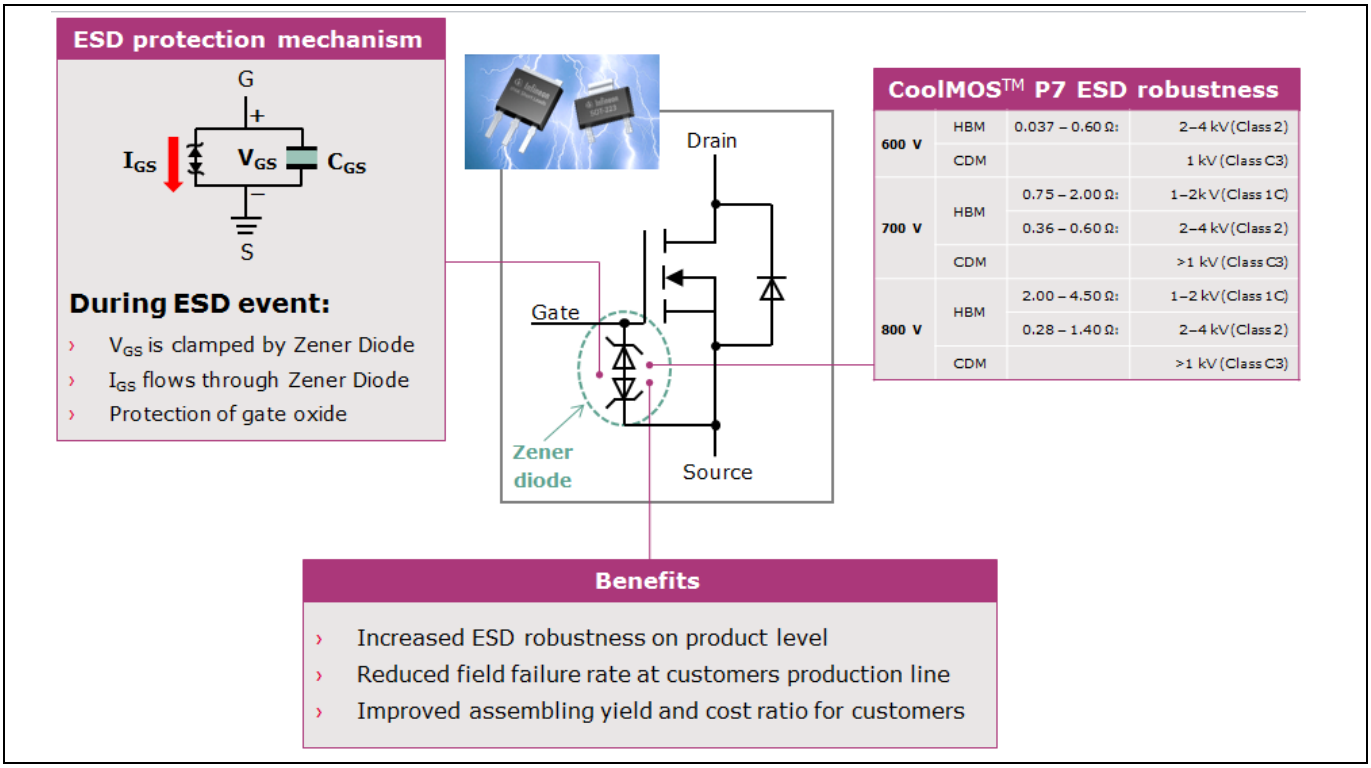


Figure 4 Built-in ESD protection from the gate-to-source electrode in the 700 V CoolMOS™ P7 series

3 Reference board specifications and descriptions

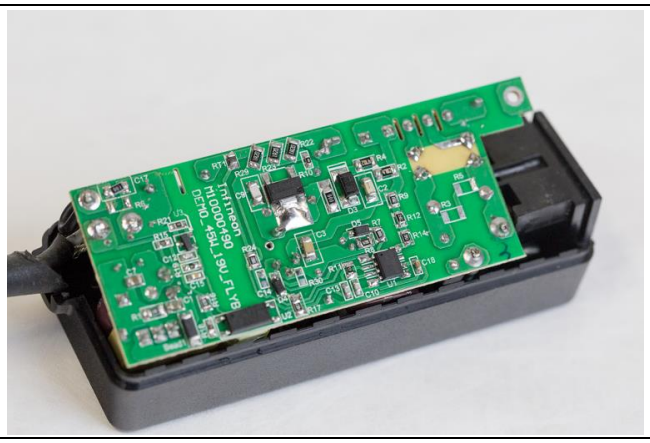


Figure 5 The bottom side of the 45 W P7 SOT-223 demo board shown inside an enclosure

Table 1 45 W notebook adapter reference board specifications

Input voltage and frequency	**90 V AC (60 Hz) ~ 264 V AC (50 Hz)**
Output voltage, current and power	19 V/2.37 A/45 W
Active-mode four-point average efficiency (25%, 50%, 75%, 100% load) (EU CoC Version 6)	More than 88%
No-load power consumption	Less than 100 mW
Conducted emissions (EN 55022 class B)	Pass with 6 dB margin for QP and average
Radiated emissions (EN 55022 class B)	Pass with 6 dB margin for QP
PCB form factor (L × W × H)	86 × 35 × 20 mm

For improved efficiency and reduced EMI, many controllers are designed to support Continuous Conduction Mode (CCM) control at full load, valley switching for QR control and frequency jittering for notebook adapters. It is well-known that non-valley switching of the main switch of a flyback converter increases conducted emissions at 230 V AC input and that CCM operation of a flyback converter increases radiated emissions at 115 V AC input. To demonstrate the performance of the 700 V CoolMOS™ P7 in SOT-223, a controller with QR control is excluded in this reference design board. This causes challenges in meeting EMI requirements for the notebook adapter, which will be addressed in the upcoming sections.

The controller, LD7750R, is designed by Leadtrend Co. Ltd. and is utilized in this reference design board. Figure 5 shows the application circuit and basic control of the LD7750R.

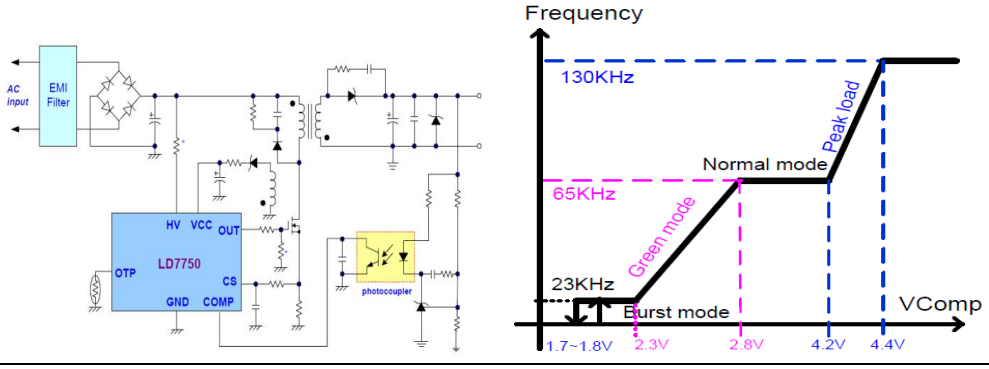


Figure 6 Application circuit and basic control of LD7750

The operation mode and switching frequency of this controller depend primarily on the V_{Comp} level. In a no-load or light-load condition, it operates at burst mode for low standby power. As the output power increases, burst mode stops and the switching frequency begins increasing. A constant frequency of 65 kHz with jittering for CCM operation is used for higher power conditions. Finally a maximum switching frequency of 130 kHz is used under the peak load requirement of the notebook adapter.

The designer may enjoy improved thermal and efficiency performance but suffer EMI from switching to the new 700 V CoolMOS™ P7 MOSFET. The typical approach that is used to solve EMI when using a new MOSFET is to increase the gate resistance and to add external drain-source capacitance. In some cases this might make efficiency and thermal results from the new MOSFET worse because the solutions above lead to more power losses in the MOSFET.

The purpose of this reference design board using the 700 V CoolMOS™ P7 in SOT-223 is not only to show that the new devices meet efficiency, thermal and EMC requirements, but to also bring together all of the workable solutions for notebook adapters in this application note for the reader.

4 Solutions for conducted emissions

To completely understand the solutions for conducted emissions, one must first understand the test connection, conducted emissions requirements, and the notebook adapter circuit including the filter and transformer.

4.1 Measurement of conducted emissions

The conducted emissions limitation from FCC and CISPR is shown in Figure 6. The test frequency is from 150 kHz to 30 MHz. In general, there are different limitations for Quasi Peak (QP) and average detection mode for conducted emissions.

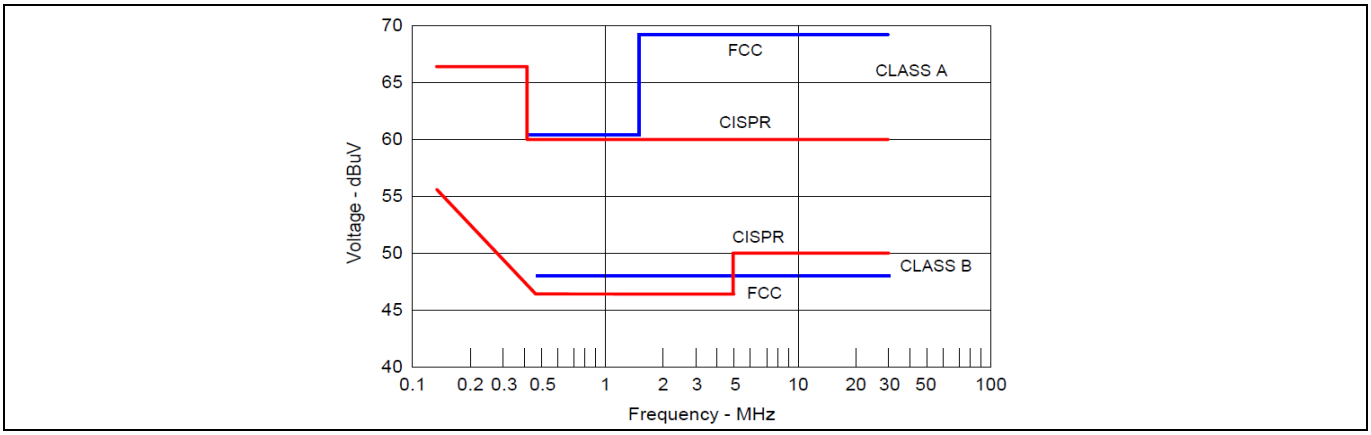


Figure 7 Conducted emissions limitation

The Line Impedance Stabilization Network (LISN), which is connected between the AC-line voltage and the power supply, converts noise current into voltage which is then transferred to the spectrum analyzer in the conducted emissions test. Figure 7 shows the equivalent circuit of a LISN.

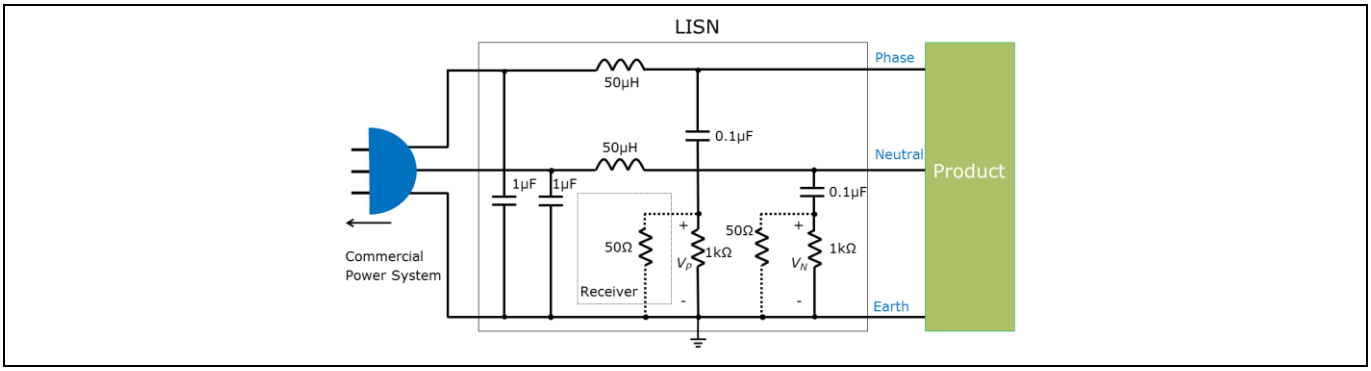


Figure 8 Equivalent circuit of a LISN

In the conducted emissions test, the measured results from phase and neutral in the LISN are different, as shown in Figure 8. The current on the phase line is the sum of Common Mode (CM) current and Differential Mode (DM) current while the current on the neutral line is the difference between the CM current and DM current. Consider two extreme conditions. In the first the DM current is much higher than the CM current and the voltage on the phase line is the same amplitude, but out of phase with that of the neutral line. In the second case both voltages are of the same amplitude, in phase with each other since CM current is much higher than DM current. This is a smart way to figure out which current is dominant. In fact for most cases in the notebook

adapter, the voltage signal on the phase and neutral lines is similar, which means that the CM current is dominant.

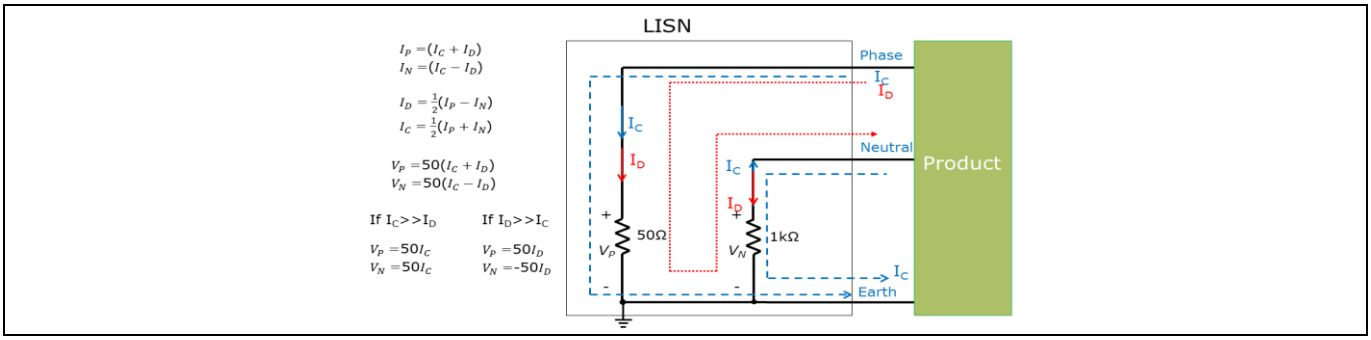


Figure 9 The measured results of the LISN in phase and neutral lines

4.2 Filter for conducted emissions

A standard filter for conducted emissions in SMPS is shown in Figure 9. It consists of a Differential Mode Choke (DMC), X-capacitors, a Common Mode Choke (CMC) and Y-capacitors. In general, the DMC and X-capacitors are designed for suppressing or diverting the DM conduction emissions. The CMC and Y-capacitors are designed to suppress or divert the CM conducted emissions. The DMC is not commonly used in low-power notebook adapters due to cost concerns. To suppress the DM current, we rely on the leakage inductance of the CMC, which behaves like a DMC.

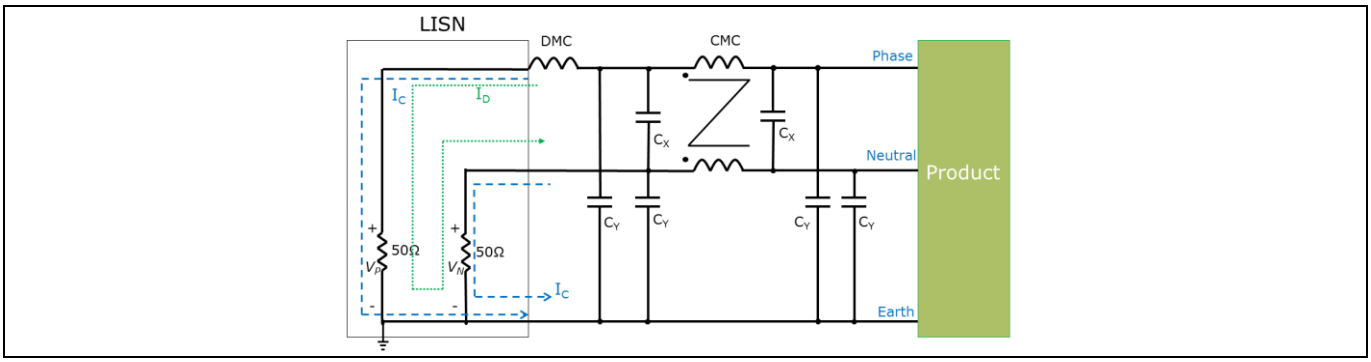


Figure 10 Standard conducted filter for a power supply

The Y-capacitor is used to improve the CM emissions at a higher frequency range (greater than 1 MHz) by diverting the CM current. It is not used in the notebook adapter due to the limitation of leakage current in equipment shown in Table 2. The Y-capacitor can only be used during the debugging phase to check whether or not the conducted emissions are from CM current.

Table 2 Leakage current limitation of IT and medical equipment

Standard	Type	Limit
IEC69050-1 (IT equipment)	Hand-held	0.25 mA
	Movable (not hand-held) or pluggable	3.5 mA
	Permanently connected	3.5 mA
IEC6060-1 medical		0.1 mA

Now we will take a look at the CMC, assuming the self-inductance of each winding in the CMC is L and the mutual inductance between windings is M. The total inductance (L + M) is seen by the CM current and the difference in inductance (L - M) is seen by DM current. This means that the CMC behaves as a higher impedance for CM current to suppress the CM noise and behaves as a lower impedance for DM current, as shown in Figure 10.

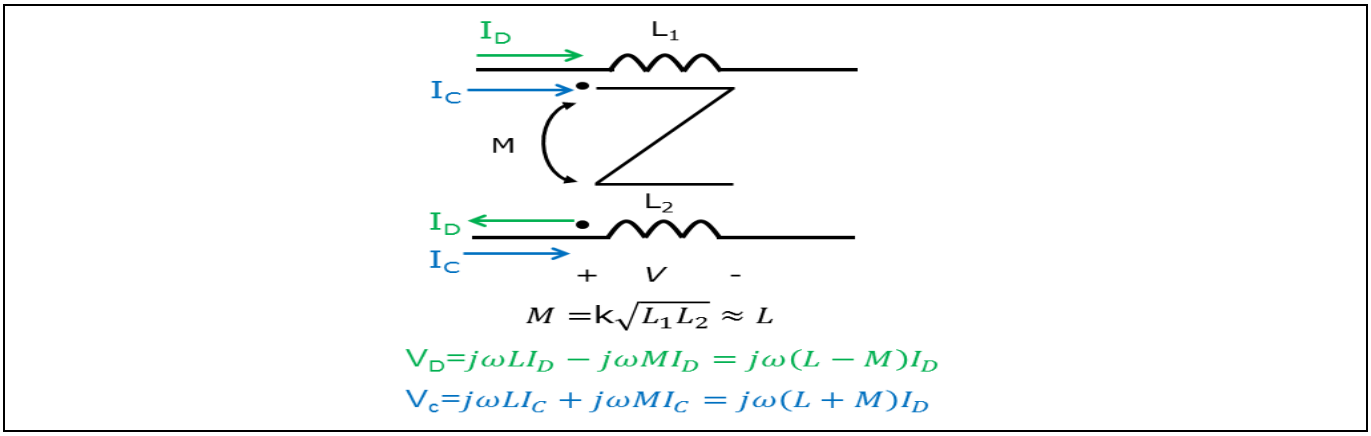


Figure 11 Impedance of a CMC for DM vs CM current

The impedance of a CMC is determined by the core size, core material and winding method. It is expected that it represents high impedance in the entire test frequency range. Ideally, the initial inductance of CMC is proportional to the square of the turns. Therefore more windings would create a higher inductance. However parasitic capacitance exists between windings, so more turns will create a higher parasitic capacitance, as shown in Figure 11. A suitable winding method is introduced to provide a higher inductance and a smaller parasitic capacitance with higher self-resonant frequency of the CMC.

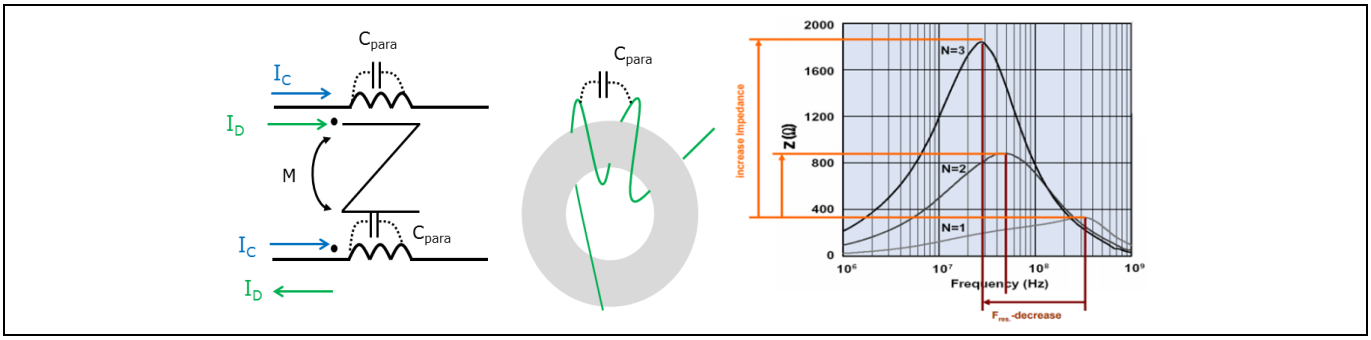


Figure 12 Parasitic capacitance and impedance of the CMC

The traditional winding method for a CMC is shown in Figure 12 (left-hand side). Two wires are wound from the bottom to the top of the core and then from the back to the bottom. The maximum number of layers for this winding method is two layers. The two winding endpoints being near one another may cause a higher intrawinding capacitance.

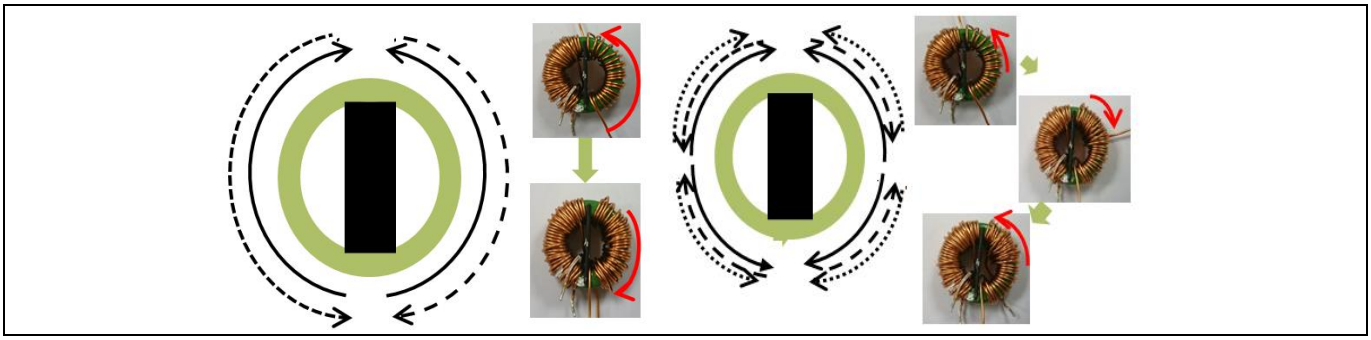


Figure 13 Traditional winding method for CMC (left); butterfly winding for CMC (right)

Figure 12 (right-hand side) introduces a new winding method for CMC. Start winding from the 3 o'clock and 9 o'clock positions up and forward to the top side and bottom and forward to the bottom side of the core, respectively. The maximum number of layers for this winding method is three. In contrast with the traditional winding method the endpoints of the winding are far away from each other, leading to a reduced intrawinding capacitance. The conducted emissions results from both CMCs are shown in Figure 13. The major difference between the CMCs is the conducted emissions at higher frequency range (greater than 10 MHz).

Figure 14 Conducted emissions results with traditional and butterfly wiring CMC

4.3 Reducing conducted emissions from the transformer

Normally it is not easy for the reader to visualize the CM current. One of the CM currents in the notebook adapter is induced by a high dv/dt node such as the drain electrode of the main switch. For example, there exists a capacitance between the earth plane and the copper area connected to the drain pin of the flyback MOSFET. Assuming a 1 cm^2 copper area has a 1.11 fF (10^{-15}F) equivalent capacitance then this would cause an 11.1 µA CM current to be generated with 10 V/ns voltage swing on main switch. This would lead to 555 µV measured by the LISN or, in case of no filter, 27.4 dBµV in the spectrum analyzer, as shown in Figure 14.

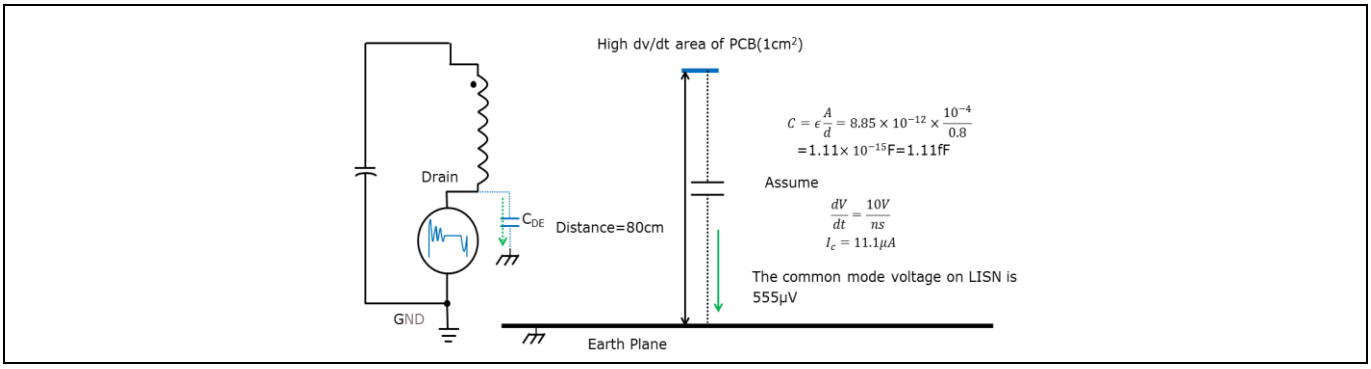


Figure 15 CM current from PCB copper to earth plane with high dv/dt

In addition, another CM current is derived from the voltage swing of the windings of the transformer as the MOSFET switches on and off. Plenty of parasitic capacitances exist in flyback transformers between the primary and secondary winding and the core and earth plane, as shown in Figure 15. CM currents flow through the parasitic capacitances between the primary and secondary windings and the core as the main MOSFET switches on or off.

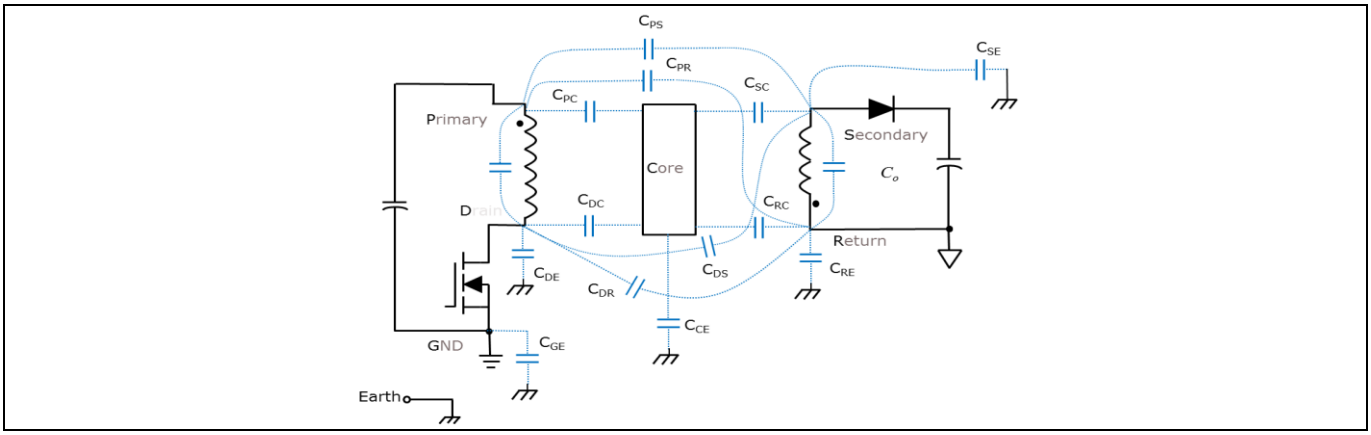


Figure 16 Capacitor model between windings, core and earth

Traditionally a non-closed copper strip, called Faraday's shielding, is placed between the primary-side and secondary-side winding to reduce the parasitic capacitance between windings. It is also connected to the primary GND node to provide another path to convert the CM current to DM current and reduce the total CM current in the flyback converter.

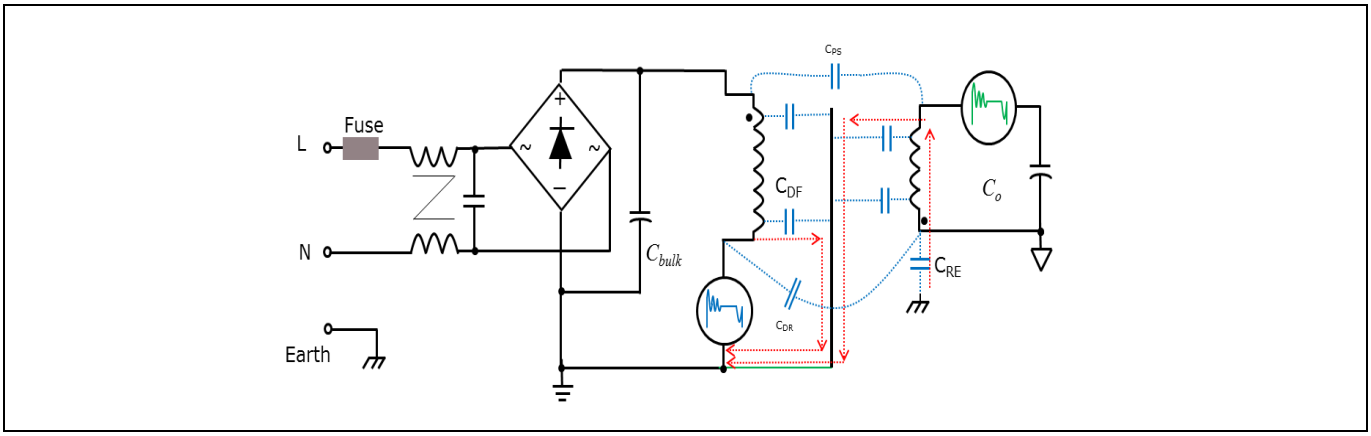


Figure 17 Capacitance model with Faraday's shielding in the transformer

Another method is called the "E-shield™ Transformer Technique," which is proposed by Power Integration Co. Instead of a copper strip a winding is wound inside of the transformer. It not only works as a shielding but also provides another current to internally cancel the CM current. Based on the test results, there will be three key characteristics for the "shielding winding." First of all the shielding winding is similar to Faraday's shielding, which means that a tight winding is better than a sparse winding for reducing the parasitic capacitance. Second, shielding winding is different from Faraday's shielding, which only provides a GND plate inside of the transformer. The shielding winding also provides a voltage source that is proportional to the turn ratio and voltage on the main winding. The voltage source of the shielding winding provides an opposing current to cancel the CM current inside of the transformer. It needs to be well designed. Finally, shielding winding is not always connected to primary-side GND.

Design transformers with shielding winding of 0.2 Φ single-wire/30 turns (A) and 0.2 Φ triple-wire/10 turns (B). Both shielding windings are connected to the primary side GND, as shown in Figure 17. A transformer with a shielding winding of 0.2 Φ single-wire/30 turns performs with worse conducted emissions than that with 0.2 Φ triple-wire/10 turns. The maximum difference is around 20 dB at 2 MHz. Mechanically, 0.2 Φ single-wire/30 turns and 0.2 Φ triple-wire/10 turns both offer the same coverage area in the transformer. The difference between them is that three times the voltage is induced in the winding of 0.2 Φ single-wire/30 turns compared with the winding of 0.2 Φ triple-wire/10 turns, which may generate an over-estimated current in the transformer.

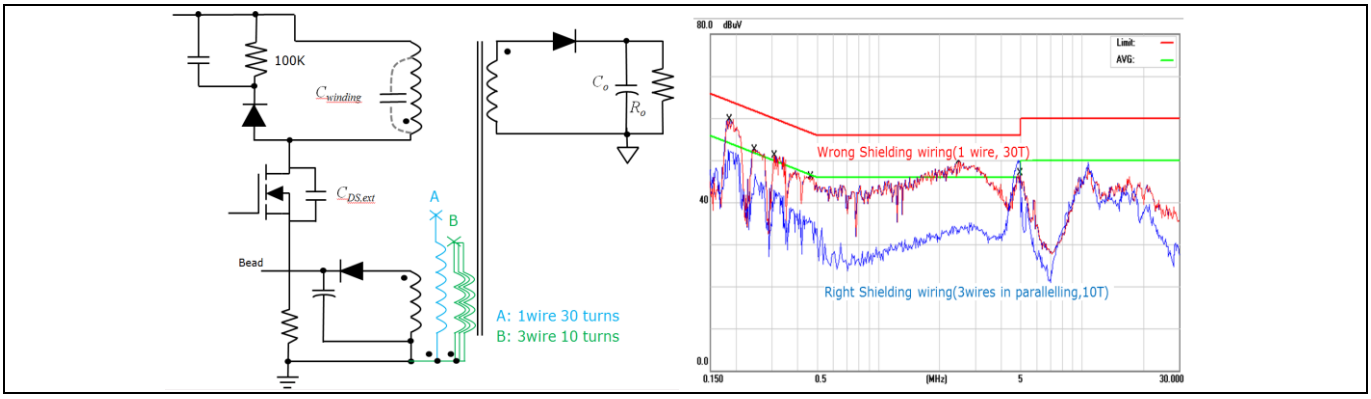


Figure 18 Conducted emissions results with one wire/30 T and three wires/10 T shielding winding at 115 V AC

In addition to the turn number of the shielding winding, the connection also influences the conducted emissions results. Adopting 0.2 Φ triple-insulated-wire/10 turns shielding winding in transformers with different connection to the V_{bulk} pin (case A) and GND (case B) is shown in Figure 18. Both transformers give similar results in the low frequency range (less than 1MHz), but that with shielding winding connected to the V_{bulk} pin (A) gives a higher maximum of 10 dB conducted emissions in the high frequency range (greater than 1MHz).

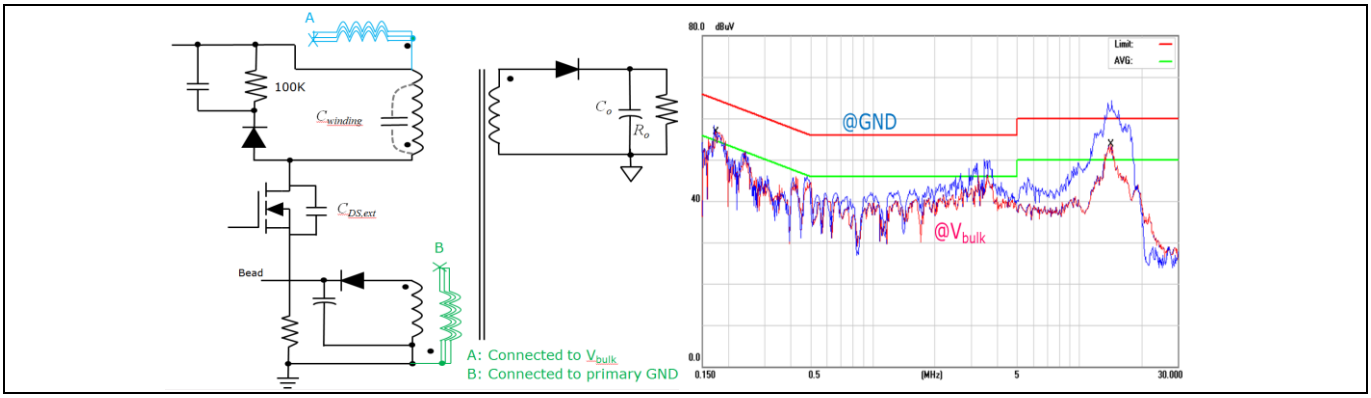


Figure 19 Conducted emissions results from different connections of shielding winding (at 230 V AC)

As described above, the transformer plays an important role in the conducted emissions in the flyback converter. The different transformer structure is the key to determining the conducted emissions in the notebook adapter. The reader may use this concept to design a new transformer and compare the results.

4.4 Reducing conducted emissions from the circuit

The transformer and CMC are the key components in the flyback converter that determine the conducted emissions. On the other hand, conducted emissions can be improved by other methods in the circuit. For example, a ferrite bead in series with the rectifier improves the conducted emissions. A ferrite bead in series with the V_{CC} loop improves the conducted emissions up to 8 dB, as shown in Figure 19.

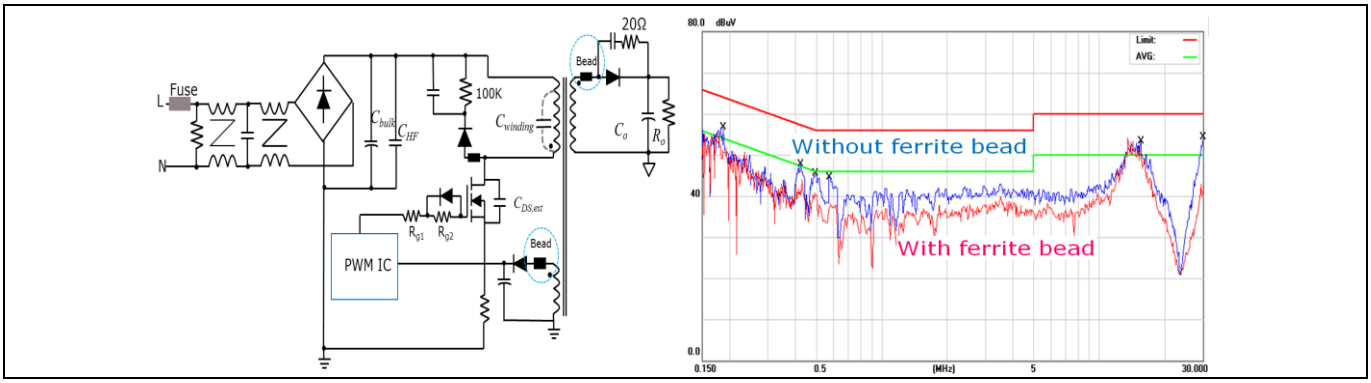


Figure 20 Schematic with the ferrite bead in series with the rectifier (left); conducted emissions comparison with and without bead in V_{CC} circuit (at 230 V AC) (right)

Another efficient way to improve the CM conducted emissions is to use a Y-capacitor between the primary and secondary sides. This Y-capacitor provides a path to divert the CM current from the secondary side back to the primary side. It turns a partial CM current into a DM current and improves the conducted emissions. Ideally, a larger Y-capacitance results in better conducted emissions but with the consequence of increased leakage current, which means that the Y-capacitance is limited by the leakage current. Figure 20 (right) shows that the notebook adapter with a 680 pF Y1-capacitance improves by about 10 dB when compared to one with a 330 pF Y1-capacitance.

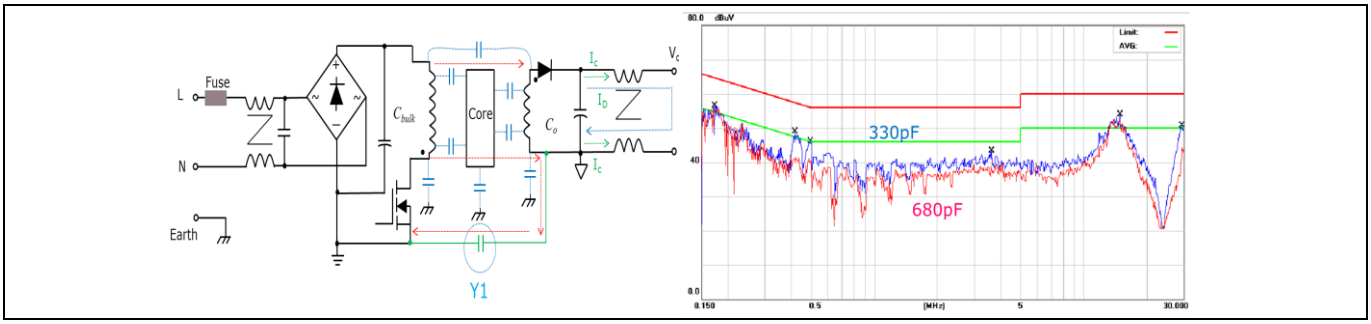


Figure 21 Y1-capacitor between primary and secondary sides to improve conducted EMI (left); Y1-capacitance influences the common EMI (at 230 V AC) (right)

So far, all of the solutions introduced above are methods of “attenuating transmission efficiency” between the noise source and receiver (LISN). It is well known that a faster switching MOSFET improves efficiency at the cost of EMI. The best way to have a high-efficiency notebook adapter is to make the noise transmission inefficient rather than reduce the switching speed.

The MOSFET is the key component determining the noise magnitude in the flyback converter. During the MOSFET turn-on period, the MOSFET charges the winding capacitor of the transformer, discharges the $C_{DS,ext}$ and turns off the rectifiers in the circuit. The on-gate resistance ($R_{g,on}$) of the MOSFET influences the conducted emissions in the HF range. For notebook adapters with an $R_{g,on}$ of 300 Ω and 680 Ω, the conducted emissions are almost the same in the LF area (less than 1 MHz) but the maximum difference at 12 MHz is 15 dB, as shown in Figure 21.

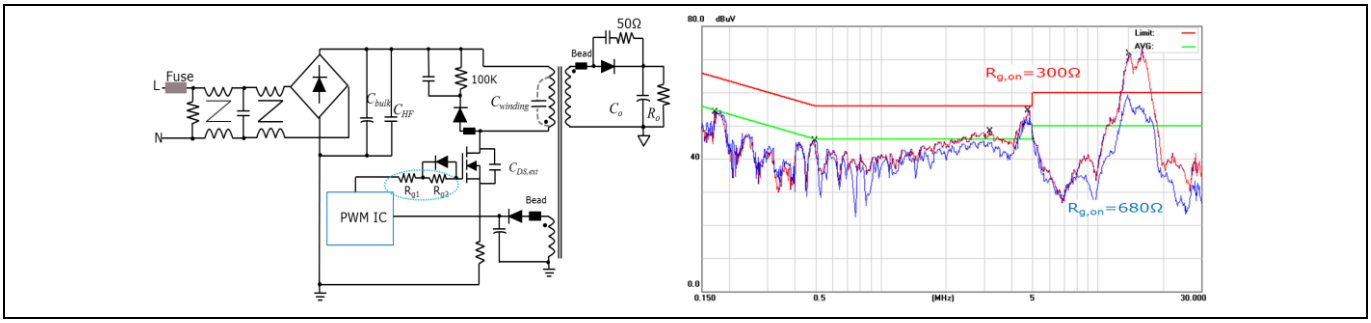


Figure 22 Conducted EMI comparison with different $R_{g,on}$ (at 230 V AC)

5 Solutions for radiated emissions

To understand the solutions for radiated emissions, one must first understand the test connection, radiated emissions requirement, and the factors that influence the spectrum amplitude and transmission efficiency.

5.1 Measurement of radiated emissions

Figure 22 shows the radiated emissions limitations from FCC and CISPR. The test frequency is from 30 MHz to 1 GHz.

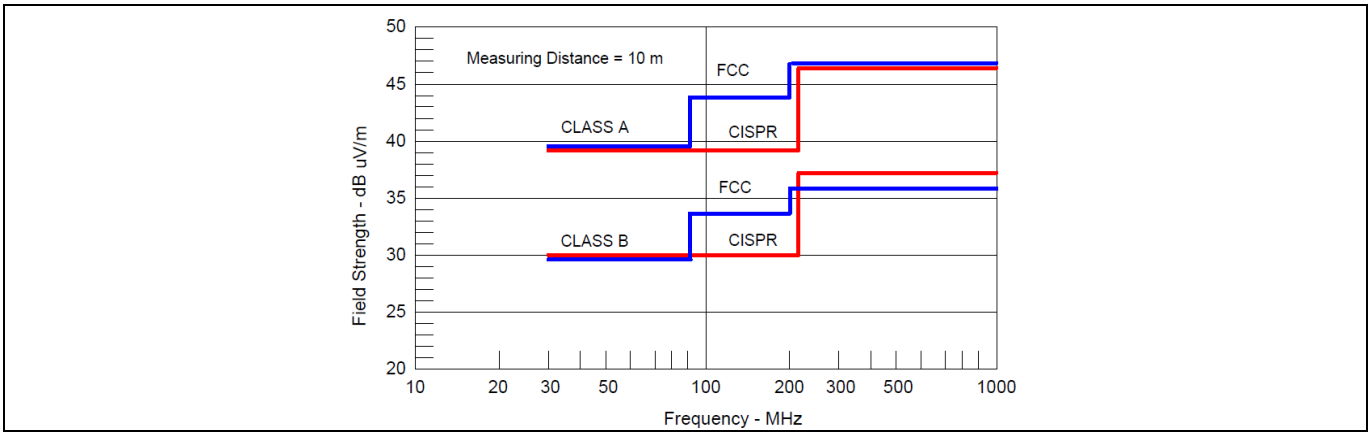


Figure 23 Radiated emissions limitation from FCC and CISPR

The radiated emissions test is shown in Figure 23; it includes the PSU, antenna and EMI receiver. The set-up of the EMI chamber or open EMI test site is made according to requirements.

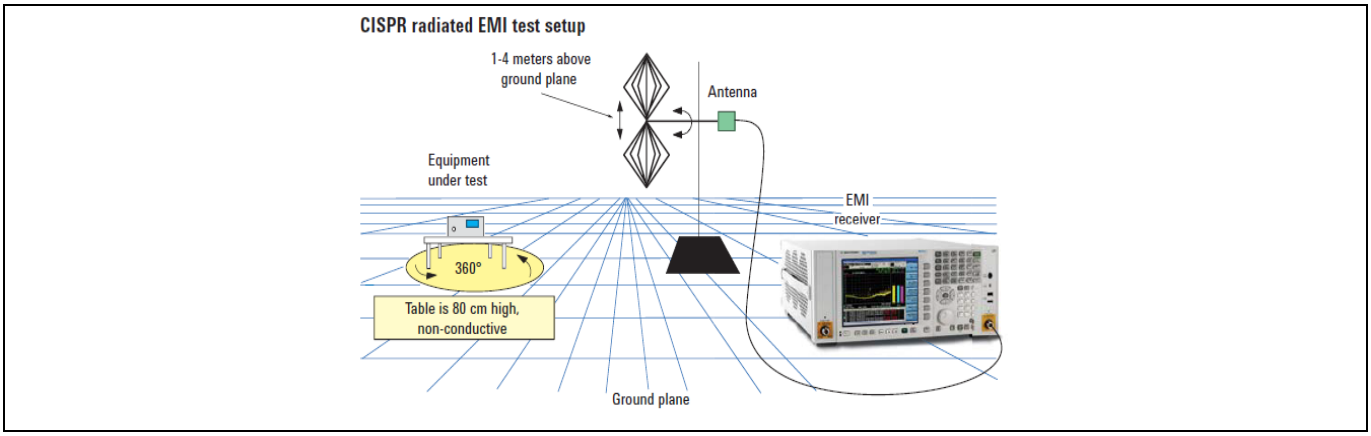


Figure 24 Radiated EMI measurement (from Agilent Technology)

5.2 Spectrum of signals

Consider a periodic trapezoidal wave of period T, signal level A, on-time, and an equal rising/falling time t_r. The corresponding spectrum is obtained as shown in Figure 24. The amplitude of the spectrum is as F is less than F1, which decays with a slope of -20 dB/decade when F1 is less than F is less than F2 and with a slope of -40 dB/decade when F is greater than F2.

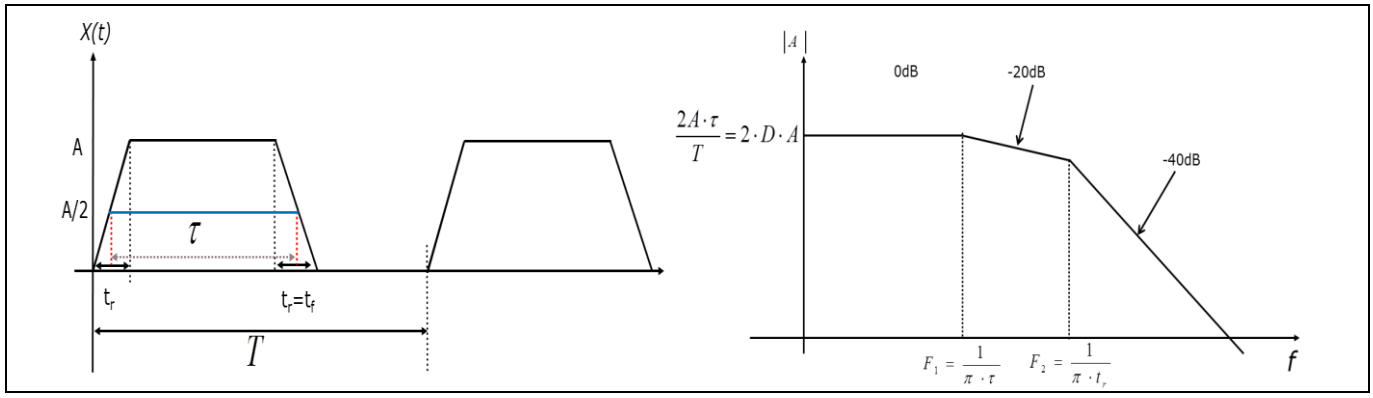


Figure 25 Time domain and spectrum of a periodic trapezoidal wave

Figure 25 shows the time domain and spectrum of an isosceles triangular-pulse waveform with signal level A and rising/falling time t_r. The amplitude of the spectrum is $2A \cdot t_r$ when F is less than F1, which decays with a slope of -40 dB/decade when F is greater than F1.

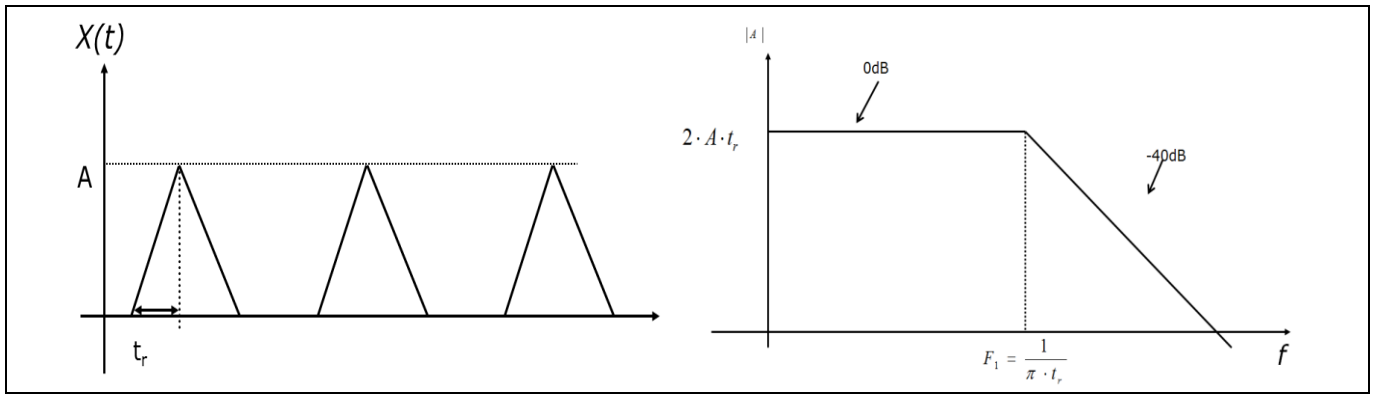


Figure 26 Time domain and spectrum of isosceles triangular-pulse waveform

According to the description above, the amplitude of the spectrum is determined by the signal level, period, on-time and rising/falling time of the signal. The corner frequency is determined by the on-time and rising/falling time. Even the voltage or current waveform in the flyback converter is not a signal with a single frequency or on-time. The spectrum consists of a main switching signal of LF (~ several 10 kHz) with jitter, a signal of parasitic resonant frequency (~ MHz), and the board band signal as the MOSFET and rectifier turn on/off. Further detailed information is shown in [4]. The voltage waveform is separated into several individual elements. The spectrum of each element is obtained and recombined as a total spectrum, as shown in Figure 26.

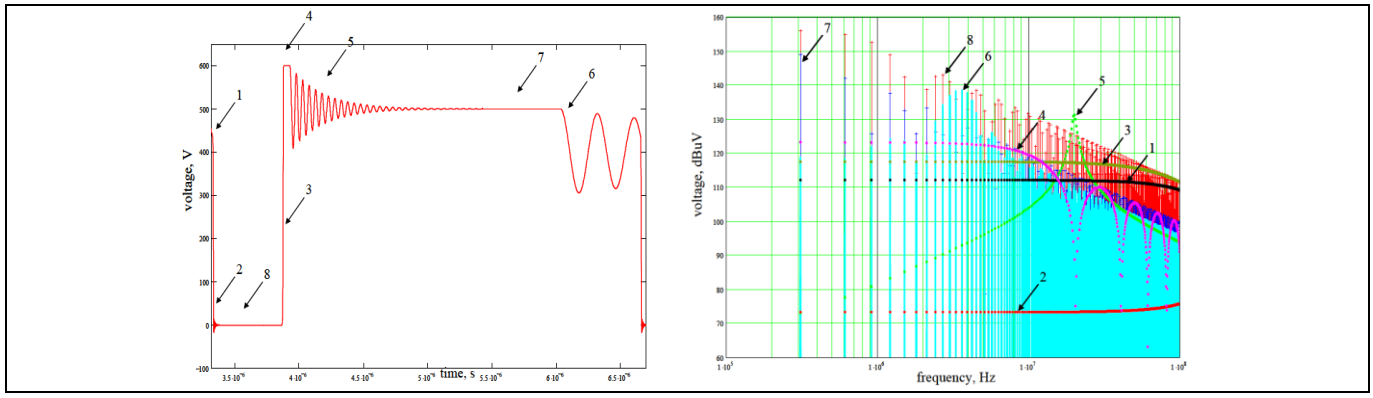


Figure 27 The voltage waveform of the flyback MOSFET and its spectrum

From the voltage waveform and its spectrum, it is easy to find the possible corresponding noise source from the radiated emissions test results.

5.3 Simple emissions models for wires and PCB lands

Understanding the possible path and radiation transmission in the system is also important when resolving radiated emissions issues. Major radiated emissions in a notebook adapter come from the DM/CM voltage/current that radiates through the antenna unexpectedly, such as the current loop, copper area, transformer, input cable and output cable, as illustrated in Figure 27.

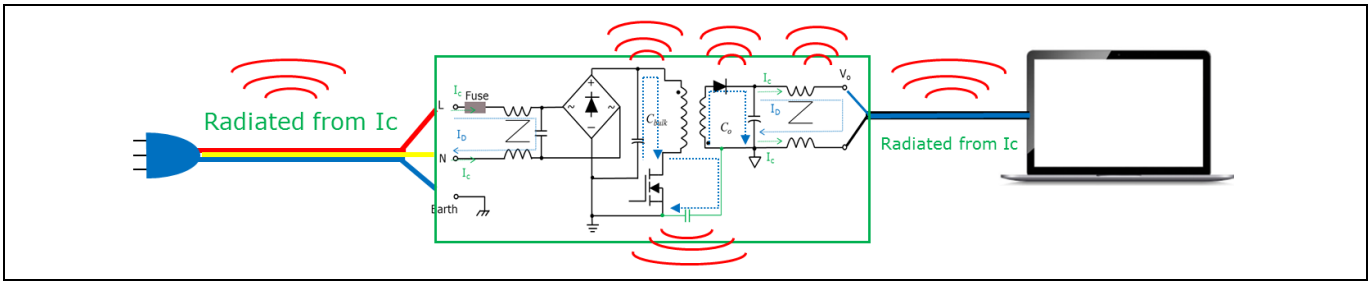


Figure 28 Simple radiated emissions model in a notebook adapter

The complicated theory describing the electromagnetic waves of an antenna will not be discussed or applied here. We will only try to describe the radiated emissions in a simplified manner. Consider a loop of length L and width W with a current I_1 and I_2 in the circuit. In the circuit a DM current I_D and CM current I_C are involved in making it so $I_1 = I_C + I_D$ and $I_2 = I_C - I_D$. Obviously, the magnetic field generated by DM current is enhanced inside of the loop but canceled outside of the loop. In contrast, the magnetic field generated by CM current is canceled inside of the loop but enhanced outside of the loop, as shown in Figure 28.

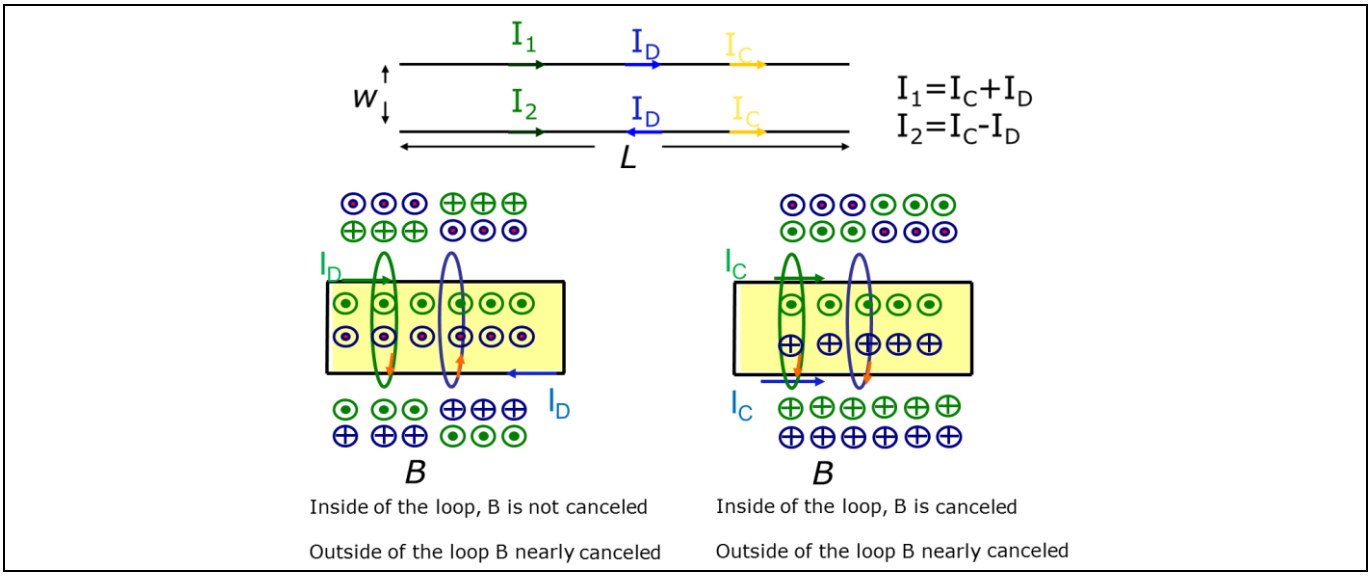


Figure 29 Magnetic field inside/outside of current loop by DM/CM current

Furthermore, consider the electric field outside of the loop as shown in Figure 29. The electric field generated by the DM current I_D is E_D and the electric field generated by a CM current I_C is E_C. According to [1], E_D and E_C are as shown below in (1) and (2).

$$|E_{D,max}| = 1.316 \times 10^{-14} \frac{|I_D| \cdot f^2 \cdot L \cdot W}{d} \quad (1)$$

$$|E_{C,max}| = 1.257 \times 10^{-6} \frac{|I_C| \cdot f \cdot L}{d} \quad (2)$$

Where d is the distance from the current loop to the receiver or antenna.

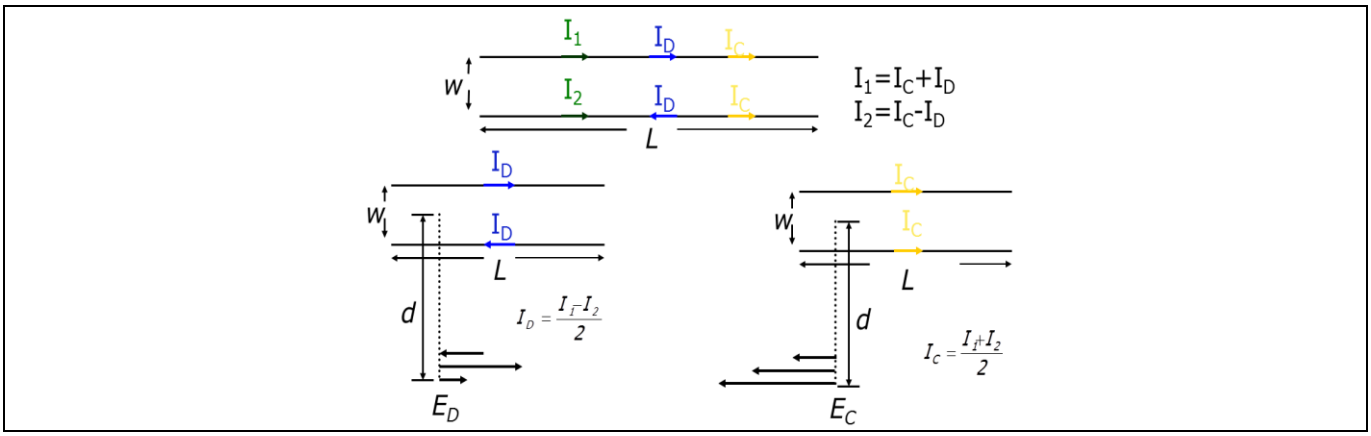


Figure 30 Simplified estimate of the maximum radiated emissions

According to formula (1), it is found that the electrical field E_D is proportional to the DM current I_D and the loop area L × W. In principle, two methods are useful for attenuating the electrical field generated by a DM current, reducing the DM current level, or shrinking the loop area. However, the DM current in the circuit is a function current that cannot be reduced. One method for reducing the amplitude at HF is to extend the rising/falling time of the signal and create a lower corner frequency of $\frac{1}{\pi \cdot t_r}$.

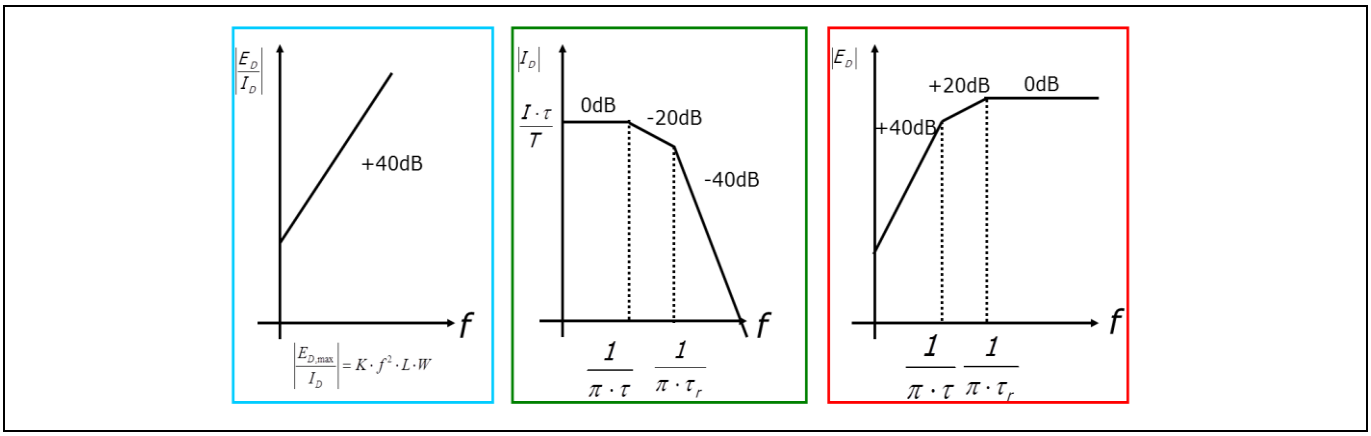


Figure 31 Spectrum of the electrical field generated by DM current

Another method is to shrink the loop area of the DM current. A decoupling capacitor is used to provide a low impedance path to effectively minimize the loop area, especially for the high di/dt current loop, as shown in Figure 31.

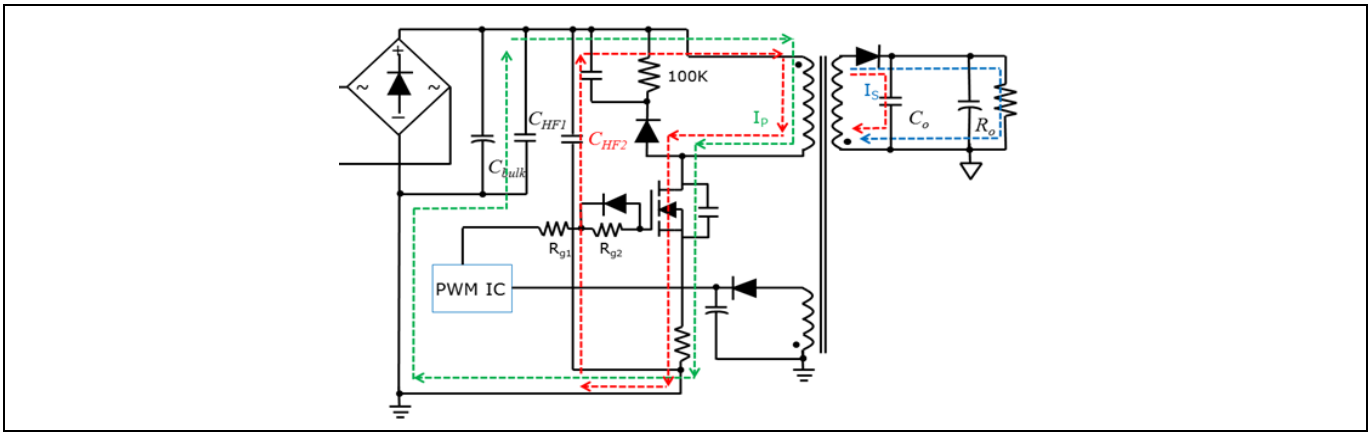


Figure 32 A decoupling capacitor shrinks the DM current loop area

In a SMPS the differential current is the functional current that offers power such as the primary-side current, which stores energy in the transformer as the MOSFET is turned on. However, the CM current is an unintentional current generated from inductive or capacitive coupling. In formula (2) we can see that the electrical field E_c generated by the CM current is proportional to the amplitude of I_c and the loop length L. As described above, the CM noise is from capacitive coupling of the high dv/dt node such as the drain of the primary-side MOSFET or the anode of the output rectifier. Besides reducing parasitic capacitance, it is useful for slowing the voltage slope of the high dv/dt node. An effective method is not to reduce the original CM current amplitude ($i = C\frac{dv}{dt}$) but to reduce the frequency of the concert ($\frac{1}{\pi \cdot t_r}$). Doing so also attenuates the spectrum amplitude at high frequencies.

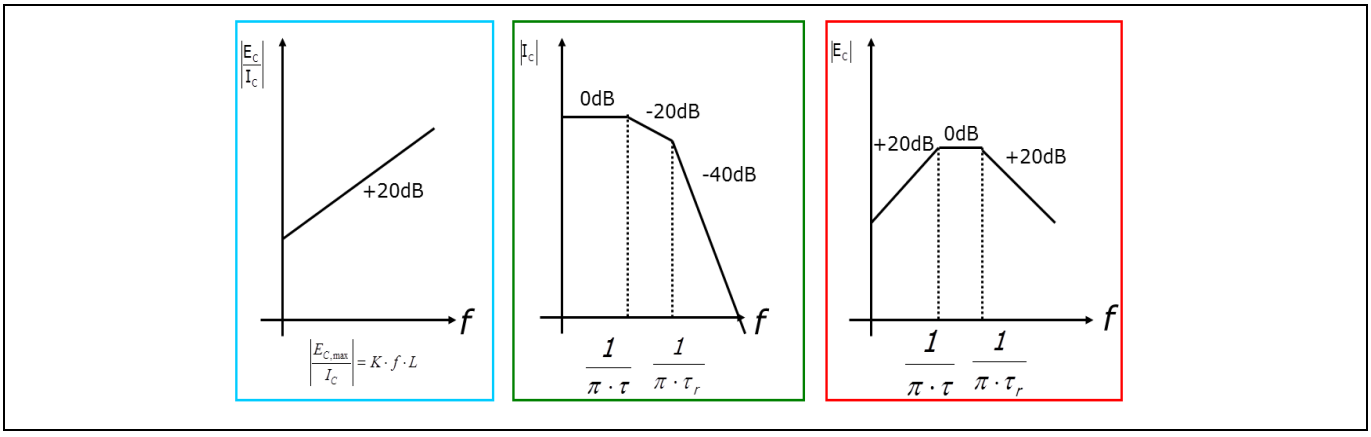


Figure 33 Spectrum of electrical field generated by CM current

Another CM noise source is that of a cable in a time-variant magnetic field. CM current is inducted by the magnetic field with same frequency as the magnetic field. Such magnetic fields may be caused by an unshielded transformer or inductor in circuit or by an ungrounded heatsink. An antenna which is induced through a parasitic capacitor between the MOSFET and heatsink with high dv/dt radiates in the field, as shown in Figure 33. A method for attenuating the magnetic field is to internally ground the connection of the heatsink and shield the transformer with a copper strip.

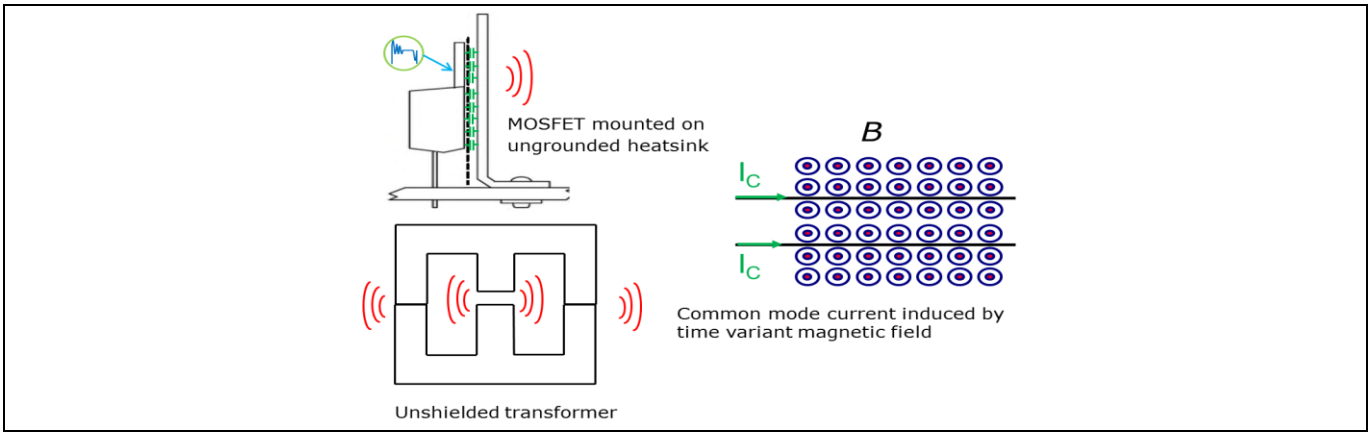


Figure 34 CM current induced by time-variant magnetic field

According to antenna theory, a cable is considered as an effective unintended radiator when the cable length is equal to the half-wavelength (λ/2) or quarter-wavelength (λ/4) of the noise signal. A notebook adapter with a long input and output cable length radiates more effectively than other SMPS. This means that the receiver obtains higher radiated emissions even with the noise source at the same level. For example, in an adapter with a 2 m input and output cable 75 MHz and 150 MHz noise radiated emissions will be more significant due to the wavelength. Besides trying to reduce the noise level, using some other filter is helpful in suppressing the noise emissions through the input and output cable.

5.4 Reducing the radiated emissions from the circuit input and output common mode choke

Normally, the basic purpose of the input CMC is to suppress the conducted emissions. However, the maximum frequency of the conducted emissions limit is 30 MHz, which is also the beginning frequency of the radiated emissions. A power supply with a CMC that has a lower self-resonant frequency may pass the conducted emissions but fail in radiated emissions at around 30 MHz. This may be a result of the parasitic capacitance tolerance of the CMC, transformer and MOSFET. An extra CMC of higher self-resonant frequency used in the input or output is helpful for reducing the radiated emissions.

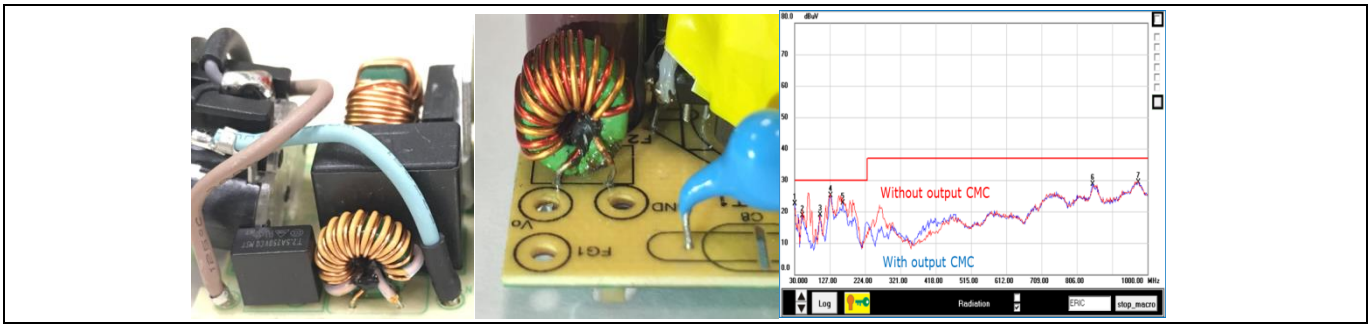


Figure 35 Extra CMCs for suppressing the radiated EMI

5.5 Ferrite bead

A ferrite bead in series with the output rectifier suppresses the current slope of the reverse recovery current on the output rectifier and is useful for reducing radiated emissions, as shown in Figure 35.

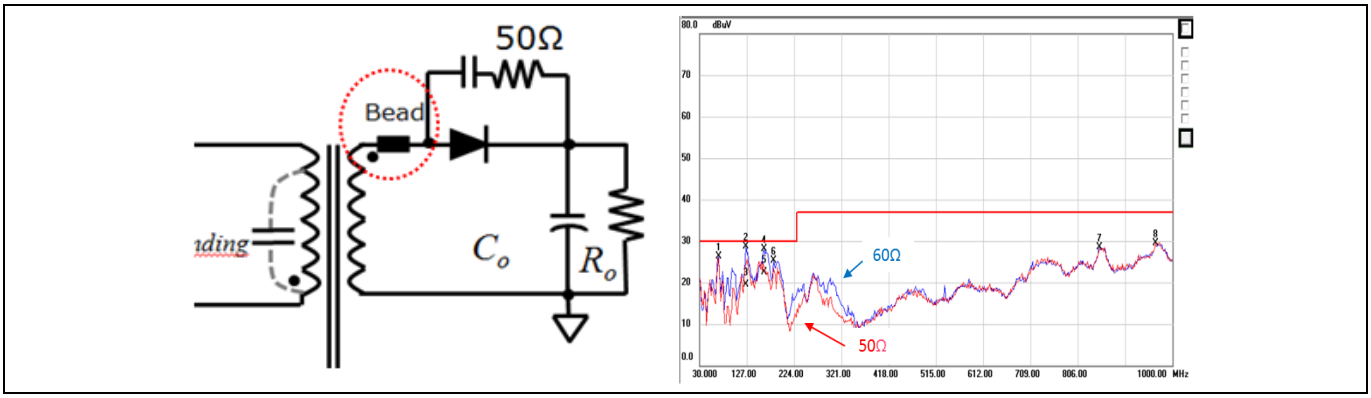


Figure 36 Radiated emissions with 50 Ω and 60 Ω ferrite bead

5.6 On-gate resistance, $R_{g,on}$

When the MOSFET turns on, the currents on the MOSFET come from the charging current of the transformer winding parasitic capacitance, the discharging current of $C_{DS,ext}$ and the reflected reversed recovery current from the output rectifier. It is possible that the reflected reverse recovery current level on the primary side can be greater than the current offering energy when the MOSFET is turned on. Radiated emissions at 115 V AC may be worse than that at 230 V AC due to the reflected reverse recovery current. A higher on-gate resistance ($R_{g,on}$) controls the current rising slope and the current level as the MOSFET is turning on. The reverse recovery current level and voltage slope on the anode of the output rectifier is minimized as well. 700 V CoolMOS™ P7 has an efficient performance even with a higher $R_{g,on}$ and improves the radiated emissions. From the current waveform in Figure 36 and the radiated emissions in Figure 37 it is shown that a higher $R_{g,on}$ is helpful in reducing the current level, the rise time and the spectrum level.

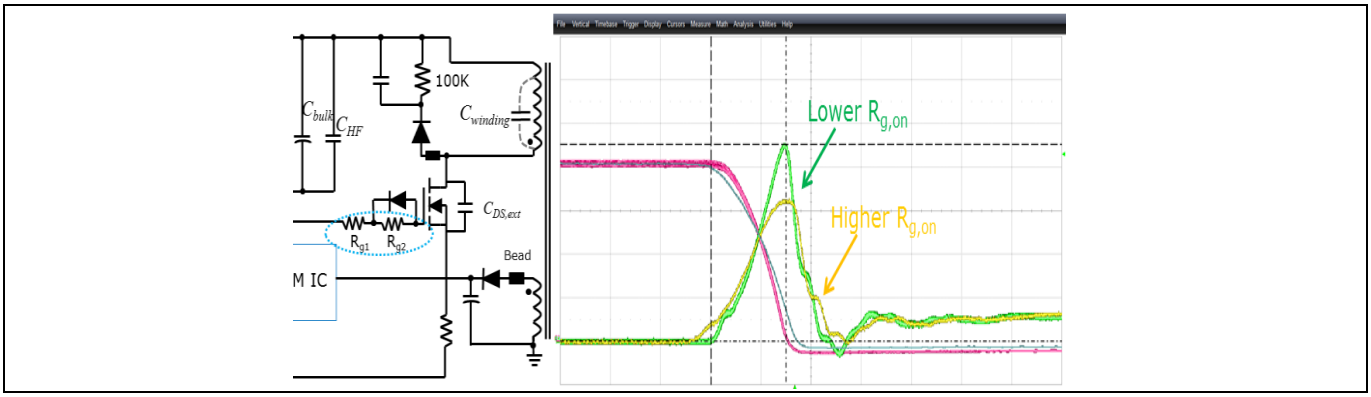


Figure 37 Current waveforms with different $R_{g,on}$

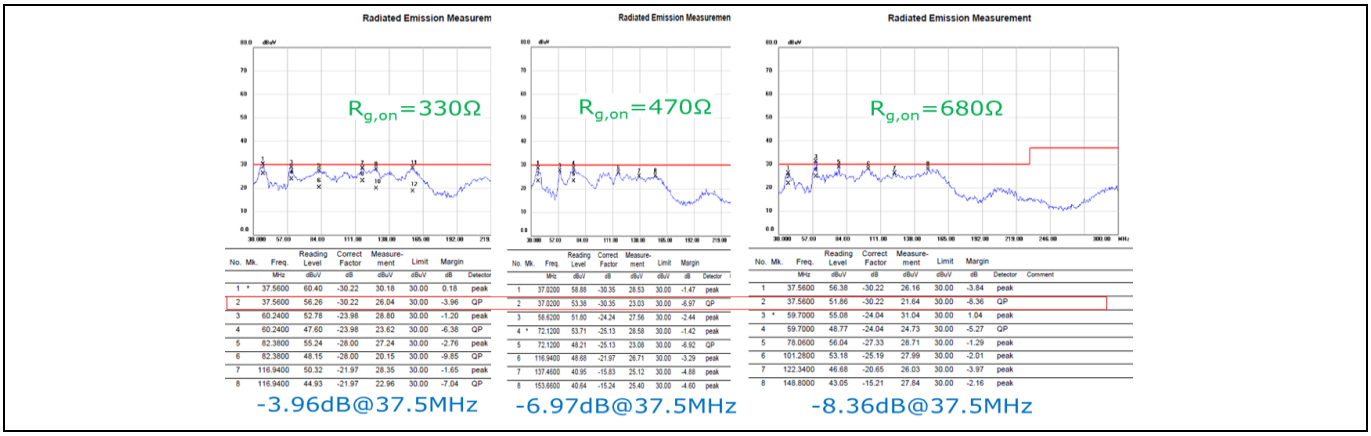


Figure 38 Radiated emissions with different $R_{g,on}$

5.7 Off-gate resistance ($R_{g,off}$) and $C_{DS,ext}$

The voltage slope of the MOSFET and the rectifier influence CM noise in the notebook adapter. The former is determined by the off-gate resistance ($R_{g,off}$) and C_{oss} value of the MOSFET. In general, to prevent the MOSFET from additional turn-off losses the maximum acceptable $R_{g,off}$ is 20 Ω. The alternative effective solution is to parallel an extra HV capacitor $C_{DS,ext}$ with the MOSFET to reduce the voltage slope of the MOSFET and the CM current. A side-effect of using $C_{DS,ext}$ is that there will be more power dissipation on the MOSFET. Traditionally, a smaller capacitor is used in parallel with a non-SJ MOSFET due to efficiency and thermal concerns. Failed radiated emissions may occur after mass production, which is different from that of the design phase. The high tolerance of the output capacitance of the MOSFET is not considered to be covered by a higher $C_{DS,ext}$. A higher $C_{DS,ext}$ may possibly be paralleled with the 700 V CoolMOS™ P7 due to the smaller capacitive and switching losses. Controllers with valley switching or QR control help to minimize the capacitive losses at high-line input voltages.

6 Thermal solutions

The thermal tests of the notebook adapter are completed in a thermal chamber set at 40°C with a 90 V AC input to measure the temperature of power components and the surface of the notebook adapter. In general, a notebook adapter is filled with thermally conductive adhesive to distribute the heat through the adapter. The MOSFET, whose thermal conductivity is primarily transferred by the lead-frame, is mounted on the bottom side of the PCB and does not as easily conduct heat. A higher thermal resistance between the die and molding compound constrains heat from spreading from the top of the MOSFET. Relying on the PCB copper area alone is not enough in a high-density and cost-optimized application. A jumper on the top side soldered on the copper area of the drain pin spreads the heat to the heatsink to reach ambient temperature through the thermal conductivity adhesive material, as shown in Figure 38.

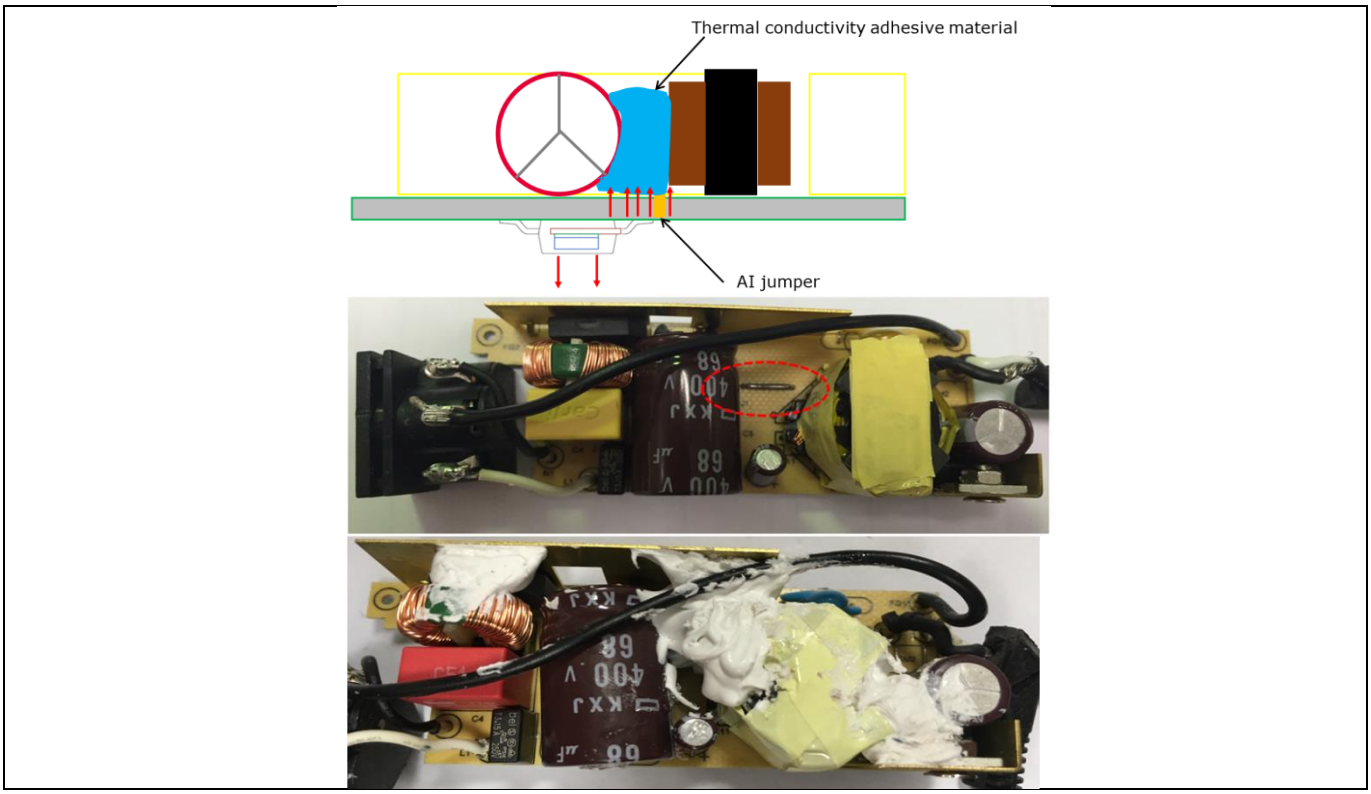


Figure 39 Thermal solutions from MOSFET to heatsink

A thermal conductive pad is also helpful for reducing the temperature of the MOSFET.

Figure 40 Thermal pad from MOSFET to bottom side

Due to the restrictions of the equipment, the thermal testing of the reference board is performed in a 25°C ambient temperature. The temperatures are measured with a thermocouple. Operating the reference board at

45 W and 25°C with 90 V AC input, we can measure the temperature of the key components, such as the MOSFET, bulk capacitor, winding and core of the transformer, as shown in Figure 40.

Table 3 Temperature of key power components

Component	Temperature
Flyback MOSFET (IPN70R600P7S)	96.2°C
Bulk capacitor	94.5°C
Transformer wire	91.6°C
Transformer core	99.4°C

Based on the measured temperature and waveform of the MOSFET, the power loss of the MOSFET is around 0.83 W. The temperature of the MOSFET is around 110°C, with a thermal resistance of 18.2°C/W.

7 Schematic

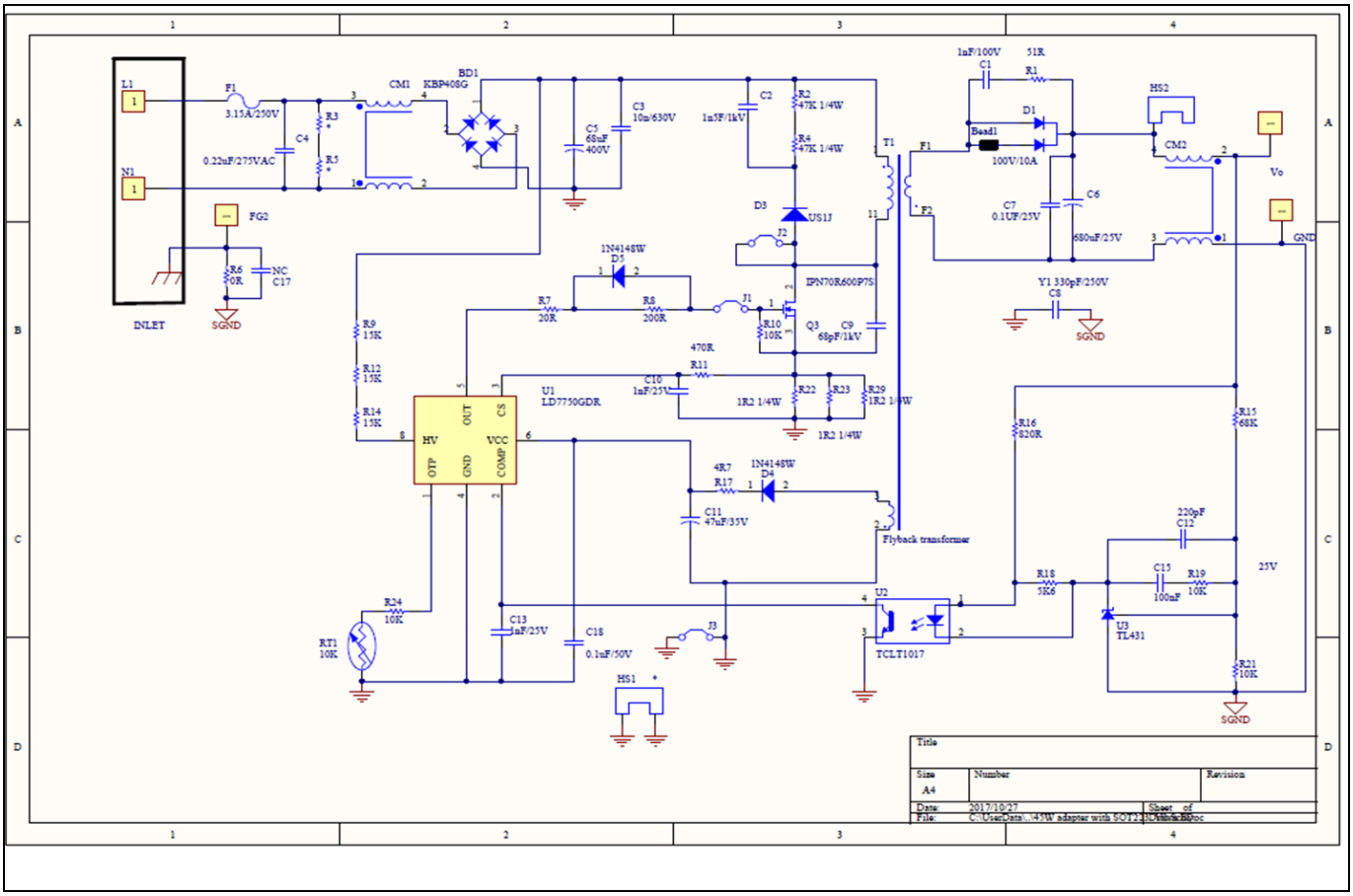


Figure 41 Schematic of reference board

8 PCB layout

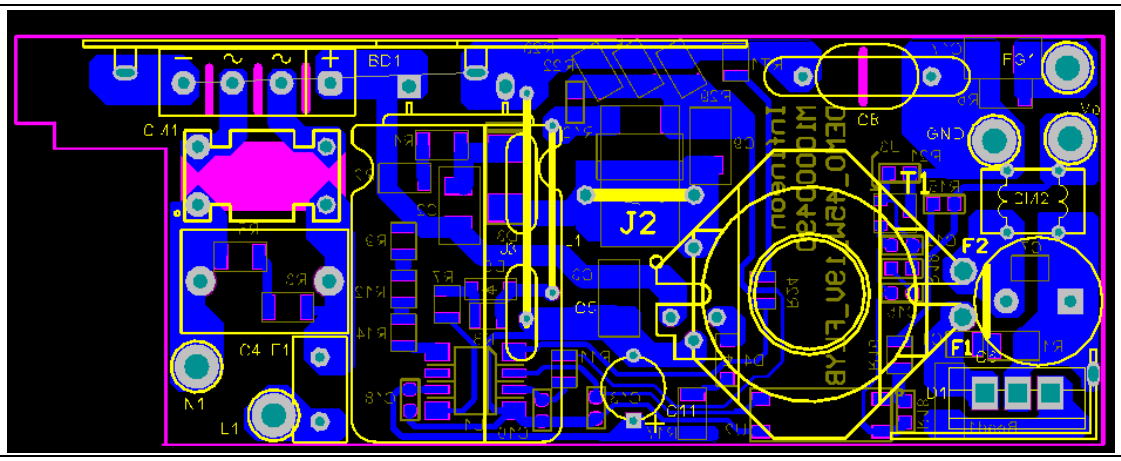


Figure 42 PCB layout reference board

9 Bill of Materials (BoM)

Table 4 Bill of materials with Infineon components in bold

Designator	Comment	Description	Part no./Order no.	Manufacturer
BD1	KBP208G	2.0 A glass passivated bridge rectifier	KBP208G	Diodes
Bead1	SMD 50 Ω ferrite bead	SMD 50 Ω ferrite bead	2518065007Y6	Fair-Rite Product Corp
C1	1 nF/100 V	Ceramic capacitor, X7R, CAP0805	C2012X7R2A102K085AA	TDK
C2	1 nF/630 V	1 nF multi-layer ceramic capacitor MLCC 630 V DC ±5 percent C0G dielectric 1206 SMD, max. temp. 125°C	CGA5F4C0G2J102J085AA	TDK
C3	10 nF/630 V	10 nF multi-layer ceramic capacitor MLCC 630 V DC ±5 percent C0G dielectric 1206 SMD, max. temp. 125°C	CGA5L4C0G2J103J160AA	TDK
C17	Not connected	Not connected		
C4	0.22 µF/275 V AC	X2 safety capacitor	890334023028	Wurth Elektronik
C5	68 µF/400 V	Aluminum electrolytic capacitor	EKXJ401ELL680ML25S	NipponChemi-Con
C6	680 µF/25 V	Aluminum electrolytic capacitor	EEUFM1E681B	Panasonic
C7	1 µF/25 V	General-purpose ceramic capacitor, CAP0805	C0805C105K3PACTU	KEMET
C8	Y1 680 pF	AC-line rated ceramic disk capacitors	VY1681M31Y5UQ63V0	Vishay
C9	68 pF/1 kV	68 pF multi-layer ceramic capacitor MLCC 1 kV DC ±5 percent C0G dielectric 1206 SMD, max. temp. 125°C	1206AA680JAT2A	AVX
C10, C12, C13, C15	1 nF/25 V	Ceramic capacitor, NPO, CAP0603	GRM1885C1E102JA01D	Murata
C11	47 µF/35 V	Aluminum electrolytic capacitor	EKZH350ELL470ME11D	NipponChemi-Con
C14	Not connected	Not connected		
C18	0.1 µF/50 V	General-purpose ceramic capacitor, X7R, CAP0603	C1608X7R1H104K080AA	TDK
CM1	20 mH CMC	EMI CMC		Customized component
CM2	Short-circuit	Short-circuit		
D1	NTSV30H10G	100 V/30 A, very low forward voltage trench-based Schottky rectifier	NTSV30H10G	ON-SEMI
D3	US1J	Surface-mounted ultra-fast diode	US1J	US1J-E3/61T
D4, D5	1N4148WS	Ultra-fast diode	1n4148WS	Diodes
F1	3.15 A/250 V	Fuse	6973150	Bel Fuse Inc.
J1	Jumper	0.4 Φ		
J2	Jumper	1.2 Φ		
J3	Jumper	0.6 Φ		
Q3	**IPN70R600P7S**	**NMOS, 700 V**	**IPN70R600P7S**	**Infineon**
R1	51 R	Chip resistor, 5 percent, RES0805	CRCW0805051R0JKEA	Vishay
R2, R4	47 K/0.25 W	Chip resistor, 5 percent, RES1206	CRCW120647K0JKEA	Vishay
R3, R5	Not connected	Not connected		
R6	0 R	Chip resistor, 5 percent, RES0805	CRCW08050000Z0EA	Vishay
R7	20 R	Chip resistor, 5 percent, RES0805	CRCW0805020R0JKEA	Vishay
R8	620 R	Chip resistor, 5 percent, RES0805	CRCW0805620R0JKEA	Vishay
R9, R12, R14	15 K	Chip resistor, 5 percent, RES0805	CRCW080515K0JKEA	Vishay

R10, R19, R21	10 K	Chip resistor, 1 percent, RES0603	CRCW060310K0FKEA	Vishay
R11	470 R	Chip resistor, 5 percent, RES0805	CRCW0805470R0JKEA	Vishay
R15	68 K	Chip resistor, 1 percent, RES0603	CRCW060368K0JKEA	Vishay
R16	820 R	Chip resistor, 5 percent, RES0805	CRCW0805820R0JKEA	Vishay
R17	4R7	Chip resistor, 5 percent, RES0805	CRCW08054R70JKEA	Vishay
R18	5K6	Chip resistor, 5 percent, RES0603	CRCW060305K6JKEA	Vishay
R24	10K	Chip resistor, 1 percent, RES0805	CRCW080510K0FKEA	Vishay
R22, R23, R29	1R2/0.25 W	Chip resistor, 1 percent, RES1206	CRCW12061R20FNEA	Vishay
RT1	10 K	Chip resistor, NTC thermistors, RES0805	NCP21XV103J03RA	Murata
R30	Not connected	Not connected		
T1	Flyback transformer			Custom component
U1	LD7750RGR, SOP-8	Flyback controller	LD7750R GR	Leadtrend
U2	TCLT1000	Photocoupler	TCLT1000	Vishay
U3	TL431 (SOT-23-3)	TL431 precision programmable reference	TL431ACDBZR	TI

10 Transformer construction

Inductance: Pin 1 to pin 11 inductance = 700 µH ± 3 percent; leakage inductance less than 25 µH

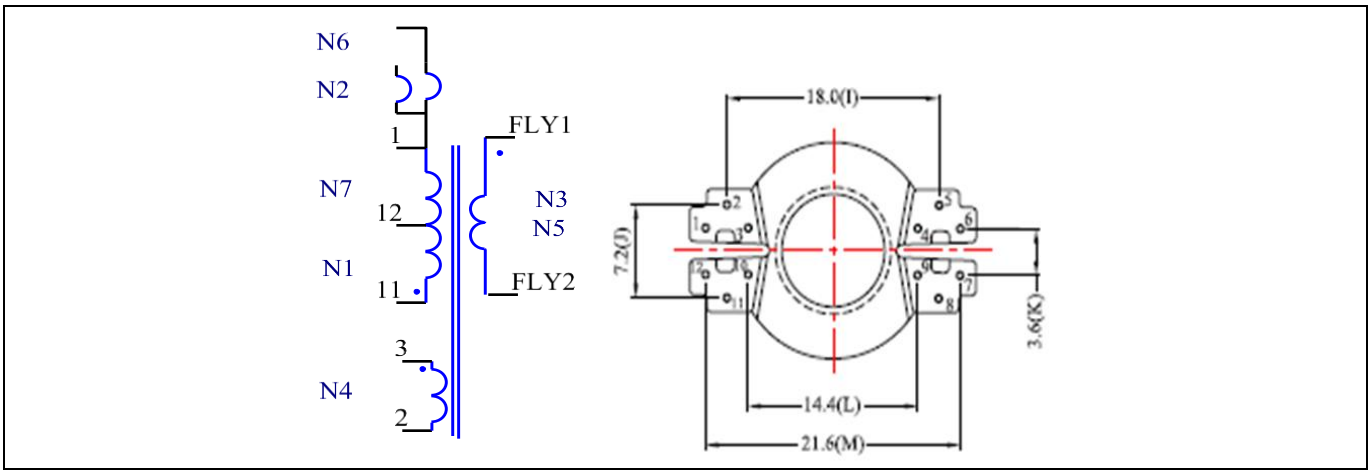


Figure 43 Pin assignment of the transformer and bobbin of RM8

Table 5 Transformer construction

No.	Start	End	Wire	Turns	Wire mode	Tape	Remark
N1	11	12	0.25Φ × 1	32	1 layer	2 layer	
N2	1	-	0.2Φ × 3	10	1 layer	2 layer	
N3	Fly1	Fly2	0.5 × 1	10	1 layer	2 layer	*
N4	3	2	0.2Φ × 3	10	1 layer	2 layer	
N5	Fly1	Fly2	0.5Φ × 1	10	1 layer	2 layer	*
N6	1	-	0.2Φ × 3	10	1 layer	2 layer	
N7	12	1	0.25Φ × 1	30	1 layer	2 layer	
N8	2		0	–			Copper strip

* Triple-insulated wire

11 Common mode choke construction

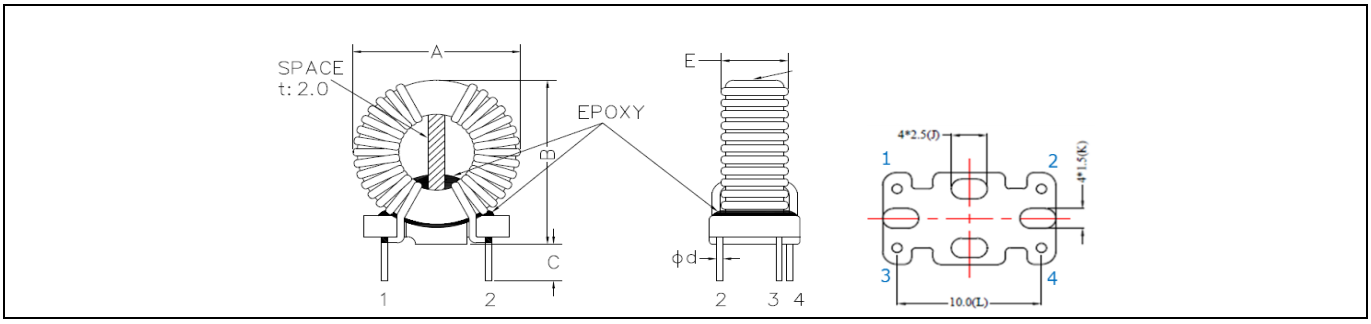


Figure 44 Construction and base of CMC

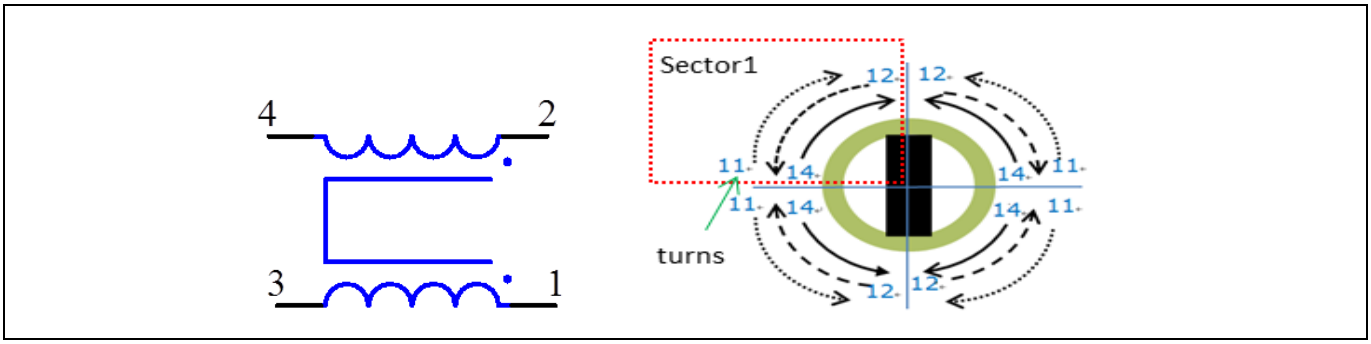


Figure 45 Winding rule for CMC

11.1 Core specifications

Material: Mn-Zn

Outline: 14 mm (OD) × 9 mm (ID) × 5 mm (H)

AL: 4420 ± 30 percent nH/N2

11.2 Winding configuration

Complete 74 turns of each winding with 0.32 Φ X1 wire, separated into two sections. Start winding 14 turns from 9 to 12 o'clock, 12 turns from 12 to 9 o'clock and, finally, 11 turns from 9 to 12 o'clock in section 1. Follow this same rule for the other sections.

11.3 Inductance of each winding

21.7 mH ± 30 percent at 10 kHz/0.1 V

12 mH ± 30 percent at 200 kHz/0.1 V

12 Test results

12.1 Efficiency results

The table below shows the measured efficiency results of the final reference board meeting the EU CoC Version 6 requirements.

Table 6 Efficiency test results from the reference board

Input voltage	Rated power	P_{in}	V_{out}	I_{out}	P_{out}	Efficiency	Average η
115 V AC	25%	12.93	19.32	0.592	11.45	88.53%	88.53%
	50%	25.72	19.25	1.186	22.84	88.82%	
	75%	38.43	19.2	1.773	34.05	88.62%	
	100%	51.68	19.13	2.375	45.44	87.95%	
Input voltage	**Rated power**	**P_{in}**	**V_{out}**	**I_{out}**	**P_{out}**	**Efficiency**	**Average η**
230 V AC	25%	12.97	19.32	0.592	11.45	88.23%	88.79%
	50%	25.71	19.25	1.185	22.83	88.82%	
	75%	38.25	19.19	1.771	34.00	88.91%	
	100%	50.96	19.13	2.375	45.44	89.19%	

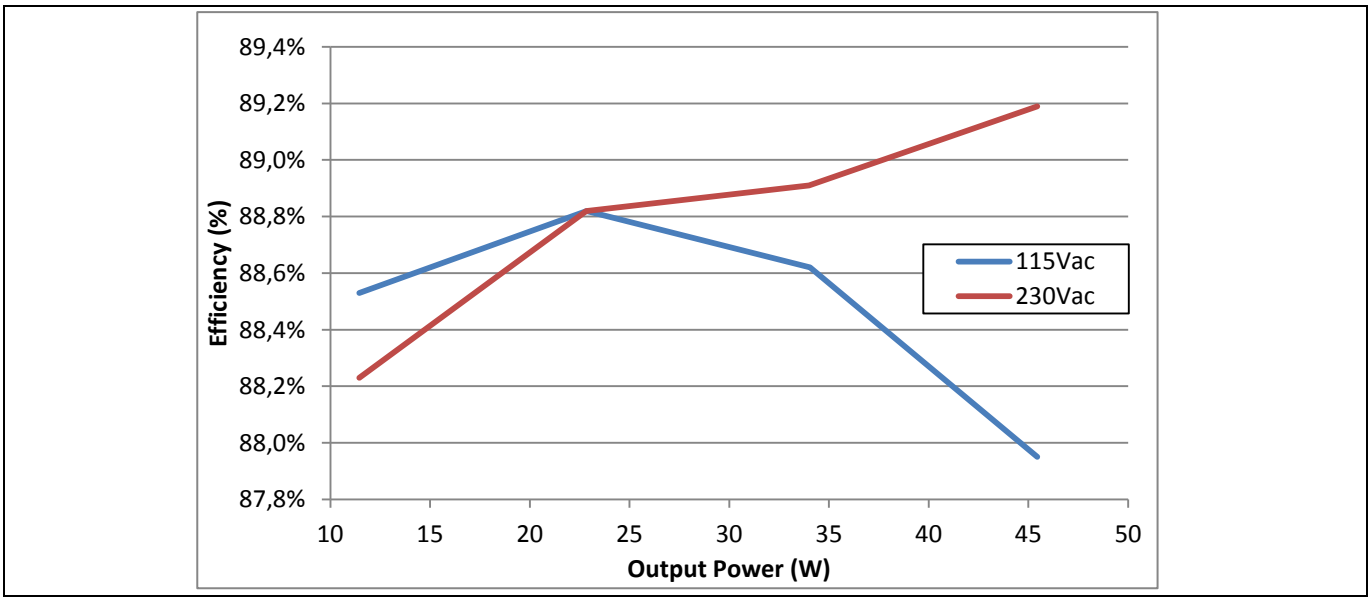
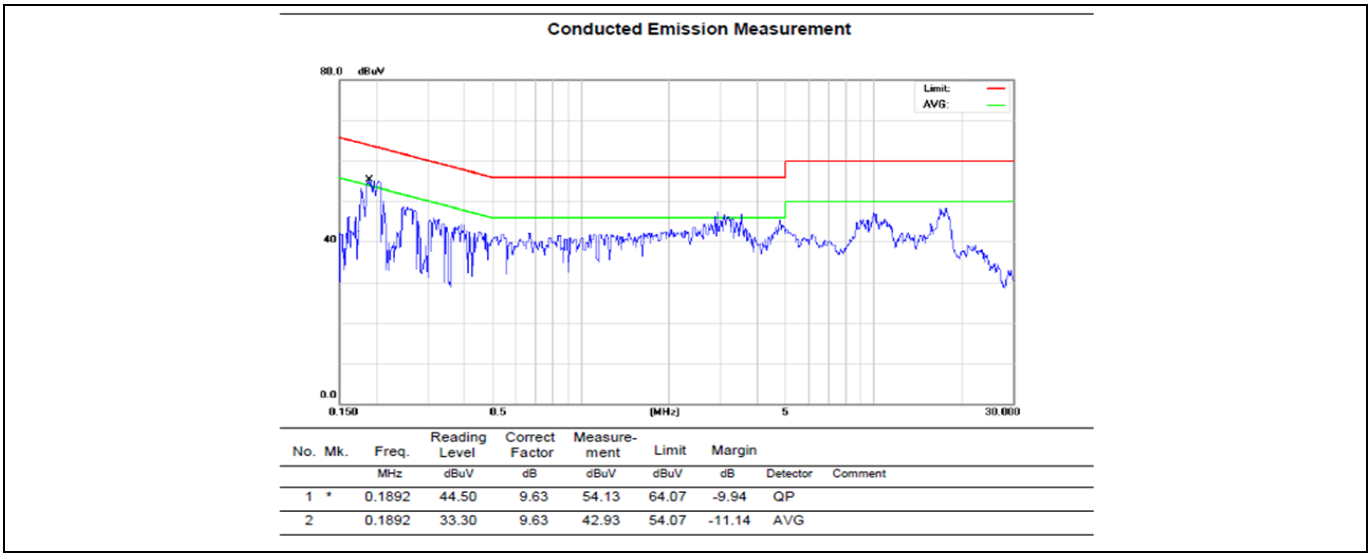


Figure 46 Efficiency test results from the reference board

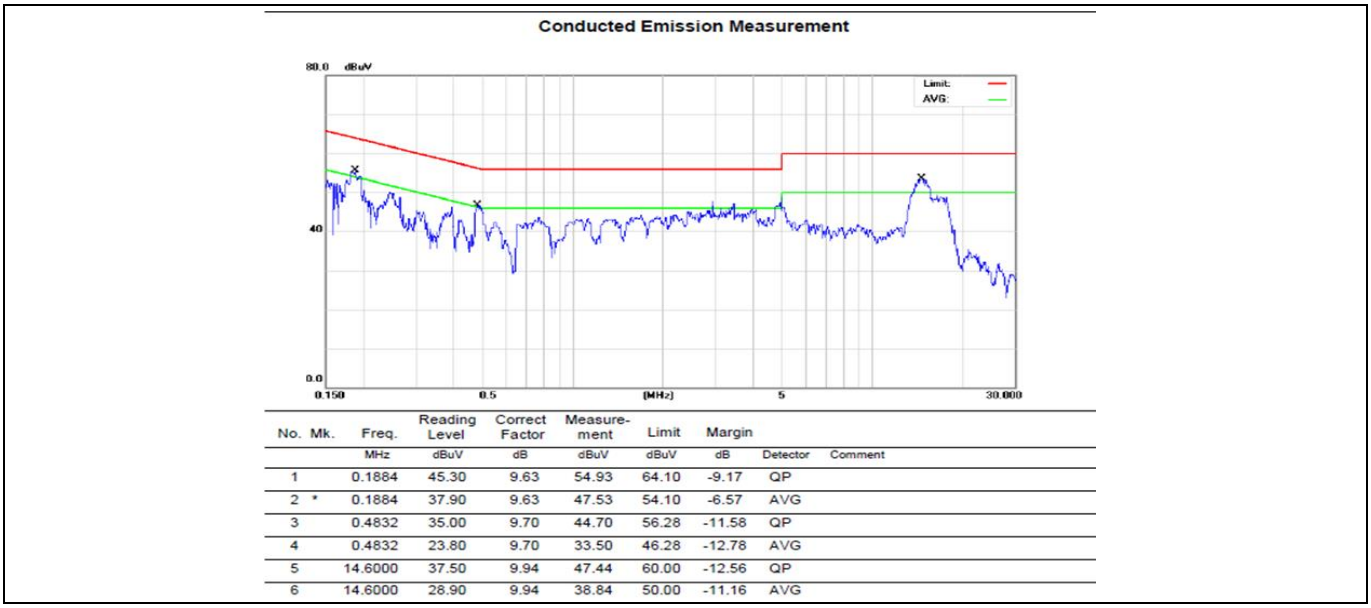
12.2 Conducted EMI results

Below are the conducted emissions test results. The results are tested to the EN 55022 class B limit. With the changes mentioned in the previous sections, the reference design is capable of meeting the requirements with the QP measurement 9.94 dB below the QP limit line.



No.	Mk.	Freq.	Reading Level	Correct Factor	Measure-ment	Limit	Margin		
		MHz	dBuV	dB	dBuV	dBuV	dB	Detector	Comment
1	*	0.1892	44.50	9.63	54.13	64.07	-9.94	QP	
2		0.1892	33.30	9.63	42.93	54.07	-11.14	AVG	

Figure 47 Conducted emissions results from the reference board at 115 V AC (line)

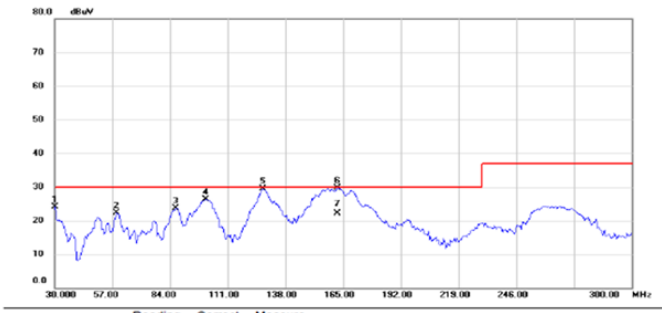


No.	Mk.	Freq.	Reading Level	Correct Factor	Measure-ment	Limit	Margin		
		MHz	dBuV	dB	dBuV	dBuV	dB	Detector	Comment
1		0.1884	45.30	9.63	54.93	64.10	-9.17	QP	
2	*	0.1884	37.90	9.63	47.53	54.10	-6.57	AVG	
3		0.4832	35.00	9.70	44.70	56.28	-11.58	QP	
4		0.4832	23.80	9.70	33.50	46.28	-12.78	AVG	
5		14.6000	37.50	9.94	47.44	60.00	-12.56	QP	
6		14.6000	28.90	9.94	38.84	50.00	-11.16	AVG	

Figure 48 Conducted emissions results from the reference board at 230 V AC (line)

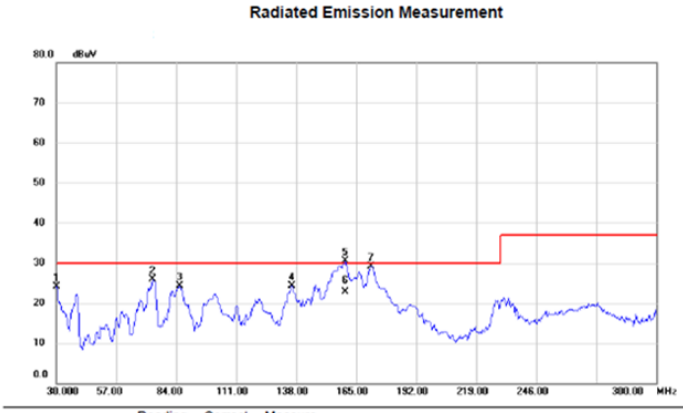
12.3 Radiated EMI results

Below are the radiated emissions test results done in at an external EMI chamber. The results are tested to the EN 55022 class B limit. With the changes mentioned in the previous sections, the reference design is capable of meeting the requirements with the QP measurement 7.32 dB below the QP limit line.



No.	Mk.	Freq.	Reading Level	Correct Factor	Measure-ment	Limit	Margin		
		MHz	dBuV	dB	dBuV	dBuV	dB	Detector	Comment
1		30.0000	56.02	-31.87	24.15	30.00	-5.85	peak	
2		59.1600	46.52	-24.15	22.37	30.00	-7.63	peak	
3		86.7000	51.31	-27.70	23.61	30.00	-6.39	peak	
4		100.7400	51.58	-25.25	26.33	30.00	-3.67	peak	
5		127.2000	49.32	-19.89	29.43	30.00	-0.57	peak	
6	*	162.3000	45.70	-15.95	29.75	30.00	-0.25	peak	
7		162.3000	38.04	-15.95	22.09	30.00	-7.91	QP	

Figure 49 Radiated emissions results from the reference board at 115 V AC (vertical)



No.	Mk.	Freq.	Reading Level	Correct Factor	Measure-ment	Limit	Margin		
		MHz	dBuV	dB	dBuV	dBuV	dB	Detector	Comment
1		30.0000	56.03	-31.87	24.16	30.00	-5.84	peak	
2		73.2000	51.35	-25.54	25.81	30.00	-4.19	peak	
3		85.6200	52.10	-27.87	24.23	30.00	-5.77	peak	
4		135.8400	40.91	-16.60	24.31	30.00	-5.69	peak	
5	*	160.1400	45.70	-15.19	30.51	30.00	0.51	peak	
6		160.1400	37.87	-15.19	22.68	30.00	-7.32	QP	
7		171.4800	48.45	-19.32	29.13	30.00	-0.87	peak	

Figure 50 Radiated emissions results from the reference board at 230 V AC (vertical)

13 Conclusion

Chargers and adapters are cost-sensitive products. One strategy to reduce BOM costs is to reduce the package cost by switching from a FullPAK package to an SOT-223 package. This also gives the secondary benefit of reducing manufacturing costs by switching to automated assembly due to the SMD package. The 700 V CoolMOS™ P7 in SOT-223 offers the benefit of extremely low switching losses and a lower effective $R_{DS(on)}$ at high junction temperatures. These improved parameters help the 700 V CoolMOS™ P7 in SOT-223 meet the requirements of system efficiency and component temperature even with a higher $R_{g,on}$. The implementation of an internal ESD protection mitigates damage from ESD during production and improves the reliability of products. In this application note for the 45 W notebook adapter reference design board, some information about conducted and radiated emissions, including root causes and solutions, has been introduced. As this 45 W adapter reference design shows, the 700 V CoolMOS™ P7 in SOT-223 is a perfect fit for charger and adapter applications.

14 References

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[5] Michel Mardiguian, “Controlling Radiated Emission by Design”, Springer

Revision history

Major changes since the last revision

Page or reference	Description of change

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