

1200 V CoolSiC™ Schottky Diode Generation 5

Authors:

Omar Harmon (IFAT IPC APS AE)
Dr. Vladimir Scarpa (IFAT IPC APS AE)

Application Note

About this document

Scope and purpose

This document introduces the newest 5th Generation 1200 V CoolSiC™ Schottky Diodes (Generation 5) which presents a series of improvements with respect to the previous Infineon SiC Diodes. Based on the exclusive thin-wafer technology, the new Generation 5 offers the best ratio between conduction and switching losses, resulting in higher system efficiency.

In addition, a merged pn-junction has been added to the device structure in order to reduce the diode losses under high current conditions, thus enhancing the surge current capability of the devices.

The following sections describe the main features brought by this technology and its main benefits, from the wafer up to application levels.

Intended audience

This Application Note is of interest for design engineers who intend to reduce the system cost, improve the system efficiency and increase the power density.

Table of contents

1	The thin wafer technology	2
2	The merged pin-Schottky Diode	3
3	Improvements of CoolSiC™ Generation 5.....	4
3.1	Reduction of forward voltage	4
3.2	Improved thermal performance	5
3.3	Surge capability.....	5
4	Application of 1200 V SiC Schottky Diodes	7
4.1	Application of SiC in photovoltaic inverters.....	7
5	Portfolio	9
6	Summary.....	10
7	References	11

The thin wafer technology

1 The thin wafer technology

Generation 5 SiC Diodes make use of Infineon's exclusive thin-wafer technology. Here, the thickness of substrate, the dominant factor in the overall diode resistance, is reduced to around 1/3 of the former 1200 V SiC Diode technologies. As it is going to be explained in the following sections, this has a direct impact on the forward voltage, as well as on thermal characteristics and surge current capability.

A schematic representation of a SiC Schottky Diode is shown Figure 1. Besides the bond metal and the Schottky contact, two other layers are represented in Figure 1: The drift layer, which provides the blocking capability during reverse voltage application, the SiC substrate which provides mechanical stability and the backside metal. The merged pn junction, also present in Generation 5, is not represented in Figure 1 for simplicity. It will be discussed in details in Section 2 of this document.

In Figure 1, the current flow direction during forward biased operation is from top to bottom. The SiC substrate contributes to the electrical resistance, represented as R_{bulk} , which is the main contributor to the diode's differential resistance R_{diff} . Reducing the substrate's thickness reduces the diode's overall resistance thus lowering the forward voltage when the diode is conducting.

Moreover, as it is deeply analyzed in section 3.1, Generation 5 also presents a lower dependency of the forward voltage on temperature.

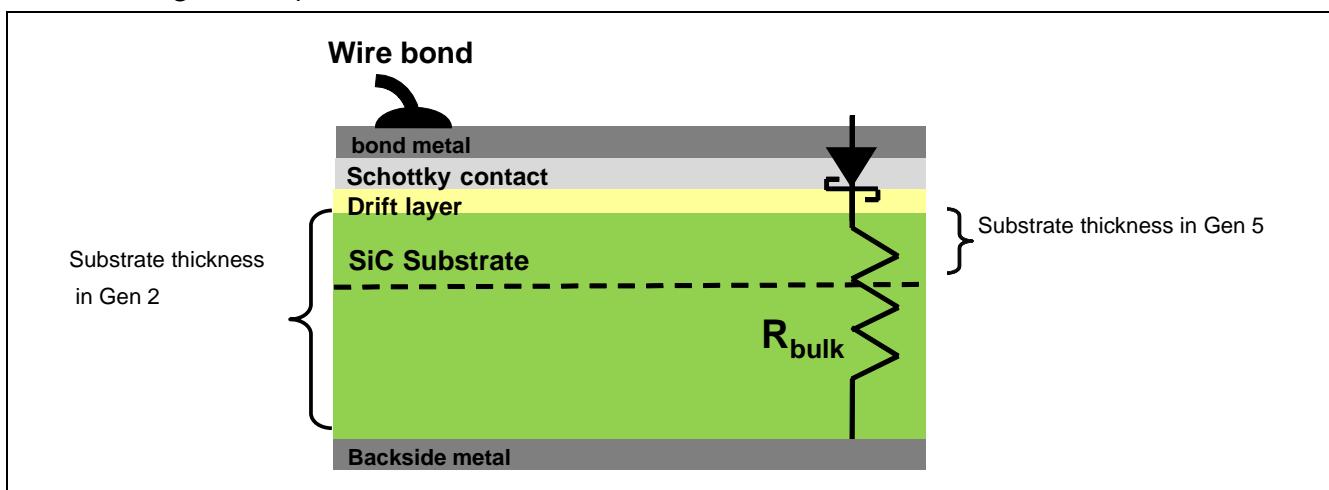


Figure 1 Schematic representation of a SiC Schottky Diode indicating thick and thin wafers. Merged pn junction is not represented for simplicity.

The merged pin-Schottky Diode

2 The merged pin-Schottky Diode

As mentioned in the former section, the Generation 5 structure also contains a merged pn-Schottky (MPS) diode structure. The same concept is already present in 600 V SiC diodes since its 2nd Generation [6]. However this is the first time MPS is implemented in 1200 V SiC diodes. As displayed in Figure 2, the epitaxial layer of the diode additionally contains p-doped regions labeled as p+. At low current densities, the current flows through the Schottky regions, while surge current flows through the p-regions. Both paths for the current flow are depicted in Figure 2.

For surge currents, for example the in-rush current to a capacitor during the turn-on of the system, the p-regions become active and gives additional total current carrying capability. Additionally, this also leads to a much lower overall voltage drop than in a common Schottky diode.

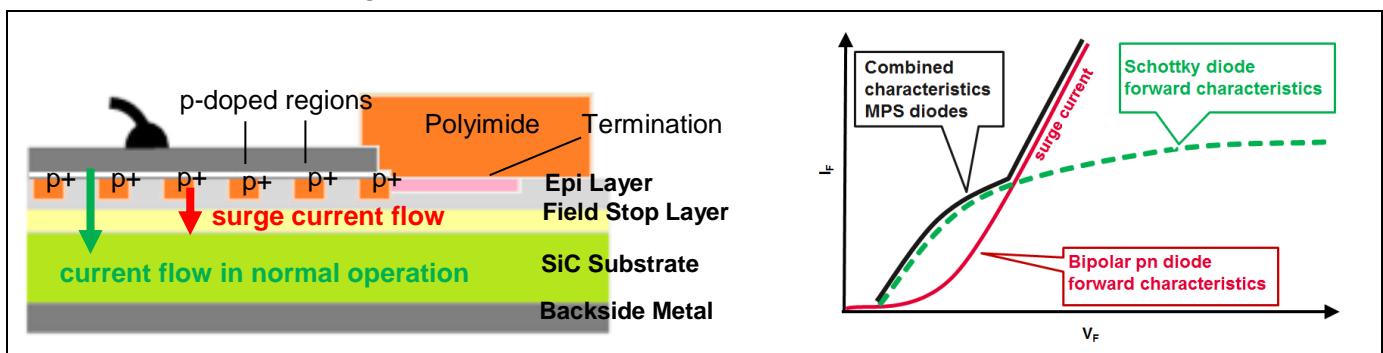


Figure 2 SiC diode with MPS structure during normal and surge current operation

The right side of Figure 2 also presents the V_F - I_F characteristics of a Schottky and MPS diode during nominal current and surge current. The combined V_F - I_F characteristic of the Schottky diode plus MPS results in the lowest power losses, even at current levels well above the diode rated current. As a result, SiC diodes with MPS can withstand a much higher surge current than conventional SiC-Schottky diodes. A quantified evaluation of this benefit is presented in Section 3.3.

Improvements of CoolSiC™ Generation 5

3 Improvements of CoolSiC™ Generation 5

This section summarizes the features introduced by the thin-wafer technology featuring MPS and quantifies their benefits on the new Generation 5 SiC-diode devices.

3.1 Reduction of forward voltage

For a system to run in high efficiency, system power losses need to be minimized. Due to the absence of reverse recovery charge, the conduction losses P_{cond} usually are the main source of losses in a SiC Schottky diode. This contribution can be mathematically expressed to be:

$$P_{cond} = V_F \cdot I_F, \quad (1)$$

where I_F is the current through the diode. Therefore, in order to lower conduction losses, the forward voltage V_F in conduction mode has to be reduced.

It is also important to understand that V_F has two components: The threshold voltage V_{th} needed for the diode to start conducting current and a differential resistance R_{diff} , that represents the overall diode resistance. The diode forward voltage can be approximated by:

$$V_F = V_{th} + (I_F \cdot R_{diff}) \quad (2)$$

Therefore, by reducing R_{diff} , the diode's conduction losses are lowered.

Figure 3 depicts the V_F characteristic of a Generation 5 chip rated for 5 A, compared to a chip with the same current rating from former Generation 2 from Infineon. At nominal current, the forward voltage of the Generation 5 chip is measured to be 1.37 V in accordance to the nominal datasheet value $V_F=1.40$ V at $T_j=25^\circ\text{C}$.

For Generation 2, 1.74 V are measured, 21% higher than Generation 5. At $T_j=175^\circ\text{C}$, the difference between Generation 2 and Generation 5 increases up to 38%. Generation 5 achieves 1.85 V compared to 2.99 V in Generation 2.

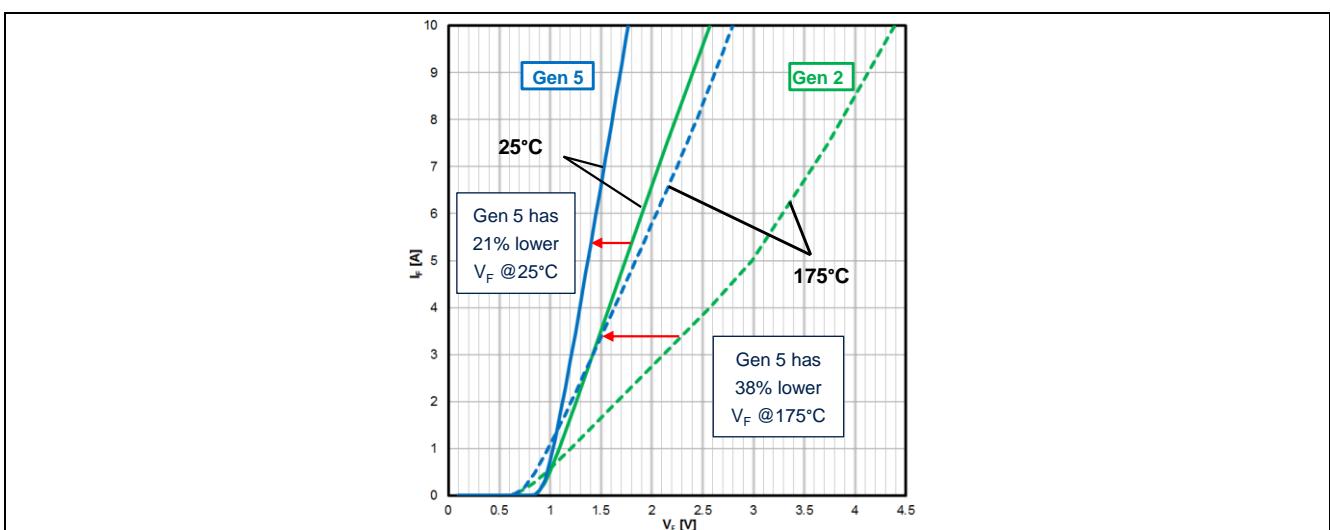


Figure 3 Comparison of forward voltage between Gen 5 and Gen 2 at 25°C and 175°C junction temperature

Improvements of CoolSiC™ Generation 5

3.2 Improved thermal performance

Besides electrical behavior, the thin-wafer technology also improves the thermal performance of the new 1200 V Generation 5 diodes. A thinner substrate layer offers a shorter thermal path for the heat generated inside the Schottky junction of the diode. The heat spread from the junction is enhanced, thus reducing the thermal resistance between junction and the package lead-frame or case. This effect is schematically represented in Figure 4.

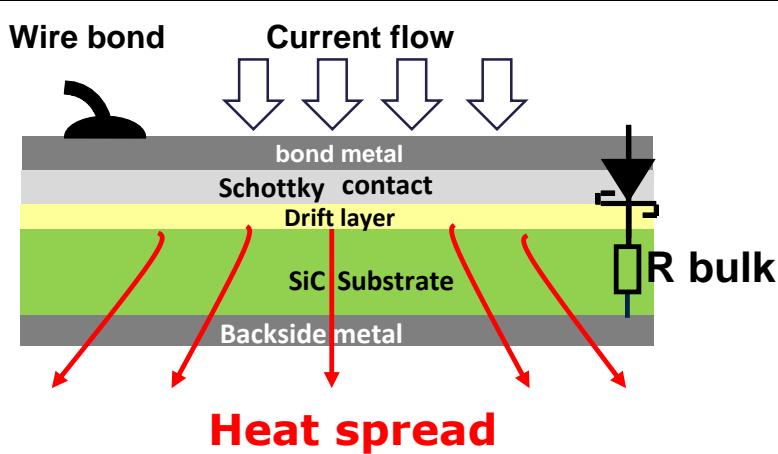


Figure 4 Schematic representation of a thin-wafer SiC Schottky diode

The thin substrate features a reduced thermal capacitance and this will help the thermal flux to propagate from the chip to the backside metal with no noticeable barrier. In addition, the thin substrate enhances the lateral flux of the heat. This is represented in Figure 4 by the arrows coming from the Schottky contact in direction to the backside metal. As a consequence, the thermal resistance between junction and case is reduced up to 10% for a chip with the same current rating. Since the maximum power that can be handled by the diode is given by:

$$P_{\max} = \frac{T_{j,max} - T_c}{R_{th,JC}} \quad (3)$$

A reduction in the $R_{th,JC}$ thus corresponds to an equivalent increase of power dissipation for the same case temperature.

3.3 Surge capability

As seen in Section 2 of this document, 1200 V Generation 5 has an integrated merged pn-Schottky diode structure which reduces the forward voltage of the diode at higher current conditions. Combined with lower differential resistance achieved by the wafer thinning, this results in a massive increase of the surge current capability in Generation 5 devices.

Referring to Figure 2, the chart on the right side shows how the forward voltage will be reduced by the MPS under high current lowering the power losses. This enhances the diode surge current capability, represented in datasheets by the parameter $I_{F,SM}$. The parameter is given for half a sinusoidal current waveform of 10 ms, refers to the peak of the sinusoidal and is given in ampere.

Improvements of CoolSiC™ Generation 5

The chart in Figure 5 gives the non-repetitive surge forward current $I_{F,SM}$ at $T_j=25^\circ\text{C}$ for 1200 V Generation 2, Generation 5 and two further alternatives, all rated for 10 A nominal current. It is possible to see the improvement of the surge current capability in Gen 5, which is almost 3 times higher than the Generation 2 diode counterpart, and even 40% higher than the best competitor part considered.

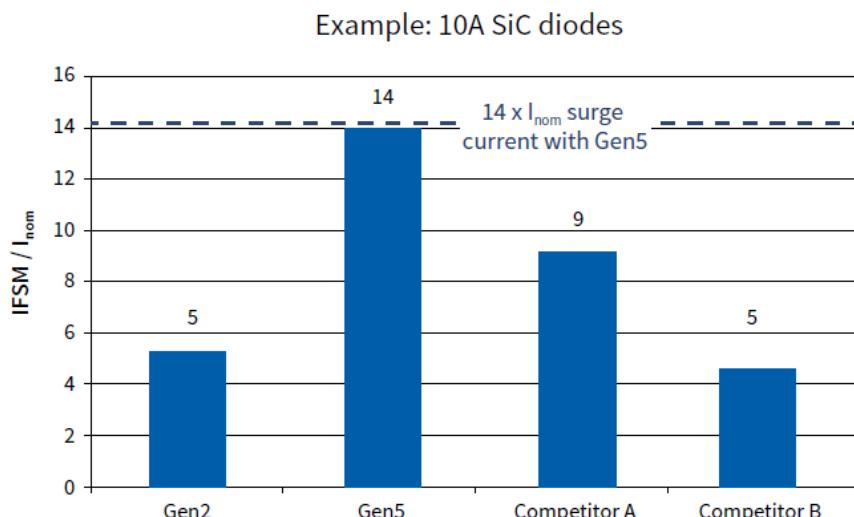


Figure 5 Comparison between Generation 5, Generation 2 and a competitor 1200 V SiC diode, all rated for 10 A

Application of 1200 V SiC Schottky Diodes

4 Application of 1200 V SiC Schottky Diodes

The absence of reverse recovery charge makes SiC Schottky Diodes a good option when high efficiency and low EMI are required. In addition, SiC Schottky Diodes enable higher frequency operation and as a consequence, size reduction of the magnetic components in use. SiC then brings higher efficiency and increased power density to these systems.

Table 1 summarizes the target applications of 1200 V SiC Schottky Diodes operating at a typical switching frequency range of 20 to 50 kHz. The next section will show an example of how Generation 5 increases system efficiency in a photovoltaic inverter even further.

Table 1 1200 V SiC Schottky Diode target applications

Target application	Stage
Solar inverters	Front-end booster
UPS, 3-Phase SMPS	PFC
Motor drives	Inverter

4.1 Application of SiC in photovoltaic inverters

The reduction in losses brought by Generation 5 can be calculated for a front-end booster stage for a photovoltaic inverter, as the one depicted in Figure 6. Main electrical parameters of the inverter are summarized in the table aside.

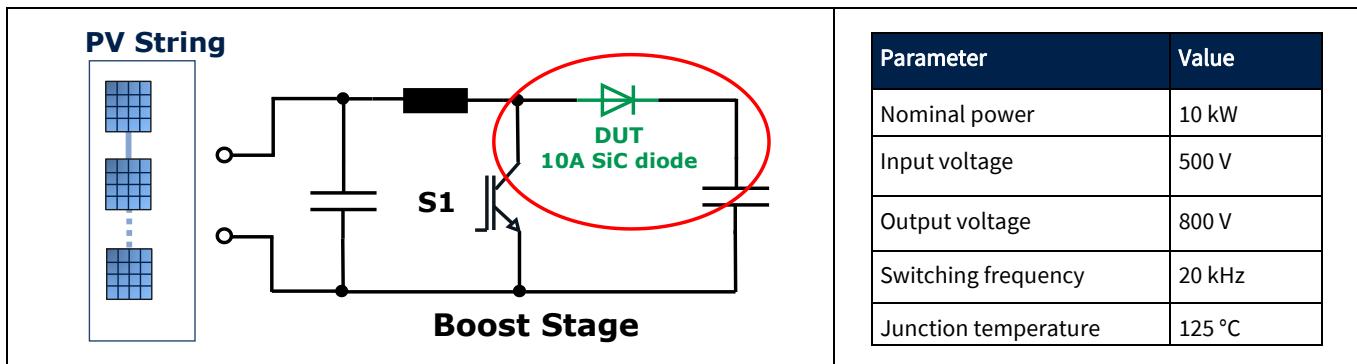


Figure 6 Front-end Booster stage of a photovoltaic inverter

The losses of the boost diode have been calculated, taking devices from different Infineon generations into consideration, all of them rated with the same nominal current. As predicted by equation (1), the lower forward voltage of Generation 5 results in lower conduction losses.

Application of 1200 V SiC Schottky Diodes

Figure 7 shows that the difference in losses between Generation 2 and Generation 5 parts increases with the load, both in Watt and in percentage from the load. For load conditions below 10% of the nominal power, the smaller output capacitance of Generation 2 results in a slightly better efficiency. With the increase of the load, the lower forward voltage of Generation 5 is responsible for its better performance. At nominal load, the difference is in favor of Generation 5 and results in more than 12 W or 30% difference at nominal power. In terms of system efficiency, this results in 0.12% higher efficiency at nominal load.

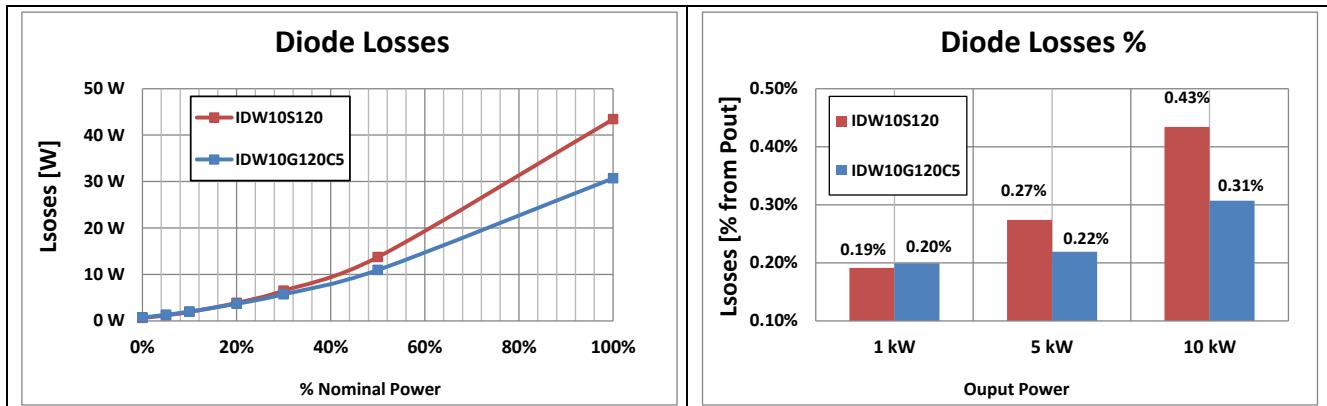


Figure 7 Calculated losses of 10 A Generation 5 and Generation 2 diodes, and the percentage of diode losses for three different load conditions of 1 kW, 5 kW and 10 kW

Portfolio

5 Portfolio

Generation 5 product naming includes the package type, the diode's rated current in ampere and the voltage class in Volt, divided by 10. Letter "B" at the end indicates two chips inside, in common cathode configuration. Table 2 presents the portfolio of the 1200V CoolSiC™ Generation 5 diodes.

Table 2 1200 V CoolSiC™ Generation 5 portfolio

Continuous Forward Current, I_F [A]	TP-252 (DPAK real 2-leg)	TO-220 (real 2-leg)	TO-247-3
2	IDM02G120C5	IDH02G120C5	
5	IDM05G120C5	IDH05G120C5	
8	IDM08G120C5	IDH08G120C5	
10	IDM10G120C5	IDH10G120C5	IDW10G120C5B ¹⁾
15-16		IDH16G120C5	IDW15G120C5B ¹⁾
20		IDH20G120C5	IDW20G120C5B ¹⁾
30			IDW30G120C5B ¹⁾
40			IDW40G120C5B ¹⁾

¹⁾B = dual-configuration with common cathode

Summary

6 Summary

1200 V CoolSiC™ SiC Schottky Diode Generation 5 introduces many enhancements compared to former Infineon SiC-Diode generations, among them the thin-wafer technology and the merged pn structure. On the application level, these translate into less overall losses due to lowest forward voltage in the market, as well as high reliability due to higher surge current capability.

The surge current capability of Generation 5 has been more than doubled with respect to former Generation 2, for the same current class. Finally, the efficiency increase can be quantified in the example of a photovoltaic inverter, where the use of Generation 5 1200 V diode resulted in up to 30% less diode losses leading to 0.1% system efficiency improvement.

References

7 References

- [1] Rupp, R., Gerlach R., Kirchner U., Schlägl A., Ronny Kern R., "Performance of a 650V SiC diode with reduced chip thickness", proceedings of ICSCRM, 2011.
- [2] Fichtner, S., Lutz, J., Basler, T., Rupp, R., Gerlach R. (2014). "Electro – Thermal Simulations and Experimental Results on the Surge Current Capability of 1200 V SiC MPS Diodes" proceedings of CIPS, 2014.
- [3] Scarpa, V., Kirchner, U., Gerlach, R., Kern, R. (2012). „New SiC Thin-Wafer Technology Paving the Way of Schottky Diodes with Improved Performance and Reliability,” PCIM Europe 2012.
- [4] Harmon, O. "650V Rapid Diode for Industrial Applications", Infineon Technologies Application Note 2013.
- [5] CoolSiC™ diodes datasheets. Available in internet: www.infineon.com/sic.
- [6] Bjoerk, F. et al, "2nd Generation 600V SiC Schottky Diodes Use Merged pn/Schottky Structure for Surge Overload Protection", APEC 2006, proceedings of.

Revision history

Major changes since the last revision

Page or reference	Description of change
--	First release

Trademarks of Infineon Technologies AG

AURIX™, C166™, CanPAK™, CIPOS™, CoolGaN™, CoolMOS™, CoolSET™, CoolSiC™, CORECONTROL™, CROSSAVE™, DAVE™, DI-POL™, DrBlade™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, Infineon™, ISOFACE™, IsoPACK™, i-Wafer™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OmniTune™, OPTIGA™, OptiMOS™, ORIGA™, POWERCODE™, PRIMARION™, PrimePACK™, PrimeSTACK™, PROFET™, PRO-SIL™, RASIC™, REAL3™, ReverSave™, SatRIC™, SIEGET™, SIPMOS™, SmartLEWIS™, SOLID FLASH™, SPOCT™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™.

Trademarks updated August 2015

Other Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

www.infineon.com

Edition 2014-07-10

Published by

Infineon Technologies AG
81726 Munich, Germany

© 2016 Infineon Technologies AG.
All Rights Reserved.

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Legal Disclaimer

THE INFORMATION GIVEN IN THIS APPLICATION NOTE (INCLUDING BUT NOT LIMITED TO CONTENTS OF REFERENCED WEBSITES) IS GIVEN AS A HINT FOR THE IMPLEMENTATION OF THE INFINEON TECHNOLOGIES COMPONENT ONLY AND SHALL NOT BE REGARDED AS ANY DESCRIPTION OR WARRANTY OF A CERTAIN FUNCTIONALITY, CONDITION OR QUALITY OF THE INFINEON TECHNOLOGIES COMPONENT. THE RECIPIENT OF THIS APPLICATION NOTE MUST VERIFY ANY FUNCTION DESCRIBED HEREIN IN THE REAL APPLICATION. INFINEON TECHNOLOGIES HEREBY DISCLAIMS ANY AND ALL WARRANTIES AND LIABILITIES OF ANY KIND (INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS OF ANY THIRD PARTY) WITH RESPECT TO ANY AND ALL INFORMATION GIVEN IN THIS APPLICATION NOTE.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office. Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.