



**SAMSUNG**  
**ARTIK**<sup>™</sup> Modules

**5**

**ARTIK 530/530s Module Datasheet**

MODULE OVERVIEW

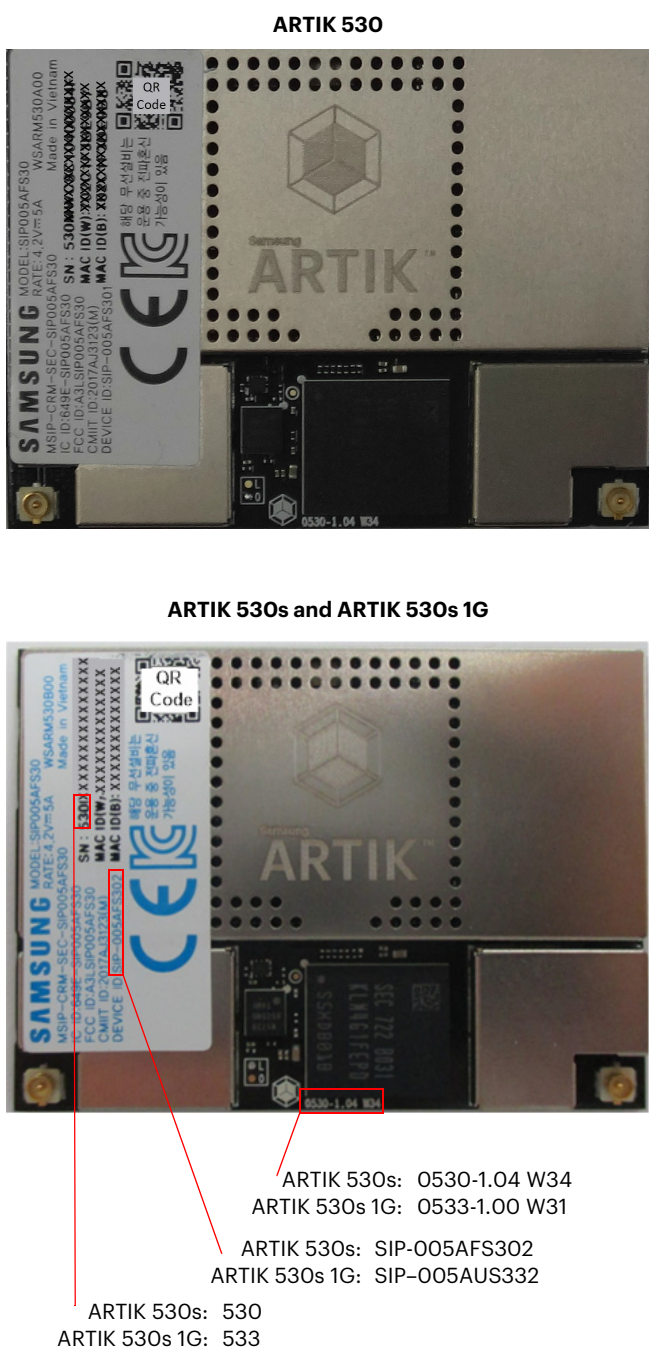


Figure 1. ARTIK™ 530/530s Module Top View

The Samsung ARTIK™ 530/530s Module is a highly-integrated System-in-Module that combines a quad-core ARM® Cortex®-A9 processor packaged with 512MB or 1GB DRAM and Flash memory, a Security Subsystem, and a wide range of wireless communication options—such as 802.11a/b/g/n for Wi-Fi®, Bluetooth® 4.2 (BLE+Classic), and 802.15.4 for Zigbee—all into one 49×36mm footprint. The many standard digital control interfaces support external sensors and higher performance peripherals to expand the module’s capabilities. With the combination of 802.11, Bluetooth® and 802.15.4, the ARTIK 530/530s Module is the perfect choice for home automation and home hub devices, while also supporting a rich UI/UX capability for camera and display requirements. The inclusion of a hardware-based Secure Element provides end-to-end security.

| Processor                     |                                                                                                     |
|-------------------------------|-----------------------------------------------------------------------------------------------------|
| CPU                           | Quad-core ARM® Cortex®-A9@1.2GHz                                                                    |
| GPU                           | 3D graphics accelerator                                                                             |
| Media                         |                                                                                                     |
| Camera I/F                    | 4-lane MIPI CSI up to 5M (1920x1080@30fps)                                                          |
| Display                       | 4-lane MIPI DSI and HDMI1.4a (1920x1080p@60fps) or LVDS (1280x720p@60fps)                           |
| Audio                         | Two I <sup>2</sup> S audio interfaces                                                               |
| Memory                        |                                                                                                     |
| DRAM                          | 512MB or 1GB DDR3 @ 800MHz                                                                          |
| FLASH                         | 4GB eMMC v4.5                                                                                       |
| Security                      |                                                                                                     |
| Secure Element                | Secure point to point authentication and data transfer                                              |
| Trusted Execution Environment | Trustware                                                                                           |
| Radio                         |                                                                                                     |
| WLAN                          | IEEE 802.11a/b/g/n, dual-band SISO                                                                  |
| Bluetooth®                    | 4.2 (Classic+BLE)                                                                                   |
| LR_WPAN                       | IEEE 802.15.4                                                                                       |
| Power Management              |                                                                                                     |
| PMIC                          | Provides all power of the ARTIK 530/530s Module using onboard bucks and LDOs                        |
| Interfaces                    |                                                                                                     |
| Ethernet                      | 10/100/1000Base-T MAC (External PHY required)                                                       |
| Analog and Digital I/O        | GPIO, UART, I <sup>2</sup> C, SPI, SDIO, USB Host, USB OTG, HSIC, ADC, PWM, I <sup>2</sup> S, JTAG, |

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## Version History

| Revision | Date              | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|----------|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V1.0     | January 20, 2017  | First release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| V1.01    | February 07, 2017 | Updated Module PAD's section. Updated look and feel.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| V1.02    | April 12, 2017    | Updated default behavior of GPIO pins to latest software release.<br>Updated Booting Sequence section. 802.15.4 RF Specifications section. Updated Tables 1–36.<br>Updated SD/MMC AC Electrical Characteristics section. Updated Recommended Operating Conditions section. Updated ESD section. Updated Power management section.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| V1.03    | November 20, 2017 | In <u>Table 1</u> , definition of PU/PD and I/O columns for ballout and signal-description tables more explicitly defined.<br>Characteristics for LDO3 (VCC3P3_SYS) removed, as using the output to drive external ICs is highly discouraged. Descriptions of other LDOs was removed, as they are not available externally.<br><br>In <u>Functional Interfaces</u> , each subsection describing an interface that has alternate functions clarifies which are selected by hardware at power-on reset. Cross references added to the appropriate tables in <u>GPIO Alternate Functions</u> .<br><br>Changed format of default functions in tables of <u>GPIO Alternate Functions</u> to make it easier to see which function number is the default.<br><br><u>Booting Selection</u> section rewritten for clarity.<br><br>Power Sequence section divided into <u>Power Sequence</u> and <u>Power States</u> . Simplified power management state diagram, <u>Figure 5</u> .<br><u>Power/Current Consumption</u> section added. |
| V1.04    | November 30, 2017 | Added ARTIK 530s and ARTIK 530s 1G features in <u>Module Overview</u> , <u>Block Diagram and Module Features</u> , and <u>Security Subsystem</u> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| V1.05    | November 30, 2017 | <u>Ordering Information</u> : Added ordering part numbers for ARTIK 530s 1G and its associated development kit.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| V1.06    | December 20, 2017 | <u>USB HOST/USB OTG</u> : Changed function description of AP_OTG_ID signal.<br><u>802.15.4 for Zigbee</u> : Changed function descriptions for balls PAK12–14 and PAL12–14.<br><u>Mechanical Specifications</u> : Changed ball names in <u>Figure 13</u> and <u>Table 60</u> to correlate with ball organization shown in <u>Figure 3</u> . Note that the changes address a labeling consistency issue only; no electrical or layout changes are required.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| V1.07    | February 2, 2018  | <u>CE</u> : Radio Equipment Directive (RED) certification update.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| V1.08    | April 5, 2018     | <u>I<sup>2</sup>C</u> : Removed support for slave mode.<br><u>Table 3</u> , <u>Table 26</u> : Marked pad PAL15 for internal use only.<br><u>Table 30</u> : Removed pad PAL15 from GPIO function table because it is reserved for internal use.<br>Added <u>Temperature Thresholds for Operating Frequency Throttling</u> under new section <u>Thermal and Environmental Specifications</u> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

## BLOCK DIAGRAM AND MODULE FEATURES

*Figure 2* shows the functional block diagram of the ARTIK 530/530s Module. It consists of a quad-core ARM® Cortex®-A9 application processor with 512MB or 1GB of DDR3 and 4GB eMMC Flash, PMIC power management, Security Subsystem, 802.11 for Wi-Fi®, Bluetooth®, 802.15.4 for Zigbee, and RF connectors.

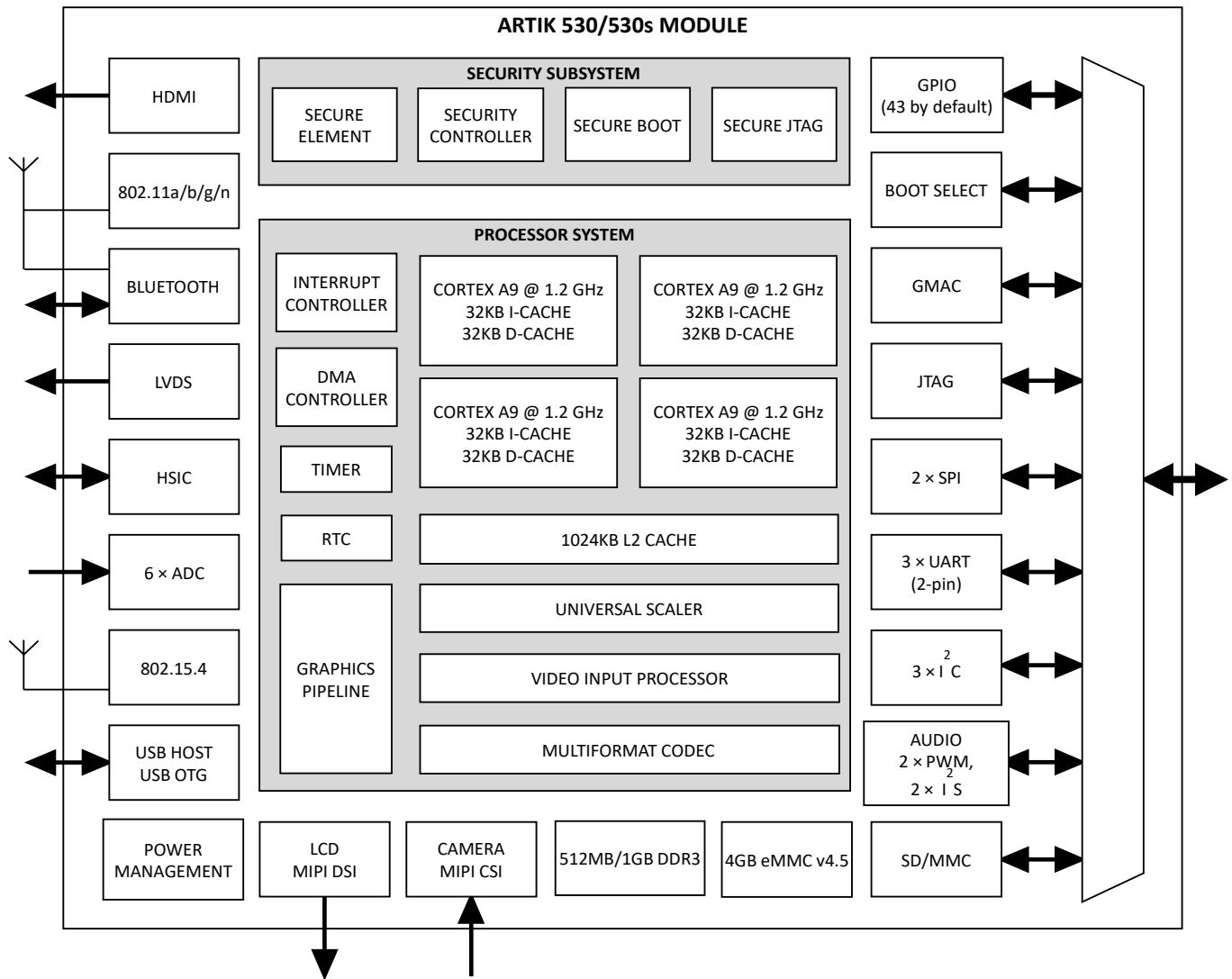


Figure 2. ARTIK 530/530s Module Functional Block Diagram

## ARTIK 530/530s Module Features

The following subsections describe the functions of the various ARTIK 530/530s Module blocks depicted in [Figure 2](#).

### ADC

The ADC interface controls one 28nm low-power CMOS 1.8V 12-bit ADC. The key features of the ADC sub-system are

- Up to six channels of analog input can be selected
- Conversion of analog input into 12-bit binary code up to 1 Mega Sample Per Second (MSPS)
- 1.0mW power consumption when running 1MSPS
- Input frequency up to 100kHz

### GPIO

The ARTIK 530/530s Module provides a GPIO system with up to 107 GPIOs multiplexed with other I/O interface lines, as shown in [Figure 2](#) to support a wide variety of use-cases. The key features of the GPIO system are as follows:

- Programmable pull-up control
- Both edge detect and level detect functionality
- Support for programmable pull-up resistors
- Support for fast or normal slew operation
- Drive strength can be set from a register:

| Value | Drive Strength *              |
|-------|-------------------------------|
| 0     | 2.6mA approximately (default) |
| 1     | 5.2mA approximately           |
| 2     | 10.4mA approximately          |
| 3     | 15.6mA approximately          |

\*. Assumes the reference I/O voltage is 3.3V.  
All drive-strength values are approximate.

- Support for interrupt generation that can be triggered on one of the following:
  - Rising edge
  - Falling edge
  - High level detection
  - Low level detection
- The I/O data is clocked up to 50MHz

## I<sup>2</sup>S

The ARTIK 530/530s Module provides two 5-line Inter-IC Sound (I<sup>2</sup>S) channels. I<sup>2</sup>S is one of the most popular digital audio interfaces. The I<sup>2</sup>S bus handles audio data and other signals, such as subcoding and control. It is possible to transmit data between two I<sup>2</sup>S buses. The key features of the I<sup>2</sup>S sub-system are

- One-port stereo (1 channel) I<sup>2</sup>S-bus for audio with DMA based operation
- Serial data transfer of 16/24 bits per channel in Master and Slave mode
- A variety of interface modes:
  - I<sup>2</sup>S, Left justified, Right justified, DSP mode

## PWM

The ARTIK 530/530s Module provides two pulse width modulation (PWM) instances with the following key features:

- Two individual PWM channels with independent duty control and polarity
- Two 32-bit PWM timers, one per channel
- Support for static as well as dynamic setup
- Support for auto-reload and one shot pulse mode
- Dead zone generator
- Level interrupt generation

## SPI

The ARTIK 530/530s Module provides two Serial Peripheral Interface (SPI) ports that transfer serial data. SPI support includes 8-bit/16-bit shift registers to transmit and receive data. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The SPI implementation adheres to the protocols described by Texas Instruments Synchronous Serial Interface, National Semiconductor's Microwire, and Motorola's Serial Peripheral Interface. The key features of the SPI sub-system are

- Support for full-duplex
- 8-bit/16-bit shift register for Tx and Rx
- Compliant with the SPI protocol described by Texas Instruments, National Semiconductor and Motorola
- Support for independent 16-bit wide transmit and receive FIFOs 8 locations deep
- Support for master mode and slave mode
- Support for receive-without-transmit operation
- Max operating frequency :
  - Master Mode : Supports Tx up to 50MHz, Rx up to 20MHz
  - Slave Mode : Supports Tx up to 8MHz, Rx up to 8MHz

## UART

The ARTIK 530/530s Module provides three 2-pin universal asynchronous receiver transmitters (UARTs). The key features of the UART sub-system are

- Separate 64×8 Tx and 64×8 Rx FIFO memory buffers
- Support for DMA-mode and interrupt-based mode of operation
- All independent channels support IrDA 1.0
- Each UART channel contains:
  - Programmable baud-rates
  - 1 or 2 stop bit insertion
  - 5-bit, 6-bit, 7-bit, or 8-bit data width
  - Parity checking

## I<sup>2</sup>C

The ARTIK 530/530s Module provides three generic I<sup>2</sup>C blocks supporting both 100kb/s and 400kb/s speed modes. The key features of the I<sup>2</sup>C sub-system are

- Support for multi-master mode
- 7-bit addressing mode only
- Serial, 8-bit oriented and bi-directional data transfer
- Up to 100 kb/s in the standard mode
- Up to 400 kb/s in the fast mode
- Support for both interrupt and polling events

## Power Management

The ARTIK 530/530s Module power requirements are managed using a power management integrated circuit (PMIC). This PMIC device has four fully-integrated fixed-frequency current-mode synchronous PWM step-down converters that can achieve peak efficiencies of up to 97%. The regulators operate at a fixed high frequency, minimizing noise in sensitive applications and allowing the use of small form factor components. These four regulators fully satisfy the power and control requirements of the ARTIK 530/530s Module. Dynamic Voltage Scaling (DVS) of the various core voltages is supported using I<sup>2</sup>C control.

## Wi-Fi®

The ARTIK 530/530s Module has a fully integrated WLAN block covering IEEE 802.11 a/b/g/n. The most important hardware features of the module are

- 802.11 a/b/g/n dual-band SISO that is 2.4GHz/5GHz-compliant
- 1T1R 2.4GHz/5GHz band
- Support for 20MHz and 40MHz bandwidth (72.2/150Mbps PHY rate)
- Enhanced 802.11/Bluetooth coexistence control to improve transmission quality in different profiles
- Use of an SDIO interface

## Bluetooth®

The ARTIK 530/530s Module has a fully integrated 4.2 block (BLE+Classic). The most important hardware features of the module are

- Bluetooth 4.2 (BLE+Classic)
- Enhanced 802.11/Bluetooth Coexistence control to improve transmission quality in different profiles

## 802.15.4 for Zigbee

The ARTIK 530/530s Module carries fully-integrated 802.15.4 functionality. The most important hardware features are

- Fully integrated 2.4 GHz, IEEE 802.15.4-compliant transceiver
- Complete system-on-chip using 32-bit ARM® Cortex®-M4 processor
- Flash and RAM memory and peripherals.
- Extremely low power consumption.
- Excellent RF performance.

## PCM

The ARTIK 530/530s Module provides one PCM channel. The PCM interface provides a bi-directional serial interface that can be connected to an external audio codec. The key features of the PCM subsystem are

- Supports both Master and Slave mode external audio codecs
- Supports both short and long frame synchronization
- Supports a variety of data formats with a default format of 13-bit 2's complement, left justified, clock MSB first

## USB OTG

The ARTIK 530/530s Module provides one USB2.0 OTG interface supporting both device and host functionality. The key features of the USB2.0 OTG sub-system are

- Compliant with the USB 2.0 on-the-go specification revision 1.3a and 2.0
- High-speed (480Mbps) mode
- Full-speed (12Mbps) mode
- Low-speed (1.5Mbps) mode (host only)
- Support for session request protocol (SRP) and host negotiation protocol (HNP)
- One control endpoint 0 for control transfer
- Up to 15 device-programmable endpoints:
  - Programmable endpoint type: Bulk, Isochronous, Interrupt
  - Programmable In/Out direction
- 16 host channels

## USB HOST

The ARTIK 530/530s Module provides one USB2.0 controller that is fully compliant with the USB 2.0 Host specifications, and the enhanced host controller Interface (EHCI) specification. The key features of the USB2.0 Host sub-system are

- Detecting the attachment and removal of USB devices
- Collecting status and activity statistics
- Controlling power supply to attached USB devices
- In compliance with the UTMI+ Level 3 revision 1.0
- Controlling the association to either the open host controller interface (OHCI) or the EHCI via a port router
- Root Hub functionality to support upstream/downstream port

## HSIC

The ARTIK 530/530s Module provides one high-speed inter-chip (HSIC) version 1.0 module. The key features of the HSIC sub-system are

- Support for ping and split transactions
- Up to 30MHz operation for a 16-bit interface
- Up to 60MHz operation for a 8-bit interface
- Support for HSIC version 1.0

## MIPI CSI

The ARTIK 530/530s Module provides one 4-lane mobile industry processor interface (MIPI) interface that complies with the MIPI camera serial interface (CSI) standard specification V1.01r06 and D-PHY standard specification v1.0. The key features of the MIPI CSI sub-system are

- 1, 2, 3 or 4 data lanes
- Support for the following image formats:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), 8-bit YUV422, 10-bit YUV422
  - User-defined byte-based data packet
  - Compatible to PPI (Protocol to PHY interface)

## MIPI DSI

The ARTIK 530/530s Module provides one 4-lane MIPI interface that complies with the MIPI DSI standard specification V1.01r11. The key features of the MIPI DSI sub-system are

- Maximum resolution ranges up to WUXGA 1920 × 1200
- Supports 1, 2, 3 or 4 data lanes
- Supports pixel format:
  - 16bpp, 18bpp packed, 18bpp loosely packed (3 byte), 24bpp

- Supported interfaces are
  - Protocol-to-PHY Interface (PPI) up to 1.5Gbps, in MIPI D-PHY
  - RGB Interface for video image input from display controller
  - PMS control interface for PLL to configure byte clock frequency
  - Prescaler to generate escape clock from byte clock

## HDMI

The ARTIK 530/530s Module provides one HDMI v1.4a interface. The key features of the HDMI sub-system are

- Support for v1.4a spec
- Up to 1080p video resolution
- HDMI Link + HDMI PHY
- Support for the following video formats:
  - 480p@59.94/60Hz
  - 576p@50Hz
  - 720p@50/59.94/60Hz
  - 1080p@50/59.94/60Hz (No support for interlaced format)
- Support for 4:4:4 RGB
- Support for up to 8-bits per color

## LVDS

The ARTIK 530/530s Module provides five low voltage differential signaling (LVDS) output channels with one clock channel. The key features of the LVDS channel system are

- Output clock range 30–125MHz
- Support for 630 Mbps per channel
- Up to 393.75MB/s data transport
- Support for power down mode

## Gigabit EMAC

The ARTIK 530/530s Module provides one Gigabit EMAC interface. The most important features of the Ethernet MAC module are

- Standard compliance
  - IEEE 802.3az-2010: energy efficient Ethernet (EEE)
  - RGMII v2.6



- MAC supports the following features:
  - 10/100/1000 Mbps data transfer rates with an RGMII interface to communicate with external Gigabit PHY
  - Full duplex operation
  - Half duplex operation
  - Flexible address filtering
  - Additional frame filtering

## SD/MMC

The ARTIK 530/530s Module provides one SD/MMC interface. The Mobile Storage Host is an interface between the system and the SD/MMC. The key features of mobile storage host sub-system are as follows:

### SD

- Support for Secure Digital I/O (SDIO – version 3.0)
- Support for Secure Digital Memory (SDMEM – version 3.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA-version 1.1)
- Support 4-bit SDR mode up to 50MHz
- Support for PIO and DMA mode data transfer
- Support for 4- bit data bus width

### MMC

- Support for Multimedia Cards (MMC – version 4.41)
- Support for Embedded Multimedia Cards (eMMC – version 4.5)
- Support for 4-bit SDR mode up to 50MHz
- Support for PIO and DMA mode data transfer
- Support for 4- bit data bus width

## Memory Controller

The ARTIK 530/530s Module has one DDR3 memory interface. The key features are

- One 32-bit DDR3 memory interface
- Two 256MB or two 512MB DDR3 16-bit memory chips, for a total of 512MB or 1GB
- Up to 800MHz DDR3 speed with a maximum throughput of 6.4GB/s

## JTAG

The JTAG core provides debug capabilities for the developer and is compliant with the IEEE 1149 standard.

## Timer

The ARTIK 530/530s Module has four dedicated timer channels. The most important features of the Timer module are

- Timer or watchdog timer modes
- Four dedicated Timer channels with watchdog timer
- Normal interval timer mode with interrupt request
- Reset on timer countdown
- Level-triggered interrupt mechanism

## Interrupt Controller

The ARTIK 530/530s Module has one interrupt controller module. The most important features of the interrupt module are

- Vectored interrupt controller
- Support for 64 channel-interrupt sources
- For each interrupt source the following properties are available:
  - Fixed hardware interrupt priority level
  - Programmable interrupt priority level
  - Hardware interrupt priority level masking
  - IRQ and FIQ generation
  - Software interrupt generation
  - Test registers
  - Raw interrupt status
  - Interrupt request status

## DMA

The ARTIK 530/530s Module has one scatter-gather DMA module. The most important features of the DMA module are

- 16 channels of dedicated DMA
- 16 DMA request lines
- Various operating modes
  - Single DMA mode
  - Burst DMA mode
  - Memory-to-memory transfer
  - Memory-to-peripheral transfer
  - Peripheral-to-memory transfer
  - Peripheral-to-peripheral transfer
- Support for 8/16/32 bit wide transactions
- Big endian and little endian (default) support

## RTC

The ARTIK 530/530s Module has one real time clock (RTC) module. The most important features are

- Four spread-spectrum PLLs
- Two external crystals: one 24MHz crystal for the PLLs and one 32.768KHz crystal for the RTC
- One 32-bit RTC counter
- Support for alarm interrupt using RTC
- 

## Video Input Processor

The ARTIK 530/530s Module provides one video input processor (VIP). The key features of the VIP sub-system are

- Support for external 8-bit and 16-bit MIPI
- Support for internal MIPI-CSI
- Support for images up to 8192×8192
- Support for clipping and scale-down
- Support for YUV420 memory format

## Scaler

The ARTIK 530/530s Module provides one universal scaler. The key features of the scaler are

- Support for different input formats:
  - YUV420, YUV422, YUV444
- Flexible size, from 8×8 up to 1920×1080 with a granularity of 8
- Upscale ratio from 8×8 to 1920×1080
- Downscale ratio from 1920×1080 to 8×8
- Low pass filter available after upscale or before downscale
- Horizontal 5-tab filter with 64 sets of coefficients
- Vertical 3-tab filter with 32 sets of coefficients

## Multiformat Codec

The ARTIK 530/530s Module provides one integrated Multiformat Codec (MFC) module. The key features of the MFC sub-system are

- Decoder:
  - H.264 : BP, MP, HP Level 4.2 up to 1920×1080, up to 50MBps
  - MPEG4 : Advanced Simple Profile (ASP) up to 1920×1080, at up to 40Mbps
  - H.263 : Profile 3 up to 1920×1080, up to 20Mbps
  - MPEG 1,2 : Main Profile, High Level up to 1920×1080, up to 80MBps

- Encoder:
  - H.264 : Baseline profile, Level 4.0 up to 1080p, up to 20Mbps
  - MPEG4 : Simple profile, Level 5.6 up to 1080p, up to 20Mbps
  - H.263 : Profile 3, Level 70 up to 1080p, up to 20Mbps

## Graphics Pipeline

The ARTIK 530/530s Module provides one 2D and 3D graphics pipeline module. The key features of the graphics pipeline are

- Two pixel processors:
  - Tile oriented processing
  - Alpha blending
  - Texture support, non-power-of-2
  - Cube mapping
  - Fast dynamic branching
  - Trigonometric acceleration
  - Full floating-point arithmetic
  - Line, quad, triangle and point sprites
  - Perspective correct texturing
  - Point sampling, bilinear and trilinear filtering
  - 8-bit stencil buffering
  - 4-level hierarchical Z and stencil operation
- Geometry processor:
  - Programmable vertex shader
  - Flexible input and output formats
  - Autonomous operation tile list generation
  - Indexed and non-indexed geometry input
  - Primitive constructions with points, lines, triangles and quads
- Support for OpenGL ES 1.0 and 2.0

## Security Subsystem

In addition to the Secure Element, the main processor on the module provides additional security features. The key features of the Security Controller sub-system are

- Secure 128-bit die ID (available to the ARTIK 530s Modules only)
- Secure JTAG featuring a secure 128-bit JTAG ID (available to the ARTIK 530s Modules only)
- Secure boot featuring a 128-bit boot ID (available to the ARTIK 530s Modules only)
- Security Controller (available to the ARTIK 530s Modules only)
- Secure Element (all features in ARTIK 530s Modules; limited features in ARTIK 530 Module)

## Security Controller

The Security Controller provides a Trusted Execution Environment (TEE) and hardware cryptographic accelerators as follows:

- TEE
  - Register Protection Controller
  - Memory Protection Controller
- Hardware cryptographic accelerators
  - DES, Triple DES
  - AES
  - SHA-1
  - MD5

## Secure Element

The ARTIK 530/530s Module has a dedicated Secure Element to assure end-to-end authentication and communication between nodes in an IoT setting. The most important hardware features of the Secure Element are

- An ISO/IEC 7816 14443-compliant interface.
- Dedicated 16-bit SecuCalm CPU core
- Crypto co-processor
  - Modular exponential accelerator
  - RSA 2080 bits
  - ECC 512 bits
- Data security
  - Memory encryption for all memory
  - 256B read-only and 256B nonerasable Flash area
  - Selective reset operation if abnormal voltages/frequencies are detected
- Embedded tamper-free memory
  - 32KB ROM
  - 264KB Flash
  - 2.5KB cryptographic memory
- Serial interfaces:
  - ISO 7816-3-compliant interface
  - Asynchronous half-duplex character receive/transmit serial interface

## Quad-Core Processor System

The processor system architecture that resides on the ARTIK 530/530s Module is a system-on-a-chip (SoC) based on a 32-bit RISC architecture. Designed using the 28nm low power process, the processor system architecture provides superior performance using a quad-core CPU. The key features of the ARTIK 530/530s Module are

- Quad-core ARM® Cortex®-A9, 32-bit RISC architecture
- Maximum core speed 1.2GHz

- 32KB I-Cache per core
- 32KB D-Cache per core
- 1024KB L2-Cache shared between four cores
- Support for dynamic virtual-address mapping

MODULE PADS

The ARTIK 530/530s Module utilizes 292 signal and ground balls providing all the relevant signaling. *Figure 3* shows how the balls are oriented and how signal coordinates are assigned to the PADS of the ARTIK 530/530s Module. *Table 2–Table 6* describe the relation between the ball coordinates and the ball signal names. These tables also provide detailed characteristics for each ball signal name.

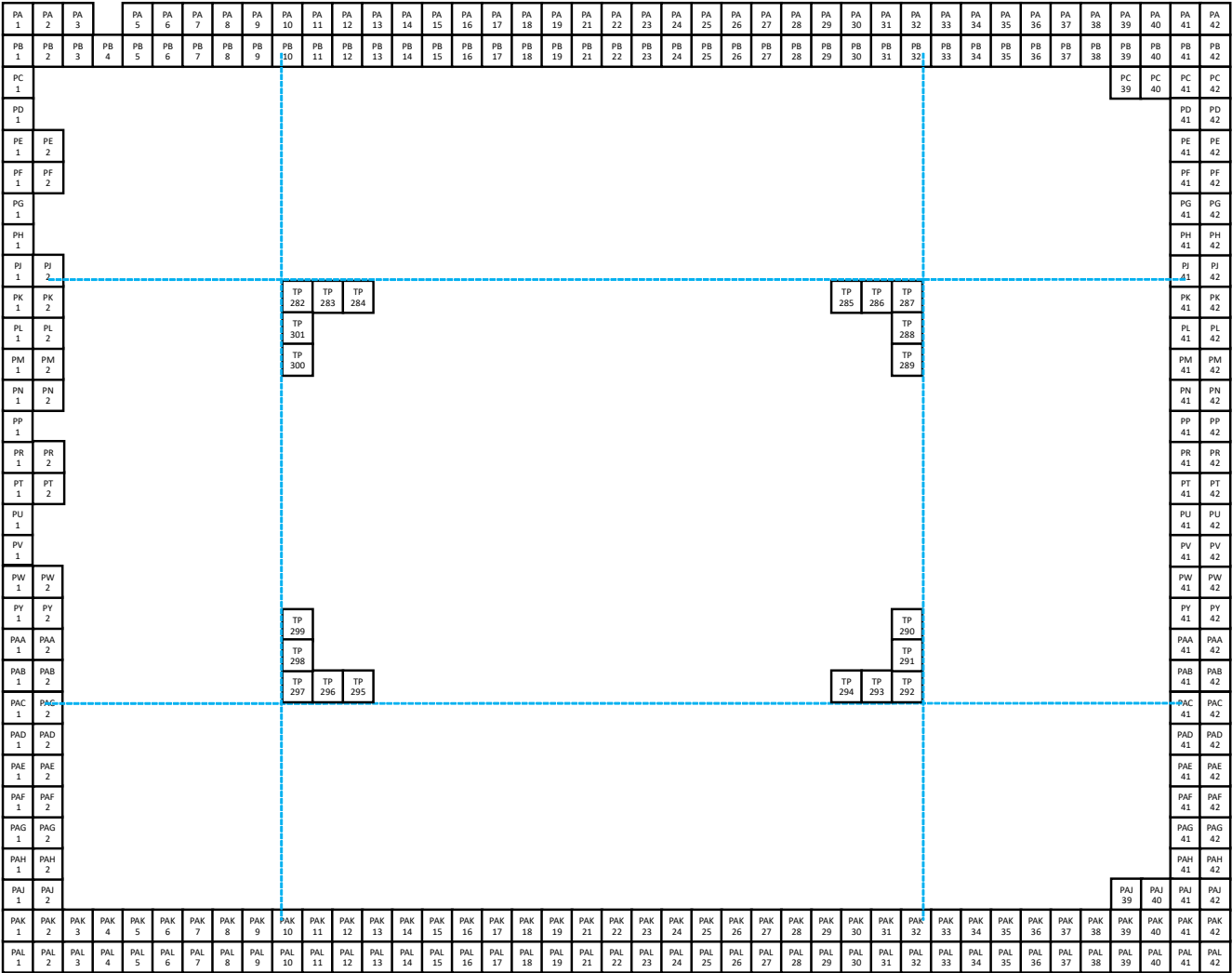


Figure 3. ARTIK 530/530s Module Top View Ball Organization

## Ball Table Column Definitions

The meaning of the various columns used in [Table 2](#) - [Table 6](#) is explained in [Table 1](#).

Table 1. Ball Table Column Definition

| Column Name | Column Definition                                                                                                                                                              |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Ball Loc.   | Ball location on the ARTIK 530/530s Module as shown in <a href="#">Figure 3</a> .                                                                                              |
| Ball Name   | The ball name on the ARTIK 530/530s Module.                                                                                                                                    |
| Voltage     | Voltage level on the ball.                                                                                                                                                     |
| Default     | Default function of the main SoC at hardware power-on.                                                                                                                         |
| Type        | S: Signal ball, P: Power ball, G: GND ball.                                                                                                                                    |
| I/O         | I: Input, O: Output, IO: Input/Output to/from module                                                                                                                           |
| PU/PD       | Indicates the presence of module-internal pull-up or pull-down. PU: Pull-Up, PD: Pull-Down, N: No Pull-Up/Pull-Down.                                                           |
| Group       | Nominal function group set according to pad name. For more information see the ARTIK 530/530s Module Hardware User Guide. Usually the function of the pin can be reprogrammed. |
| Function    | Explanation on the function of the ball.                                                                                                                                       |

## North Ball Array

Table 2. North Ball Array

| Ball Loc. | Ball Name        | Voltage | Type | I/O | PU/PD | Group   | Function                         |
|-----------|------------------|---------|------|-----|-------|---------|----------------------------------|
| PA1       | GMAC_TXEN        | 3.3V    | S    | IO  | N     | GMAC    | GMAC Transmit Enable             |
| PA2       | GMAC_TXD1        | 3.3V    | S    | IO  | N     | GMAC    | GMAC Transmit Data 1             |
| PA3       | GMAC_TXD3        | 3.3V    | S    | IO  | N     | GMAC    | GMAC Transmit Data 3             |
| PA4       | NO BALL          | –       | –    | –   | –     | NO BALL | –                                |
| PA5       | GMAC_GTXCLK      | 3.3V    | S    | IO  | N     | GMAC    | GMAC Transmit Clock              |
| PA6       | GMAC_RXDV        | 3.3V    | S    | IO  | N     | GMAC    | GMAC Receive Enable              |
| PA7       | GMAC_RXD2        | 3.3V    | S    | IO  | N     | GMAC    | GMAC Receive Data 2              |
| PA8       | GMAC_RXD0        | 3.3V    | S    | IO  | N     | GMAC    | GMAC Receive Data 0              |
| PA9       | GND              | 0.0V    | G    | –   | –     | GND     | Ground                           |
| PA10      | AP_MIPICSI_DNCLK | 1.8V    | S    | IO  | N     | CSI     | MIPI CSI Data Negative Clock     |
| PA11      | AP_MIPICSI_DN0   | 1.8V    | S    | IO  | N     | CSI     | MIPI CSI Data Negative 0         |
| PA12      | AP_MIPICSI_DN1   | 1.8V    | S    | IO  | N     | CSI     | MIPI CSI Data Negative 1         |
| PA13      | AP_MIPICSI_DN2   | 1.8V    | S    | IO  | N     | CSI     | MIPI CSI Data Negative 2         |
| PA14      | AP_MIPICSI_DN3   | 1.8V    | S    | IO  | N     | CSI     | MIPI CSI Data Negative 3         |
| PA15      | GND              | 0.0V    | G    | –   | –     | GND     | Ground                           |
| PA16      | AP_MIPIDSI_DNCLK | 1.8V    | S    | IO  | N     | DSI     | MIPI DSI Data Negative Clock     |
| PA17      | AP_MIPIDSI_DN0   | 1.8V    | S    | IO  | N     | DSI     | MIPI DSI Data Negative 0         |
| PA18      | AP_MIPIDSI_DN1   | 1.8V    | S    | IO  | N     | DSI     | MIPI DSI Data Negative 1         |
| PA19      | AP_MIPIDSI_DN2   | 1.8V    | S    | IO  | N     | DSI     | MIPI DSI Data Negative 2         |
| PA20      | AP_MIPIDSI_DN3   | 1.8V    | S    | IO  | N     | DSI     | MIPI DSI Data Negative 3         |
| PA21      | GND              | 0.0V    | G    | –   | –     | GND     | Ground                           |
| PA22      | AP_LVDS_TN0      | 1.8V    | S    | O   | N     | LVDS    | LVDS Transmit Channel 0 Negative |
| PA23      | AP_LVDS_TN1      | 1.8V    | S    | O   | N     | LVDS    | LVDS Transmit Channel 1 Negative |



Table 2. North Ball Array (Continued)

| Ball Loc. | Ball Name        | Voltage | Type | I/O | PU/PD | Group    | Function                          |
|-----------|------------------|---------|------|-----|-------|----------|-----------------------------------|
| PA24      | AP_LVDS_TN2      | 1.8V    | S    | O   | N     | LVDS     | LVDS Transmit Channel 2 Negative  |
| PA25      | AP_LVDS_TNCLK    | 1.8V    | S    | O   | N     | LVDS     | LVDS Transmit Negative Clock      |
| PA26      | AP_LVDS_TN3      | 1.8V    | S    | O   | N     | LVDS     | LVDS Transmit Channel 3 Negative  |
| PA27      | AP_LVDS_TN4      | 1.8V    | S    | O   | N     | LVDS     | LVDS Transmit Channel 4 Negative  |
| PA28      | GND              | 0.0V    | G    | -   | -     | GND      | Ground                            |
| PA29      | AP_HDMI_CEC      | 3.3V    | S    | IO  | N     | HDMI     | HDMI Consumer Electronics Control |
| PA30      | AP_HDMI_TX2N     | 1.8V    | S    | O   | N     | HDMI     | HDMI Transmit Channel 2 Negative  |
| PA31      | AP_HDMI_TX1N     | 1.8V    | S    | O   | N     | HDMI     | HDMI Transmit Channel 1 Negative  |
| PA32      | AP_HDMI_TX0N     | 1.8V    | S    | O   | N     | HDMI     | HDMI Transmit Channel0 Negative   |
| PA33      | AP_HDMI_TXCN     | 1.8V    | S    | O   | N     | HDMI     | HDMI Transmit Negative Clock      |
| PA34      | GND              | 0.0V    | G    | -   | -     | GND      | Ground                            |
| PA35      | AP_OTG_DM        | 3.3V    | S    | IO  | N     | USB OTG  | USB OTG Data Minus                |
| PA36      | AP_USBH_DM       | 3.3V    | S    | IO  | N     | USB HOST | USB HOST Data Minus               |
| PA37      | AP_GPA13         | 3.3V    | S    | IO  | N     | GPIO     | Generic GPIO                      |
| PA38      | AP_HSIC_STROBE   | 1.2V    | S    | IO  | N     | HSIC     | HSIC Strobe                       |
| PA39      | AP_GPA14         | 3.3V    | S    | IO  | N     | GPIO     | Generic GPIO                      |
| PA40      | AP_GPA9          | 3.3V    | S    | IO  | N     | GPIO     | Generic GPIO                      |
| PA41      | AP_GPA15         | 3.3V    | S    | IO  | N     | GPIO     | Generic GPIO                      |
| PA42      | AP_GPA12         | 3.3V    | S    | IO  | N     | GPIO     | Generic GPIO                      |
| PB1       | GND              | 0.0V    | G    | -   | -     | GND      | Ground                            |
| PB2       | GMAC_TXD0        | 3.3V    | S    | IO  | N     | GMAC     | GMAC Transmit Data 0              |
| PB3       | GMAC_TXD2        | 3.3V    | S    | IO  | N     | GMAC     | GMAC Transmit Data 2              |
| PB4       | GMAC_MDC         | 3.3V    | S    | IO  | N     | GMAC     | GMAC MDC                          |
| PB5       | GMAC_RXCLK       | 3.3V    | S    | IO  | N     | GMAC     | GMAC Receive Clock                |
| PB6       | GMAC_RXD3        | 3.3V    | S    | IO  | N     | GMAC     | GMAC Receive Data 3               |
| PB7       | GMAC_RXD1        | 3.3V    | S    | IO  | N     | GMAC     | GMAC Receive Data 1               |
| PB8       | GMAC_MDIO        | 3.3V    | S    | IO  | N     | GMAC     | GMAC MDIO                         |
| PB9       | GND              | 0.0V    | G    | -   | -     | GND      | Ground                            |
| PB10      | AP_MIPICSI_DPCLK | 1.8V    | S    | IO  | N     | CSI      | MIPI CSI Data Positive Clock      |
| PB11      | AP_MIPICSI_DP0   | 1.8V    | S    | IO  | N     | CSI      | MIPI CSI Data Positive 0          |
| PB12      | AP_MIPICSI_DP1   | 1.8V    | S    | IO  | N     | CSI      | MIPI CSI Data Positive 1          |
| PB13      | AP_MIPICSI_DP2   | 1.8V    | S    | IO  | N     | CSI      | MIPI CSI Data Positive 2          |
| PB14      | AP_MIPICSI_DP3   | 1.8V    | S    | IO  | N     | CSI      | MIPI CSI Data Positive 3          |
| PB15      | GND              | 0.0V    | G    | -   | -     | GND      | Ground                            |
| PB16      | AP_MIPIDSI_DPCLK | 1.8V    | S    | IO  | N     | DSI      | MIPI DSI Data Positive Clock      |
| PB17      | AP_MIPIDSI_DP0   | 1.8V    | S    | IO  | N     | DSI      | MIPI DSI Data Positive 0          |
| PB18      | AP_MIPIDSI_DP1   | 1.8V    | S    | IO  | N     | DSI      | MIPI DSI Data Positive 1          |
| PB19      | AP_MIPIDSI_DP2   | 1.8V    | S    | IO  | N     | DSI      | MIPI DSI Data Positive 2          |
| PB20      | AP_MIPIDSI_DP3   | 1.8V    | S    | IO  | N     | DSI      | MIPI DSI Data Positive 3          |
| PB21      | GND              | 0.0V    | G    | -   | -     | GND      | Ground                            |
| PB22      | AP_LVDS_TP0      | 1.8V    | S    | O   | N     | LVDS     | LVDS Transmit Channel 0 Positive  |
| PB23      | AP_LVDS_TP1      | 1.8V    | S    | O   | N     | LVDS     | LVDS Transmit Channel 1 Positive  |

Table 2. North Ball Array (Continued)

| Ball Loc. | Ball Name     | Voltage | Type | I/O | PU/PD | Group    | Function                         |
|-----------|---------------|---------|------|-----|-------|----------|----------------------------------|
| PB24      | AP_LVDS_TP2   | 1.8V    | S    | O   | N     | LVDS     | LVDS Transmit Channel 2 Positive |
| PB25      | AP_LVDS_TPCLK | 1.8V    | S    | O   | N     | LVDS     | LVDS Transmit Positive Clock     |
| PB26      | AP_LVDS_TP3   | 1.8V    | S    | O   | N     | LVDS     | LVDS Transmit Channel 3 Positive |
| PB27      | AP_LVDS_TP4   | 1.8V    | S    | O   | N     | LVDS     | LVDS Transmit Channel 4 Positive |
| PB28      | GND           | 0.0V    | G    | -   | -     | GND      | Ground                           |
| PB29      | AP_HDMI_HPD   | 3.3V    | S    | I   | N     | HDMI     | HDMI Hot Plug Detect             |
| PB30      | AP_HDMI_TX2P  | 1.8V    | S    | O   | N     | HDMI     | HDMI Transmit Channel 2 Positive |
| PB31      | AP_HDMI_TX1P  | 1.8V    | S    | O   | N     | HDMI     | HDMI Transmit Channel 1 Positive |
| PB32      | AP_HDMI_TXOP  | 1.8V    | S    | O   | N     | HDMI     | HDMI Transmit Channel 0 Positive |
| PB33      | AP_HDMI_TXCP  | 1.8V    | S    | O   | N     | HDMI     | HDMI Transmit Positive Clock     |
| PB34      | GND           | 0.0V    | G    | -   | -     | GND      | Ground                           |
| PB35      | AP_OTG_DP     | 3.3V    | S    | IO  | N     | USB OTG  | USB OTG Data Plus                |
| PB36      | AP_USBH_DP    | 3.3V    | S    | IO  | N     | USB HOST | USB HOST Data Plus               |
| PB37      | AP_OTG_ID     | -       | S    | I   | N     | USB HOST | USB HOST ID                      |
| PB38      | AP_HSIC_DATA  | 1.2V    | S    | IO  | N     | HSIC     | HSIC Data                        |
| PB39      | AP_GPA4       | 3.3V    | S    | IO  | N     | GPIO     | Generic GPIO                     |
| PB40      | AP_GPA5       | 3.3V    | S    | IO  | N     | GPIO     | Generic GPIO                     |
| PB41      | AP_GPA16      | 3.3V    | S    | IO  | N     | GPIO     | Generic GPIO                     |
| PB42      | AP_GPA11      | 3.3V    | S    | IO  | N     | GPIO     | Generic GPIO                     |

## South Ball Array

Table 3. South Ball Array

| Ball Loc. | Ball Name             | Voltage | Type | I/O | PU/PD | Group            | Function                     |
|-----------|-----------------------|---------|------|-----|-------|------------------|------------------------------|
| PAK1      | AP_I2S0_DOUT          | 3.3V    | S    | IO  | N     | I2S0             | I <sup>2</sup> S 0 Data Out  |
| PAK2      | AP_I2S0_BCLK          | 3.3V    | S    | IO  | N     | I2S0             | I <sup>2</sup> S 0 Bit Clock |
| PAK3      | AP_GPC11_SPI2_MISO    | 3.3V    | S    | IO  | N     | SPI2             | SPI 2 Receive Data           |
| PAK4      | AP_GPC9_SPI2_CLK      | 3.3V    | S    | IO  | N     | SPI2             | SPI 2 Clock                  |
| PAK5      | AP_SPIO_MISO          | 3.3V    | S    | IO  | N     | SPIO             | SPI 0 Receive Data *         |
| PAK6      | AP_SPIO_CLK           | 3.3V    | S    | IO  | N     | SPIO             | SPI 0 Clock *                |
| PAK7      | AP_GPC14_PWM2         | 3.3V    | S    | IO  | N     | PWM              | PWM 2                        |
| PAK8      | AP_GPD6_SCL2          | 3.3V    | S    | IO  | PU    | I <sup>2</sup> C | I <sup>2</sup> C SCL 2       |
| PAK9      | AP_GPD4_SCL1          | 3.3V    | S    | IO  | PU    | I <sup>2</sup> C | I <sup>2</sup> C SCL 1       |
| PAK10     | AP_GPD2_SCL0          | 3.3V    | S    | IO  | PU    | I <sup>2</sup> C | I <sup>2</sup> C SCL 0       |
| PAK11     | AP_GPA23_HDMI_I2C_SCL | 3.3V    | S    | IO  | N     | I <sup>2</sup> C | HDMI I <sup>2</sup> C SCL *  |
| PAK12     | ZB_DEBUG_TDO_SWO      | 3.3V    | -    | -   | -     | 802.15.4         | 802.15.4 JTAG TMS            |
| PAK13     | ZB_PTI_DATA_FRC_DOUT  | 3.3V    | -    | -   | -     | 802.15.4         | 802.15.4 JTAG TCK            |
| PAK14     | ZB_DEBUG_TCK_SWCLK    | 3.3V    | -    | -   | -     | 802.15.4         | 802.15.4 Control             |
| PAK15     | COMBO_ZIG_UART_TXD    | 3.3V    | S    | IO  | -     | 802.15.4         | 802.15.4 UART                |
| PAK16     | GND                   | 0.0V    | G    | -   | -     | GND              | Ground                       |

Table 3. South Ball Array (Continued)

| Ball Loc. | Ball Name                | Voltage | Type | I/O | PU/PD | Group            | Function                               |
|-----------|--------------------------|---------|------|-----|-------|------------------|----------------------------------------|
| PAK17     | VCC3P3_SYS               | 3.3V    | P    | O   | –     | POWER            | VCC 3.3V Power: voltage reference only |
| PAK18     | VCC3P3_SYS               | 3.3V    | P    | O   | –     | POWER            | VCC 3.3V Power: voltage reference only |
| PAK19     | AP_GPD28                 | 3.3V    | S    | IO  | N     | GPIO             | Generic GPIO                           |
| PAK20     | AP_GPE2                  | 3.3V    | S    | IO  | N     | GPIO             | Generic GPIO                           |
| PAK21     | AP_GPE1                  | 3.3V    | S    | IO  | N     | GPIO             | Generic GPIO                           |
| PAK22     | AP_UARTTX3               | 3.3V    | S    | IO  | N     | UART             | UART Transmit Data 3                   |
| PAK23     | AP_UARTTX4               | 3.3V    | S    | IO  | N     | UART             | UART Transmit Data 4                   |
| PAK24     | AP_UARTTX0               | 3.3V    | S    | IO  | N     | UART             | UART Transmit Data 0                   |
| PAK25     | AP_GPBO_VID1_1_I2SLRCK1  | 3.3V    | S    | IO  | PU    | I2S1             | I <sup>2</sup> S 1 Left Right Clock *  |
| PAK26     | AP_GPA28_I2SMCLK1        | 3.3V    | S    | IO  | N     | I2S1             | I <sup>2</sup> S 1 Master Clock *      |
| PAK27     | AP_GPA30_VID1_0_I2SBCLK1 | 3.3V    | S    | IO  | PU    | I2S1             | I <sup>2</sup> S 1 Bit Clock *         |
| PAK28     | AP_SDO_CMD               | 3.3V    | S    | IO  | N     | SD/MMC           | SD Command                             |
| PAK29     | AP_SDO_D1                | 3.3V    | S    | IO  | N     | SD/MMC           | SD Data 1                              |
| PAK30     | AP_SDO_CLK               | 3.3V    | S    | IO  | N     | SD/MMC           | SD Clock                               |
| PAK31     | NO CONNECTION            | –       | –    | –   | –     | NC               | NA                                     |
| PAK32     | AP_GPB13_SDO_BOOT        | 3.3V    | S    | I   | PU    | BOOTING          | Select Booting Scenario                |
| PAK33     | AP_GPC17                 | 3.3V    | S    | IO  | N     | GPIO             | Generic GPIO                           |
| PAK34     | AP_GPC0                  | 3.3V    | S    | IO  | N     | GPIO             | Generic GPIO                           |
| PAK35     | AP_GPC26                 | 3.3V    | S    | IO  | PU    | GPIO             | Generic GPIO                           |
| PAK36     | AP_GPB8                  | 3.3V    | S    | IO  | N     | GPIO             | Generic GPIO                           |
| PAK37     | AP_GPB14                 | 3.3V    | S    | IO  | N     | GPIO             | Generic GPIO                           |
| PAK38     | AP_GPA20                 | 3.3V    | S    | IO  | N     | GPIO             | Generic GPIO                           |
| PAK39     | AP_GPA18                 | 3.3V    | S    | IO  | N     | GPIO             | Generic GPIO                           |
| PAK40     | AP_GPA21                 | 3.3V    | S    | IO  | N     | GPIO             | Generic GPIO                           |
| PAK41     | AP_GPA10                 | 3.3V    | S    | IO  | N     | GPIO             | Generic GPIO                           |
| PAK42     | AP_GPA6                  | 3.3V    | S    | IO  | N     | GPIO             | Generic GPIO                           |
| PAL1      | AP_I2S0_DIN              | 3.3V    | S    | IO  | N     | I2S0             | I <sup>2</sup> S 0 Data In             |
| PAL2      | AP_I2S0_MCLK             | 3.3V    | S    | IO  | N     | I2S0             | I <sup>2</sup> S 0 Master Clock        |
| PAL3      | AP_GPC12_SPI2_MOSI       | 3.3V    | S    | IO  | N     | SPI2             | SPI 2 Transmit Data                    |
| PAL4      | AP_GPC10_SPI2_CS         | 3.3V    | S    | IO  | PU    | SPI2             | SPI 2 Frame                            |
| PAL5      | AP_SPIO_MOSI             | 3.3V    | S    | IO  | N     | SPIO             | SPI 0 Transmit Data *                  |
| PAL6      | AP_SPIO_CS               | 3.3V    | S    | IO  | N     | SPIO             | SPI 0 Frame *                          |
| PAL7      | AP_GPD1_PWM0             | 3.3V    | S    | IO  | N     | PWM              | PWM 0                                  |
| PAL8      | AP_GPD7_SDA2             | 3.3V    | S    | IO  | PU    | I <sup>2</sup> C | I <sup>2</sup> C SDA 2                 |
| PAL9      | AP_GPD5_SDA1             | 3.3V    | S    | IO  | PU    | I <sup>2</sup> C | I <sup>2</sup> C SDA 1                 |
| PAL10     | AP_GPD3_SDA0             | 3.3V    | S    | IO  | PU    | I <sup>2</sup> C | I <sup>2</sup> C SDA 0                 |
| PAL11     | AP_GPA24_HDMI_I2C_SDA    | 3.3V    | S    | IO  | N     | I <sup>2</sup> C | HDMI I <sup>2</sup> C SDA *            |
| PAL12     | ZB_DEBUG_TMS_SWDIO       | 3.3V    | –    | –   | –     | 802.15.4         | 802.15.4 JTAG TDI                      |
| PAL13     | ZB_PTI_SYNC_FRC_DFRAME   | 3.3V    | –    | –   | –     | 802.15.4         | 802.15.4 JTAG TDO                      |
| PAL14     | PAD_ZB_RSTn              | 3.3V    | S    | O   | N     | 802.15.4         | 802.15.4 Reset                         |
| PAL15     | COMBO_ZIG_UART_RXD       | 3.3V    | S    | IO  | PU    | 802.15.4         | 802.15.4 UART (for internal use only)  |
| PAL16     | GND                      | 0.0V    | G    | –   | –     | GND              | Ground                                 |

Table 3. South Ball Array (Continued)

| Ball Loc. | Ball Name               | Voltage | Type | I/O | PU/PD | Group   | Function                              |
|-----------|-------------------------|---------|------|-----|-------|---------|---------------------------------------|
| PAL17     | VCC3P3_SYS              | 3.3V    | P    | O   | –     | POWER   | VCC 3V3 Power: voltage reference only |
| PAL18     | VCC3P3_SYS              | 3.3V    | P    | O   | –     | POWER   | VCC 3V3 Power: voltage reference only |
| PAL19     | AP_VDDPWON              | 3.3V    | S    | O   | N     | MISC    | VDD Power On                          |
| PAL20     | AP_GPE3                 | 3.3V    | S    | IO  | N     | GPIO    | Generic GPIO                          |
| PAL21     | AP_GPE0                 | 3.3V    | S    | IO  | N     | GPIO    | Generic GPIO                          |
| PAL22     | AP_UART_RX3             | 3.3V    | S    | IO  | N     | UART    | UART Receive Data 3                   |
| PAL23     | AP_UART_RX4             | 3.3V    | S    | IO  | N     | UART    | UART Receive Data 4                   |
| PAL24     | AP_UART_RX0             | 3.3V    | S    | IO  | N     | UART    | UART Receive Data 0                   |
| PAL25     | AP_GPD31                | 3.3V    | S    | IO  | N     | GPIO    | Generic GPIO                          |
| PAL26     | AP_GPB9_I2SDIN1         | 3.3V    | S    | IO  | N     | I2S1    | I <sup>2</sup> S 1 Data In *          |
| PAL27     | AP_GPB6_VID1_4_I2SDOUT1 | 3.3V    | S    | IO  | PD    | I2S1    | I <sup>2</sup> S 1 Data Out *         |
| PAL28     | AP_SDO_D3               | 3.3V    | S    | IO  | N     | SD/MMC  | SD Data 3                             |
| PAL29     | AP_SDO_D2               | 3.3V    | S    | IO  | N     | SD/MMC  | SD Data 2                             |
| PAL30     | AP_SDO_D0               | 3.3V    | S    | IO  | N     | SD/MMC  | SD Data 0                             |
| PAL31     | AP_GPB4_VID1_3_BOOT     | 3.3V    | S    | I   | PU    | BOOTING | Select Booting Scenario               |
| PAL32     | AP_GPB15_SD1_BOOT       | 3.3V    | S    | I   | PD    | BOOTING | Select Booting Scenario               |
| PAL33     | AP_GPD8                 | 3.3V    | S    | IO  | N     | GPIO    | Generic GPIO                          |
| PAL34     | AP_GPE30                | 3.3V    | S    | IO  | PU    | GPIO    | Generic GPIO                          |
| PAL35     | AP_GPC27                | 3.3V    | S    | IO  | PU    | GPIO    | Generic GPIO                          |
| PAL36     | AP_GPB22                | 3.3V    | S    | IO  | N     | GPIO    | Generic GPIO                          |
| PAL37     | AP_GPB16                | 3.3V    | S    | IO  | N     | GPIO    | Generic GPIO                          |
| PAL38     | AP_GPB23                | 3.3V    | S    | IO  | N     | GPIO    | Generic GPIO                          |
| PAL39     | AP_GPA22                | 3.3V    | S    | IO  | N     | GPIO    | Generic GPIO                          |
| PAL40     | AP_GPA19                | 3.3V    | S    | IO  | N     | GPIO    | Generic GPIO                          |
| PAL41     | AP_GPA17                | 3.3V    | S    | IO  | N     | GPIO    | Generic GPIO                          |
| PAL42     | AP_GPA3                 | 3.3V    | S    | IO  | N     | GPIO    | Generic GPIO                          |

\*. Functions as general-purpose GPIO by default

## East Ball Array

Table 4. East Ball Array

| Ball | Ball Name | Voltage | Type | I/O | PU/PD | Group   | Function |
|------|-----------|---------|------|-----|-------|---------|----------|
| PC1  | GND       | 0.0V    | G    | –   | –     | GND     | Ground   |
| PC2  | NO BALL   | –       | –    | –   | –     | NO BALL | –        |
| PD1  | GND       | 0.0V    | G    | –   | –     | GND     | Ground   |
| PD2  | NO BALL   | –       | –    | –   | –     | NO BALL | –        |
| PE1  | GND       | 0.0V    | G    | –   | –     | GND     | Ground   |
| PE2  | GND       | 0.0V    | G    | –   | –     | GND     | Ground   |
| PF1  | GND       | 0.0V    | G    | –   | –     | GND     | Ground   |
| PF2  | GND       | 0.0V    | G    | –   | –     | GND     | Ground   |

Table 4. East Ball Array (Continued)

| Ball | Ball Name         | Voltage | Type | I/O | PU/PD | Group         | Function                    |
|------|-------------------|---------|------|-----|-------|---------------|-----------------------------|
| PG1  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PG2  | NO BALL           | -       | -    | -   | -     | NO BALL       | -                           |
| PH1  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PH2  | NO BALL           | -       | -    | -   | -     | NO BALL       | -                           |
| PJ1  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PJ2  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PK1  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PK2  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PL1  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PL2  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PM1  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PM2  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PN1  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PN2  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PP1  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PP2  | NO BALL           | -       | -    | -   | -     | NO BALL       | -                           |
| PR1  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PR2  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PT1  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PT2  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PU1  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PU2  | NO BALL           | -       | -    | -   | -     | NO BALL       | -                           |
| PV1  | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PV2  | NO BALL           | -       | -    | -   | -     | NO BALL       | -                           |
| PW1  | AP_ADC4           | 1.8V    | S    | I   | N     | ADC           | ADC Channel 4               |
| PW2  | AP_ADC5           | 1.8V    | S    | I   | N     | ADC           | ADC Channel 5               |
| PY1  | AP_ADC0           | 1.8V    | S    | I   | N     | ADC           | ADC Channel 0               |
| PY2  | AP_ADC1           | 1.8V    | S    | I   | N     | ADC           | ADC Channel 1               |
| PAA1 | AP_ADC2           | 1.8V    | S    | I   | N     | ADC           | ADC Channel 2               |
| PAA2 | AP_ADC3           | 1.8V    | S    | I   | N     | ADC           | ADC Channel 3               |
| PAB1 | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PAB2 | GND               | 0.0V    | G    | -   | -     | GND           | Ground                      |
| PAC1 | AP_TCK            | 3.3V    | S    | IO  | PD    | JTAG          | JTAG TCK                    |
| PAC2 | AP_TMS            | 3.3V    | S    | IO  | PU    | JTAG          | JTAG TMS                    |
| PAD1 | AP_TDO            | 3.3V    | S    | IO  | N     | JTAG          | JTAG TDO                    |
| PAD2 | AP_TDI            | 3.3V    | S    | IO  | PU    | JTAG          | JTAG TDI                    |
| PAE1 | AP_NTRST          | 3.3V    | S    | IO  | PU    | JTAG          | JTAG NTRST                  |
| PAE2 | AP_AGP2_RTC_INT_N | 3.3V    | S    | IO  | N     | KEY/<br>ALIVE | AliveGPIO                   |
| PAF1 | AP_PWRKEY         | 3.3V    | S    | IO  | N     | KEY/<br>ALIVE | Power Key part of AliveGPIO |
| PAF2 | AP_AGP1           | 3.3V    | S    | IO  | N     | ALIVE         | AliveGPIO                   |
| PAG1 | AP_NRESET         | 3.3V    | S    | I   | N*    | KEY           | Reset                       |

Table 4. East Ball Array (Continued)

| Ball | Ball Name     | Voltage | Type | I/O | PU/PD | Group | Function                            |
|------|---------------|---------|------|-----|-------|-------|-------------------------------------|
| PAG2 | AP_GPA25      | 3.3V    | S    | IO  | N     | GPIO  | Generic GPIO                        |
| PAH1 | AP_GPA26      | 3.3V    | S    | IO  | N     | GPIO  | Generic GPIO                        |
| PAH2 | AP_GPA0       | 3.3V    | S    | IO  | N     | GPIO  | Generic GPIO                        |
| PAJ1 | AP_I2SO_LRCLK | 3.3V    | S    | IO  | N     | I2SO  | I <sup>2</sup> S 0 Left Right Clock |
| PAJ2 | AP_GPA27      | 3.3V    | S    | IO  | N     | I2SO  | Generic GPIO                        |

\*. External 100kΩ pull-up resistor required.

## West Ball Array

Table 5. West Ball Array

| Ball | Ball Name      | Voltage | Type | I/O | PU/PD | Group | Function             |
|------|----------------|---------|------|-----|-------|-------|----------------------|
| PC39 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |
| PC40 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |
| PC41 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |
| PC42 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |
| PD41 | VCC5P0_OTGVBUS | -       | P    | I   | -     | POWER | USB2.0 OTG BUS Power |
| PD42 | VCC5P0_OTGVBUS | -       | P    | I   | -     | POWER | USB2.0 OTG BUS Power |
| PE41 | NO CONNECTION  | -       | -    | -   | -     | NC    | -                    |
| PE42 | NO CONNECTION  | -       | -    | -   | -     | NC    | -                    |
| PF41 | NO CONNECTION  | -       | -    | -   | -     | NC    | -                    |
| PF42 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |
| PG41 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |
| PG42 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |
| PH41 | NO CONNECTION  | -       | -    | -   | -     | NC    | -                    |
| PH42 | NO CONNECTION  | -       | -    | -   | -     | NC    | -                    |
| PJ41 | NO CONNECTION  | -       | -    | -   | -     | NC    | -                    |
| PJ42 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |
| PK41 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |
| PK42 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |
| PL41 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |
| PL42 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |
| PM41 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |
| PM42 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |
| PN41 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |
| PN42 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |
| PP41 | AP_GPB30       | 3.3V    | S    | IO  | -     | GPIO  | Generic GPIO         |
| PP42 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |
| PR41 | NO CONNECTION  | -       | -    | -   | -     | NC    | -                    |
| PR42 | NO CONNECTION  | -       | -    | -   | -     | NC    | -                    |
| PT41 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |
| PT42 | GND            | 0.0V    | G    | -   | -     | GND   | Ground               |

Table 5. West Ball Array (Continued)

| Ball  | Ball Name     | Voltage  | Type | I/O | PU/PD | Group  | Function                     |
|-------|---------------|----------|------|-----|-------|--------|------------------------------|
| PU41  | GND           | 0.0V     | G    | -   | -     | GND    | Ground                       |
| PU42  | GND           | 0.0V     | G    | -   | -     | GND    | Ground                       |
| PV41  | VIN           | 3.7~5.0V | P    | I   | -     | POWER  | Main Power Supply for Module |
| PV41  | VIN           | 3.7~5.0V | P    | I   | -     | POWER  | Main Power Supply for Module |
| PW41  | VIN           | 3.7~5.0V | P    | I   | -     | POWER  | Main Power Supply for Module |
| PW42  | VIN           | 3.7~5.0V | P    | I   | -     | POWER  | Main Power Supply for Module |
| PY41  | VIN           | 3.7~5.0V | P    | I   | -     | POWER  | Main Power Supply for Module |
| PY42  | VIN           | 3.7~5.0V | P    | I   | -     | POWER  | Main Power Supply for Module |
| PAA41 | VIN           | 3.7~5.0V | P    | I   | -     | POWER  | Main Power Supply for Module |
| PAA42 | VIN           | 3.7~5.0V | P    | I   | -     | POWER  | Main Power Supply for Module |
| PAB41 | VIN           | 3.7~5.0V | P    | I   | -     | POWER  | Main Power Supply for Module |
| PAB42 | VIN           | 3.7~5.0V | P    | I   | -     | POWER  | Main Power Supply for Module |
| PAC41 | GND           | 0.0V     | G    | -   | -     | GND    | Ground                       |
| PAC42 | GND           | 0.0V     | G    | -   | -     | GND    | Ground                       |
| PAD41 | NO CONNECTION | -        | -    | -   | -     | NC     | -                            |
| PAD42 | NO CONNECTION | -        | -    | -   | -     | NC     | -                            |
| PAE41 | GND           | 0.0V     | G    | -   | -     | GND    | Ground                       |
| PAE42 | NO CONNECTION | -        | -    | -   | -     | NC     | -                            |
| PAF41 | GND           | 0.0V     | G    | -   | -     | GND    | Ground                       |
| PAF42 | GND           | 0.0V     | G    | -   | -     | GND    | Ground                       |
| PAG41 | AP_GPB11      | 3.3V     | S    | IO  | N     | GPIO   | Generic GPIO                 |
| PAG42 | AP_GPB18      | 3.3V     | S    | IO  | N     | GPIO   | Generic GPIO                 |
| PAH41 | AP_GPC25      | 3.3V     | S    | IO  | PU    | GPIO   | Generic GPIO                 |
| PAH42 | AP_GPE31      | 3.3V     | S    | IO  | PU    | GPIO   | Generic GPIO                 |
| PAJ39 | BT_PCM_CLK    | 3.3V     | S    | IO  | N     | BT PCM | PCM Clock                    |
| PAJ40 | BT_PCM_D_IN   | 3.3V     | S    | I   | N     | BT PCM | PCM Data In                  |
| PAJ41 | BT_PCM_D_OUT  | 3.3V     | S    | O   | N     | BT PCM | PCM Data Out                 |
| PAJ42 | BT_PCM_LRCK   | 3.3V     | S    | IO  | N     | BT PCM | PCM LR Clock                 |

## Center Ball Array

Table 6. Center Ball Array

| Ball  | Ball Name | Voltage | Type | I/O | PU/PD | Group | Function |
|-------|-----------|---------|------|-----|-------|-------|----------|
| TP282 | GND       | 0.0V    | NA   | -   | -     | GND   | Ground   |
| TP283 | GND       | 0.0V    | NA   | -   | -     | GND   | Ground   |
| TP284 | GND       | 0.0V    | NA   | -   | -     | GND   | Ground   |
| TP285 | GND       | 0.0V    | NA   | -   | -     | GND   | Ground   |
| TP286 | GND       | 0.0V    | NA   | -   | -     | GND   | Ground   |
| TP287 | GND       | 0.0V    | NA   | -   | -     | GND   | Ground   |
| TP288 | GND       | 0.0V    | NA   | -   | -     | GND   | Ground   |
| TP289 | GND       | 0.0V    | NA   | -   | -     | GND   | Ground   |
| TP290 | GND       | 0.0V    | NA   | -   | -     | GND   | Ground   |

Table 6. Center Ball Array (Continued)

| Ball  | Ball Name | Voltage | Type | I/O | PU/PD | Group | Function |
|-------|-----------|---------|------|-----|-------|-------|----------|
| TP291 | GND       | 0.0V    | NA   | –   | –     | GND   | Ground   |
| TP292 | GND       | 0.0V    | NA   | –   | –     | GND   | Ground   |
| TP293 | GND       | 0.0V    | NA   | –   | –     | GND   | Ground   |
| TP294 | GND       | 0.0V    | NA   | –   | –     | GND   | Ground   |
| TP295 | GND       | 0.0V    | NA   | –   | –     | GND   | Ground   |
| TP296 | GND       | 0.0V    | NA   | –   | –     | GND   | Ground   |
| TP297 | GND       | 0.0V    | NA   | –   | –     | GND   | Ground   |
| TP298 | GND       | 0.0V    | NA   | –   | –     | GND   | Ground   |
| TP299 | GND       | 0.0V    | NA   | –   | –     | GND   | Ground   |
| TP300 | GND       | 0.0V    | NA   | –   | –     | GND   | Ground   |
| TP301 | GND       | 0.0V    | NA   | –   | –     | GND   | Ground   |



## FUNCTIONAL INTERFACES

This section shows the functional interfaces that are available at the pads of the ARTIK 530/530s Module. The functions provided are related to the development environment used. Depending on your project you can always choose to reprogram some of the GPIOs that are currently assigned to the predefined functional interfaces.

### ADC

Table 7. ADC

| Function      | Ball Loc. | Ball Name | Voltage | I/O | PU/PD |
|---------------|-----------|-----------|---------|-----|-------|
| ADC Channel 0 | PY1       | AP_ADC0   | 1.8V    | I   | N     |
| ADC Channel 1 | PY2       | AP_ADC1   | 1.8V    | I   | N     |
| ADC Channel 2 | PAA1      | AP_ADC2   | 1.8V    | I   | N     |
| ADC Channel 3 | PAA2      | AP_ADC3   | 1.8V    | I   | N     |
| ADC Channel 4 | PW1       | AP_ADC4   | 1.8V    | I   | N     |
| ADC Channel 5 | PW2       | AP_ADC5   | 1.8V    | I   | N     |

### Booting

Table 8. Booting

| Function                | Ball Loc. | Ball Name           | Voltage | I/O | PU/PD |
|-------------------------|-----------|---------------------|---------|-----|-------|
| Booting Configuration 1 | PAK32     | AP_GPB13_SDO_BOOT   | 3.3V    | I   | PU    |
| Booting Configuration 2 | PAL32     | AP_GPB15_SD1_BOOT   | 3.3V    | I   | PD    |
| Booting Configuration 3 | PAL31     | AP_GPB4_VID1_3_BOOT | 3.3V    | I   | PU    |



If a preferred boot device fails, the above pins select whether secondary and/or tertiary boot options are available. For details, see [Booting Selection](#).

The above signals can be reassigned by software to alternate functions; see [Table 30](#) for details.

### Bluetooth PCM

Table 9. Bluetooth PCM

| Function     | Ball Loc. | Ball Name    | Voltage | I/O | PU/PD |
|--------------|-----------|--------------|---------|-----|-------|
| PCM Clock    | PAJ39     | BT_PCM_CLK   | 3.3V    | IO  | N     |
| PCM LR Clock | PAJ42     | BT_PCM_LRCK  | 3.3V    | IO  | N     |
| PCM Data In  | PAJ40     | BT_PCM_D_IN  | 3.3V    | I   | N     |
| PCM Data Out | PAJ41     | BT_PCM_D_OUT | 3.3V    | O   | N     |

## MIPI CSI

Table 10. MIPI CSI

| Function                     | Ball Loc. | Ball Name        | Voltage | I/O | PU/PD |
|------------------------------|-----------|------------------|---------|-----|-------|
| MIPI CSI Data Negative Clock | PA10      | AP_MIPICSI_DNCLK | 1.8V    | IO  | N     |
| MIPI CSI Data Negative 0     | PA11      | AP_MIPICSI_DN0   | 1.8V    | IO  | N     |
| MIPI CSI Data Negative 1     | PA12      | AP_MIPICSI_DN1   | 1.8V    | IO  | N     |
| MIPI CSI Data Negative 2     | PA13      | AP_MIPICSI_DN2   | 1.8V    | IO  | N     |
| MIPI CSI Data Negative 3     | PA14      | AP_MIPICSI_DN3   | 1.8V    | IO  | N     |
| MIPI CSI Data Positive Clock | PB10      | AP_MIPICSI_DPCLK | 1.8V    | IO  | N     |
| MIPI CSI Data Positive 0     | PB11      | AP_MIPICSI_DP0   | 1.8V    | IO  | N     |
| MIPI CSI Data Positive 1     | PB12      | AP_MIPICSI_DP1   | 1.8V    | IO  | N     |
| MIPI CSI Data Positive 2     | PB13      | AP_MIPICSI_DP2   | 1.8V    | IO  | N     |
| MIPI CSI Data Positive 3     | PB14      | AP_MIPICSI_DP3   | 1.8V    | IO  | N     |

## MIPI DSI

Table 11. MIPI DSI

| Function                     | Ball Loc. | Ball Name        | Voltage | I/O | PU/PD |
|------------------------------|-----------|------------------|---------|-----|-------|
| MIPI DSI Data Negative Clock | PA16      | AP_MIPIDSI_DNCLK | 1.8V    | IO  | N     |
| MIPI DSI Data Negative 0     | PA17      | AP_MIPIDSI_DN0   | 1.8V    | IO  | N     |
| MIPI DSI Data Negative 1     | PA18      | AP_MIPIDSI_DN1   | 1.8V    | IO  | N     |
| MIPI DSI Data Negative 2     | PA19      | AP_MIPIDSI_DN2   | 1.8V    | IO  | N     |
| MIPI DSI Data Negative 3     | PA20      | AP_MIPIDSI_DN3   | 1.8V    | IO  | N     |
| MIPI DSI Data Positive Clock | PB16      | AP_MIPIDSI_DPCLK | 1.8V    | IO  | N     |
| MIPI DSI Data Positive 0     | PB17      | AP_MIPIDSI_DP0   | 1.8V    | IO  | N     |
| MIPI DSI Data Positive 1     | PB18      | AP_MIPIDSI_DP1   | 1.8V    | IO  | N     |
| MIPI DSI Data Positive 2     | PB19      | AP_MIPIDSI_DP2   | 1.8V    | IO  | N     |
| MIPI DSI Data Positive 3     | PB20      | AP_MIPIDSI_DP3   | 1.8V    | IO  | N     |

## GMAC

Table 12. GMAC

| Function            | Ball Loc. | Ball Name  | Voltage | I/O | PU/PD |
|---------------------|-----------|------------|---------|-----|-------|
| GMAC MDC            | PB4       | GMAC_MDC   | 3.3V    | IO  | N     |
| GMAC MDIO           | PB8       | GMAC_MDIO  | 3.3V    | IO  | N     |
| GMAC Receive Clock  | PB5       | GMAC_RXCLK | 3.3V    | IO  | N     |
| GMAC Receive Data 0 | PA8       | GMAC_RXD0  | 3.3V    | IO  | N     |
| GMAC Receive Data 1 | PB7       | GMAC_RXD1  | 3.3V    | IO  | N     |
| GMAC Receive Data 2 | PA7       | GMAC_RXD2  | 3.3V    | IO  | N     |
| GMAC Receive Data 3 | PB6       | GMAC_RXD3  | 3.3V    | IO  | N     |

Table 12. GMAC (Continued)

| Function             | Ball Loc. | Ball Name   | Voltage | I/O | PU/PD |
|----------------------|-----------|-------------|---------|-----|-------|
| GMAC Receive Enable  | PA6       | GMAC_RXDV   | 3.3V    | IO  | N     |
| GMAC Transmit Clock  | PA5       | GMAC_GTXCLK | 3.3V    | IO  | N     |
| GMAC Transmit Data 0 | PB2       | GMAC_TXD0   | 3.3V    | IO  | N     |
| GMAC Transmit Data 1 | PA2       | GMAC_TXD1   | 3V3     | IO  | N     |
| GMAC Transmit Data 2 | PB3       | GMAC_TXD2   | 3.3V    | IO  | N     |
| GMAC Transmit Data 3 | PA3       | GMAC_TXD3   | 3.3V    | IO  | N     |
| GMAC Transmit Enable | PA1       | GMAC_TXEN   | 3.3V    | IO  | N     |

The above signals can be reassigned by software to alternate functions; see [Table 29](#) for details.

## GPIO

Table 13. GPIO

| Function     | Ball Loc. | Ball Name | Voltage | I/O | PU/PD <sup>+</sup> |
|--------------|-----------|-----------|---------|-----|--------------------|
| Generic GPIO | PAH2      | AP_GPA0   | 3.3V    | IO  | N                  |
| Generic GPIO | PAL42     | AP_GPA3   | 3.3V    | IO  | N                  |
| Generic GPIO | PB39      | AP_GPA4   | 3.3V    | IO  | N                  |
| Generic GPIO | PB40      | AP_GPA5   | 3.3V    | IO  | N                  |
| Generic GPIO | PAK42     | AP_GPA6   | 3.3V    | IO  | N                  |
| Generic GPIO |           | AP_GPA7   | 3.3V    | IO  | N                  |
| Generic GPIO |           | AP_GPA8   | 3.3V    | IO  | N                  |
| Generic GPIO | PA40      | AP_GPA9   | 3.3V    | IO  | N                  |
| Generic GPIO | PAK41     | AP_GPA10  | 3.3V    | IO  | N                  |
| Generic GPIO | PB42      | AP_GPA11  | 3.3V    | IO  | N                  |
| Generic GPIO | PA42      | AP_GPA12  | 3.3V    | IO  | N                  |
| Generic GPIO | PA37      | AP_GPA13  | 3.3V    | IO  | N                  |
| Generic GPIO | PA39      | AP_GPA14  | 3.3V    | IO  | N                  |
| Generic GPIO | PA41      | AP_GPA15  | 3.3V    | IO  | N                  |
| Generic GPIO | PB41      | AP_GPA16  | 3.3V    | IO  | N                  |
| Generic GPIO | PAL41     | AP_GPA17  | 3.3V    | IO  | N                  |
| Generic GPIO | PAK39     | AP_GPA18  | 3.3V    | IO  | N                  |
| Generic GPIO | PAL40     | AP_GPA19  | 3.3V    | IO  | N                  |
| Generic GPIO | PAK38     | AP_GPA20  | 3.3V    | IO  | N                  |
| Generic GPIO | PAK40     | AP_GPA21  | 3.3V    | IO  | N                  |
| Generic GPIO | PAL39     | AP_GPA22  | 3.3V    | IO  | N                  |
| Generic GPIO | PAG2      | AP_GPA25  | 3.3V    | IO  | N                  |
| Generic GPIO | PAH1      | AP_GPA26  | 3.3V    | IO  | N                  |
| Generic GPIO | PAJ2      | AP_GPA27  | 3.3V    | IO  | N                  |
| Generic GPIO | PAJ2      | AP_GPA28  | 3.3V    | IO  | N                  |
| Generic GPIO | PAK36     | AP_GPB8   | 3.3V    | IO  | N                  |
| Generic GPIO | PAG41     | AP_GPB11  | 3.3V    | IO  | N                  |
| Generic GPIO | PAK37     | AP_GPB14  | 3.3V    | IO  | N                  |

Table 13. GPIO (Continued)

| Function     | Ball Loc. | Ball Name | Voltage | I/O | PU/PD * |
|--------------|-----------|-----------|---------|-----|---------|
| Generic GPIO | PAL37     | AP_GPB16  | 3.3V    | IO  | N       |
| Generic GPIO | PAG42     | AP_GPB18  | 3.3V    | IO  | N       |
| Generic GPIO | PAL36     | AP_GPB22  | 3.3V    | IO  | N       |
| Generic GPIO | PAL38     | AP_GPB23  | 3.3V    | IO  | N       |
| Generic GPIO | PP41      | AP_GPB30  | 3.3V    | IO  | –       |
| Generic GPIO | PAK34     | AP_GPC0   | 3.3V    | IO  | N       |
| Generic GPIO | PAK33     | AP_GPC17  | 3.3V    | IO  | N       |
| Generic GPIO | PAH41     | AP_GPC25  | 3.3V    | IO  | PU      |
| Generic GPIO | PAK35     | AP_GPC26  | 3.3V    | IO  | PU      |
| Generic GPIO | PAL35     | AP_GPC27  | 3.3V    | IO  | PU      |
| Generic GPIO | PAL33     | AP_GPD8   | 3.3V    | IO  | N       |
| Generic GPIO | PAK19     | AP_GPD28  | 3.3V    | IO  | N       |
| Generic GPIO | PAL25     | AP_GPD31  | 3.3V    | IO  | N       |
| Generic GPIO | PAL21     | AP_GPE0   | 3.3V    | IO  | N       |
| Generic GPIO | PAK21     | AP_GPE1   | 3.3V    | IO  | N       |
| Generic GPIO | PAK20     | AP_GPE2   | 3.3V    | IO  | N       |
| Generic GPIO | PAL20     | AP_GPE3   | 3.3V    | IO  | N       |
| Generic GPIO | PAL34     | AP_GPE30  | 3.3V    | IO  | PU      |
| Generic GPIO | PAH42     | AP_GPE31  | 3.3V    | IO  | PU      |

\*. The GPIO lines can be pulled up or down by 100k $\Omega$  internal registers under register control. By default, the pull-ups and pull-downs are disabled. For details about reconfiguring the GPIO lines, refer to the *ARTIK 530/710 System Design Guide*.

The above signals can be reassigned by software to alternate functions; see *Table 29–Table 32* for details.

## HDMI

Table 14. HDMI

| Function                            | Ball Loc. | Ball Name    | Voltage | I/O | PU/PD |
|-------------------------------------|-----------|--------------|---------|-----|-------|
| HDMI Consumer Electronics Control * | PA29      | AP_HDMI_CEC  | 3.3V    | IO  | N     |
| HDMI Hot Plug Detect                | PB29      | AP_HDMI_HPD  | 3.3V    | I   | N     |
| HDMI Transmit Channel 0 Negative    | PA32      | AP_HDMI_TX0N | 1.8V    | O   | N     |
| HDMI Transmit Channel 0 Positive    | PB32      | AP_HDMI_TX0P | 1.8V    | O   | N     |
| HDMI Transmit Channel 1 Negative    | PA31      | AP_HDMI_TX1N | 1.8V    | O   | N     |
| HDMI Transmit Channel 1 Positive    | PB31      | AP_HDMI_TX1P | 1.8V    | O   | N     |
| HDMI Transmit Channel 2 Negative    | PA30      | AP_HDMI_TX2N | 1.8V    | O   | N     |
| HDMI Transmit Channel 2 Positive    | PB30      | AP_HDMI_TX2P | 1.8V    | O   | N     |
| HDMI Transmit Negative Clock        | PA33      | AP_HDMI_TXCN | 1.8V    | O   | N     |
| HDMI Transmit Positive Clock        | PB33      | AP_HDMI_TXCP | 1.8V    | O   | N     |

\*. Alternate GPIO function that can be selected by software but is not selected by hardware at power-on. See *Table 29* for details.

## HSIC

Table 15. HSIC

| Function    | Ball Loc. | Ball Name      | Voltage | I/O | PU/PD |
|-------------|-----------|----------------|---------|-----|-------|
| HSIC Data   | PB38      | AP_HSIC_DATA   | 1.2V    | IO  | N     |
| HSIC Strobe | PA38      | AP_HSIC_STROBE | 1.2V    | IO  | N     |

## I<sup>2</sup>C

Table 16. I<sup>2</sup>C

| Function                    | Ball Loc. | Ball Name             | Voltage | I/O | PU/PD |
|-----------------------------|-----------|-----------------------|---------|-----|-------|
| HDMI I <sup>2</sup> C SCL * | PAK11     | AP_GPA23_HDMI_I2C_SCL | 3.3V    | IO  | N     |
| HDMI I <sup>2</sup> C SDA * | PAL11     | AP_GPA24_HDMI_I2C_SDA | 3.3V    | IO  | N     |
| I <sup>2</sup> C SCL 0 †    | PAK10     | AP_GPD2_SCL0          | 3.3V    | IO  | PU    |
| I <sup>2</sup> C SDA 0 †    | PAL10     | AP_GPD3_SDA0          | 3.3V    | IO  | PU    |
| I <sup>2</sup> C SCL 1 †    | PAK9      | AP_GPD4_SCL1          | 3.3V    | IO  | PU    |
| I <sup>2</sup> C SDA 1 †    | PAL9      | AP_GPD5_SDA1          | 3.3V    | IO  | PU    |
| I <sup>2</sup> C SCL 2 †    | PAK8      | AP_GPD6_SCL2          | 3.3V    | IO  | PU    |
| I <sup>2</sup> C SDA 2 †    | PAL8      | AP_GPD7_SDA2          | 3.3V    | IO  | PU    |

\*. Not selected by default by hardware at power-on. The signal can be reassigned by software. See [Table 30](#) for details.

†. Selected by default by hardware at power on, but can be reassigned to an alternate function by software. See [Table 30](#) for details.

## I<sup>2</sup>S

Table 17. I<sup>2</sup>S

| Function                              | Ball Loc. | Ball Name                | Voltage | I/O | PU/PD |
|---------------------------------------|-----------|--------------------------|---------|-----|-------|
| I <sup>2</sup> S 0 Bit Clock *        | PAK2      | AP_I2S0_BCLK             | 3.3V    | IO  | N     |
| I <sup>2</sup> S 0 Data In *          | PAL1      | AP_I2S0_DIN              | 3.3V    | IO  | N     |
| I <sup>2</sup> S 0 Data Out *         | PAK1      | AP_I2S0_DOUT             | 3.3V    | IO  | N     |
| I <sup>2</sup> S 0 Left Right Clock * | PAJ1      | AP_I2S0_LRCLK            | 3.3V    | IO  | N     |
| I <sup>2</sup> S 0 Master Clock *     | PAL2      | AP_I2S0_MCLK             | 3.3V    | IO  | N     |
| I <sup>2</sup> S 1 Bit Clock †        | PAK27     | AP_GPA30_VID1_0_I2SBCLK1 | 3.3V    | IO  | PU    |
| I <sup>2</sup> S 1 Data In †          | PAL26     | AP_GPB9_I2SDIN1          | 3.3V    | IO  | N     |
| I <sup>2</sup> S 1 Data Out †         | PAL27     | AP_GPB6_VID1_4_I2SDOUT1  | 3.3V    | IO  | PD    |
| I <sup>2</sup> S 1 Left Right Clock † | PAK25     | AP_GPB0_VID1_1_I2SLRCK1  | 3.3V    | IO  | PU    |
| I <sup>2</sup> S 1 Master Clock †     | PAK26     | AP_GPA28_I2SMCLK1        | 3.3V    | IO  | N     |

\*. Selected by default by hardware at power on, but can be reassigned to an alternate function by software. See [Table 30](#) and [Table 31](#) for details.

†. Alternate GPIO function that can be selected by software but is not selected by hardware at power-on. See [Table 30](#) for details.

## JTAG

Table 18. JTAG

| Function   | Ball Loc. | Ball Name | Voltage | I/O | PU/PD |
|------------|-----------|-----------|---------|-----|-------|
| JTAG NTRST | PAE1      | AP_NTRST  | 3.3V    | IO  | PD    |
| JTAG TCK   | PAC1      | AP_TCK    | 3.3V    | IO  | PD    |
| JTAG TDI   | PAD2      | AP_TDI    | 3.3V    | IO  | PU    |
| JTAG TDO   | PAD1      | AP_TDO    | 3.3V    | IO  | N     |
| JTAG TMS   | PAC2      | AP_TMS    | 3.3V    | IO  | PU    |

The above signals can be reassigned by software to alternate functions; see [Table 31](#) for details.

## AliveGPIO

Table 19. Key

| Function                    | Ball Loc. | Ball Name         | Voltage | I/O | PU/PD |
|-----------------------------|-----------|-------------------|---------|-----|-------|
| AliveGPIO 1                 | PAF2      | AP_AGP1           | 3.3V    | IO  | N     |
| AliveGPIO 2                 | PAE2      | AP_AGP2_RTC_INT_N | 3.3V    | IO  | N     |
| Power Key part of AliveGPIO | PAF1      | AP_PWRKEY         | 3.3V    | IO  | N     |
| Reset                       | PAG1      | AP_NRESET         | 3.3V    | I   | N *   |

\*. External 100kΩ pull-up resistor required.

## LVDS

Table 20. LVDS

| Function                         | Ball Loc. | Ball Name     | Voltage | I/O | PU/PD |
|----------------------------------|-----------|---------------|---------|-----|-------|
| LVDS Transmit Channel 0 Negative | PA22      | AP_LVDS_TN0   | 1.8V    | O   | N     |
| LVDS Transmit Channel 0 Positive | PB22      | AP_LVDS_TP0   | 1.8V    | O   | N     |
| LVDS Transmit Channel 1 Negative | PA23      | AP_LVDS_TN1   | 1.8V    | O   | N     |
| LVDS Transmit Channel 1 Positive | PB23      | AP_LVDS_TP1   | 1.8V    | O   | N     |
| LVDS Transmit Channel 2 Negative | PA24      | AP_LVDS_TN2   | 1.8V    | O   | N     |
| LVDS Transmit Channel 2 Positive | PB24      | AP_LVDS_TP2   | 1.8V    | O   | N     |
| LVDS Transmit Channel 3 Negative | PA26      | AP_LVDS_TN3   | 1.8V    | O   | N     |
| LVDS Transmit Channel 3 Positive | PB26      | AP_LVDS_TP3   | 1.8V    | O   | N     |
| LVDS Transmit Channel 4 Negative | PA27      | AP_LVDS_TN4   | 1.8V    | O   | N     |
| LVDS Transmit Channel 4 Positive | PB27      | AP_LVDS_TP4   | 1.8V    | O   | N     |
| LVDS Transmit Negative Clock     | PA25      | AP_LVDS_TNCLK | 1.8V    | O   | N     |
| LVDS Transmit Positive Clock     | PB25      | AP_LVDS_TPCLK | 1.8V    | O   | N     |

## PWM

Table 21. PWM

| Function | Ball Loc. | Ball Name     | Voltage | I/O | PU/PD |
|----------|-----------|---------------|---------|-----|-------|
| PWM 0    | PAL7      | AP_GPD1_PWM0  | 3.3V    | IO  | N     |
| PWM 2    | PAK7      | AP_GPC14_PWM2 | 3.3V    | IO  | N     |

The above signals can be reassigned by software to alternate functions; see [Table 30](#) for details.

## SD/MMC

Table 22. SD/MMC

| Function   | Ball Loc. | Ball Name  | Voltage | I/O | PU/PD |
|------------|-----------|------------|---------|-----|-------|
| SD Clock   | PAK30     | AP_SDO_CLK | 3.3V    | IO  | N     |
| SD Command | PAK28     | AP_SDO_CMD | 3.3V    | IO  | N     |
| SD Data 0  | PAL30     | AP_SDO_D0  | 3.3V    | IO  | N     |
| SD Data 1  | PAK29     | AP_SDO_D1  | 3.3V    | IO  | N     |
| SD Data 2  | PAL29     | AP_SDO_D2  | 3.3V    | IO  | N     |
| SD Data 3  | PAL28     | AP_SDO_D3  | 3.3V    | IO  | N     |

The above signals can be reassigned by software to alternate functions; see [Table 30](#) for details.

## SPI

Table 23. SPI

| Function              | Ball Loc. | Ball Name          | Voltage | I/O | PU/PD |
|-----------------------|-----------|--------------------|---------|-----|-------|
| SPI 0 Clock *         | PAK6      | AP_SPIO_CLK        | 3.3V    | IO  | N     |
| SPI 0 Frame *         | PAL6      | AP_SPIO_CS         | 3.3V    | IO  | N     |
| SPI 0 Receive Data *  | PAK5      | AP_SPIO_MISO       | 3.3V    | IO  | N     |
| SPI 0 Transmit Data * | PAL5      | AP_SPIO_MOSI       | 3.3V    | IO  | N     |
| SPI 2 Clock †         | PAK4      | AP_GPC9_SPI2_CLK   | 3.3V    | IO  | N     |
| SPI 2 Frame           | PAL4      | AP_GPC10_SPI2_CS   | 3.3V    | IO  | PU    |
| SPI 2 Receive Data    | PAK3      | AP_GPC11_SPI2_MISO | 3.3V    | IO  | N     |
| SPI 2 Transmit Data   | PAL3      | AP_GPC12_SPI2_MOSI | 3.3V    | IO  | N     |

\*. Alternate GPIO function that can be reassigned by software but is not selected by hardware at power-on; see [Table 30](#) for details.

†. Selected by default by hardware at power on, but can be reassigned to an alternate function by software. See [Table 30](#) for details.

## UART

Table 24. UART

| Function             | Ball Loc. | Ball Name   | Voltage | I/O | PU/PD |
|----------------------|-----------|-------------|---------|-----|-------|
| UART 0 Receive Data  | PAL24     | AP_UART_RX0 | 3.3V    | IO  | N     |
| UART 0 Transmit Data | PAK24     | AP_UART_TX0 | 3.3V    | IO  | N     |
| UART 3 Receive Data  | PAL22     | AP_UART_RX3 | 3.3V    | IO  | N     |
| UART 3 Transmit Data | PAK22     | AP_UART_TX3 | 3.3V    | IO  | N     |
| UART 4 Receive Data  | PAL23     | AP_UART_RX4 | 3.3V    | IO  | N     |
| UART 4 Transmit Data | PAK23     | AP_UART_TX4 | 3.3V    | IO  | N     |

The above signals can be reassigned by software to alternate functions; see [Table 30](#) for details.

## USB HOST/USB OTG

Table 25. USB Host/USB OTG

| Function            | Ball Loc. | Ball Name  | Voltage | I/O | PU/PD |
|---------------------|-----------|------------|---------|-----|-------|
| USB Host Data Minus | PA36      | AP_USBH_DM | 3.3V    | IO  | N     |
| USB Host Data Plus  | PB36      | AP_USBH_DP | 3.3V    | IO  | N     |
| USB OTG ID          | PB37      | AP_OTG_ID  | –       | I   | N     |
| USB OTG Data Minus  | PA35      | AP_OTG_DM  | 3.3V    | IO  | N     |
| USB OTG Data Plus   | PB35      | AP_OTG_DP  | 3.3V    | IO  | N     |

## 802.15.4 for Zigbee

Table 26. 802.15.4

| Function                                          | Ball Loc. | Ball Name              | Voltage | I/O | PU/PD |
|---------------------------------------------------|-----------|------------------------|---------|-----|-------|
| 802.15.4 JTAG Test Clock                          | PAK14     | ZB_DEBUG_TCK_SWCLK     | 3.3V    | –   | –     |
| 802.15.4 Frame Control                            | PAK13     | ZB_PTI_DATA_FRC_DOUT   | 3.3V    | –   | –     |
| 802.15.4 Debug Serial Wire I/O & Test Mode Select | PAL12     | ZB_DEBUG_TMS_SWDIO     | 3.3V    | –   | –     |
| 802.15.4 Debug Serial Wire Viewer Out             | PAL13     | ZB_PTI_SYNC_FRC_DFRAME | 3.3V    | –   | –     |
| 802.15.4 JTAG Test Data Out                       | PAK12     | ZB_DEBUG_TDO_SWO       | 3.3V    | –   | –     |
| 802.15.4 Reset                                    | PAL14     | PAD_ZB_RSTn            | 3.3V    | O   | N     |
| 802.15.4 UART                                     | PAK15     | COMBO_ZIG_UART_TXD     | 3.3V    | IO  | –     |
| 802.15.4 UART *                                   | PAL15     | COMBO_ZIG_UART_RXD     | 3.3V    | IO  | PU    |

\*. For internal use only.



## Miscellaneous

Table 27. Miscellaneous

| Function     | Ball Loc. | Ball Name   | Voltage | I/O | PU/PD |
|--------------|-----------|-------------|---------|-----|-------|
| VDD Power On | PAL19     | AP_VDDPWRON | 3.3V    | O   | N     |

## Power

Table 28. Power

| Function                     | Ball Loc.                                                       | Ball Name      | Voltage  | I/O | PU/PD |
|------------------------------|-----------------------------------------------------------------|----------------|----------|-----|-------|
| RTC LDO                      | PE42                                                            | RTCLDO_OUT     | ?        | O   | –     |
| 3.3V System Power            | PAK[17,18]<br>PAL[17,18]                                        | VCC3P3_SYS*    | 3.3V     | O   | –     |
| USB2.0 OTG Bus Power         | PD[41,42]                                                       | VCC5P0_OTGVBUS | 5.0V     | I   | –     |
| Main Power Supply for Module | PV[41,42]<br>PW[41,42]<br>PY[41,42]<br>PAA[41,42]<br>PAB[41,42] | VIN            | 3.7–5.0V | I   | –     |

\*. VCC3P3\_SYS pads are not recommended as a current source; do not use them to drive external ICs. VCC3P3\_SYS pads turn off when the ARTIK 530/530s Module goes into sleep mode.

## GPIO ALTERNATE FUNCTIONS

A number of the GPIOs can be programmed to have alternate functions beyond their default behavior using the GPIO API provided in the SW development environment. *Table 29–Table 32* provide the alternate functions of all the GPIOs that are available on the PADS of the ARTIK 530/530s Module that can be user programmed.



In the following tables, the hardware power-up default functions are shown emboldened. Software may subsequently select an alternate function.

Table 29. GPIO Alternate Functions—North Part

| Ball Loc. | Ball Name   | Function 0     | Function 1         | Function 2 | Function 3 | Group |
|-----------|-------------|----------------|--------------------|------------|------------|-------|
| PA1       | GMAC_TXEN   | GPIOE11        | <b>GMAC_TXEN</b>   | –          | –          | GMAC  |
| PA2       | GMAC_TXD1   | GPIOE8         | <b>GMAC_TXD1</b>   | –          | –          | GMAC  |
| PA3       | GMAC_TXD3   | GPIOE10        | <b>GMAC_TXD3</b>   | –          | –          | GMAC  |
| PA5       | GMAC_GTXCLK | GPIOE24        | <b>GMAC_GTXCLK</b> | –          | –          | GMAC  |
| PA6       | GMAC_RXDV   | GPIOE19        | <b>GMAC_RXDV</b>   | SPITXD1    | –          | GMAC  |
| PA7       | GMAC_RXD2   | GPIOE16        | <b>GMAC_RXD2</b>   | –          | –          | GMAC  |
| PA8       | GMAC_RXD0   | GPIOE14        | <b>GMAC_RXD0</b>   | SPICLK1    | –          | GMAC  |
| PA29      | AP_HDMI_CEC | <b>SA3</b>     | GPIOC3             | HDMI_CEC   | SDnRST0    | HDMI  |
| PA37      | AP_GPA13    | <b>GPIOA13</b> | DISD12             | –          | –          | GPIO  |
| PA39      | AP_GPA14    | <b>GPIOA14</b> | DISD13             | –          | –          | GPIO  |
| PA40      | AP_GPA9     | <b>GPIOA9</b>  | DISD8              | –          | –          | GPIO  |
| PA41      | AP_GPA15    | <b>GPIOA15</b> | DISD14             | –          | –          | GPIO  |
| PA42      | AP_GPA12    | <b>GPIOA12</b> | DISD11             | –          | –          | GPIO  |
| PB2       | GMAC_TXD0   | GPIOE7         | <b>GMAC_TXD0</b>   | VIVSYNC1   | –          | GMAC  |
| PB3       | GMAC_TXD2   | GPIOE9         | <b>GMAC_TXD2</b>   | –          | –          | GMAC  |
| PB4       | GMAC_MDC    | GPIOE20        | <b>GMAC_MDC</b>    | –          | –          | GMAC  |
| PB5       | GMAC_RXCLK  | GPIOE18        | <b>GMAC_RXCLK</b>  | SPIRXD1    | –          | GMAC  |
| PB6       | GMAC_RXD3   | GPIOE17        | <b>GMAC_RXD3</b>   | –          | –          | GMAC  |
| PB7       | GMAC_RXD1   | GPIOE15        | <b>GMAC_RXD1</b>   | SPIFRM1    | –          | GMAC  |
| PB8       | GMAC_MDIO   | GPIOE21        | <b>GMAC_MDIO</b>   | –          | –          | GMAC  |
| PB39      | AP_GPA4     | <b>GPIOA4</b>  | DISD3              | –          | –          | GPIO  |
| PB40      | AP_GPA5     | <b>GPIOA5</b>  | DISD4              | –          | –          | GPIO  |
| PB41      | AP_GPA16    | <b>GPIOA16</b> | DISD15             | –          | –          | GPIO  |
| PB42      | AP_GPA11    | <b>GPIOA11</b> | DISD10             | –          | –          | GPIO  |

Table 30. GPIO Alternate Functions—South Part

| Ball Loc. | Ball Name                | Function 0     | Function 1      | Function 2     | Function 3         | Group            |
|-----------|--------------------------|----------------|-----------------|----------------|--------------------|------------------|
| PAK1      | AP_I2SO_DOUT             | GPIOD9         | <b>I2SDOUT0</b> | AC97_DOUT      | –                  | I2SO             |
| PAK2      | AP_I2SO_BCLK             | GPIOD10        | <b>I2SBCLK0</b> | AC97_BCLK      | –                  | I2SO             |
| PAK3      | AP_GPC11_SPI2_MISO       | SA11           | GPIOC11         | <b>SPIRXD2</b> | USB2.0OTG_DrvV BUS | SPI2             |
| PAK4      | AP_GPC9_SPI2_CLK         | SA9            | GPIOC9          | <b>SPICLK2</b> | –                  | SPI2             |
| PAK5      | AP_SPIO_MISO             | <b>GPIOD0</b>  | SPIRXD0         | PWM3           | –                  | SPIO             |
| PAK6      | AP_SPIO_CLK              | <b>GPIOC29</b> | SPICLK0         | –              | –                  | SPIO             |
| PAK7      | AP_GPC14_PWM2            | SA14           | GPIOC14         | <b>PWM2</b>    | VICLK2             | PWM              |
| PAK8      | AP_GPD6_SCL2             | GPIOD6         | <b>SCL2</b>     | –              | –                  | I <sup>2</sup> C |
| PAK9      | AP_GPD4_SCL1             | GPIOD4         | <b>SCL1</b>     | –              | –                  | I <sup>2</sup> C |
| PAK10     | AP_GPD2_SCL0             | GPIOD2         | <b>SCLO</b>     | ISO7816        | –                  | I <sup>2</sup> C |
| PAK11     | AP_GPA23_HDMI_I2C_SCL    | <b>GPIOA23</b> | DISD22          | –              | –                  | I <sup>2</sup> C |
| PAK19     | AP_GPD28                 | <b>GPIOD28</b> | VID0_0          | TSIDATA1_0     | SA24               | GPIO             |
| PAK20     | AP_GPE2                  | <b>GPIOE2</b>  | VID0_6          | TSIDATA1_6     | –                  | GPIO             |
| PAK21     | AP_GPE1                  | <b>GPIOE1</b>  | VID0_5          | TSIDATA1_5     | –                  | GPIO             |
| PAK22     | AP_UART_TX3              | GPIOD21        | <b>UARTTXD3</b> | SDnCD1         | –                  | UART             |
| PAK23     | AP_UART_TX4              | SD13           | GPIOB29         | TSIDATA0_5     | <b>UARTTXD4</b>    | UART             |
| PAK24     | AP_UART_TX0              | <b>GPIOD18</b> | UARTTXD0        | ISO7816        | SDWP2              | UART             |
| PAK25     | AP_GPB0_VID1_1_I2SLRCK1  | <b>GPIOB0</b>  | VID1_1          | SDEX1          | I2SLRCLK1          | I2S1             |
| PAK26     | AP_GPA28_I2SMCLK1        | <b>GPIOA28</b> | VICLK1          | I2SMCLK2       | I2SMCLK1           | I2S1             |
| PAK27     | AP_GPA30_VID1_0_I2SBCLK1 | <b>GPIOA30</b> | VID1_0          | SDEX0          | I2SBCLK1           | I2S1             |
| PAK28     | AP_SDO_CMD               | GPIOA31        | <b>SDCMD0</b>   | –              | –                  | SD/MMC           |
| PAK29     | AP_SDO_D1                | GPIOB3         | <b>SDDATO_1</b> | –              | –                  | SD/MMC           |
| PAK30     | AP_SDO_CLK               | GPIOA29        | <b>SDCLK0</b>   | –              | –                  | SD/MMC           |
| PAK32     | AP_GPB13_SDO_BOOT        | <b>SD0</b>     | GPIOB13         | –              | –                  | BOOTING          |
| PAK33     | AP_GPC17                 | SA17           | <b>GPIOC17</b>  | TSIDP0         | VID2_0             | GPIO             |
| PAK34     | AP_GPC0                  | SA0            | <b>GPIOC0</b>   | TSERRO         | –                  | GPIO             |
| PAK35     | AP_GPC26                 | RDNWR          | <b>GPIOC26</b>  | –              | –                  | GPIO             |
| PAK36     | AP_GPB8                  | <b>GPIOB8</b>  | VID1_5          | SDEX5          | I2SDOUT2           | GPIO             |
| PAK37     | AP_GPB14                 | RnB0           | RnB1            | <b>GPIOB14</b> | –                  | GPIO             |
| PAK38     | AP_GPA20                 | <b>GPIOA20</b> | DISD19          | –              | –                  | GPIO             |
| PAK39     | AP_GPA18                 | <b>GPIOA18</b> | DISD17          | –              | –                  | GPIO             |
| PAK40     | AP_GPA21                 | <b>GPIOA21</b> | DISD20          | –              | –                  | GPIO             |
| PAK41     | AP_GPA10                 | <b>GPIOA10</b> | DISD9           | –              | –                  | GPIO             |
| PAK42     | AP_GPA6                  | <b>GPIOA6</b>  | DISD5           | –              | –                  | GPIO             |
| PAL1      | AP_I2SO_DIN              | GPIOD11        | <b>I2SDINO</b>  | AC97_DIN       | –                  | I2SO             |
| PAL2      | AP_I2SO_MCLK             | GPIOD13        | <b>I2SMCLK0</b> | AC97_nRST      | –                  | I2SO             |
| PAL3      | AP_GPC12_SPI2_MOSI       | SA12           | GPIOC12         | <b>SPITXD2</b> | SDnRST2            | SPI2             |
| PAL4      | AP_GPC10_SPI2_CS         | SA10           | GPIOC10         | <b>SPIFRM2</b> | –                  | SPI2             |
| PAL5      | AP_SPIO_MOSI             | <b>GPIOC31</b> | SPITXD0         | –              | –                  | SPIO             |
| PAL6      | AP_SPIO_CS               | <b>GPIOC30</b> | SPIFRM0         | –              | –                  | SPIO             |
| PAL7      | AP_GPD1_PWM0             | GPIOD1         | <b>PWM0</b>     | SA25           | –                  | PWM              |

Table 30. GPIO Alternate Functions—South Part (Continued)

| Ball Loc. | Ball Name               | Function 0     | Function 1      | Function 2     | Function 3      | Group            |
|-----------|-------------------------|----------------|-----------------|----------------|-----------------|------------------|
| PAL8      | AP_GPD7_SDA2            | GPIOD7         | <b>SDA2</b>     | –              | –               | I <sup>2</sup> C |
| PAL9      | AP_GPD5_SDA1            | GPIOD5         | <b>SDA1</b>     | –              | –               | I <sup>2</sup> C |
| PAL10     | AP_GPD3_SDA0            | GPIOD3         | <b>SDA0</b>     | ISO7816        | –               | I <sup>2</sup> C |
| PAL11     | AP_GPA24_HDMI_I2C_SDA   | <b>GPIOA24</b> | DISD23          | –              | –               | I <sup>2</sup> C |
| PAL20     | AP_GPE3                 | <b>GPIOE3</b>  | VID0_7          | TSIDATA1_7     | –               | GPIO             |
| PAL21     | AP_GPE0                 | <b>GPIOE0</b>  | VID0_4          | TSIDATA1_4     | –               | GPIO             |
| PAL22     | AP_UART_RX3             | GPIOD17        | <b>UARTRXD3</b> | –              | –               | UART             |
| PAL23     | AP_UART_RX4             | SD12           | GPIOB28         | TSIDATA0_4     | <b>UARTRXD4</b> | UART             |
| PAL24     | AP_UART_RX0             | <b>GPIOD14</b> | UARTRXD0        | ISO7816        | –               | UART             |
| PAL25     | AP_GPD31                | <b>GPIOD31</b> | VID0_3          | TSIDATA1_3     | –               | GPIO             |
| PAL26     | AP_GPB9_I2SDIN1         | <b>GPIOB9</b>  | VID1_6          | SDEX6          | I2SDIN1         | I2S1             |
| PAL27     | AP_GPB6_VID1_4_I2SDOUT1 | <b>GPIOB6</b>  | VID1_4          | SDEX4          | I2SDOUT1        | I2S1             |
| PAL28     | AP_SDO_D3               | GPIOB7         | <b>SDDATO_3</b> | –              | –               | SD/MMC           |
| PAL29     | AP_SDO_D2               | GPIOB5         | <b>SDDATO_2</b> | –              | –               | SD/MMC           |
| PAL30     | AP_SDO_D0               | GPIOB1         | <b>SDDATO_0</b> | –              | –               | SD/MMC           |
| PAL31     | AP_GPB4_VID1_3_BOOT     | GPIOB4         | <b>VID1_3</b>   | SDEX3          | I2SLRCLK2       | BOOTING          |
| PAL32     | AP_GPB15_SD1_BOOT       | <b>SD1</b>     | GPIOB15         | –              | –               | BOOTING          |
| PAL33     | AP_GPD8                 | <b>GPIOD8</b>  | PPM             | –              | –               | GPIO             |
| PAL34     | AP_GPE30                | NSOE           | <b>GPIOE30</b>  | –              | –               | GPIO             |
| PAL35     | AP_GPC27                | NSDQM          | <b>GPIOC27</b>  | –              | –               | GPIO             |
| PAL36     | AP_GPB22                | SD6            | <b>GPIOB22</b>  | –              | –               | GPIO             |
| PAL37     | AP_GPB16                | NNFOE0         | NNFOE1          | <b>GPIOB16</b> | –               | GPIO             |
| PAL38     | AP_GPB23                | SD7            | <b>GPIOB23</b>  | –              | –               | GPIO             |
| PAL39     | AP_GPA22                | <b>GPIOA22</b> | DISD21          | –              | –               | GPIO             |
| PAL40     | AP_GPA19                | <b>GPIOA19</b> | DISD18          | –              | –               | GPIO             |
| PAL41     | AP_GPA17                | <b>GPIOA17</b> | DISD16          | –              | –               | GPIO             |
| PAL42     | AP_GPA3                 | <b>GPIOA3</b>  | DISD2           | –              | –               | GPIO             |

Table 31. GPIO Alternate Functions—East Part

| Ball Loc. | Ball Name     | Function 0     | Function 1       | Function 2 | Function 3 | Group |
|-----------|---------------|----------------|------------------|------------|------------|-------|
| PAC1      | AP_TCK        | <b>TCLK</b>    | GPIOE28          | –          | –          | JTAG  |
| PAC2      | AP_TMS        | <b>TMS</b>     | GPIOE26          | –          | –          | JTAG  |
| PAD1      | AP_TDO        | <b>TDO</b>     | GPIOE29          | –          | –          | JTAG  |
| PAD2      | AP_TDI        | <b>TDI</b>     | GPIOE27          | –          | –          | JTAG  |
| PAE1      | AP_NTRST      | <b>NTRST</b>   | GPIOE25          | –          | –          | JTAG  |
| PAG2      | AP_GPA25      | <b>GPIOA25</b> | DISVSYNC         | –          | –          | GPIO  |
| PAH1      | AP_GPA26      | <b>GPIOA26</b> | DISHSYNC         | –          | –          | GPIO  |
| PAH2      | AP_GPA0       | <b>GPIOA0</b>  | DISCLK           | –          | –          | GPIO  |
| PAJ1      | AP_I2S0_LRCLK | GPIOD12        | <b>I2SLRCLKO</b> | AC97_SYNC  | –          | I2S0  |
| PAJ2      | AP_GPA27      | <b>GPIOA27</b> | DISDE            | –          | –          | GPIO  |

Table 32. GPIO Alternate Functions—West Part

| Ball Loc. | Ball Name  | Function 0  | Function 1     | Function 2     | Function 3 | Group |
|-----------|------------|-------------|----------------|----------------|------------|-------|
| PP41      | AP_GPIOB30 | SD14        | <b>GPIOB30</b> | TSIDATA0_6     | –          | GPIO  |
| PAG41     | AP_GPB11   | <b>CLE0</b> | CLE1           | GPIOB11        | –          | GPIO  |
| PAG42     | AP_GPB18   | NNFWEO      | nNFW1          | <b>GPIOB18</b> | –          | GPIO  |
| PAH41     | AP_GPC25   | NSWAIT      | <b>GPIOC25</b> | SPDIFTX        | –          | GPIO  |
| PAH42     | AP_GPE31   | NSWE        | <b>GPIOE31</b> | –              | –          | GPIO  |

**NOTE**

All functions on the West Part are dedicated; there are no applicable alternate functions.

## BOOTING SELECTION

The ARTIK 530/530s Module supports a variety of booting scenarios as depicted in [Table 33](#). The table describes the values of the boot-configuration pad signals needed to initiate the booting scenarios. When nothing is done, the default booting scenario is Configuration Option 1. In this case, the primary booting device is eMMC. If the primary booting device fails, the secondary booting device (SD0) will attempt to boot the module. If the secondary booting device fails, the tertiary booting device will boot the module.

Table 33. Boot Selection Configuration

| Config.<br>Option | Boot Configuration Signals * |                       |                         | Primary<br>Booting<br>Device | Secondary<br>Booting<br>Device | Tertiary<br>Booting<br>Device |
|-------------------|------------------------------|-----------------------|-------------------------|------------------------------|--------------------------------|-------------------------------|
|                   | AP_GPB13_<br>SD0_BOOT        | AP_GPB15_<br>SD1_BOOT | AP_GPB4_<br>VID1_3_BOOT |                              |                                |                               |
| 1                 | High                         | Low                   | High                    | eMMC                         | SD0                            | USB OTG Device                |
| 2                 | High                         | Low                   | Low                     | SD0                          | USB OTG Device                 | –                             |
| 3                 | Low                          | High                  | X                       | USB OTG Device               | –                              | –                             |

\*. Internal pull-up and pull-down resistors automatically select Config Option 1 by default. External pull-up and pull-down resistors are required to select configuration options 2 and 3. The recommended resistor value is 10kΩ.

POWER SEQUENCE

Figure 4 below shows the ARTIK 530/530s Module Power-On Sequence (Timing).

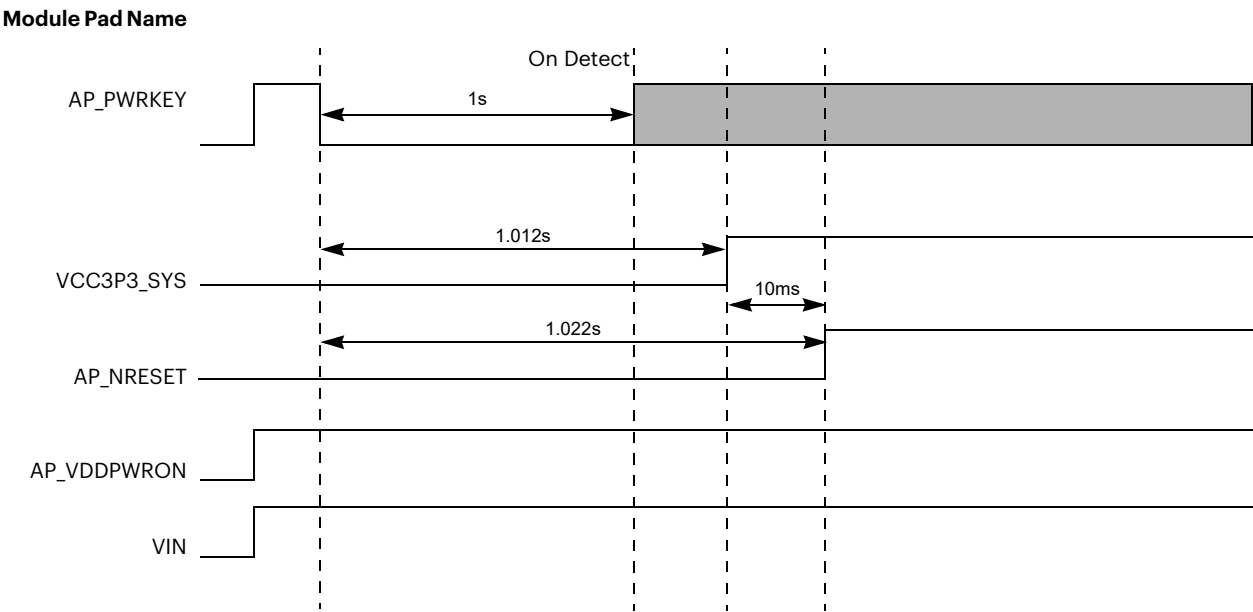
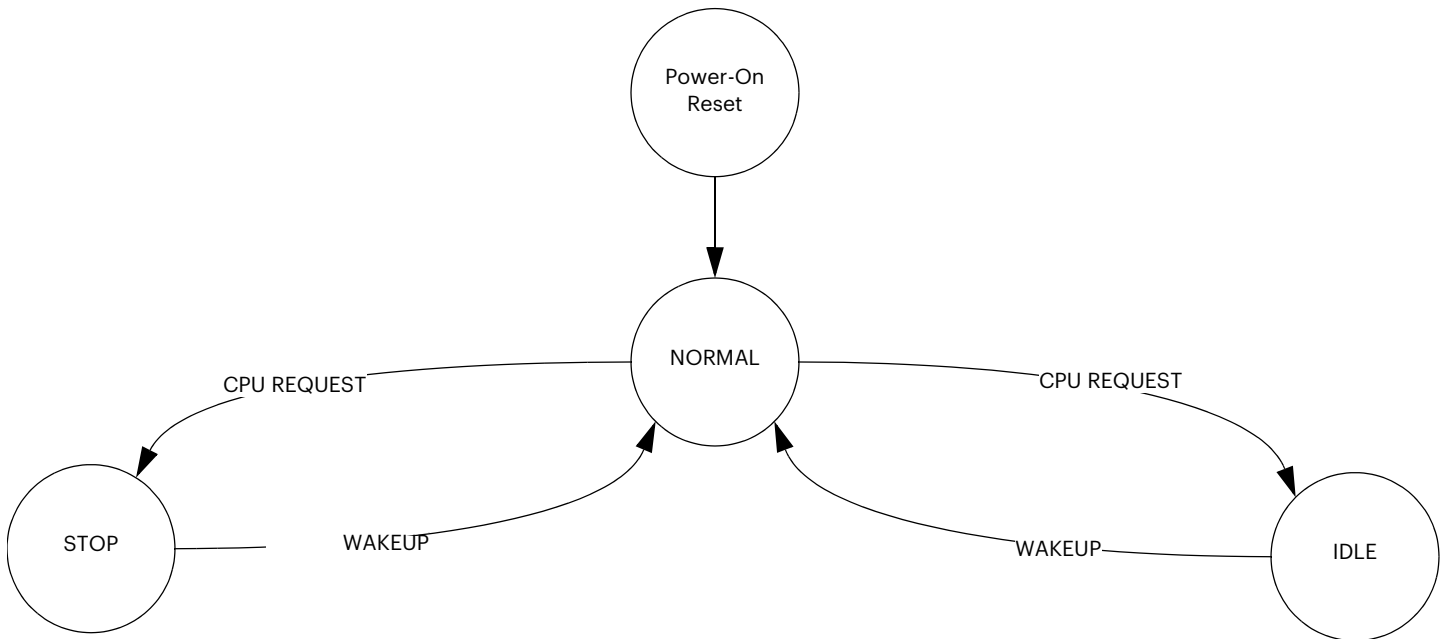


Figure 4. ARTIK 530/530s Module Power-On Sequence (Timing) Diagram

## POWER STATES

*Figure 5* shows the Power Management state diagram. In this diagram, the entry and WAKEUP conditions for each power down mode are given.



*Figure 5. ARTIK 530/530s Module Power Management State Diagram*

The following Modes of operation can be distinguished:

- **NORMAL Mode**
  - Everything is running, this is the normal mode of operation when applications are executed on the ARM cores
- **IDLE Mode**
  - CPU clocks are turned off
  - IDLE state can be initiated by CPU using Software API
  - The following WAKEUP sources can be used to return to NORMAL Mode:
    - GPIO Interrupt, RTC Interrupt, AliveGPIO Interrupt (see PAE2, PAF:[1,2]), External IRQ
- **STOP Mode**
  - PLLs are turned off, DRAM goes into self-refresh
  - STOP state can be initiated by CPU using Software API
  - Certain WAKEUP sources can be used to transition to NORMAL Mode
  - The following WAKEUP sources can be used to return to NORMAL Mode:
    - RTC Interrupt, AliveGPIO Interrupt

For more information on how to access discussed WAKEUP mechanisms like AliveGPIO interrupts, GPIO Interrupts, RTC Interrupts and External Interrupts, refer to the Software User Guide.



## ANTENNA CONNECTIONS

Two antennas are required to use the full set of radio communication links on the ARTIK 530/530s Module. One supports the combination of Wi-Fi/Bluetooth, and the other is dedicated to Zigbee.

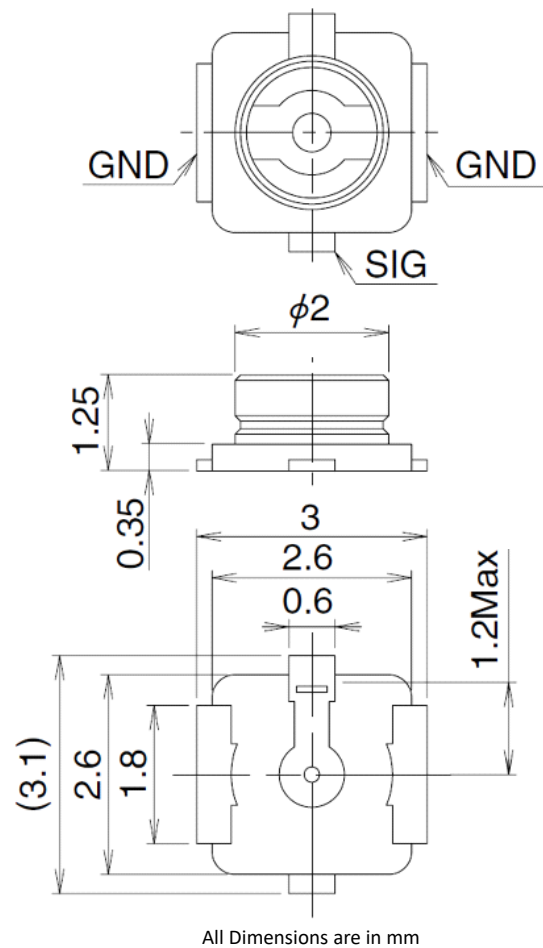


Figure 6. RF Connector for Bluetooth/Wi-Fi and Zigbee

The U.FL-R-SMT Hirose connector is used for both the Bluetooth/Wi-Fi and the Zigbee antenna connectors on the ARTIK 530/530s Module.

The mechanical size of the connector (receptacle) is described in [Figure 6](#). For suggestions on mating the plug and more details on the connector, contact Hirose Electric Co., LTD.

## ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings

The ratings given in this section are associated only with stress. It does not imply any functional operation of the device. Exposure to the absolute-maximum rated conditions for long duration affects the reliability of the device.

Table 34. Absolute Maximum Ratings

| Parameter               | Symbol                                                                                                                                                                                                                                                                                                                                                                              | Condition              | Min  | Max | Units |
|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|------|-----|-------|
| Main power supply       | VIN                                                                                                                                                                                                                                                                                                                                                                                 | –                      | –0.3 | 6.0 | V     |
| DC input/output voltage | PA:[1,2,3,5,6,7,8,29,37,39,40,41,42]<br>PB:[2,3,4,5,6,7,8,39,40,41,42]<br>PAK:[1,2,3,4,5,6,7,8,9,10,11,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,37,38,39,40,41,42]<br>PAL:[1,2,3,4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42]<br>PP:[41]<br>PAC:[1,2]<br>PAD:[1,2]<br>PAE:[1]<br>PAG:[2,41,42]<br>PAH:[1,2,41,42]<br>PAJ:[1,2] | 3.3V Buffer            | –0.5 | 3.8 | V     |
|                         | PAK:[12,13,14]<br>PAL:[12,13]                                                                                                                                                                                                                                                                                                                                                       | 5V Tolerant buffer     | –0.3 | 5.3 |       |
|                         | PAK:[15]<br>PAL:[15]                                                                                                                                                                                                                                                                                                                                                                | Non 5V Tolerant Buffer | –0.3 | 3.6 |       |
|                         | PAL:[19]<br>PAF:[1]<br>PAG:[1]                                                                                                                                                                                                                                                                                                                                                      | –                      | –0.3 | 3.8 |       |
|                         | PAL:[14]                                                                                                                                                                                                                                                                                                                                                                            | Voltage at Pin         | –0.5 | 3.8 | V     |
| DC Input/output current | PA:[1,2,3,5,6,7,8,29,37,39,40,41,42]<br>PB:[2,3,4,5,6,7,8,39,40,41,42]<br>PAK:[1,2,3,4,5,6,7,8,9,10,11,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,37,38,39,40,41,42]<br>PAL:[1,2,3,4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42]<br>PP:[41]<br>PAC:[1,2]<br>PAD:[1,2]<br>PAE:[1]<br>PAG:[2,41,42]<br>PAH:[1,2,41,42]<br>PAJ:[1,2] | –                      | –20  | 20  | mA    |
|                         | PAK:[12,13,14,15]<br>PAL:[12,13]                                                                                                                                                                                                                                                                                                                                                    | –                      | –50  | 50  | mA    |
|                         | PAL:[14]                                                                                                                                                                                                                                                                                                                                                                            | Current at Pin         | –1   | 1   | mA    |

## Power Supply Operating Voltage Range

Table 35. Power Supply Operating Voltage Range

| Parameter         | Symbol                                                       | Min | Typ | Max | Units |
|-------------------|--------------------------------------------------------------|-----|-----|-----|-------|
| Main Power Supply | VIN PV:[42,43],PW:[42,43],PY:[42,43],PAA:[42,43],PAB:[42,43] | 3.7 | 4.2 | 5.0 | V     |

## Power/Current Consumption

The values in this table are nominal. Measurements were taken on sample boards at room temperature using a 4.2V system power supply.

Table 36. ARTIK 530/530s Module Power/Current Consumption

| No. | Category     | Scenario                         |                 | I (mA) | Peak/Typ | Condition                                              |
|-----|--------------|----------------------------------|-----------------|--------|----------|--------------------------------------------------------|
| 1   | Boot         | AP boot                          |                 | 700    | Peak     | Peek current during boot-up                            |
|     |              |                                  |                 | 450    | Typ      | Average current during boot-up                         |
| 2   | Idle         | Idle                             |                 | 140    | Typ      | Idle current                                           |
| 3   | Sleep        | Sleep                            |                 | 20     | Typ      | Sleep current                                          |
| 4   | Storage      | Large file transfer              | eMMC to SD Card | 230    | Typ      | Copying 512MB test file from eMMC to SD                |
| 5   |              |                                  | SD Card to eMMC | 270    | Typ      | Copying 512MB test file from SD to eMMC                |
| 6   | Connectivity | Bluetooth                        | Transmit        | 170    | Typ      | Transfer test file using obexftp from the device       |
| 7   |              |                                  | Receive         | 160    | Typ      | Receive test file using obexftp from the Android phone |
| 8   |              | Wi-Fi                            | Transmit        | 430    | Typ      | Transfer packet using iperf3 (802.11n)                 |
| 9   |              |                                  | Receive         | 320    | Typ      | Receive packet using iperf3 (802.11n)                  |
| 10  |              | 802.15.4 for Zigbee              | Transmit        | 150    | Typ      | Transfer packet using ember tool                       |
| 11  |              |                                  | Receive         | 150    | Typ      | Receive packet using ember tool                        |
| 12  | Multimedia   | Audio play                       |                 | 150    | Typ      | Playback audio file using mplayer (pcm, 2ch, 48000Hz)  |
| 13  |              | Recode audio                     |                 | 140    | Typ      | Record audio using arecord (pcm, 2ch, 48000Hz)         |
| 14  |              | Display picture                  |                 | 180    | Typ      | Display picture (R/G/B, 720*1280)                      |
| 15  |              | Display video                    |                 | 330    | Typ      | Playback movie clip (big_buck_bunny_720p_50mb)         |
| 16  |              | Record video                     |                 | 300    | Typ      | Record video using ffmpeg (1280*720, 3072k)            |
| 17  |              | Live streaming from Camera       |                 | 310    | Typ      | Camera preview using ffmpeg (1280x960)                 |
| 18  |              | Live streaming over Wi-Fi        |                 | 320    | Typ      | Streaming video using ffserver/ffmpeg (640*480)        |
| 19  | CPU Load     | Running one core at 100% load    |                 | 240    | Typ      | Running while() loop                                   |
|     |              | Running two cores at 100% load   |                 | 320    |          |                                                        |
|     |              | Running three cores at 100% load |                 | 400    |          |                                                        |
|     |              | Running all cores at 100% load   |                 | 480    |          |                                                        |

## DC Electrical Characteristics

The DC characteristics for the GPIO pins of the ARTIK 530/530s Module are listed in [Table 37](#). Use the parameters from [Table 37](#) to determine maximum DC loading and to determine maximum transition times for a given load.

Table 37. I/O DC Electrical Characteristics GPIO

| GPIO Ball Coordinates                                                                                                                                                                                                                                                                                                                                                               | Parameter        |                                            | Condition *                                       |                                     | Min  | Typ | Max  | Units |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|--------------------------------------------|---------------------------------------------------|-------------------------------------|------|-----|------|-------|
| PA:[1,2,3,5,6,7,8,29,37,39,40,41,42]<br>PB:[2,3,4,5,6,7,8,39,40,41,42]<br>PAK:[1,2,3,4,5,6,7,8,9,10,11,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,37,38,39,40,41,42]<br>PAL:[1,2,3,4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42]<br>PP:[41]<br>PAC:[1,2]<br>PAD:[1,2]<br>PAE:[1]<br>PAG:[2,41,42]<br>PAH:[1,2,41,42]<br>PAJ:[1,2] | V <sub>TOL</sub> | Tolerant external voltage                  | V <sub>DD</sub> Power Off & On                    |                                     | –    | –   | 3.60 | V     |
|                                                                                                                                                                                                                                                                                                                                                                                     | V <sub>IH</sub>  | High Level Input Voltage<br>CMOS Interface | –                                                 |                                     | 2.31 | –   | 3.60 | V     |
|                                                                                                                                                                                                                                                                                                                                                                                     | V <sub>IL</sub>  | Low Level Input Voltage<br>CMOS Interface  | V <sub>DD</sub> = 3.3V ± 10%                      |                                     | –0.3 | –   | 0.70 | V     |
|                                                                                                                                                                                                                                                                                                                                                                                     | ΔV               | Hysteresis Voltage                         | –                                                 |                                     | 0.15 | –   |      | V     |
|                                                                                                                                                                                                                                                                                                                                                                                     | I <sub>IH</sub>  | High Level Input Current                   |                                                   |                                     |      |     |      |       |
|                                                                                                                                                                                                                                                                                                                                                                                     |                  | Input Buffer                               | V <sub>IN</sub> = V <sub>DD</sub>                 | V <sub>DD</sub> Power On            | –3   | –   | 3    | μA    |
|                                                                                                                                                                                                                                                                                                                                                                                     |                  |                                            |                                                   | V <sub>DD</sub> Power Off & SNS = 0 | –5   | –   | 5    |       |
|                                                                                                                                                                                                                                                                                                                                                                                     |                  | Input Buffer with pull-down                | V <sub>IN</sub> = V <sub>DD</sub>                 | V <sub>DD</sub> = 3.3V ± 10%        | 15   | 40  | 80   |       |
|                                                                                                                                                                                                                                                                                                                                                                                     | I <sub>IL</sub>  | Low Level Input Current                    |                                                   |                                     |      |     |      |       |
|                                                                                                                                                                                                                                                                                                                                                                                     |                  | Input Buffer                               | V <sub>IN</sub> = V <sub>SS</sub>                 | V <sub>DD</sub> Power On & Off      | –3   | –   | 3    | μA    |
|                                                                                                                                                                                                                                                                                                                                                                                     |                  | Input Buffer with pull-up                  | V <sub>IN</sub> = V <sub>SS</sub>                 | V <sub>DD</sub> = 3.3V ± 10%        | –15  | –40 | –110 |       |
|                                                                                                                                                                                                                                                                                                                                                                                     | V <sub>OH</sub>  | Output High Voltage                        | I <sub>OH</sub> = -1.8mA, -3.6mA, -7.2mA, -10.8mA |                                     | 2.64 | –   | 3.30 | V     |
|                                                                                                                                                                                                                                                                                                                                                                                     | V <sub>OL</sub>  | Output Low Voltage                         | I <sub>OH</sub> = -1.8mA, -3.6mA, -7.2mA, -10.8mA |                                     | 0    | –   | 0.66 |       |
|                                                                                                                                                                                                                                                                                                                                                                                     | I <sub>OZ</sub>  | Output Hi-Z current                        | –                                                 |                                     | –5   | –   | 5    | μA    |
|                                                                                                                                                                                                                                                                                                                                                                                     | C <sub>IN</sub>  | Input capacitance                          | Any input and bi-directional buffers              |                                     | –    | –   | 5    | pF    |
|                                                                                                                                                                                                                                                                                                                                                                                     | C <sub>OUT</sub> | Output capacitance                         | Any output buffer                                 |                                     | –    | –   | 5    | pF    |

\*. Operating conditions: V<sub>DD</sub> = 3.3V, V<sub>ext</sub> = 3.0 to 3.6 V, T<sub>j</sub> = –40 to 125 °C (Junction Temperature), 3.3V-tolerant

Table 38. I/O DC Electrical Characteristics 802.15.4

| Ball Coordinates                    | Symbol                  | Parameter                                                                                            | Condition | Min  | Typ | Max  | Units |
|-------------------------------------|-------------------------|------------------------------------------------------------------------------------------------------|-----------|------|-----|------|-------|
| PAK:[12,13,14,15]<br>PAL:[12,13,15] | Input Voltage Levels    |                                                                                                      |           |      |     |      |       |
|                                     | V <sub>IL</sub>         | V <sub>IL</sub> input logic level low V <sub>DD</sub> =3.3V                                          |           | –    | –   | 0.70 | V     |
|                                     | V <sub>IH</sub>         | V <sub>IH</sub> input logic level high V <sub>DD</sub> =3.3V                                         |           | 2.31 | –   | –    | V     |
|                                     | Output Voltage Levels   |                                                                                                      |           |      |     |      |       |
|                                     | V <sub>OL</sub> [3mA]   | V <sub>OL</sub> output logic level low V <sub>DD</sub> =3.3V, I <sub>OL</sub> =3ma, weak driver      |           | –    | –   | 0.66 | V     |
|                                     | V <sub>OH</sub> [–3mA]  | V <sub>OH</sub> output logic level high V <sub>DD</sub> =3.3V, I <sub>OH</sub> =–3ma, weak driver    |           | 2.64 | –   | –    | V     |
|                                     | V <sub>OH</sub> [20mA]  | V <sub>OH</sub> output logic level high V <sub>DD</sub> =3.3V, I <sub>OL</sub> =20ma, strong driver  |           | –    | –   | 0.66 | V     |
|                                     | V <sub>OH</sub> [–20mA] | V <sub>OH</sub> output logic level high V <sub>DD</sub> =3.3V, I <sub>OL</sub> =–20ma, strong driver |           | 2.64 | –   | –    | V     |

Table 38. I/O DC Electrical Characteristics 802.15.4 (Continued)

| Ball Coordinates | Symbol          | Parameter                                              | Condition                                                                      | Min   | Typ    | Max   | Units |
|------------------|-----------------|--------------------------------------------------------|--------------------------------------------------------------------------------|-------|--------|-------|-------|
| PAL:[14]         | I <sub>Q</sub>  | Quiescent Current                                      | Static Inputs and Outputs                                                      | –     | 1.00   | –     | μA    |
|                  | V <sub>O</sub>  | Maximal voltage applied to PIN in High-Impedance State | –                                                                              | –     | –      | 3.30  | V     |
|                  | V <sub>IH</sub> | High Level Input Voltage                               | Logic input at V <sub>DD</sub> =3.3V                                           | 1.84  | –      | 3.30  |       |
|                  | V <sub>IL</sub> | Low Level Input Voltage                                | Logic input at V <sub>DD</sub> =3.3V                                           | –     | –      | 1.255 |       |
|                  | I <sub>IH</sub> | High Level Input Current                               | Logic input V <sub>IN</sub> =V <sub>DD</sub> =3.3V                             | –1.00 | –      | 1.00  | μA    |
|                  | I <sub>IL</sub> | Low Level Input Current                                | Logic input V <sub>IN</sub> =0V                                                | –1.00 | –      | 1.00  |       |
|                  | V <sub>OH</sub> | High Level Output Voltage                              | Push-Pull & PMOS OD, I <sub>OL</sub> =3mA, 1× Driver at V <sub>DD</sub> =3.3V  | 2.721 | 3.108  | –     | V     |
|                  | V <sub>OL</sub> | Low Level Output Voltage                               | Push-Pull, I <sub>OL</sub> =3mA, 1× Driver at V <sub>DD</sub> =3.3V            |       | 0.175  | 0.257 |       |
|                  | I <sub>OH</sub> | High Level Output Current                              | Push-Pull & PMOS OD, V <sub>OH</sub> =2.4V, 1× Driver at V <sub>DD</sub> =3.3V | 5.774 | 11.066 | –     | mA    |
|                  | I <sub>OL</sub> | Low Level Output Current                               | Push-Pull, V <sub>OL</sub> =0.4V, 1× Driver at V <sub>DD</sub> =3.3V           | 4.491 | 6.438  | –     |       |

Table 39. I/O DC Electrical Characteristics PMIC

| Ball Coordinates  | Symbol          | Parameter                             | Condition | Min  | Typ | Max             | Units |
|-------------------|-----------------|---------------------------------------|-----------|------|-----|-----------------|-------|
| PAG:[1]           | V <sub>OL</sub> | Open drain, I <sub>OUT</sub> =2mA     | –         | –    | –   | 0.40            | V     |
|                   | V <sub>OH</sub> | Open drain, I <sub>OUT</sub> =2mA     |           | –    | –   | V <sub>IN</sub> | V     |
| PAF:[1], PAL:[19] | V <sub>IL</sub> | Input only : Low level input voltage  | –         | –    | –   | 0.40            | V     |
|                   | V <sub>IH</sub> | Input only : High level input voltage |           | 1.40 | –   | V <sub>IN</sub> | V     |

Table 40. I/O DC Electrical Characteristics PCM Signals

| Ball Coordinates  | Symbol          | Parameter                | Condition | Min   | Typ | Max  | Unit |
|-------------------|-----------------|--------------------------|-----------|-------|-----|------|------|
| PAJ:[39,40,41,42] | V <sub>IH</sub> | High-level input voltage | –         | 2.31  | –   | 3.70 | V    |
|                   | V <sub>IL</sub> | Low-level input voltage  | –         | –0.40 | –   | 0.99 |      |
|                   | V <sub>OH</sub> | Output High voltage      | –         | 2.90  | –   | –    | V    |
|                   | V <sub>OL</sub> | Output Low voltage       | –         | –     | –   | 0.40 |      |

Table 41. GPIO Pull-up Resistor Current

| Ball Coordinates                                                                                                                                                                                                                                                                                                                                                                    | Pull Up                                                                   | Min | Typ | Max | Unit    |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------|-----|-----|-----|---------|
| PA:[1,2,3,5,6,7,8,29,37,39,40,41,42]<br>PB:[2,3,4,5,6,7,8,39,40,41,42]<br>PAK:[1,2,3,4,5,6,7,8,9,10,11,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,37,38,39,40,41,42]<br>PAL:[1,2,3,4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42]<br>PP:[41]<br>PAC:[1,2]<br>PAD:[1,2]<br>PAE:[1]<br>PAG:[2,41,42]<br>PAH:[1,2,41,42]<br>PAJ:[1,2] | Enabled (where every GPIO has a 100k $\Omega$ internal pull-up resistor). | 10  | 33  | 72  | $\mu$ A |
|                                                                                                                                                                                                                                                                                                                                                                                     | Disabled (default)                                                        | –   | –   | 0.1 | $\mu$ A |

Table 42. Power-on Reset Timing Specifications

| Symbol            | Description                                 | Min. | Typ. | Max. | Unit |
|-------------------|---------------------------------------------|------|------|------|------|
| t <sub>RESW</sub> | Reset assert time after clock stabilization | 40   | –    | –    | ns   |

## AC Electrical Characteristics

AC characteristics covered in this section are preliminary and are likely to change.

### SD/MMC AC Electrical Characteristics

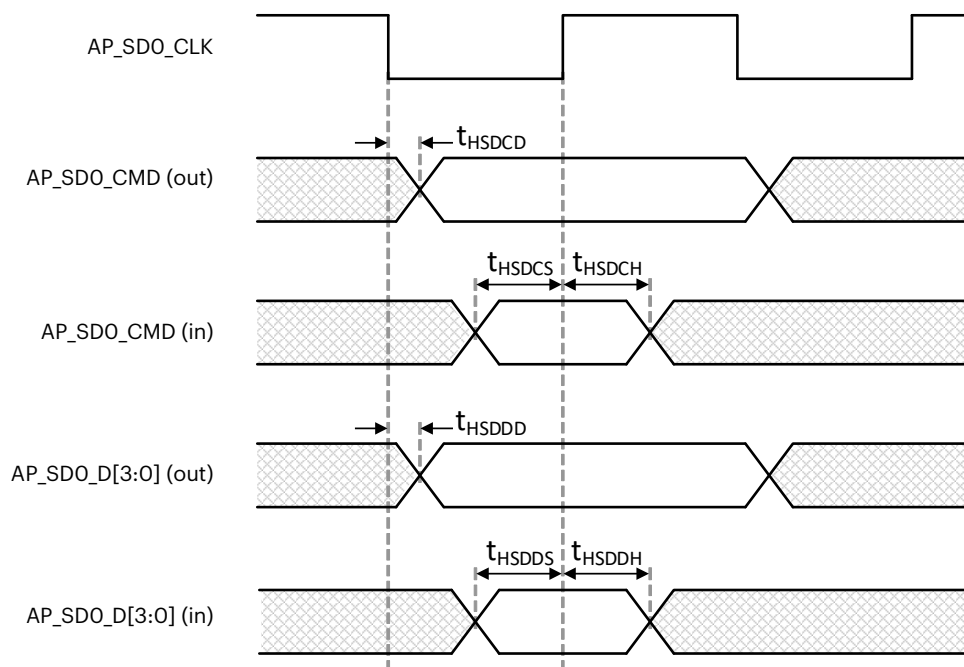


Figure 7. High-Speed SD/MMC Interface Timing

The following table assumes  $V_{\text{DDINT}} = 1.0\text{V} \pm 5\%$ ,  $T_J = -25$  to  $85^\circ\text{C}$ ,  $V_{\text{DDmmc}} = 3.3\text{V} \pm 5\%$ ,  $2.5\text{V} \pm 5\%$ ,  $1.8\text{V} \pm 5\%$

Table 43. High-Speed SD/MMC Interface Transmit/Receive Timing Constants

| Symbol             | Parameter                    | Min | Typ | Max | Unit |
|--------------------|------------------------------|-----|-----|-----|------|
| $t_{\text{HSDCD}}$ | SD command output delay time | –   | –   | 4.0 | ns   |
| $t_{\text{HSDCS}}$ | SD command input setup time  | 4.0 | –   | –   |      |
| $t_{\text{HSDCH}}$ | SD command input hold time   | 0   | –   | –   |      |
| $t_{\text{HSDDD}}$ | SD data output delay time    | –   | –   | 4.0 |      |
| $t_{\text{HSDDS}}$ | SD data input setup time     | 4.0 | –   | –   |      |
| $t_{\text{HSDDH}}$ | SD data input hold time      | 0   | –   | –   |      |

## SPI AC Electrical Characteristics

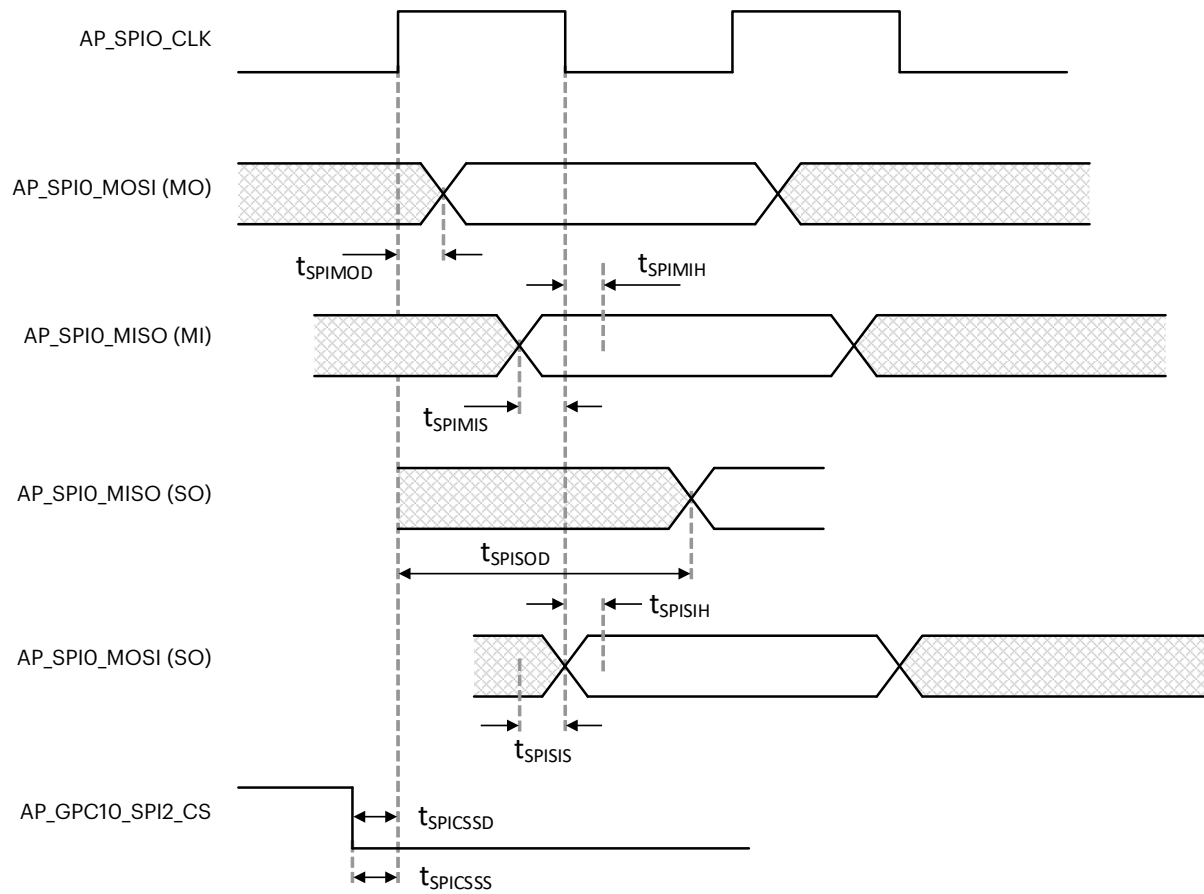


Figure 8. SPI Interface Timing (CPHA = 0, CPOL = 1 (Format A))



The following table assumes  $V_{DDINT} = 1.0 \text{ V} \pm 5\%$ ,  $T_J = -25 \text{ to } 85 \text{ }^\circ\text{C}$ ,  $V_{DDext} = 1.8 \text{ V} \pm 10\%$ , load = 15pF.

Table 44. SPI Interface Transmit/ Receive Timing Constants with 15pF Load

|      | Parameter                                          | Symbol        | Min. | Typ. | Max. | Units |
|------|----------------------------------------------------|---------------|------|------|------|-------|
| Ch 0 | SPI MOSI Master Output Delay time                  | $t_{SPIMOD}$  | –    | –    | 5    | ns    |
|      | SPI MISO Master Input Setup time (FB_CLK_SEL = 00) | $t_{SPIMIS}$  | 12   | –    | –    |       |
|      | SPI MISO Master Input Setup time (FB_CLK_SEL = 01) |               | 7    | –    | –    |       |
|      | SPI MISO Master Input Setup time (FB_CLK_SEL = 10) |               | 2    | –    | –    |       |
|      | SPI MISO Master Input Setup time (FB_CLK_SEL = 11) |               | –3   | –    | –    |       |
|      | SPI MISO Master Input Hold time                    | $t_{SPIMIH}$  | 5    | –    | –    |       |
|      | SPI MOSI Slave Input Setup time                    | $t_{SPISIS}$  | 2    | –    | –    | ns    |
|      | SPI MOSI Slave Input Hold time                     | $t_{SPISIH}$  | 5    | –    | –    |       |
|      | SPI MISO Slave Output Delay time                   | $t_{SPISOD}$  | –    | –    | 17   |       |
|      | SPI nSS Master Output Delay time                   | $t_{SPICSSD}$ | 7    | –    | –    |       |
|      | SPI nSS Slave Input Setup time                     | $t_{SPICSSS}$ | 5    | –    | –    |       |
| Ch 1 | SPI MOSI Master Output Delay time                  | $t_{SPIMOD}$  | –    | –    | 4    | ns    |
|      | SPI MISO Master Input Setup time (FB_CLK_SEL = 00) | $t_{SPIMIS}$  | 13   | –    | –    |       |
|      | SPI MISO Master Input Setup time (FB_CLK_SEL = 01) |               | 8    | –    | –    |       |
|      | SPI MISO Master Input Setup time (FB_CLK_SEL = 10) |               | 3    | –    | –    |       |
|      | SPI MISO Master Input Setup time (FB_CLK_SEL = 11) |               | –2   | –    | –    |       |
|      | SPI MISO Master Input Hold time                    | $t_{SPIMIH}$  | 5    | –    | –    |       |
|      | SPI MOSI Slave Input Setup time                    | $t_{SPISIS}$  | 3    | –    | –    | ns    |
|      | SPI MOSI Slave Input Hold time                     | $t_{SPISIH}$  | 5    | –    | –    |       |
|      | SPI MISO Slave Output Delay time                   | $t_{SPISOD}$  | –    | –    | 18   |       |
|      | SPI nSS Master Output Delay time                   | $t_{SPICSSD}$ | 7    | –    | –    |       |
|      | SPI nSS Slave Input Setup time                     | $t_{SPICSSS}$ | 5    | –    | –    |       |

$SPICLK_{out} = 50 \text{ MHz}$



NOTE

- $t_{SPIMIS,CH0} = 12 - (\text{cycle period}/4) \times \text{FB\_CLK\_SEL}$
- $t_{SPIMIS,CH1} = 13 - (\text{cycle period}/4) \times \text{FB\_CLK\_SEL}$

The following table assumes  $V_{DDINT} = 1.0V \pm 5\%$ ,  $T_J = -25$  to  $85^\circ C$ ,  $V_{DDext} = 3.3V \pm 10\%$ , load = 30pF.

Table 45. SPI Interface Transmit/Receive Timing Constants with 30pF Load

| Parameter |                                                    | Symbol        | Min. | Typ. | Max. | Unit |
|-----------|----------------------------------------------------|---------------|------|------|------|------|
| Ch 0      | SPI MOSI Master Output Delay time                  | $t_{SPIMOD}$  | –    | –    | 6    | ns   |
|           | SPI MISO Master Input Setup time (FB_CLK_SEL = 00) | $t_{SPIMIS}$  | 13   | –    | –    |      |
|           | SPI MISO Master Input Setup time (FB_CLK_SEL = 01) |               | 8    | –    | –    |      |
|           | SPI MISO Master Input Setup time (FB_CLK_SEL = 10) |               | 3    | –    | –    |      |
|           | SPI MISO Master Input Setup time (FB_CLK_SEL = 11) |               | –2   | –    | –    |      |
|           | SPI MISO Master Input Hold time                    | $t_{SPIMIH}$  | 5    | –    | –    |      |
|           | SPI MOSI Slave Input Setup time                    | $t_{SPISIS}$  | 4    | –    | –    | ns   |
|           | SPI MOSI Slave Input Hold time                     | $t_{SPISIH}$  | 5    | –    | –    |      |
|           | SPI MISO Slave Output Delay time                   | $t_{SPISOD}$  | –    | –    | 18   |      |
|           | SPI nSS Master Output Delay time                   | $t_{SPICSSD}$ | 8    | –    | –    |      |
|           | SPI nSS Slave Input Setup time                     | $t_{SPICSSS}$ | 6    | –    | –    |      |
| Ch 1      | SPI MOSI Master Output Delay time                  | $t_{SPIMOD}$  | –    | –    | 5    | ns   |
|           | SPI MISO Master Input Setup time (FB_CLK_SEL = 00) | $t_{SPIMIS}$  | 14   | –    | –    |      |
|           | SPI MISO Master Input Setup time (FB_CLK_SEL = 01) |               | 9    | –    | –    |      |
|           | SPI MISO Master Input Setup time (FB_CLK_SEL = 10) |               | 4    | –    | –    |      |
|           | SPI MISO Master Input Setup time (FB_CLK_SEL = 11) |               | –1   | –    | –    |      |
|           | SPI MISO Master Input Hold time                    | $t_{SPIMIH}$  | 5    | –    | –    |      |
|           | SPI MOSI Slave Input Setup time                    | $t_{SPISIS}$  | 4    | –    | –    | ns   |
|           | SPI MOSI Slave Input Hold time                     | $t_{SPISIH}$  | 5    | –    | –    |      |
|           | SPI MISO Slave Output Delay time                   | $t_{SPISOD}$  | –    | –    | 19   |      |
|           | SPI nSS Master Output Delay time                   | $t_{SPICSSD}$ | 8    | –    | –    |      |
|           | SPI nSS Slave Input Setup time                     | $t_{SPICSSS}$ | 6    | –    | –    |      |

$SPICLK_{out} = 50$  MHz



**NOTE**

- $t_{SPIMIS,CH0} = 12 - (\text{cycle period}/4) \times \text{FB\_CLK\_SEL}$
- $t_{SPIMIS,CH1} = 13 - (\text{cycle period}/4) \times \text{FB\_CLK\_SEL}$

## I<sup>2</sup>C AC Electrical Characteristics

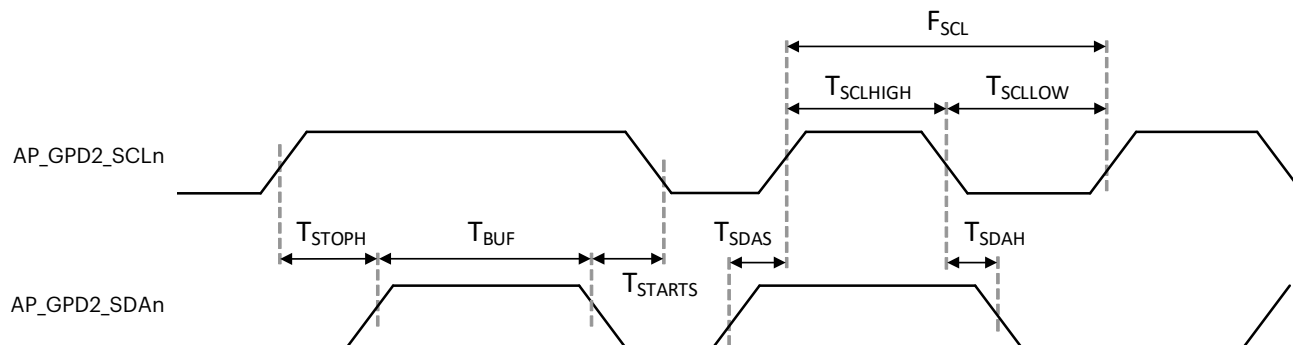


Figure 9. I<sup>2</sup>C Interface Timing

The following table assumes  $V_{DDINT}, V_{DDarm} = 1.1V \pm 5\%$ ,  $T_J = -25$  to  $85^\circ C$ ,  $V_{DDEXT} = 3.3V \pm 10\%$

Table 46. I<sup>2</sup>C BUS Controller Module Signal Timing

| Parameter                            | Symbol        | Min.                 | Typ. | Max.                 | Unit    |
|--------------------------------------|---------------|----------------------|------|----------------------|---------|
| SCL clock frequency                  | $F_{SCL}$     | –                    | –    | std. 100<br>fast 400 | kHz     |
| SCL high level pulse width           | $T_{SCLHIGH}$ | std. 4.0<br>fast 0.6 | –    | –                    | $\mu s$ |
| SCL low level pulse width            | $T_{SCLLOW}$  | std. 4.7<br>fast 1.3 | –    | –                    |         |
| Bus free time between STOP and START | $T_{BUF}$     | std 4.7<br>fast 1.3  | –    | –                    |         |
| START hold time                      | $T_{STARTS}$  | std. 4.0<br>fast 0.6 | –    | –                    |         |
| SDA hold time                        | $T_{SDAH}$    | std. 0<br>fast 0     | –    | std.<br>fast 0.9     | ns      |
| SDA setup time                       | $T_{SDAS}$    | std. 250<br>fast 100 | –    | –                    |         |
| STOP setup time                      | $T_{STOPH}$   | std. 4.0<br>fast 0.6 | –    | –                    | $\mu s$ |

Modes: std. refers to Standard Mode and fast refers to Fast Mode.



NOTE

- I<sup>2</sup>C data hold time ( $t_{SDAH}$ ) is minimum 0ns for standard/fast bus mode as defined in I<sup>2</sup>C specification v2.1. Check whether the data hold time of your I<sup>2</sup>C device is 0ns or not.
- The I<sup>2</sup>C controller supports I<sup>2</sup>C bus device only (standard/fast bus mode), and does not support a C-bus device.

## RF Electrical Characteristics

All performance numbers related to 802.11 for Wi-Fi, Bluetooth, and 802.15.4 for Zigbee mentioned in this section are preliminary and likely to change once module characterization has taken place.

### Wi-Fi, 2.4GHz Receiver RF Specifications

Table 47. Wi-Fi, 2.4GHz Receiver RF Specifications

| Parameter                                             | Conditions                                                         | Min  | Typ | Max  | Unit |
|-------------------------------------------------------|--------------------------------------------------------------------|------|-----|------|------|
| Frequency Range                                       | –                                                                  | 2400 | –   | 2500 | MHz  |
| Minimum receiver sensitivity in 802.11b mode (2.4GHz) |                                                                    |      |     |      |      |
| 1Mbps                                                 | PER < 8%,<br><br>Packet size = 1024 bytes                          | –    | –97 | –    | dBm  |
| 2Mbps                                                 |                                                                    | –    | –95 | –    | dBm  |
| 5.5Mbps                                               |                                                                    | –    | –94 | –    | dBm  |
| 11Mbps                                                |                                                                    | –    | –90 | –    | dBm  |
| Minimum receiver sensitivity in 802.11g mode (2.4GHz) |                                                                    |      |     |      |      |
| 6Mbps                                                 | PER < 10%,<br><br>Packet size= 1024 bytes                          | –    | –91 | –    | dBm  |
| 9Mbps                                                 |                                                                    | –    | –90 | –    | dBm  |
| 12Mbps                                                |                                                                    | –    | –89 | –    | dBm  |
| 18Mbps                                                |                                                                    | –    | –87 | –    | dBm  |
| 24Mbps                                                |                                                                    | –    | –84 | –    | dBm  |
| 36Mbps                                                |                                                                    | –    | –81 | –    | dBm  |
| 48Mbps                                                |                                                                    | –    | –76 | –    | dBm  |
| 54Mbps                                                |                                                                    | –    | –75 | –    | dBm  |
| Minimum receiver sensitivity in 802.11n mode (2.4GHz) |                                                                    |      |     |      |      |
| MCS 0                                                 | PER<10%,<br><br>Packet size= 4096 bytes,<br>GF, 800ns GI, Non-STBC | –    | –89 | –    | dBm  |
| MCS 1                                                 |                                                                    | –    | –88 | –    | dBm  |
| MCS 2                                                 |                                                                    | –    | –86 | –    | dBm  |
| MCS 3                                                 |                                                                    | –    | –83 | –    | dBm  |
| MCS 4                                                 |                                                                    | –    | –79 | –    | dBm  |
| MCS 5                                                 |                                                                    | –    | –75 | –    | dBm  |
| MCS 6                                                 |                                                                    | –    | –73 | –    | dBm  |
| MCS 7                                                 |                                                                    | –    | –72 | –    | dBm  |

## Wi-Fi, 2.4GHz Transmitter RF Specifications

Table 48. Wi-Fi, 2.4GHz Transmitter RF Specifications

| Parameter                                                  | Conditions                   | Min | Typ | Max | Unit |
|------------------------------------------------------------|------------------------------|-----|-----|-----|------|
| Linear output power                                        |                              |     |     |     |      |
| Maximum output power in 802.11b mode                       | As specified in IEEE802.11   | –   | 15  | –   | dBm  |
| Maximum output power in 802.11g mode                       |                              | –   | 15  | –   | dBm  |
| Maximum output power in 802.11n mode                       |                              | –   | 13  | –   | dBm  |
| Transmit spectrum mask                                     |                              |     |     |     |      |
| Margin to 802.11b spectrum mask                            | Maximum output power         | 0   | –   | –   | dBr  |
| Margin to 802.11g spectrum mask                            |                              | 0   | –   | –   | dBr  |
| Margin to 802.11n spectrum mask                            |                              | 0   | –   | –   | dBr  |
| Transmit modulation accuracy in 802.11b mode               |                              |     |     |     |      |
| 1Mbps                                                      | As specified in IEEE 802.11b | –   | –   | 35  | %    |
| 2Mbps                                                      |                              | –   | –   | 35  | %    |
| 5.5Mbps                                                    |                              | –   | –   | 35  | %    |
| 11Mbps                                                     |                              | –   | –   | 35  | %    |
| Transmit modulation accuracy in 802.11g mode               |                              |     |     |     |      |
| 6Mbps                                                      | As specified in IEEE 802.11g | –   | –   | –5  | dB   |
| 9Mbps                                                      |                              | –   | –   | –8  | dB   |
| 12Mbps                                                     |                              | –   | –   | –10 | dB   |
| 18Mbps                                                     |                              | –   | –   | –13 | dB   |
| 24Mbps                                                     |                              | –   | –   | –16 | dB   |
| 36Mbps                                                     |                              | –   | –   | –19 | dB   |
| 48Mbps                                                     |                              | –   | –   | –22 | dB   |
| 54Mbps                                                     |                              | –   | –   | –25 | dB   |
| Transmit modulation accuracy in 802.11n mode               |                              |     |     |     |      |
| MCS7                                                       | As specified in IEEE 802.11n | –   | –   | –27 | dB   |
| Transmit power-on and power-down ramp time in 802.11b mode |                              |     |     |     |      |
| Transmit power-on ramp time from 10% to 90% output power   | –                            | –   | –   | 2   | μs   |
| Transmit power-down ramp time from 90% to 10% output power | –                            | –   | –   | 2   | μs   |

## Wi-Fi, 5GHz Receiver RF Specifications

Table 49. Wi-Fi, 5GHz Receiver RF Specifications

| Parameter                                            | Conditions | Min  | Typ | Max  | Unit |
|------------------------------------------------------|------------|------|-----|------|------|
| Frequency Range                                      | –          | 4900 | –   | 5845 | MHz  |
| Minimum receiver sensitivity in 802.11a mode         |            |      |     |      |      |
| 6Mbps                                                | PER < 10%  | –    | –90 | –    | dBm  |
| 9Mbps                                                |            | –    | –89 | –    | dBm  |
| 12Mbps                                               |            | –    | –88 | –    | dBm  |
| 18Mbps                                               |            | –    | –87 | –    | dBm  |
| 24Mbps                                               |            | –    | –84 | –    | dBm  |
| 36Mbps                                               |            | –    | –80 | –    | dBm  |
| 48Mbps                                               |            | –    | –76 | –    | dBm  |
| 54Mbps                                               |            | –    | –75 | –    | dBm  |
| Minimum receiver sensitivity in 802.11n (HT-20) mode |            |      |     |      |      |
| MCS 0                                                | PER < 10%  | –    | –89 | –    | dBm  |
| MCS 1                                                |            | –    | –88 | –    | dBm  |
| MCS 2                                                |            | –    | –85 | –    | dBm  |
| MCS 3                                                |            | –    | –82 | –    | dBm  |
| MCS 4                                                |            | –    | –79 | –    | dBm  |
| MCS 5                                                |            | –    | –75 | –    | dBm  |
| MCS 6                                                |            | –    | –72 | –    | dBm  |
| MCS 7                                                |            | –    | –71 | –    | dBm  |
| Minimum receiver sensitivity in 802.11n (HT-40) mode |            |      |     |      |      |
| MCS 0                                                | PER < 10%  | –    | –86 | –    | dBm  |
| MCS 1                                                |            | –    | –85 | –    | dBm  |
| MCS 2                                                |            | –    | –83 | –    | dBm  |
| MCS 3                                                |            | –    | –80 | –    | dBm  |
| MCS 4                                                |            | –    | –77 | –    | dBm  |
| MCS 5                                                |            | –    | –73 | –    | dBm  |
| MCS 6                                                |            | –    | –71 | –    | dBm  |
| MCS 7                                                |            | –    | –69 | –    | dBm  |

## Wi-Fi, 5GHz Transmitter RF Specifications

Table 50. Wi-Fi, 5GHz Transmitter RF Specifications

| Parameter                                                   | Conditions                   | Min  | Typ | Max  | Unit |
|-------------------------------------------------------------|------------------------------|------|-----|------|------|
| Frequency Range                                             | –                            | 4900 |     | 5845 | MHz  |
| Linear output power                                         |                              |      |     |      |      |
| Maximum output power in 802.11a mode                        | 54M, UNII-2e                 | –    | 13  | –    | dBm  |
| Maximum output power in 802.11n mode                        | HT20, MCS7, UNII-2e          | –    | 12  | –    | dBm  |
|                                                             | HT40, MCS7, UNII-2e          | –    | 11  | –    | dBm  |
| Transmit spectrum mask                                      |                              |      |     |      |      |
| Margin to 802.11a spectrum mask                             | Maximum output power         | 0    | –   | –    | dBr  |
| Margin to 802.11n spectrum mask                             |                              | 0    | –   | –    | dBr  |
| Transmit constellation error in 802.11a mode                |                              |      |     |      |      |
| 54Mbps                                                      | As specified in IEEE 802.11n | –    | –   | –25  | dB   |
| Transmit constellation error in 802.11n (HT-20, HT-40) mode |                              |      |     |      |      |
| MCS 7                                                       | As specified in IEEE 802.11n | –    | –   | –27  | dB   |

## Bluetooth RF Specifications

Table 51. Bluetooth Receiver RF Specifications

| Parameter                   | Conditions                       | Min  | Typ | Max  | Unit |
|-----------------------------|----------------------------------|------|-----|------|------|
| Frequency Range             | –                                | 2402 | –   | 2480 | MHz  |
| Sensitivity (BER)           | GPSK, BER $\leq 0.1\%$           | –    | –92 | –    | dBm  |
|                             | $\pi/4$ -DQPSK, BER $\leq 0.1\%$ | –    | –92 | –    | dBm  |
|                             | BER $\leq 0.1\%$ , 8DPSK         | –    | –89 | –    | dBm  |
| Maximum Input Level         | GPSK, BER $\leq 0.1\%$           | –20  | –   | –    | dBm  |
|                             | $\pi/4$ -DQPSK, BER $\leq 0.1\%$ | –20  | –   | –    | dBm  |
|                             | BER $\leq 0.1\%$ , 8 DPSK        | –20  | –   | –    | dBm  |
| <b>BDR</b>                  |                                  |      |     |      |      |
| Intermodulation Performance | –                                | –    | –   | 0.1  | %    |
| Rx C/I Performance          | 1DH1                             | –    | –   | 0.1  | %    |
|                             | 1DH3                             | –    | –   | 0.1  | %    |
|                             | 1DH5                             | –    | –   | 0.1  | %    |
| <b>EDR</b>                  |                                  |      |     |      |      |
| Rx C/I Performance          | 2DH1                             | –    | –   | 0.1  | %    |
|                             | 2DH3                             | –    | –   | 0.1  | %    |
|                             | 2DH5                             | –    | –   | 0.1  | %    |
|                             | 3DH1                             | –    | –   | 0.1  | %    |
|                             | 3DH3                             | –    | –   | 0.1  | %    |
|                             | 3DH5                             | –    | –   | 0.1  | %    |
| Rx BER Floor Performance    | BER $\leq 0.001\%$               | –    | –   | –70  | dBm  |

Table 52. Bluetooth Transmitter RF Specifications

| Parameter                     | Conditions | Min  | Typ | Max  | Unit |
|-------------------------------|------------|------|-----|------|------|
| Frequency Range               | –          | 2402 | –   | 2480 | MHz  |
| <b>Output Power (Average)</b> |            |      |     |      |      |
| BDR (QPSK)                    | 2440 MHz   | –    | 6   | –    | dBm  |
| EDR ( $\pi/4$ -DQPSK)         | 2440 MHz   | –    | 2   | –    | dBm  |
| EDR (8DPSK)                   | 2440 MHz   | –    | 2   | –    | dBm  |

Table 53. Bluetooth Low Energy (BLE) RF Specifications

| Parameter                                       | Conditions | Min  | Typ | Max  | Unit |
|-------------------------------------------------|------------|------|-----|------|------|
| Frequency Range                                 | –          | 2402 | –   | 2480 | MHz  |
| Rx Receiver Sensitivity PER                     | At –70dBm  | –    | –   | 30.8 | %    |
| Rx C/I and Receiver Selectivity Performance PER | –          | –    | –   | 30.8 | %    |
| Tx Power                                        | –          | –    | 6   | –    | dBm  |



## 802.15.4 Receiver RF Specifications

The typical numbers indicated in *Table 54* and *Table 55* are one standard deviation below the mean, measured at room temperature 25°C. The Min and Max numbers were measured over process corners at room temperature.

Table 54. 802.15.4 Receiver RF Specifications

| Parameter                                      | Test Condition                         | Min  | Typ | Max    | Unit |
|------------------------------------------------|----------------------------------------|------|-----|--------|------|
| Operating Frequency Range                      | –                                      | 2400 | –   | 2483.5 | MHz  |
| Receiver Sensitivity PER                       | At –95dBm                              | –    | –   | 1      | %    |
| Receiver Sensitivity Search                    | At PER 1%                              | –    | –95 | –      | dBm  |
| Receiver Interference Rejection PER            | At –2 Channel, Alternate Channel, 30dB | –    | –   | 1      | %    |
| Receiver Interference Rejection PER            | At –1 Channel, Adjacent Channel, 0dB   | –    | –   | 1      | %    |
| Receiver Interference Rejection PER            | At +1 Channel, Adjacent Channel, 0dB   | –    | –   | 1      | %    |
| Receiver Interference Rejection PER            | At +2 Channel, Alternate Channel, 30dB | –    | –   | 1      | %    |
| Error Vector Magnitude - RMS (EVM)             | At Target Power                        | –    | –   | 30     | %    |
| Error Vector Magnitude - Offset (EVM)          | At Target Power                        | –    | –   | 10     | %    |
| Receiver Maximum Input Level of Desired Signal | At –20dBm Input                        | –    | –   | 1      | %    |

Table 55. 802.15.4 Transmitter RF Specifications

| Parameter                           | Test Condition                                             | Min | Typ   | Max | Unit |
|-------------------------------------|------------------------------------------------------------|-----|-------|-----|------|
| Maximum output power                | At highest normal mode power setting                       |     | 6/16* | –   | dBm  |
| Minimum output power                | At lowest power setting                                    | –   | –27   | –   | dBm  |
| Error vector magnitude (Offset-EVM) | As defined by IEEE 802.15.4-2003, which sets a 35% maximum | –   | –     | 10  | %    |
| Carrier frequency error             | –                                                          | –40 | –     | +40 | ppm  |
| PSD mask relative                   | 3.5 MHz away (Normal)                                      | –20 | –     | –   | dBm  |
| PSD mask absolute                   | 100 KHz BW                                                 | –30 | –     | –   | dBm  |

\*. The ARTIK 530/530s Module default setting is 6dBm for CE. You can change the setting to 16dBm for FCC testing.

## THERMAL AND ENVIRONMENTAL SPECIFICATIONS

### Recommended Operating Conditions

The recommended operation of the ARTIK 530/530s Module is based on the operating conditions listed in [Table 56](#).

Table 56. Recommended Operating Conditions

| Parameter                                        | Symbol                                                       | Min | Typ | Max | Units |
|--------------------------------------------------|--------------------------------------------------------------|-----|-----|-----|-------|
| Main Power Supply                                | VIN PV:[42,43],PW:[42,43],PY:[42,43],PAA:[42,43],PAB:[42,43] | 3.7 | 4.2 | 5.0 | V     |
| Operating Temperature<br>(ARTIK 530/530s 512 MB) | T <sub>C</sub>                                               | -25 | -   | 85  | °C    |
| Operating Temperature<br>(ARTIK 530s 1GB)        | T <sub>C</sub>                                               | 0   | -   | 85  | °C    |
| Storage Temperature                              | T <sub>A</sub>                                               | -   | -40 | 85  | °C    |

### Temperature Thresholds for Operating Frequency Throttling

The ARTIK 530/530s Module automatically performs frequency throttling under software control at the thresholds indicated in the following table:

Table 57. Case Temperature vs Maximum Operating Frequency

| Temperature | Maximum Operating Frequency |
|-------------|-----------------------------|
| <50°C       | 1.2 GHz                     |
| 50° to 60°C | 1.0 GHz                     |
| 60° to 85°C | 400 MHz                     |

Module temperatures are dependent on processing load. For high processor loads, these thresholds may be reduced by up to 10 degrees.

For more information, refer to the [ARTIK 530 Thermal Guide](#).

### ESD Ratings

Table 58. ESD Ratings

| Symbol                                  | Min. | Max. | Units |
|-----------------------------------------|------|------|-------|
| ESD stress voltage Human Body Model     | -    | 1    | kV    |
| ESD stress voltage Charged Device Model | -    | TBD  | V     |

Table 59. Shock and Vibration Ratings

| Shock and Vibration |                   | Range                           |
|---------------------|-------------------|---------------------------------|
| Shock               | Packing Drop      | 75cm (10~19.9Kg) / 91cm (<10Kg) |
| Vibration           | Packing Vibration | 0.85Grms/2~200Hz (TTL Grms)     |

## MECHANICAL SPECIFICATIONS

The ARTIK 530/530s Module supports PAD Balls and two RF connectors on a 49mm × 36mm footprint as shown in [Figure 10](#). Refer to section [Antenna Connections](#) for RF connector details. In addition the top view, side view and bottom view with its dimensions can be seen in [Figure 11](#) and [Figure 12](#).

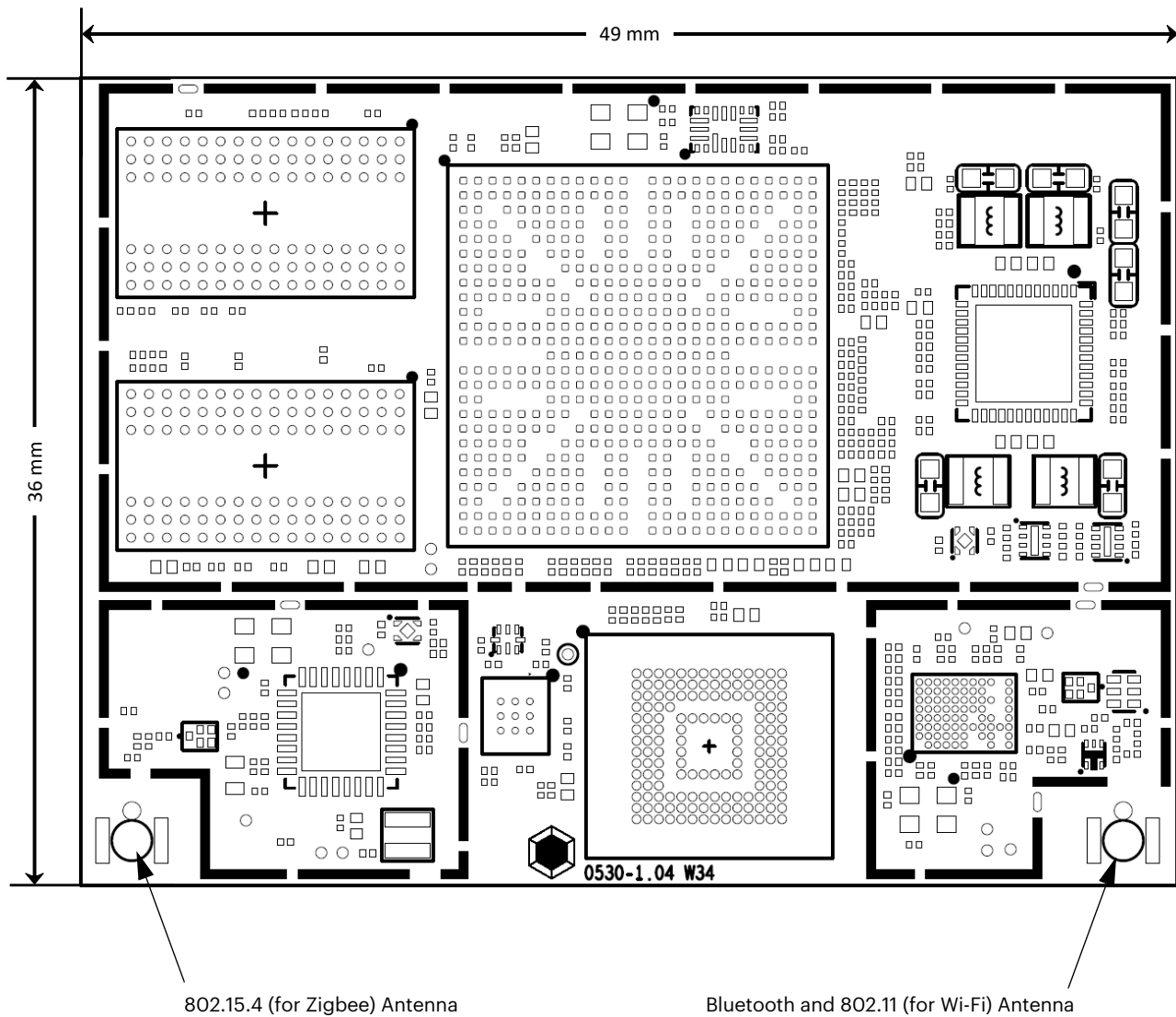
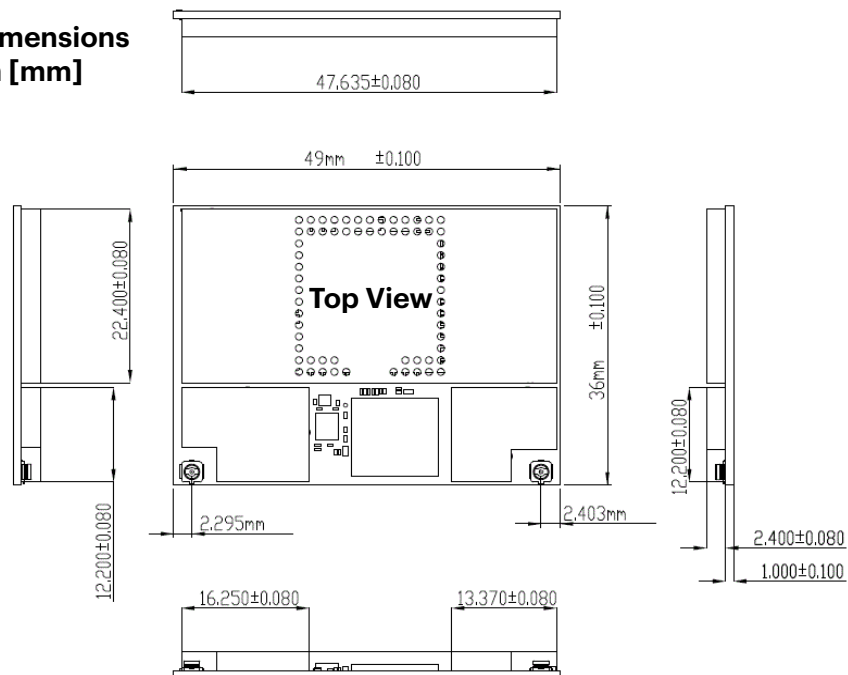


Figure 10. ARTIK 530/530s Module Top View Mechanical Dimensions and Part Location



Technical drawing of a square microfluidic chip. The chip is composed of a grid of small circles representing the microfluidic network. Key dimensions and labels include:

- Chip Size:** 12.22mm by 12.22mm.
- Channel Width:** 1.13mm.
- Channel Spacing:** 1.13mm.
- Port Dimensions:** 1.05mm by 1.34mm.
- Port Location:** 10.25mm from the bottom edge.
- Port Spacing:** 10.25mm.
- Port Diameter:**  $\phi 0.65\text{mm}$ .
- Port Label:** PA1 Ball.
- Ball Size:**  $\phi 0.65$ .
- Ball Pitch:** 1.13.



The inner pin locations on the pad, positioned in an L-shaped form, as depicted in [Figure 13](#), are described in [Table 60](#).

**CAUTION**

The inner pads are on a different grid from the outer pads as indicated with the dashed blue lines in [Figure 13](#).

**CAUTION**

The inner pads are *not* horizontally centered in the module

For exact dimensions on ball locations, see [Figure 12](#). The locations given in [Table 60](#) are the absolute coordinates measured from the edge of the ARTIK 530/530s Module to the center of each ball. All inner pads are ground (GND) balls.

Table 60. L-Shaped Ball Locations

| Ball Name | X-Location (mm) | Y-Location (mm) |
|-----------|-----------------|-----------------|
| TP282     | 11.09           | 25.75           |
| TP283     | 12.22           | 25.75           |
| TP284     | 13.35           | 25.75           |
| TP285     | 34.52           | 25.75           |
| TP286     | 35.65           | 25.75           |
| TP287     | 36.78           | 25.75           |
| TP288     | 36.78           | 24.62           |
| TP289     | 36.78           | 23.49           |
| TP290     | 36.78           | 12.51           |
| TP291     | 36.78           | 11.38           |
| TP292     | 36.78           | 10.25           |
| TP293     | 35.65           | 10.25           |
| TP294     | 34.52           | 10.25           |
| TP295     | 13.35           | 10.25           |
| TP296     | 12.22           | 10.25           |
| TP297     | 11.09           | 10.25           |
| TP298     | 11.09           | 11.38           |
| TP299     | 11.09           | 12.51           |
| TP300     | 11.09           | 23.49           |
| TP301     | 11.09           | 24.62           |

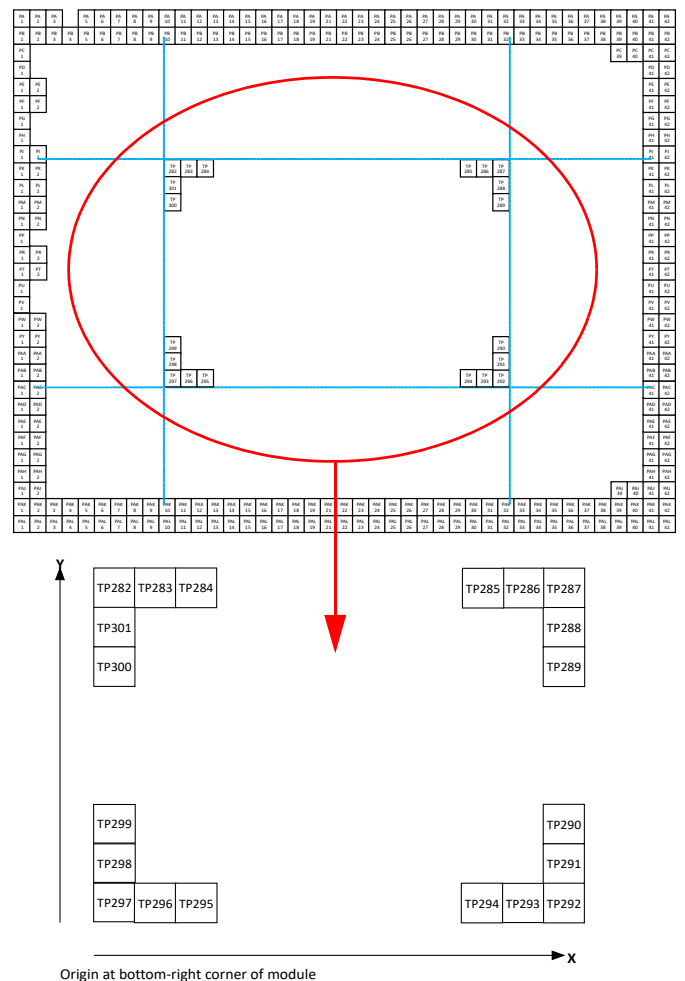


Figure 13. L-Shaped Pad Pins (Top View)

## CERTIFICATIONS AND COMPLIANCE

### Bluetooth

The ARTIK 530/530s Module is recognized as a qualified design as set out by the Bluetooth SIG.

Declaration ID: D032725

Qualified Design ID: 88390

### CE

The ARTIK 530/530s Module is in compliance with the essential requirements and other relevant provisions of Article 3 of the Radio Equipment Directive 2014/53/EU. Compliance with the following standards was confirmed:

- Article 3.1a (Health and Safety) EN 60950-1:2006 + A11:2009 + A1:2010 + A12:2001 + A2:2013  
EN62311:2008
- Article 3.1.b (EMC) EN 301 489-1 V2.1.1, draft EN 301 489-3 V2.1.0  
EN 301 489-17 V3.1.1
- Article 3.2 (Radio spectrum use) EN 300 328 V2.1.1  
EN 301 893 V1.8.1 and EN 301 893 V2.1.1 (partial)  
EN 300 440 V2.1.1
- Certificate number: AN17C10983-3 (ARTIK 530 and ARTIK 530s)  
AN17C11024-1 (ARTIK 530s 1G)

For a formal notified body statement of opinion contact your sales representative.

### FCC

The ARTIK 530/530s Module complies with the following two sections (15C and 15E) of Part 15 of the FCC rules namely:

- Spread spectrum transmitter (SST) compliance (15C):
  - 2402–2480MHz frequency range, output power 0.0049W
- Digital transmission system (DTS) compliance (15C):
  - 2402–2480MHz frequency range, output power 0.004W
  - 2405–2475MHz frequency range, output power 0.0412W
  - 2412–2462MHz frequency range, output power 0.0308W
- Unlicensed national information infrastructure TX compliance (15E) in the:
  - 5180-5240MHz frequency range, output power 0.0206W
  - 5260-5320MHz frequency range, output power 0.0221W
  - 5500-5720MHz frequency range, output power 0.0222W
  - 5745-5825MHz frequency range, output power 0.01W

FCC Identifier: A3LSIP005AFS30

Modular Type: Limited Single Modular

## IC

The ARTIK 530/530s Module complies with the IC license-exempt RSS standard.

Radio certification number: 649E-SIP005AFS30

## KCC

The ARTIK 530/530s Module complies with the standards set by the Korean communications commission (KCC).

ARTIK 530/530s Module KCC Identifier: MSIP-CRM-SEC-SIP005AFS30

## SRRC

Both the ARTIK 530/530s Module and the ARTIK 530/530s Development Kit comply with the standards set by the People's Republic of China.

CMIIT ID: 2017AJ3123 (M)(ARTIK 530/530s Module)

CMIIT ID: 2017AJ2921 (ARTIK 530/530s Development Kit)

## HDMI Compliance

The ARTIK 530/530s Module passed the self-test, HDMI CTS version 1.4b on 8/26/2016 provided by HDMI Licensing LLC.

## RoHS Compliance

The ARTIK 530/530s Module complies with the hazardous substance limits of directive 2011/65/EU and the conformity assessment procedure as outlined in Decision 768/2008/EC, Annex II, Module A, Point 2, as well as RoHS harmonized standard EN 50581.

Report reference number: F690101/LF-CTSAYGU16-06911

## FCC Regulatory Disclosures

This device complies with Part 15 of the FCC's Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesirable operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.

- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/ TV technician for help.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the transmitter's radiating structure(s) and the body of the user or nearby persons.

This module is intended for OEM integration. The OEM integrator is responsible for FCC compliance and compliance with all applicable regulations including those for modular transmitters 47 C.F.R. 15.212. The OEM product must comply with all applicable labeling requirements including those contained in 15 C.F.R. 15.19. The OEM is solely responsible for certification and testing and labeling of its own products. In addition to any independently required labels, the OEM shall also affix to the outside of a device into which the module is installed a label referring to the enclosed module. This exterior label should be prepared in a legible font and permanently affixed and using the wording "Contains Transmitter Module FCCID: A3LSIP005AFS30"

The OEM is required to ensure that the end product integrates this module so as to maintain a minimum distance of 20 cm between the equipment's radiating structure(s) and the body of the user or nearby persons. The OEM shall also advise its end user of this requirement as required by applicable rules.

The OEM shall require that the end user of its product be informed that the FCC radio frequency exposure guidelines for an uncontrolled environment can be satisfied. The OEM shall further inform its end user that any change or modifications to this module not expressly approved by the manufacturer will void the warranty and the users' authority to operate the equipment.



## Industry Canada Regulatory Disclosures

### Industry Canada Statement

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

*Cet appareil est conforme avec Industrie Canada exempts de licence standard RSS (s). L'opération est soumise aux deux conditions suivantes: (1) cet appareil ne peut causer d'interférences, et (2) cet appareil doit accepter toute interférence, y compris les interférences qui peuvent causer un mauvais fonctionnement de l'appareil.*

#### Industry Canada Radiation Exposure Statement and Limitations on Use

This equipment complies with IC RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator and your body. This equipment should be installed and must not be co-located or operating in conjunction with any other antenna or transmitter.

This equipment is restricted to indoor use in the 5.15-5.25 GHz range. This equipment is not able to be operated at 5600-5650. In the United States and Canada, only Channel 1-11 can be operated and these channel assignments deal only with the 2.4 GHz range.

The end product must be labeled to display the Industry Canada certification number of the module.

**“Contains transmitter module IC: 649E-SIP005AFS30”**

*Le dispositif d'accueil doivent être étiquetés pour afficher le numéro de certification d'Industrie Canada du module.*

**“Contient module émetteur IC : 649E-SIP005AFS30”**

## EU Regulatory Disclosures

### Statement\*

*The following statement must be supplied with each product but can be printed in the user manual, the packaging, or provided as a separated leaflet.*

Hereby, Samsung declares that this IoT Module is in compliance with the essential requirements and other relevant provisions of Article 3 of the Radio Equipment Directive 2014/53/EU and RoHS directive 2011/65/EU.

“The declaration of conformity may be consulted at [[www.artik.io/certification](http://www.artik.io/certification)]”

The 5150 - 5350 MHz and 5470 - 5725 MHz bands are for indoor use only.

The OEM is required to ensure that the end product integrates this module so as to maintain a minimum distance of 20 cm between the equipment's radiating structure(s) and the body of the user or nearby persons. The OEM shall also advise its end user of this requirement as required by applicable rules.

## ORDERING INFORMATION

| Item                          | Order Number  | Description                                                                                                                                           |
|-------------------------------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| ARTIK 530 Module              | SIP-005AFS301 | –                                                                                                                                                     |
| ARTIK 530s Module             | SIP-005AFS302 | Includes 512MB DRAM                                                                                                                                   |
| ARTIK 530s 1G Module          | SIP-005AUS332 | Includes 1GB DRAM                                                                                                                                     |
| ARTIK 530 Development Kit     | SIP-KITNXD001 | ARTIK 530 Development Module<br>ARTIK 530/530s Interposer Board<br>Platform Board<br>Interface Board<br>Two Antennas (one 802.15.4, one BT/Wi-Fi)     |
| ARTIK 530s Development Kit    | SIP-KITNXD002 | ARTIK 530s Development Module<br>ARTIK 530/530s Interposer Board<br>Platform Board<br>Interface Board<br>Two Antennas (one 802.15.4, one BT/Wi-Fi)    |
| ARTIK 530s 1G Development Kit | SIP-KITNXG002 | ARTIK 530s 1G Development Module<br>ARTIK 530/530s Interposer Board<br>Platform Board<br>Interface Board<br>Two Antennas (one 802.15.4, one BT/Wi-Fi) |

For volume ordering of evaluation kits, contact a sales representative in your area or email [sales@artik.io](mailto:sales@artik.io).

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