AN218238

Hardware Design Guidelines for Using EZ-PD CCG3PA Devices in Power Adapter Applications

Author: Madhan Kumar K

Associated Part Family: CYPD3174, CYPD3175

Related Application Notes: AN218179, AN210403, AN200210

AN218238 provides an overview of the different USB Type-C power adapter applications that EZ-PD™ CCG3PA USB Type-C controllers can support and provides hardware design guidelines for the same. The application note primarily covers the capabilities of EZ-PD CCG3PA USB Type-C controllers and its associated hardware design guidelines for typical power adapter applications like notebook power adapters and mobile power adapters.

Contents

1 Introduction

EZ-PD CCG3PA belongs to Cypress' family of USB Type-C controllers that complies with the latest USB Type-C and Power Delivery (PD) standards. In addition, with the built-in overvoltage protection (OVP) and over-current protection (OCP), it helps to reduce the need for additional components and the overall cost of a Type-C ecosystem. Typical applications using CCG3PA include mobile power adapters, PC power adapters, power banks, and car chargers.

1.1 EZ-PD CCG3PA Features

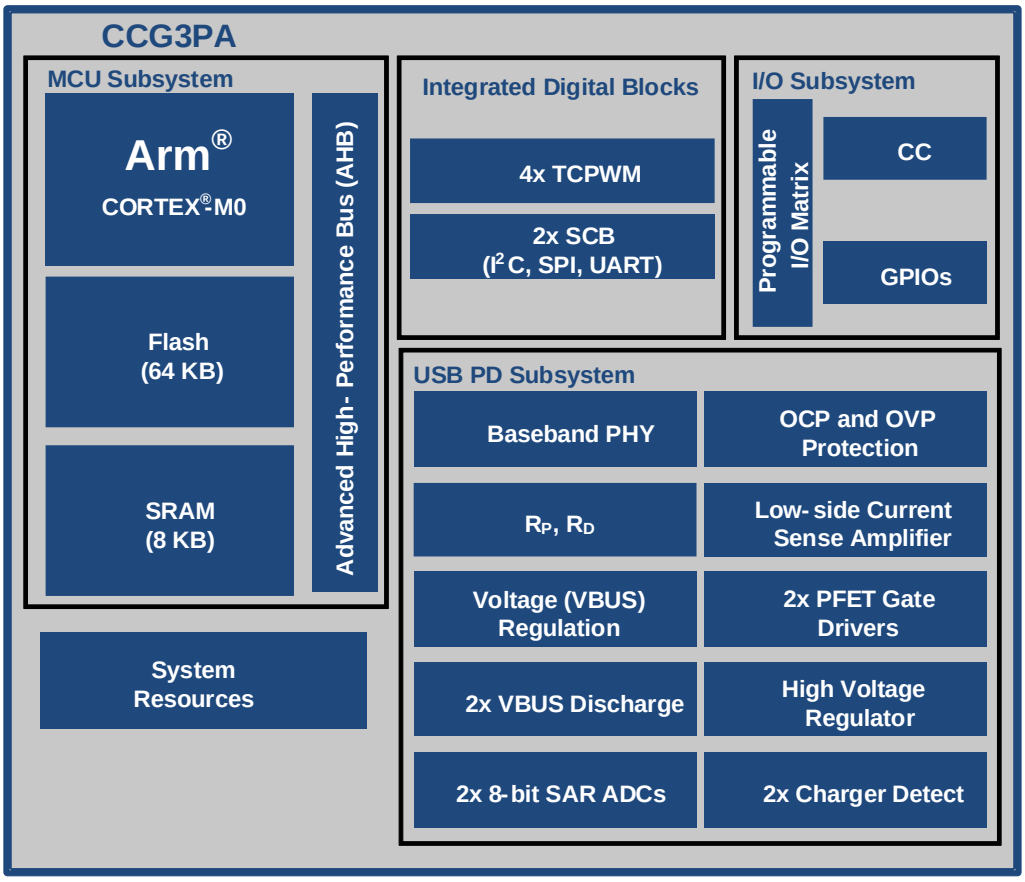
- Type-C Support and USB-PD Support
  - Supports USB PD 3.0 spec including Programmable Power Supply Mode
  - Configurable Resistors R_P and R_D
  - Supports one USB Type-C port and one Type-A port
- 2x Legacy/Proprietary Charging Blocks
  - Supports Quick Charge (QC) 4.0, Apple Charging 2.4A, Adaptive Fast Charging (AFC), Battery Charging (BC) 1.2
  - Integrates all required terminations on DP/DM lines
- Integrated Voltage (VBUS) Regulation and Current Sense Amplifier
  - Analog regulation of secondary-side feedback node (direct feedback or Opto coupler)
  - Integrated shunt regulator function for VBUS control
  - Constant current or constant voltage mode
  - Supports low-side current sensing for constant current control

- System-Level Fault Protection
  - On-chip OVP, OCP, Under Voltage Protection (UVP), and Short Circuit Protection (SCP)
  - Supports Over Temperature Protection (OTP) through integrated ADC circuit
- 32-bit MCU Subsystem
  - Arm® Cortex®-M0 CPU
  - 64 KB Flash
  - 8 KB SRAM
- Clocks and Oscillators
  - Integrated oscillator eliminating the need for external clock
- Power
  - 3.0 V to 24.5 V operation (30 V tolerant)
- System-Level ESD Protection
  - On Configuration Channel (CC), VBUS, and DP/DM pins
  - ± 8 kV Contact Discharge and ± 15 kV Air Gap Discharge based on IEC61000-4-2 level 4C
- Packages
  - 24-pin QFN and 16-pin SOIC
  - Supports extended industrial temperature range (-40° C to +105° C)

1.2 CCG3PA Block Diagram

Figure 1 shows a block diagram of the CCG3PA architecture. For more details, see the CCG3PA datasheet.

Figure 1. CCG3PA Architecture Block Diagram



1.3 CCG3PA Resources

For Type-C customers who are new to Cypress' existing hardware and software platforms, Table 1 lists the resources that will help in getting started with CCG3PA in their upcoming designs.

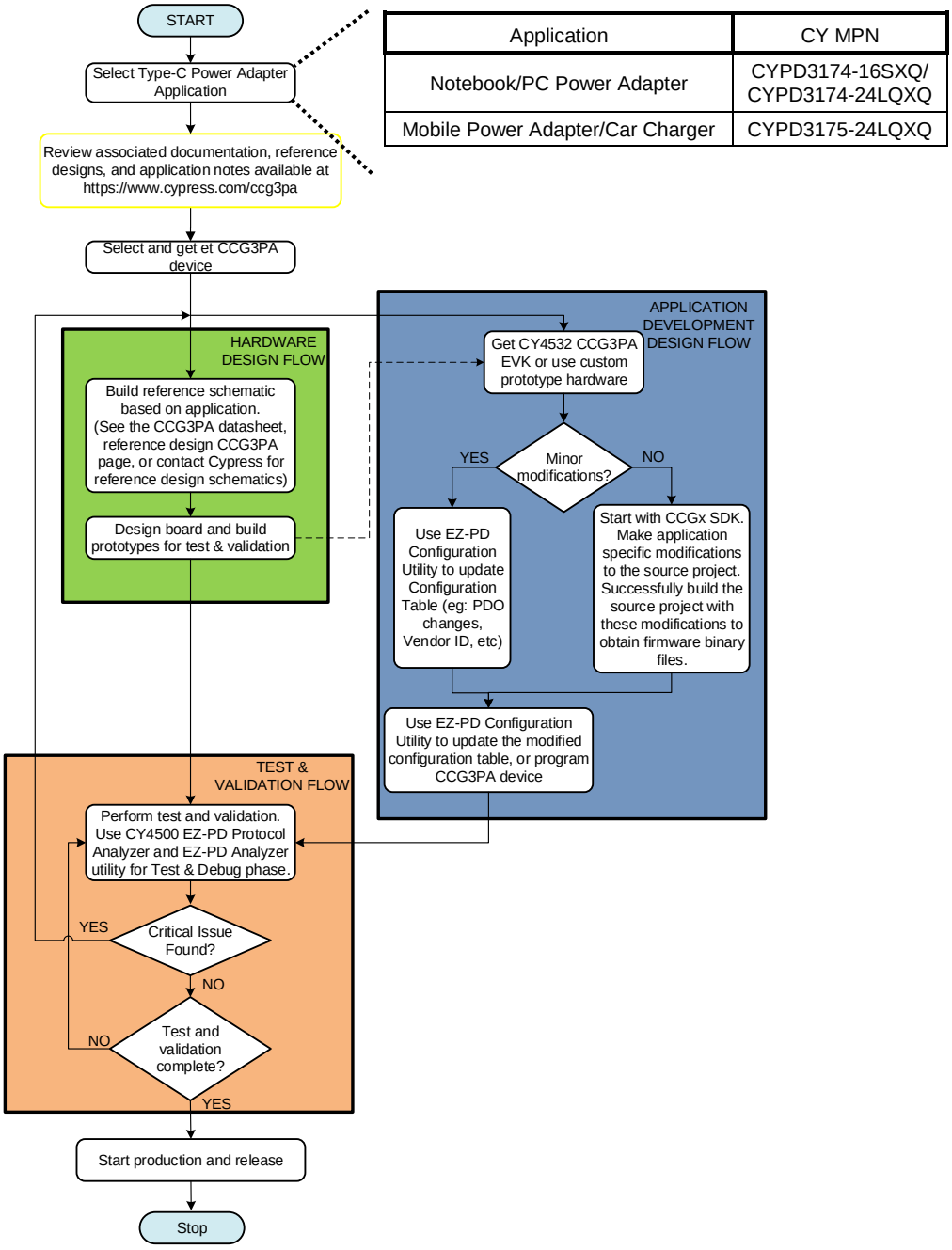
Table 1. CCG3PA Design Resources

Category	Available Resources
Datasheet	CCG3PA datasheet
Hardware	CY4532 CCG3PA EVK – Contains documentation and design files
Programming Specifications Document	CYPD3xxx Programming specifications – Provides guidelines on how to program the flash memory of CCG3PA devices
Host PC Software	EZ-PD CCGx SDK
Host PC Software Debugging Tools	EZ-PD Configuration Utility 1.1 or later (GUI-based Windows application that helps in configuring CCGx controllers)
	PSoC Creator™ 4.1 or later (firmware development tool)
	PSoC Programmer 3.26 or later (firmware programming tool)
	CY4500 EZ-PD™ Protocol Analyzer – Includes EZ-PD Analyzer Utility and documentation
Videos	USB Type-C Essentials, USB Type-C 101 Video Training Series
Other Collateral	CCG3PA specific Knowledge Base Articles
Reference Designs	CCG3PA Reference Designs

1.4 CCG3PA Design Flow

This section describes a typical design flow that you would go through during the Type-C application design from conceptual stage to manufacturing using CCG3PA devices. This section also covers how the hardware, software, and firmware resources described in this application note are used in the design flow. Figure 2 shows a typical design flow using CCG3PA devices.

Figure 2. CCG3PA Design Flow



Application	CY MPN
Notebook/PC Power Adapter	CYPD3174-16SXQ/ CYPD3174-24LQXQ
Mobile Power Adapter/Car Charger	CYPD3175-24LQXQ

After you determine the CCG3PA-based Type-C application and review the reference designers, you can start the application development phase in parallel.

The hardware development includes building reference schematics based on the end application and designing boards to get a few prototypes ready for the next phase. These reference schematics can be based on the reference designs available on Cypress' CCG3PA webpage.

The application development can begin with the CY4532 EZ-PD CCG3PA Evaluation Kit (EVK), so that it can proceed in parallel with hardware development. You can use the EZ-PD Configuration Utility to update the configuration table of the CCG3PA device (for example, changing PDOs and Vendor IDs). For making application-specific modifications, you can use the custom CCG3PA FW Package in the EZ-PD CCGx Software Development Kit (SDK).

Once the hardware and application development are completed, the existing system design is ready for the test and validation cycle. You can use the CY4500 EZ-PD Protocol Analyzer for testing, firmware debugging, and performance analysis. Mass production and manufacturing can start once test and validation is complete and the system design is final.

2 Feedback Systems

CCG3PA is the first device in the family of CCGx devices from Cypress to handle analog feedback mechanisms with upstream AC-DC or DC-DC converters so that the output VBUS voltage can be regulated.

These feedback mechanisms can be split into two main categories – Direct feedback and Opto feedback systems. Apart from these, CCG3PA (like the previous generation of CCGx devices) also provides feedback using PWM or serial interface protocols like I^2C. See the following example designs for CCG3PA that showcase the implementation of different feedback mechanisms:

- Direct Feedback – CCG3PA USB-C Mobile Power Adapter Solution
- Opto Feedback – CCG3PA USB-C Notebook Power Adapter Solution
- Direct Feedback and PWM Feedback – CY4532 EZ-PD™ CCG3PA Evaluation Kit

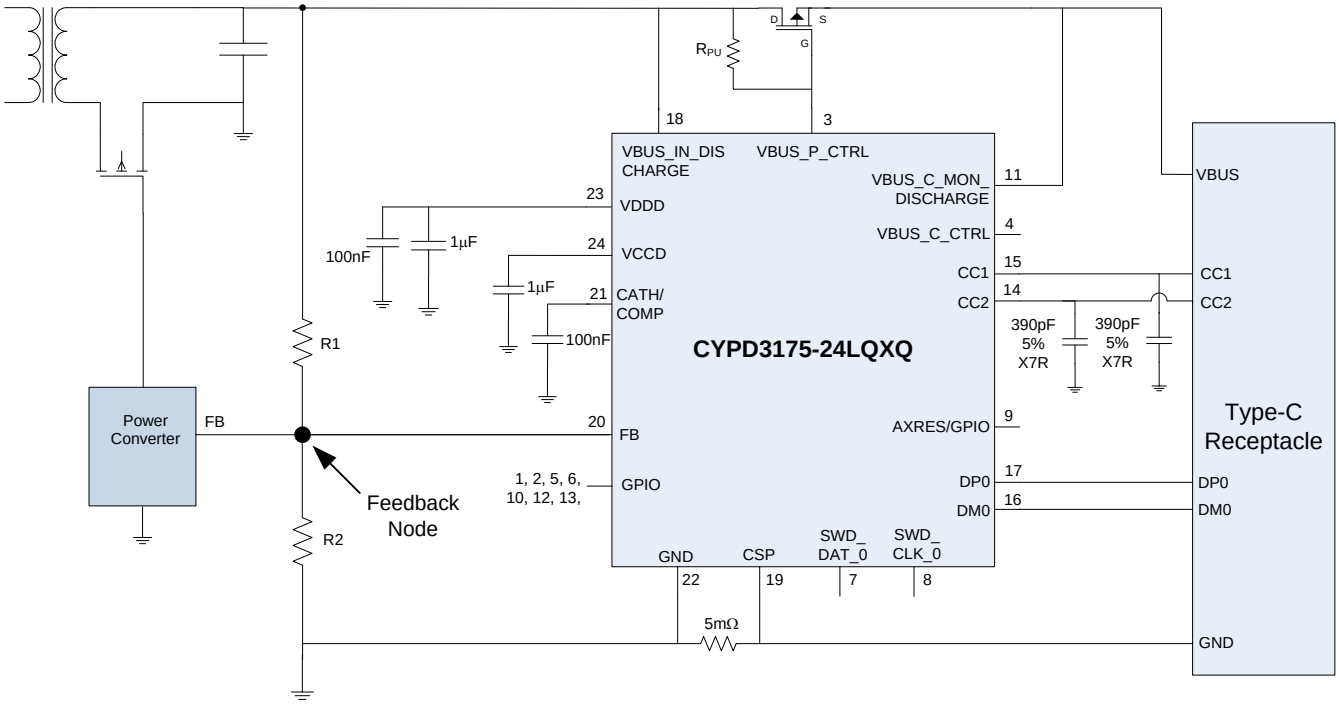
The scope of this application note does not include the hardware design guidelines for power bank applications or car charger applications. See the documentation of the CY4532 EZ-PD™ CCG3PA Evaluation Kit for further details on these applications.

2.1 Direct Feedback System

In a direct feedback system, as shown in Figure 3, CCG3PA regulates the VBUS voltage by sinking or sourcing current on the Feedback (FB) pin (pin 20 of 24-QFN parts and pin 1 of 16-SOIC parts). CCG3PA can source up to 12.7 µA and can sink up to 102.3 µA of current on the FB pin. For both source and sink, the current step size is 100 nA.

CCG3PA USB-C Mobile Power Adapter Solution uses direct feedback control to regulate VBUS.

Figure 3. CCG3PA Application Diagram Using Direct Feedback System



2.1.1 Feedback Resistor Divider

The feedback resistor divider comprises resistors R1 and R2. The resistors must be chosen to meet the below criteria:

- At 5 V VBUS, without CCG3PA sourcing or sinking any current, the voltage at the feedback node should be the default feedback voltage expected by the power converter.
- With up to 102.3 µA current sinking and up to 12.7 µA current sourcing, you should be able to regulate VBUS in the desired output voltage range by sourcing or sinking current using application firmware.
- If PPS (Programmable Power Supply) support is required, then the application should be able to achieve a 20 mV change in VBUS value with the smallest step size of current sink or source change - i.e. 100 nA.

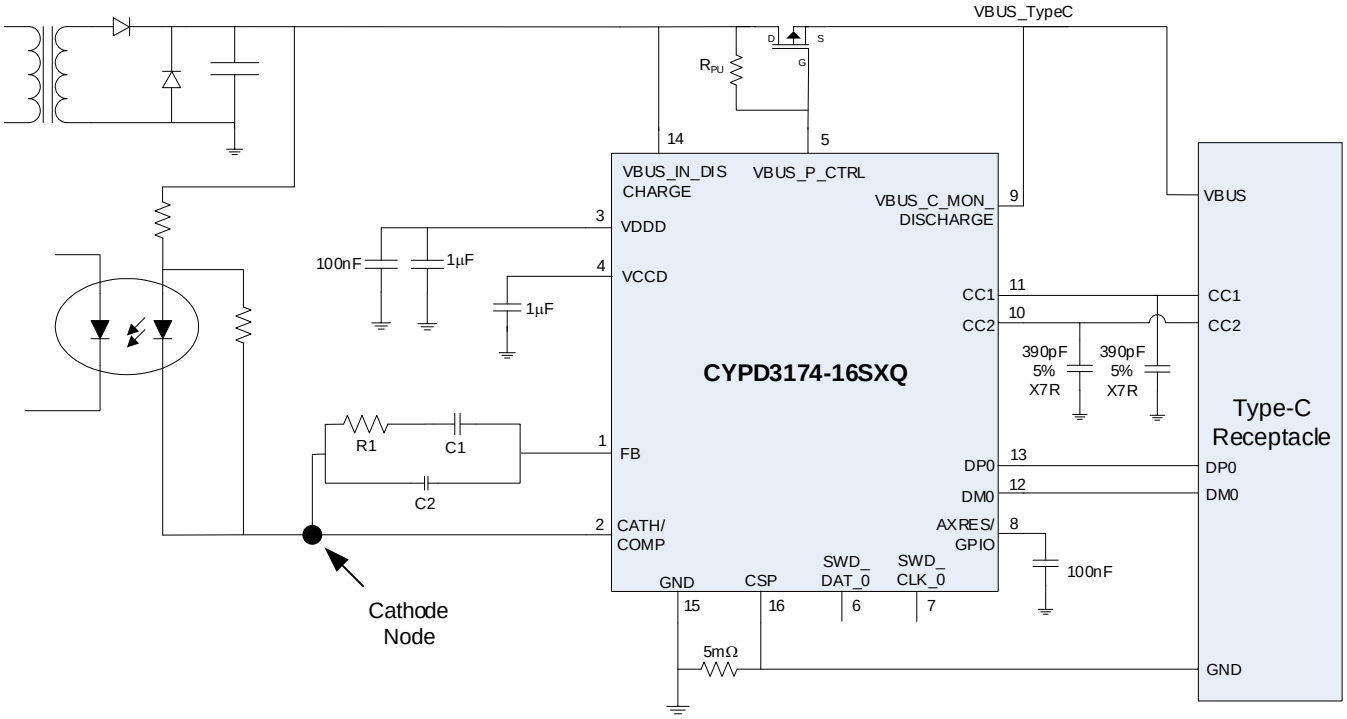
For example, consider a design where the default feedback voltage is 1.265V and the required VBUS range is 3V to 20V with PPS support. In this case, feedback resistors 200K and 68K meet all the above criteria since:

- At 5 V VBUS, the voltage at the feedback node FB is 1.265 V.
- To bring VBUS down to 3 V, CCG3PA needs to source 10 µA of current; to push VBUS to 20 V, it needs to sink 75 µA of current.
- With a step change of 100 nA, the proportional change in VBUS will be 20 mV.

2.2 Opto Feedback System

In an Opto feedback system as shown in Figure 4, CCG3PA provides feedback to the primary AC-DC converter through an Opto-coupler. CCG3PA regulates VBUS by controlling the current drawn through the cathode (CATH) node. CCG3PA USB-C Notebook Power Adapter Solution uses Opto feedback to regulate VBUS. This design uses the 16 SOIC variant of CYPD3174. There is a 24 QFN variant of CYPD3174 as well; see the CCG3PA datasheet for more information on the different packages available.

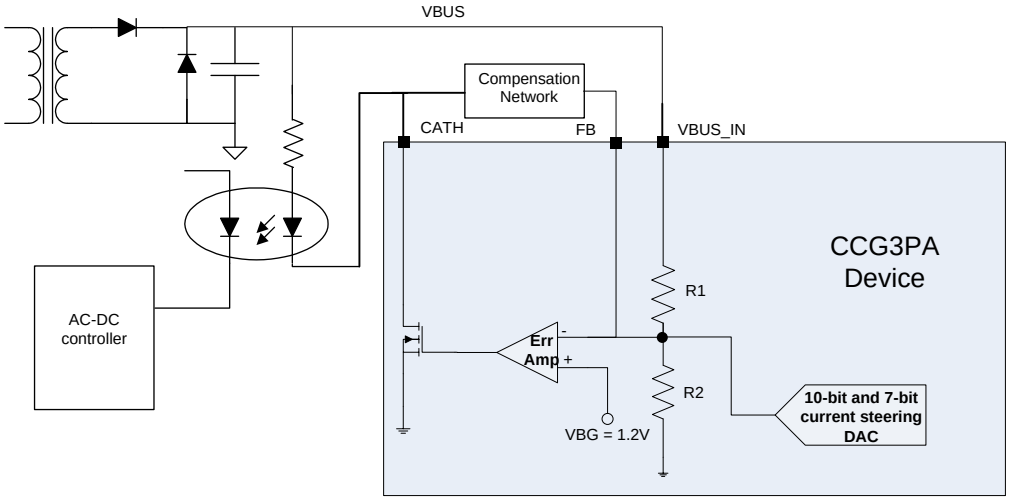
Figure 4. CCG3PA Application Diagram Using Opto Feedback System



2.2.1 Compensation Network

In an Opto feedback system, the VBUS voltage is regulated in a closed loop as shown in Figure 5. The default VBUS voltage is dictated by the VBG input voltage and resistor divider formed by R1 and R2. VBG and the internal resistor divider values are set such that the default VBUS is 5 V. Internal current steering DACs are used to modify VBUS. With an IDAC step size of 100 nA, CCG3PA can regulate VBUS in a 20 mV step size. The maximum current drawn through the feedback path via the CATH pin is 10 mA.

Figure 5. CCG3PA Internal Block Diagram with Compensation Network



An external compensation network similar to the one shown in Figure 4 is required between the FB and CATH/COMP pins (pins 20 and 21 on 24-QFN parts, pins 1 and 2 on 16-SOIC parts). Note that the compensation network component values are not generic and must be designed in alignment with the rest of the power control circuit. The value of the passive components (R1, C1, and C2) used in the Opto feedback system design CCG3PA USB-C Notebook Power Adapter Solution are specific to this particular design and were derived using simulation models.

3 CV and CC Modes of Operation

CCG3PA primarily supports two modes of regulation – Constant Voltage(CV) and Constant Current(CC) modes. In the CV mode, VBUS is held constant irrespective of the load current. In the CC mode, VBUS is varied such that the load current remains constant. In the CC mode of operation, CCG3PA monitors the load current using the internal Low Side Current Sense Amplifier (LSCSA) and varies VBUS such that the load current stays at the set target.

In terms of external components, a compensation capacitor is required for the CC mode of operation. For the Direct feedback system, the compensation capacitor must be added on the CATH/COMP pin as shown in Figure 3. In an Opto feedback system, since there is no dedicated CATH/COMP pin, the capacitor can be placed on any available GPIO. It is recommended to place the capacitor on P2.0 in an Opto feedback design as shown in Figure 4. The suggested value for the compensation capacitor is 100nF.

4 VBUS Discharge

CCG3PA supports VBUS discharge capability on both VBUS_IN and VBUS_TypeC (before the source of the provider FET and after the drain of the provider FET) ends. VBUS_IN discharge is via the VBUS_IN_DISCHARGE pin (pin 18 on 24-QFN parts, pin 14 on 16-SOIC parts) while VBUS_TypeC discharge is via the VBUS_C_MON_DISCHARGE pin (pin 11 on 24-QFN parts, pin 9 on 16-SOIC parts). The discharge FET and the resistors are internal to CCG3PA and no external components are needed for either discharge path. See application block diagrams Figure 3 and Figure 4 for the discharge path connections.

Discharge drive strength is configurable on both the VBUS_IN and VBUS_TypeC ends. The internal discharge resistor can be set in the range of 31.25 Ω to 2000 Ω. The discharge rate can also be modulated by the application using an internal PWM signal, where the discharge ON and OFF time is controlled by the PWM signal.

5 Current Sense Amplifier

CCG3PA integrates a Low Side Current Sense Amplifier (LSCSA). The suggested value for the current sense resistor is 5 mΩ. For current sense accuracy, it is critical to ensure in the layout that the sense resistor is placed close to the CS pin (pin 19 on 24-QFN parts, pin 16 on 16-SOIC parts) and the trace resistance is as minimum as possible. In many power adapter designs, the upstream AC-DC controller might also have a requirement to monitor the load current and the current sense resistor would be part of the secondary loop. As an example, see the design CCG3PA USB-C Mobile Power Adapter Solution for reference schematics and layout where the drop across the current sense resistor R12 is monitored by both CCG3PA device and the upstream AC-DC controller.

6 CC and D+/D- Terminations

CCG3PA supports the terminations needed on the CC line for Type-C power delivery. It also has the required terminations on the D+/D- lines to support legacy charging protocols such as BC1.2, Samsung AFC, Apple Charging, and Qualcomm Charging. This feature is useful in systems which require legacy charging over both Type-C and Type-A ports. The only external component needed is a 390 pF capacitor on each of the CC lines (CC1 and CC2).

For more information on the legacy protocols supported, see the CCG3PA datasheet.

7 PFET Gate Drivers

CCG3PA integrates two PFET gate drivers – one each for the VBUS provider and consumer paths. VBUS_P_CTRL and VBUS_C_CTRL are the two PFET gate driver pins. An external pull-up resistor is needed for both the gate driver circuits. This is shown as R_{PU} in Figure 3 and Figure 4. Since Figure 3 and Figure 4 are for power adapter applications only, the VBUS_C_CTRL pin (if available) is left unconnected. VBUS_C_CTRL is a simple pull-down switch where it pulls the line LOW to turn ON the PFET and stays at Hi-Z to turn OFF the PFET. VBUS_P_CTRL has similar features as VBUS_C_CTRL, except that it provides an additional feature to control the FET turn-on rate. This feature is intended to limit the in-rush current.

Document History

Document Title: AN218238 – Hardware Design Guidelines for Using EZ-PD CCG3PA Devices in Power Adapter Applications

Document Number: 002-18238

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5969811	MKKU	12/12/2017	New application note.

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Videos | Blogs | Training | Components

Technical Support

cypress.com/support

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709