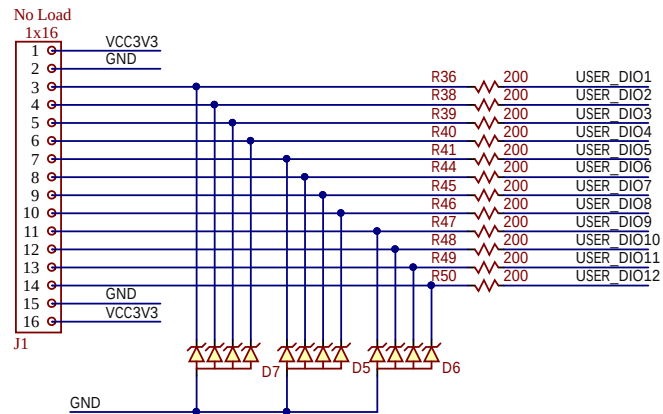
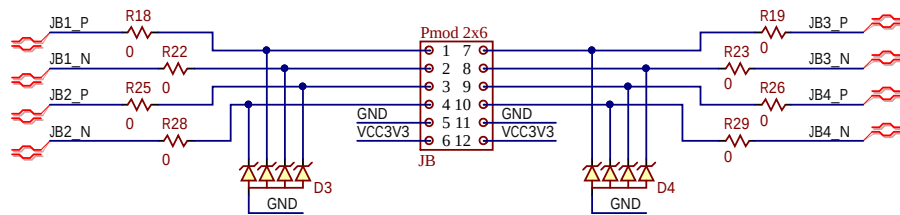
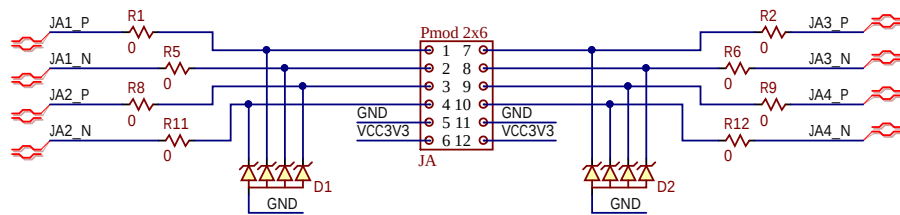
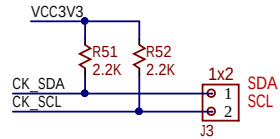
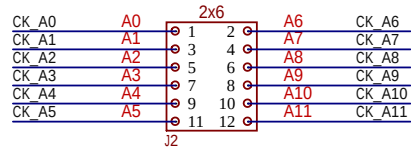


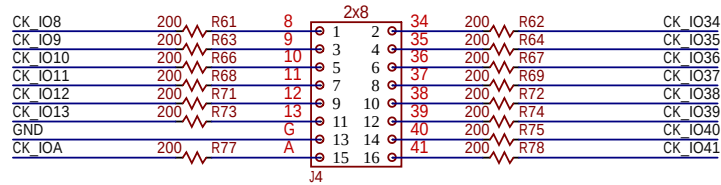
Foot
F1
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F2
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F3
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F4

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Circuit PMods, User I/O	 DIGILENT®	
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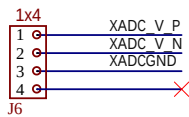
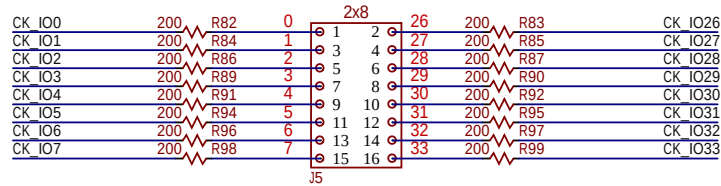
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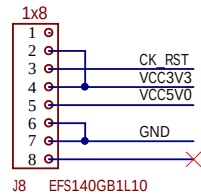
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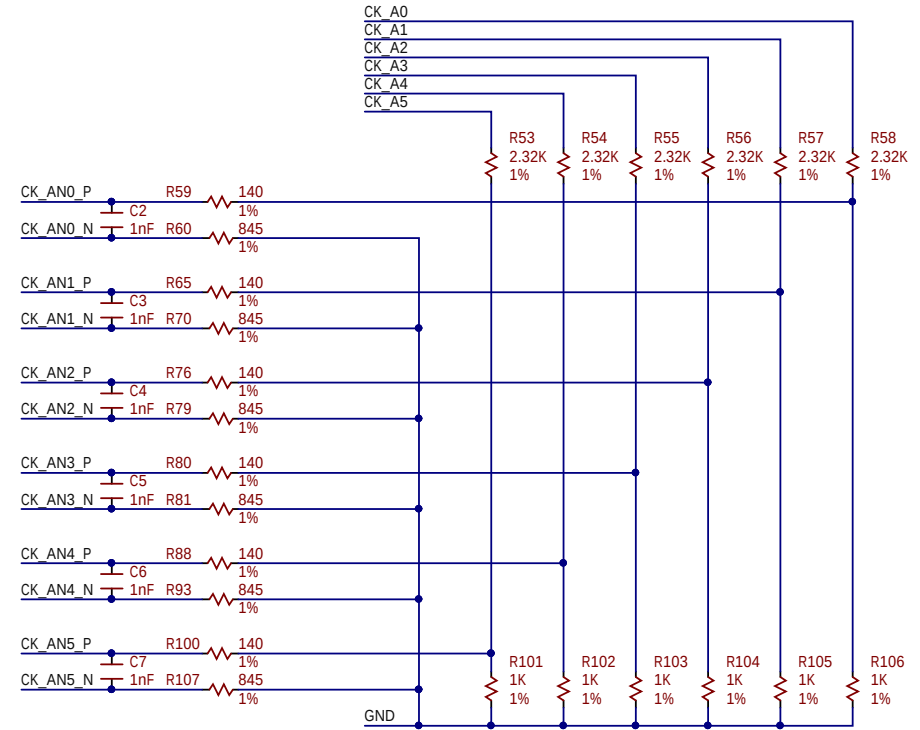
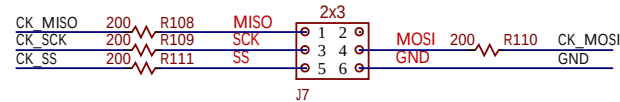
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POWER



SPI



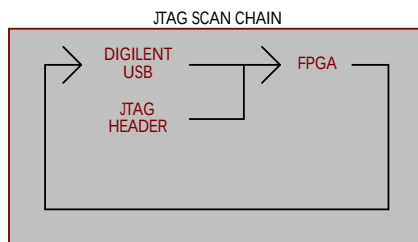
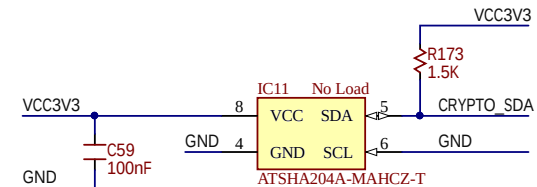
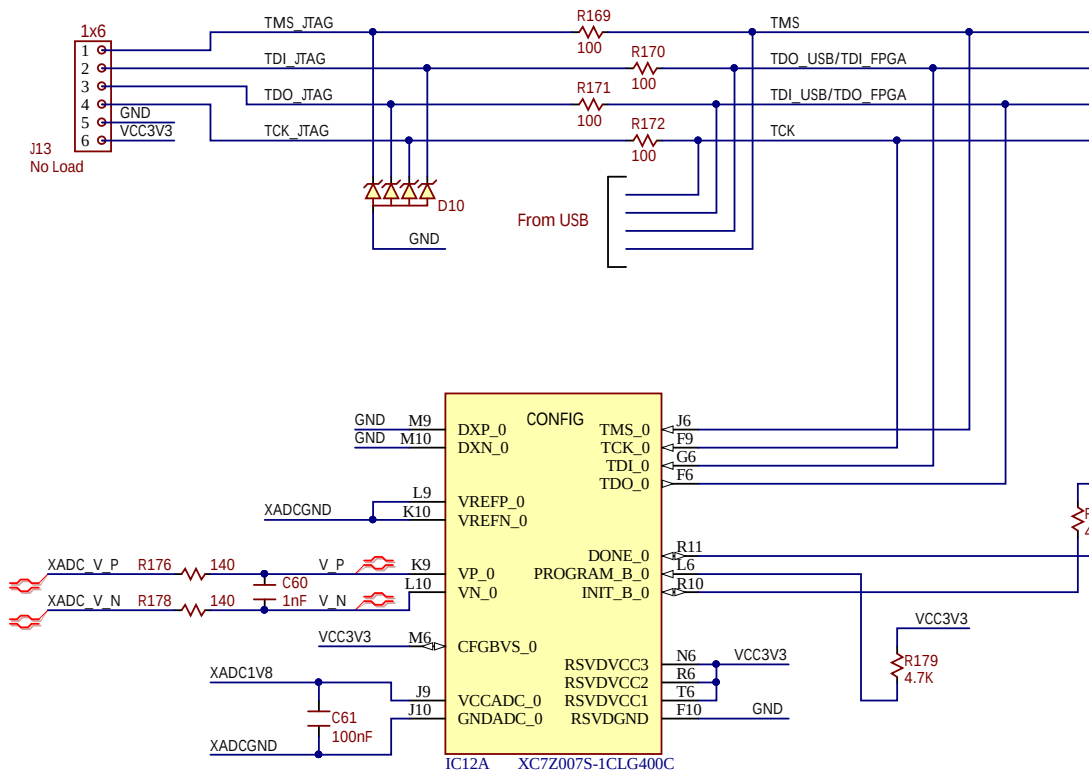
Note: Terminate N signals next to Analog Header

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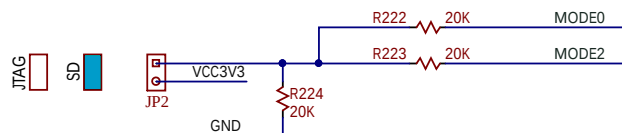
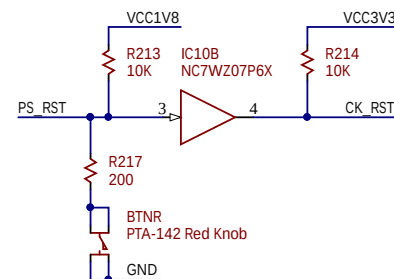
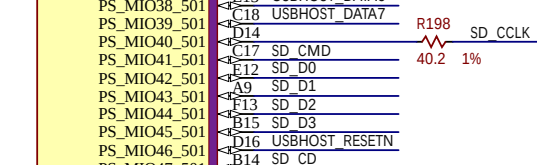
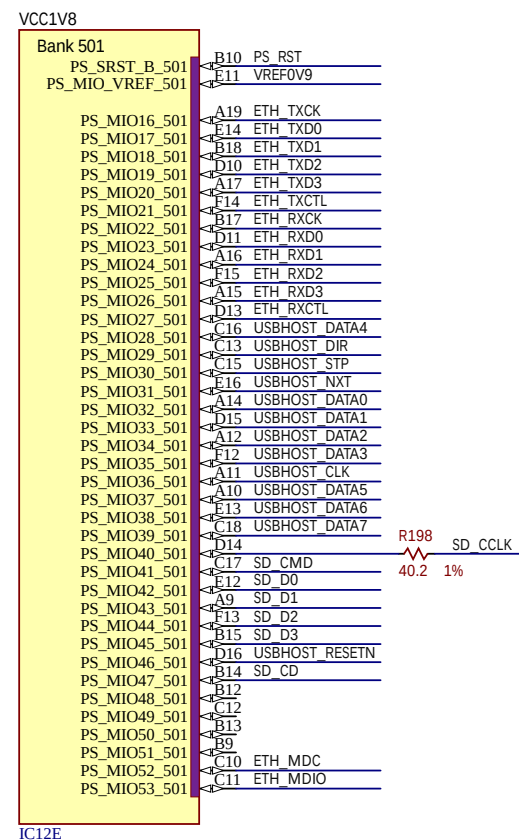
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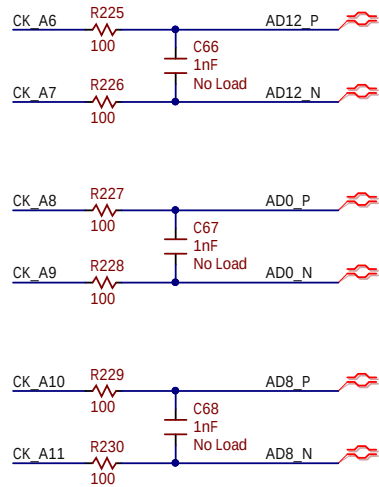
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Author GMA		
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VCC3V3

BANK 34

IO_0_34	R19	USER_DIO6
IO_L1P_T0_34	T11	JB2 P
IO_L1N_T0_34	T10	JB2 N
IO_L2P_T0_34	T12	CK MOSI
IO_L2N_T0_34	U12	CK IO27
IO_L3P_T0_DQS_PUDC_B_34	U13	CK IO28
IO_L3N_T0_DQS_34	V13	CK IO1
IO_L4P_T0_34	V12	JB4 P
IO_L4N_T0_34	W13	JB4 N
IO_L5P_T0_34	T14	CK IO2
IO_L5N_T0_34	T15	CK IO3
IO_L6P_T0_34	P14	CK A5
IO_L6N_T0_VREF_34	R14	CK IO7
IO_L7P_T1_34	Y16	JA2 P
IO_L7N_T1_34	Y17	JA2 N
IO_L8P_T1_34	W14	JB1 P
IO_L8N_T1_34	Y14	JB1 N
IO_L9P_T1_DQS_34	T16	CK IO30
IO_L9N_T1_DQS_34	U17	CK IO31
IO_L10P_T1_34	V15	CK IO29
IO_L10N_T1_34	W15	CK MISO
IO_L11P_T1_SRCC_34	U14	CK IO0
IO_L11N_T1_SRCC_34	U15	CK IO10
IO_L12P_T1_MRCC_34	U18	JA3 P
IO_L12N_T1_MRCC_34	U19	JA3 N
IO_L13P_T2_MRCC_34	N18	CK IO8
IO_L13N_T2_MRCC_34	P19	USER_DIO5
IO_L14P_T2_SRCC_34	N20	USER_DIO3
IO_L14N_T2_SRCC_34	P20	USER_DIO4
IO_L15P_T2_DQS_34	T20	USER_DIO7
IO_L15N_T2_DQS_34	U20	USER_DIO9
IO_L16P_T2_34	V20	USER_DIO10
IO_L16N_T2_34	W20	USER_DIO11
IO_L17P_T2_34	Y18	JA1 P
IO_L17N_T2_34	Y19	JA1 N
IO_L18P_T2_34	V16	JB3 P
IO_L18N_T2_34	W16	JB3 N
IO_L19P_T3_34	R16	CK IO26
IO_L19N_T3_VREF_34	R17	CK IO6
IO_L20P_T3_34	T17	CK IO32
IO_L20N_T3_34	R18	CK IO33
IO_L21P_T3_DQS_34	V17	CK IO4
IO_L21N_T3_DQS_34	V18	CK IO5
IO_L22P_T3_34	W18	JA4 P
IO_L22N_T3_34	W19	JA4 N
IO_L23P_T3_34	N17	CK IO35
IO_L23N_T3_34	P18	CK IO34
IO_L24P_T3_34	P15	CK SDA
IO_L24N_T3_34	P16	CK SCL
IO_25_34	T19	USER_DIO8

IC12B

VCC3V3

BANK 35

IO_0_35	G14	LED1 B
IO_L1P_T0_AD0P_35	C20	AD0 P
IO_L1N_T0_AD0N_35	B20	AD0 N
IO_L2P_T0_AD8P_35	B19	AD8 P
IO_L2N_T0_AD8N_35	A20	AD8 N
IO_L3P_T0_DQS_AD1P_35	E17	CK AN0 P
IO_L3N_T0_DQS_AD1N_35	D18	CK AN0 N
IO_L4P_T0_35	D19	BTN1
IO_L4N_T0_35	D20	BTN0
IO_L5P_T0_AD9P_35	E18	CK AN1 P
IO_L5N_T0_AD9N_35	E19	CK AN1 N
IO_L6P_T0_35	F16	CK SS
IO_L6N_T0_VREF_35	F17	CK A0
IO_L7P_T1_AD2P_35	M19	USER_DIO2
IO_L7N_T1_AD2N_35	M20	CK IOA
IO_L8P_T1_AD10P_35	M17	CK IO36
IO_L8N_T1_AD10N_35	M18	CK IO9
IO_L9P_T1_DQS_AD3P_35	L19	USER_DIO1
IO_L9N_T1_DQS_AD3N_35	L20	CK IO41
IO_L10P_T1_AD11P_35	K19	USER_DIO12
IO_L10N_T1_AD11N_35	T19	CK A1
IO_L11P_T1_SRCC_35	L16	CK A3
IO_L11N_T1_SRCC_35	L17	CK IO37
IO_L12P_T1_MRCC_35	K17	CK A2
IO_L12N_T1_MRCC_35	K18	CK IO11
IO_L13P_T2_MRCC_35	H16	SYSCLK
IO_L13N_T2_MRCC_35	H17	CK IO38
IO_L14P_T2_AD4P_SRCC_35	F18	CK IO12
IO_L14N_T2_AD4N_SRCC_35	F18	CK IO39
IO_L15P_T2_DQS_AD12P_35	F19	AD12 P
IO_L15N_T2_DQS_AD12N_35	F20	AD12 N
IO_L16P_T2_35	G17	LED0 G
IO_L16N_T2_35	G18	CK IO40
IO_L17P_T2_AD5P_35	H20	CK AN4 P
IO_L17N_T2_AD5N_35	H20	CK AN4 N
IO_L18P_T2_AD13P_35	G19	CK AN5 P
IO_L18N_T2_AD13N_35	G20	CK AN5 N
IO_L19P_T3_35	H15	CK SCK
IO_L19N_T3_VREF_35	G15	CK IO13
IO_L20P_T3_AD6P_35	J14	CK AN2 N
IO_L20N_T3_AD6N_35	N15	LED0 R
IO_L21P_T3_DQS_AD14P_35	N16	CK A4
IO_L21N_T3_DQS_AD14N_35	L14	LED1 G
IO_L22P_T3_AD7P_35	L15	LED0 B
IO_L22N_T3_AD7N_35	M14	
IO_L23P_T3_35	M15	LED1 R
IO_L23N_T3_35	K16	CK AN3 P
IO_L24P_T3_AD15P_35	J16	CK AN3 N
IO_L24N_T3_AD15N_35	J15	CRYPTO SDA
IO_25_35		

IC12C

Title

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FPGA Banks, Anti Alias Filters

Doc#

500-370

Engineer

MTA/IC

Author

GMA

Date

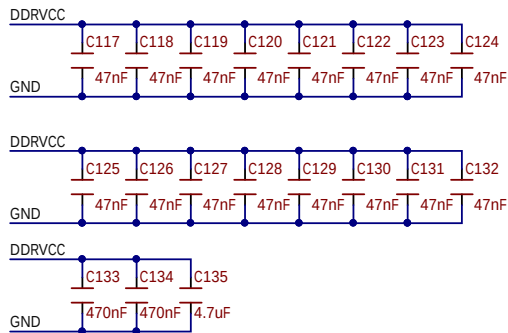
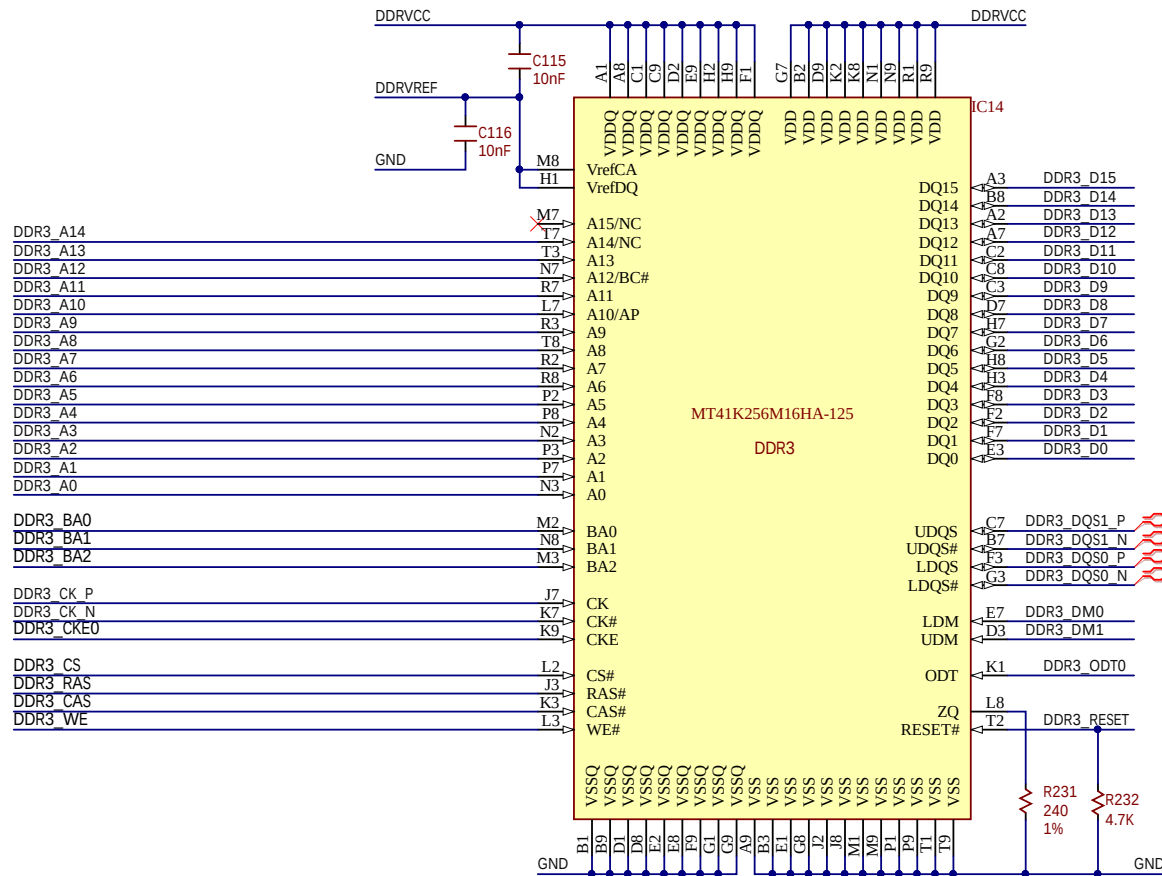
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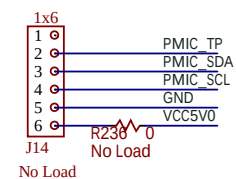
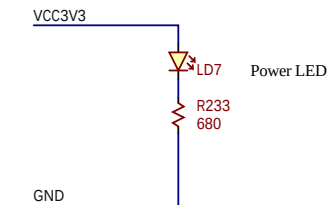
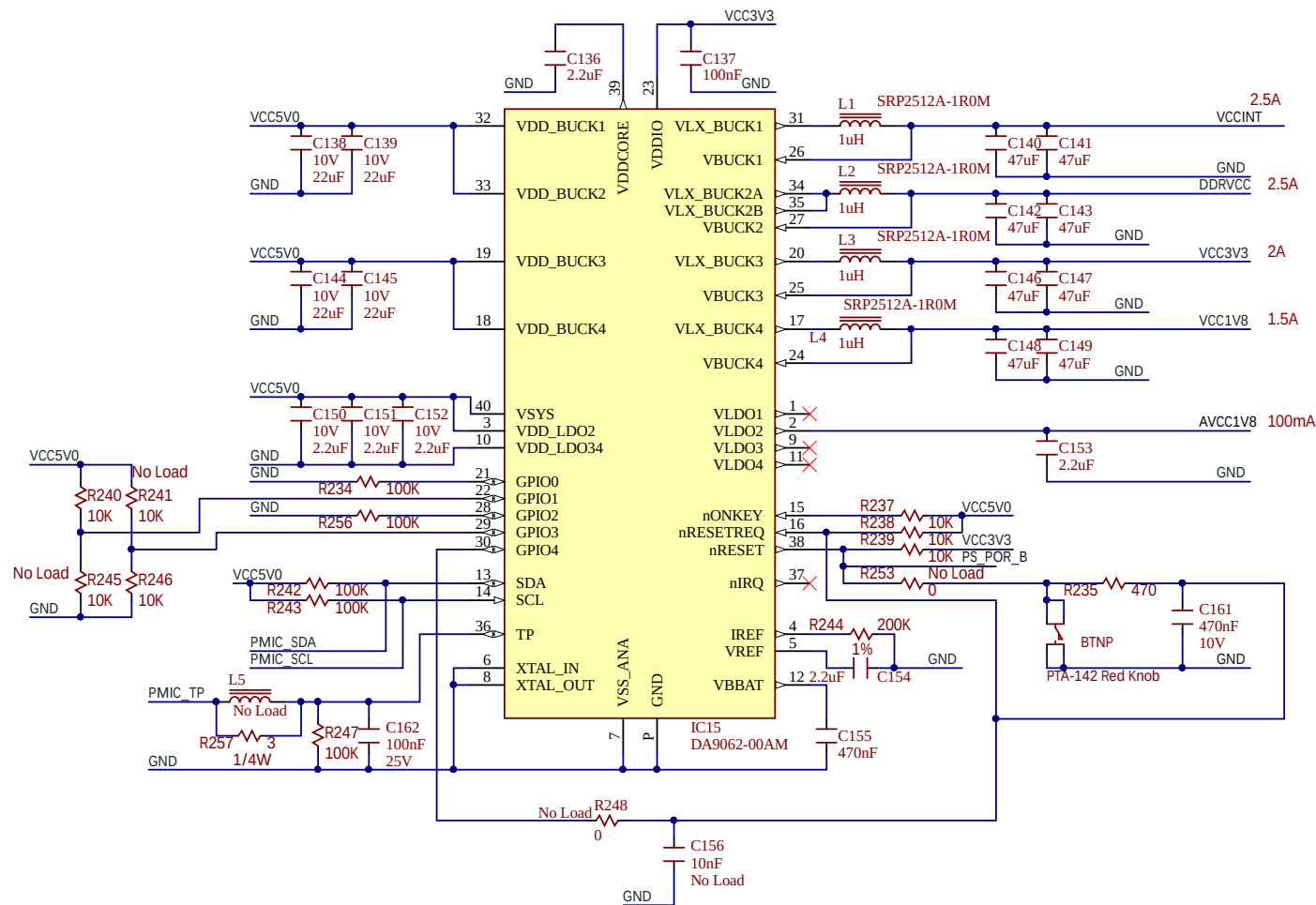






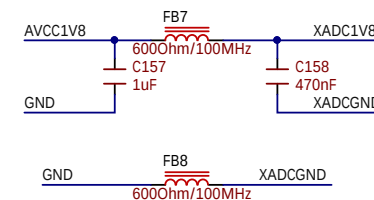
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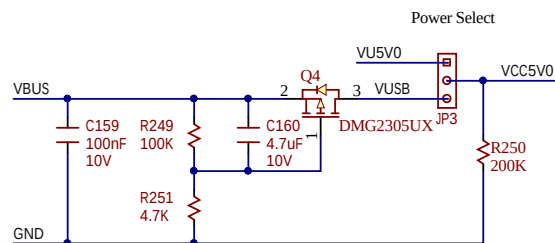
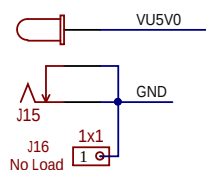


VCCINT Voltage Configuration		
R240	R245	VCCINT
Load	No Load	1.0V 0.95V

DDR Voltage Configuration		
R241	R246	DDRVCC
Load	No Load	1.5V 1.35V



Note: Input Voltage 5V only!



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