# TECHNICAL INFORMATION

## CERAMIC MULTILAYER CAPACITORS IN HF SMPS APPLICATIONS

by
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## Abstract

There has been an explosion of interest in the use of ceramic capacitors for high frequency power conversion applications. This interest is compounded with new designs striving for higher frequencies, smaller sizes and greater efficiencies. This application is an ongoing and mutual development of ceramic values, processes and sizes that were never realized prior to this application. In more and more cases, the ceramic capacitor is dictated by performance requirements never attainable in the previous styles of electrolytic and tantalum.

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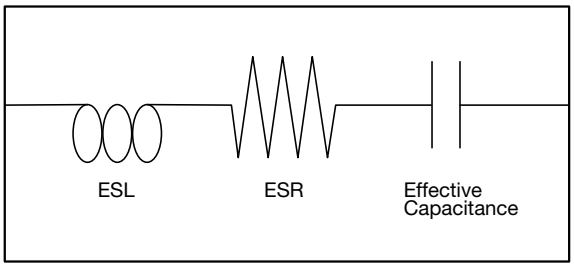
## Development

Previous to the ceramic output filter capacitor, a high energy discharge capacitor has been manufactured for the past 20 years. The application was military and replaced a reconstituted mica that was 20 times its volume and mass. The current discharge requirement was a minimum of 2100 Amperes peak. Reliability testing to assure this capability involved a discharge life test where the part was repeatedly discharged at room ambient and the temperature extremes. Each discharge current burst was monitored to assure the 2100 Ampere peak requirement.

This high current capability didn't happen as a matter of fact, but represented an understanding of elemental performance required and the processes and materials needed to achieve this high current capability.

With our first request for a ceramic output filter capacitor, 50 µF @ 50 WVDC, we knew we had capabilities of value in the design of the high energy capacitor. Modification of design that required thinner dielectric (50 WVDC vs. 750 WVDC) was a simple fix to offering samples but we wanted to know how the performance of the ceramic could be enhanced to give the greatest improvement over the previous style in this application.

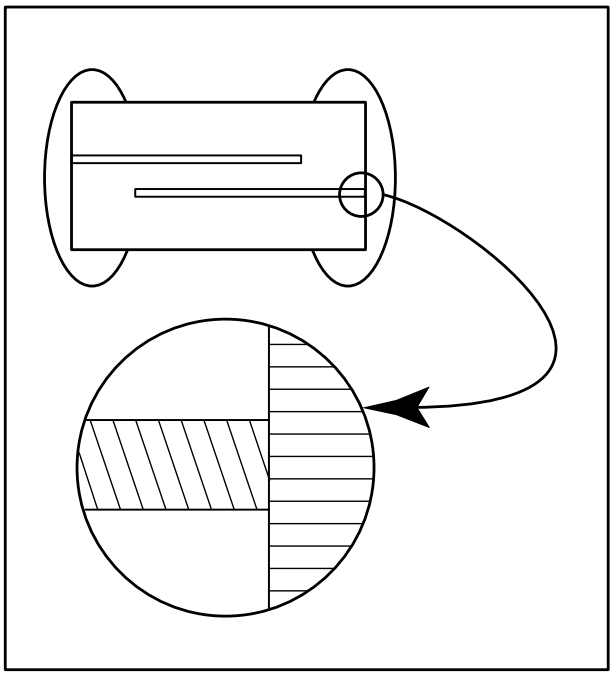
Figure 1.




From the frequency performance of this device, an equivalent circuit was constructed as in Figure 1. We decided that we could have an impact on the ESR (Effective Series Resistance) and ESL (Effective Series Inductance) by changing the geometry of the design. The aspect ratio was targeted to be as low as possible for two reasons. First, from ohms law the quick reduction in any resistance attributed to the electrode plate is effected by reducing the length while increasing the width for individual plate current. By the same geometry fix for ESR, a reduction in ESL was also to be realized.

Another improvement is traceable to the manner in which the internal electrode is electrically connected to the external termination. This contact is of two dissimilar metals and is mostly physical as depicted in Figure 2. There is a resistance attributed to this contact area and is a major contributor of the ESR. By making this contact as wide as possible, the effect of this contact resistance is greatly reduced.

Figure 2.



At this time I would like to discuss the phenomena of changing ESR noted for the ceramic capacitor. The resistance attributed to the contact between internal electrode and external metal termination is complex. There are two metallic bodies separated by a contact resistance—a capacitor with very high leakage in an extremely thin dielectric. As frequency increases, the impedance of this contact is reduced by the increasing effect of the capacitive reactance (ESR going down as frequency increases). This phenomena is then overshadowed by the increasing resistance of the plate ("skin effect") as frequency increases along with some

Figure 3.

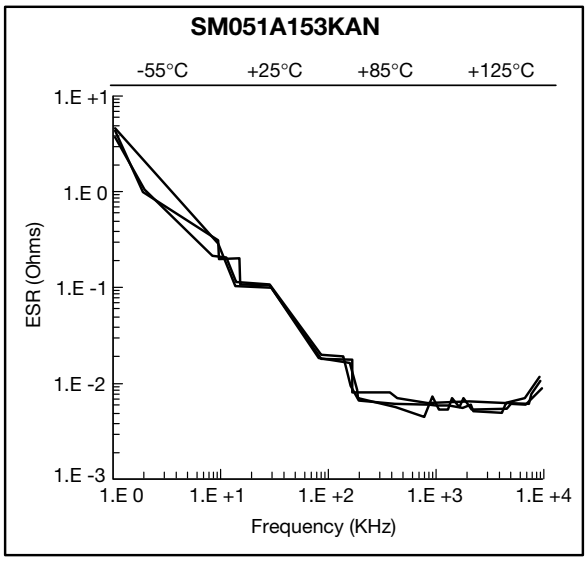
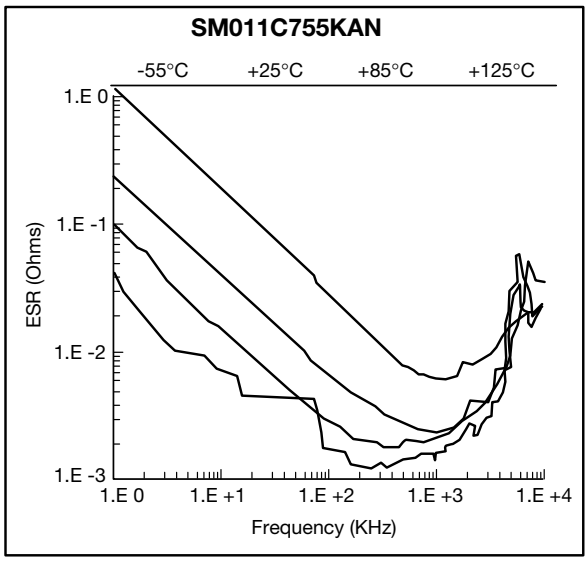



Figure 4.




increase in energy loss in the dielectric, resulting in the ESR increasing. There is also the contribution of the dielectric in ESR. There is an energy expended in aligning molecular polarization in support of an electric field. This energy loss is dependent upon the freedom of the molecular alignment and amount of support, thus dependent upon the kinetic energy or temperature and dielectric.

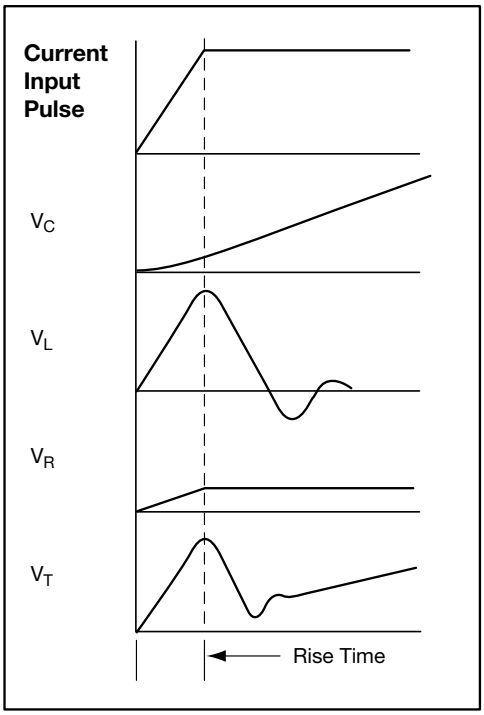
The temperature and frequency sensitivity for two dielectric types is shown in Figures 3 and 4. Figure 3 is an NP0, SM05, 100WVDC, 0.15 µF capacitor while Figure 4 is an X7R, SM01, 100 WVDC, 7.5 µF unit. With temperature, the metals contract and expand changing the pressure and resistance of the contact area. Because the energy expended in field support for the X7R is so much greater than that of the NP0, the amount of change seems proportional to dielectric constant.

The change in ESR for the X7R from the 25°C reference is almost a 500% increase at -55°C and approximately a 75% reduction at +125°C.

## Performance

A four terminal impedance meter was used to do parametric characterization through a given frequency range (HP4192 and HP4191 Impedance Analyzers) We have also used a more dynamic test by current pulse injection. By injecting a current pulse with a known rise-time into the capacitor, the elements of ESR, ESL and Capacitance can be deduced from the resulting voltage developed across the capacitor.

Figure 5.

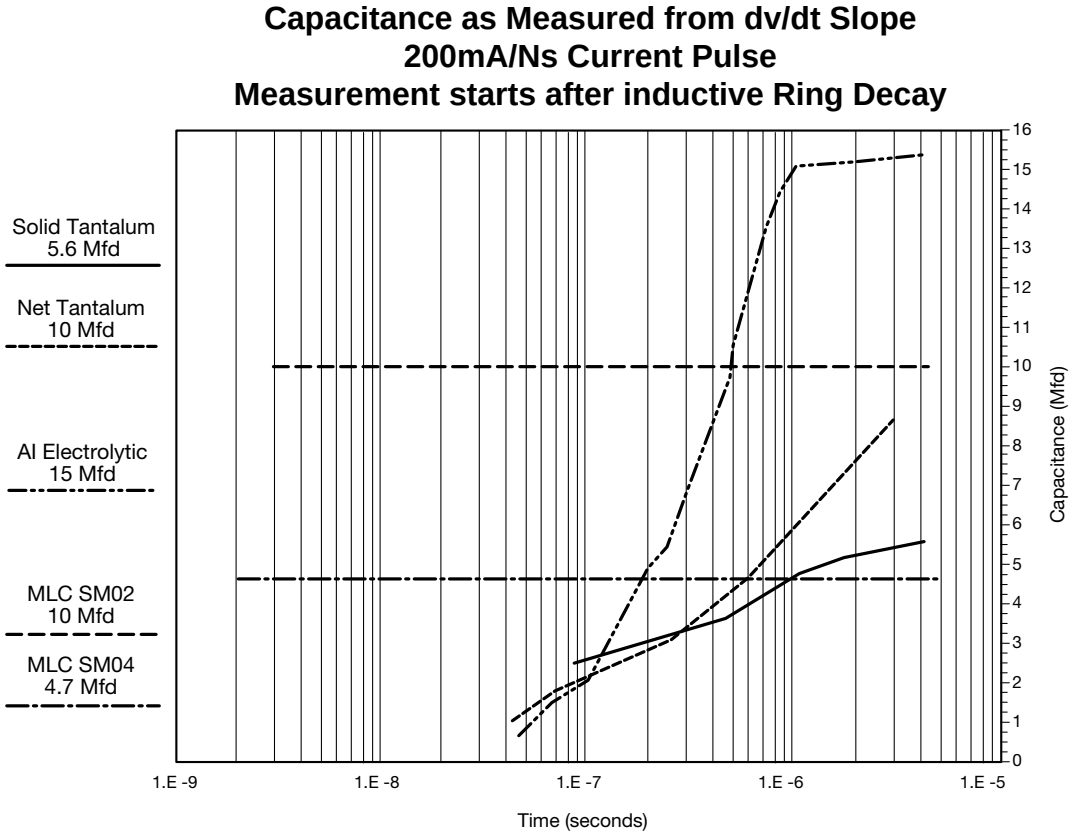



To review this test interpretation as in Figure 5, an ideal capacitor (no ESR or ESL), would have an exponentially rising voltage during the transition or rise time. During the constant current phase, a charge is being built up at a constant rate and the resulting dv/dt response would be linear and at a constant rate.

The inductive element would respond with a voltage generated during the transition equal to the product of the inductance and the di/dt. After the rise time, the voltage will fall to zero at some time depending upon the magnitude of inductance, capacitance and resistance in the circuit loop.

The resistive element generates a voltage proportional to the current pulse—symetrically rising during transition and constant during the constant current phase.

Figure 6.




The resulting composite is then analyzed as follows. First, the capacitive element is calculated from the constant dv/dt slope. The voltage due to capacitance alone is then calculated at the transition time. The voltage at any point in the constant dv/dt is then calculated by adding the rate of rise for that period, removed from the transition time, to the capacitive voltage at the rise time. The difference between the calculated voltage and measured voltage is due to the ESR. The ESR voltage and constant current are then used to calculate the ESR.

From the composite voltage at rise time, the ESR voltage and capacitive voltage are subtracted, resulting in ESL voltage. The ESL voltage is then calculated by dividing the ESL voltage by the di/dt.

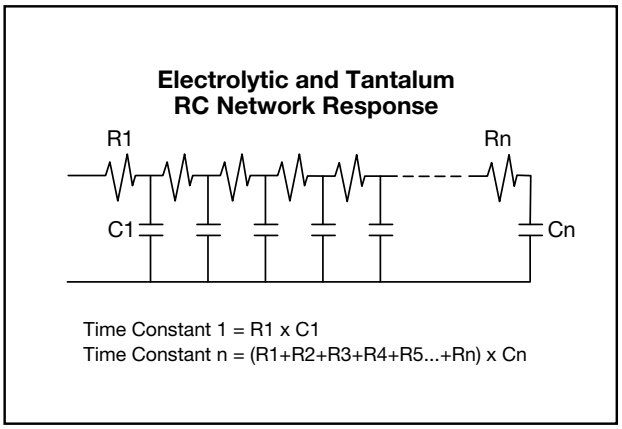
The equipment used to date has been a Hewlett Packard Pulse Generator (model #8082A) capable of supplying 200 mA in 1 nS, and a Tektronix 1 GHz Oscilloscope (model # 7104). An additional oscilloscope (Tektronix model # 7603 with digitizer) was also used in measurement of dv/dt slope as well as transfer of images to computer for enhancement and photography. A new pulse generator with a 1 ampere output in 200 ps was recently made available for further studies.

In the analysis of data from the pulse injection testing, there was a noticeable change in slope for the electrolytic and tantalum at that period where the slope should have been constant. Figure 6 shows the capacitance as calculated from the dv/dt slope after the inductive noise/ringing dampened out to the point where a measurement could be made. The ceramic show a dv/dt rate that corresponds to the marked value in as little as 1 nS post rise time . Because of the magnitude of inductance and resistance (comparative caps were used) associated with the electrolytics and tantalums, the earliest dv/dt measurement was 40 to 70 nS post rise. After this time, the measured values are fractions of their expected values until microseconds are reached.

An explanation for the cause of this response is pictured in Figure 7. These capacitors are made up of many small elemental capacitors. They are resistively connected to each other and in low frequency applications, the RC time constant of the furthest removed is insignificant. In high frequency applications, only those close to the terminal locations have a low enough RC time constant to respond continuously or in a pulse application.

In addition to the dynamic testing, we are undertaking an AC rating capability study. To date, this testing has not gone well. We keep blowing the equipment trying to supply more current into the device. We have successfully applied 5 ARMS current to a 4.7µF and a 47 µF SM02 device. The temperature rise

Figure 7.




was determined to be 60°C and 10°C, respectively. When 7.5 A was attempted, the equipment was blown ( rated @ 12000 VA @ Unity PF). We will not be able to generate an absolute maximum capability but a small increment of its capability. Even this amount should fullly surpass previous capabilities with electroytic and tantalum.

## Output Filter Requirements

In working with many designers over the past year, we have seen many outstanding examples of how close to the ideal capacitor the ceramic performs. In the calculation of required output capacitance for a choke input filter the Maximum ESR attributable to the capacitor is first made. Table 1 reflects the calculated maximum ESRs for different power levels and different output voltages. For these calculations a delta I corresponding to .25 of maximum I was assumed.

**Table 1.** Calculated Maximum Capacitance ESR for 0.050 Vripple (assuming Iripple = .25 x Imax)

| Power Watt | Vout | 5 | 10 | 15 | 20 | 25 | 50 |
|---|---|---|---|---|---|---|---|
| | | (values listed in mOhms) | | | | | |
| 5 | | 100 | 200 | 300 | 400 | 500 | 1000 |
| 10 | | 50 | 100 | 150 | 200 | 250 | 500 |
| 25 | | 20 | 40 | 60 | 80 | 100 | 200 |
| 50 | | 10 | 20 | 30 | 40 | 50 | 100 |
| 100 | | 5 | 10 | 15 | 20 | 25 | 50 |
| 250 | | 2 | 4 | 6 | 8 | 10 | 20 |

As can be seen from the calculated maximums, there is a requirement for lower ESRs as voltage decreases and power increases. Requirements below 100 millions could not readily be met with tantalums or electrolytics. This is an area where multiples are used, not to attain the required capacitance; but, required to attain the ESR demanded for performance.

Taking this one step further for the calculated capacitance required, Table 2 represents that capacitance for different frequency and power levels for a 5 VDC output supply. An additional calculation was made for an ESR that is 1/20th of required maximum. This is a guardbanded application of the ceramic in that in many instances the ESR of this capacitor is well below this figure .

**Table 2.** Output Filter Capacitor Requirements (5 VDC Output) (0.050 Vripple & Iripple = 0.25 x Imax)

| Power Watts | µF | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 20 KHz | 50 KHz | 100 KHz | 250 KHz | 20* KHz | 50* KHz | 100* KHz | 250* KHz | 500* KHz |
| 5 | 250 | 100 | 50 | 20 | 128 | 51 | 26 | 10 | 5 |
| 10 | 500 | 200 | 100 | 40 | 256 | 103 | 51 | 21 | 10 |
| 25 | 1250 | 500 | 250 | 100 | 641 | 256 | 128 | 51 | 26 |
| 50 | 2500 | 1000 | 500 | 200 | 1282 | 513 | 256 | 103 | 51 |
| 100 | 5000 | 2000 | 1000 | 400 | 2564 | 1282 | 513 | 205 | 103 |
| 250 | 12500 | 5000 | 2500 | 1000 | 6410 | 2564 | 1282 | 513 | 256 |

* Calculation for ESR 1/20th of max. allowable-Ceramic

## Input Filter Applications

For this application, two capabilities of the ceramic capacitor are highlighted. The low ESL allows high magnitude di/dt current pulses to occur without large noise pulses being generated. Secondly, in short period demands for energy, this device is responding as its marked value almost immediately. Its extremely low ESR allows lower capacitance selection to maintain a desired ripple level.

Besides the energy discharge application, we have also been involved in supplying pieces for an undersea application for the past 20 years. The customer demands reliability in the face of the unexpected as well as the normal circuit conditions. As part of the reliability testing for each lot, these pieces were subjected to multiple surge levels at voltage levels many times their ratings (6x was typical/max of 1.5 Kv restricted by equipment). They were tested for DF and ESR prior to and following surge exposure. The history in the production has given us some additional insight as to process and material requirements for high surge current capabilities that has also been carried over into design of the SMPS capacitors.

I have tested both NP0 and X7R units at 60 Ampere peak current pulses (@ 1 Kv/uS - 10 x 1000) with no failures experienced to date. If a special military specification were to be generated for this component, I would strongly urge that this testing be included. If "standard production" pieces were subjected to this test, failures would be design as well as lot related.

## Resonators

"Yeah. Yeah." with strong sarcasm, is one of the favorite responses to suggestions that the ceramic NP0 capacitor has no match in this application. The response following trial in circuit testing is usually "Eureka!!"

A 40 KHz application where 30 Amperes RMS was

applied to a capacitor was causing a "glow-in-the-dark" condition followed by flame-up. We were told that an NP0 ceramic unit was already tested and failed, and the customer required an explanation. There was an additional requirement that the piece be rated at 1000 WVDC and that the maximum height off the board was 100 mils. From calculations I performed, not only was the part physically possible, but it should have performed in circuit.

I had pieces made although the customer told us to "forget it." The project was about to be scrubbed when we sent pieces to a now desperate designer willing to try anything. He reported that the piece just gets "slightly warm to the touch" in full load application.

The same problems were being experienced at 100KHz from 10 to 40 Amperes RMS. The initial response, solution and final responses were all the same. These units are designed to not generate any heat. The heat that they do generate is self-serving in that ESR lowers as temperature increases.

In one application where an X7R was used in place of the NP0 because of height restrictions not met by the NP0, the unit was capable of handling the current, but the temperature rise was greater than allowed. An SM04, X7R, 0.4µF had 7 ARMS applied at 100 KHz. The temperature rise was 50° C. I have designed a part for this application that uses a modified NP0 composition (TCC of N2200-2200+/-300 ppm/ °C) which has a slightly higher dielectric constant. It fits the physical layout plus it carries the current capability of the NP0 with a slightly greater temperature dependence.

## DIP Leadframe

In the analysis of the ceramic devices, the performance was so outstanding that we did not want to give anything up through lead attachment These chips are large to enormous. Mounting them directly on a PC board would bring package performance to the circuit, but the reliability problems in face of temperature cycling would be enormous. These sizes and mismatches of thermal coefficients of expansion (TCE) would generate forces large enough to pull the termination off the chip or crack the chip.

The DIP leadframe gives us a distributed current path to deliver the package performance of the capacitor to the current with little additional inductance and resistance. We did try radial leads on this device, as in our normal packaging and the results were terrible. ESLs as high as the tantalums and electrolytics were realized.

We are a specialty house in that we respond to specific unique requests for individual customers. Two customers in particular wanted wire leads attached to the sides of one of our SMPS filter caps because they wanted a board fit for an existing capacitor. They were told of the performance loss, but their applications were not in the frequency range where the ESL was a factor. They needed the current capabilities.

## Future Directions

We are open to direction supplied from our customers. We are willing to work with designers on specific solutions or suggest possible directions.

We are working on projects involving the use of dielectric as a substrate material with individual capacitors sectioned within the substrate. The possible ventures of high power converters operating higher than 1 MHz will require attachment procedures beyond the present leadframe techniques.

## References

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"Functional Testing of Decoupling Capacitors for Dynamic RAMs", AVX Technical Paper, by Arch Martin, 1982

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