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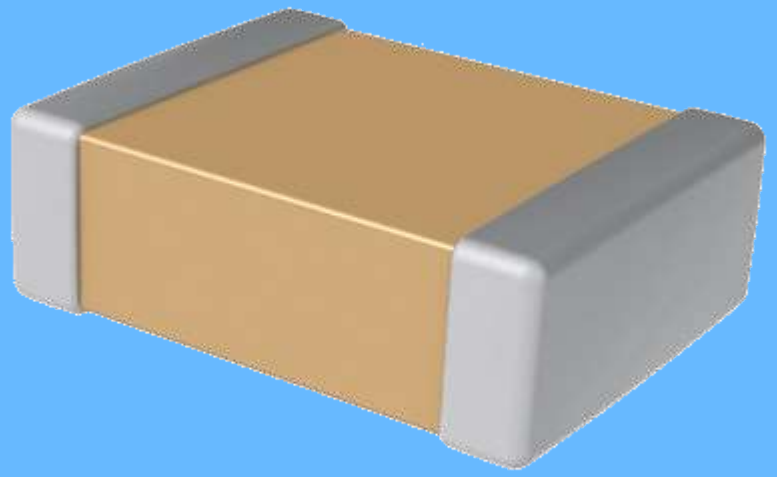
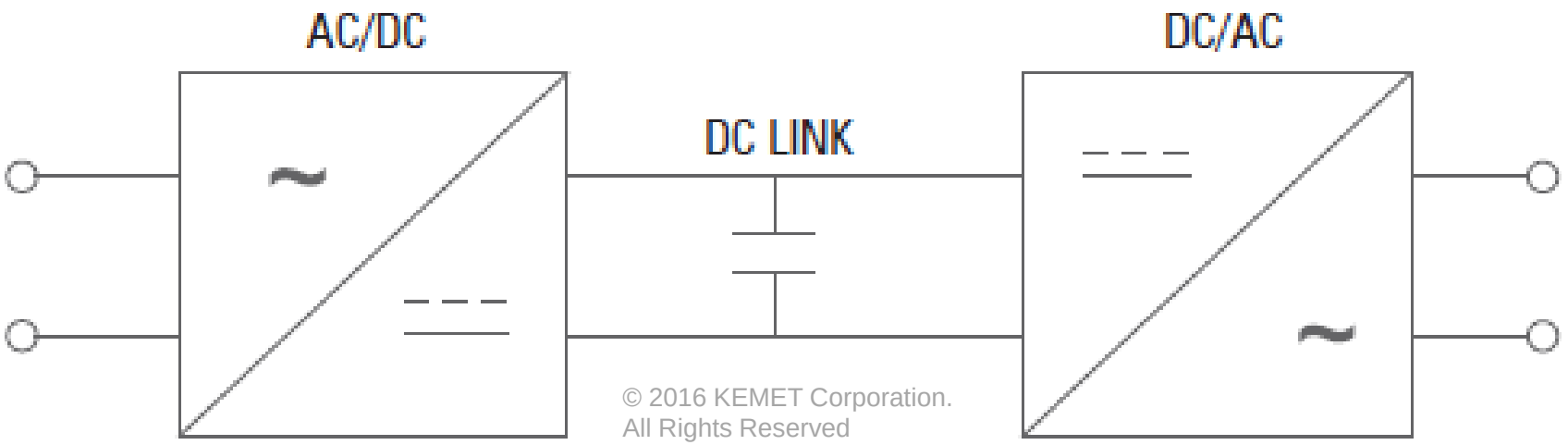
C0G MLCC DC Link

Capacitors in 3D Power Electronics





An Evaluation of BME C0G Multilayer Ceramic Capacitors as Building Blocks for DC Link Capacitors in 3-D Power Electronics

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Presentation Outline

- Introduction
- Background
- Capacitor Designs & Basic Electric Properties
- Reliability & DC Link Performance
- Assembly Considerations
- Conclusions
- Future Work

Introduction

- There is a need for DC Link capacitors that can be embedded in 3-D electronic packages close to wide band gap semiconductors to reduce inductance and improve efficiency at
  - Higher Frequencies
  - Higher Voltages
  - Higher Temperatures
- Traditional film capacitors are limited to lower operational temperatures and they do not lend themselves easily to high density 3-D assembly
- The availability of suitable multilayer ceramic capacitors (MLCC) with the necessary voltage and temperature capability as well as reliability is limited

Background

- KEMET developed 200°C MLCC solutions over 5 years ago using Ni BME C0G Dielectrics
- Since this time extensions have be made to high voltages ratings, 2000V, in large case sizes to 4540 rated for 200°C
- For immediate DC Link needs we targeted higher capacitance MLCC for rating 500VDC at 150°C
- The purpose of this work is to evaluate different 3640 MLCC of Ni C0G made with thinner active layers
- Comparisons are made to a commercial surface mountable leaded ceramic DC Link capacitor that has been extensively reviewed in the literature

MLCC Evaluation

KEMET BME
C0G 3640
Case Size

Commercial
DC Link

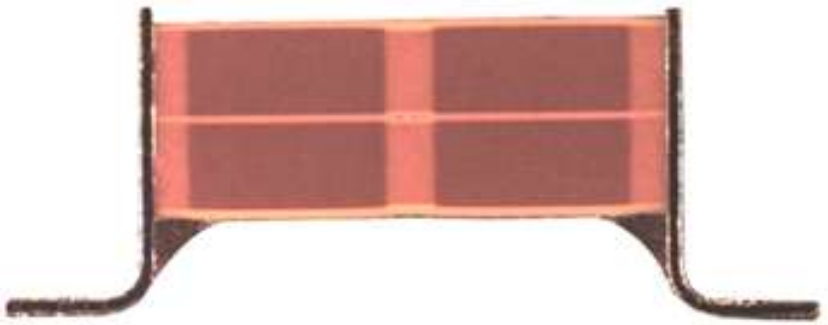
Description	C0G BME MLCC Prototypes	Commercial DC Link MLCC
Part Types	3640 Case Sizes (EIA)	4231 (2731 *no leads*)
Average. Dimensions (without leads)		
Length, mm	9.14	10.78 (6.88)
Width, mm	10.16	7.94 (7.80)
Thickness, mm	2.49	4.05 (2.67)
Volume (cm^3)	0.231	0.347 (0.143)

Capacitor Materials

Description	C0G BME MLCC Prototypes	Commercial DC-Link Capacitor
Dielectric	$CaZrO_3$	$Pb_{0.87}La_{0.07}(Na,K)_{0.05}Zr_{0.86}Ti_{0.14}O_3$ [4] PLZT
Dielectric Type	Paraelectric	Anti-Ferroelectric
Dielectric Constant (K)	32	2274
Inner Electrode	Nickel	Copper
Termination	Tin Plating Over Nickel Plating	Silver Plated Lead

[4] G. F. Engel, "Material Requirements for Power and High Temperature Multilayer Ceramic Capacitors (MLCC)", Proceedings: IMAPS/ACerS 11th International CICMT, Conference & Exhibition, Dresden, Germany, April 20-23, 2015, pp. 21-28.

Cross-Section Analysis



KEMET 3640 C0G Ni Prototype #1

- Single Monolith
- Single Overlap Area

$$C = K K_0 A n / t$$

C = capacitance

K = dielectric constant

K_0 = permittivity of free space (8.854×10^{-12} F/m)

A = Overlap Area

n = Number of active layers

t = Thickness of active layers

Commercial DC Link

- 2 Bonded Monoliths
- 2 Capacitors in Series

$$1/C = 1/C_1 + 1/C_2$$

C_1 = capacitance of 1st cap.in series

C_2 = capacitance of 2nd cap.in series

Voltage is divided between the capacitors but at the expense of lowering effective capacitance

Dielectric Strength

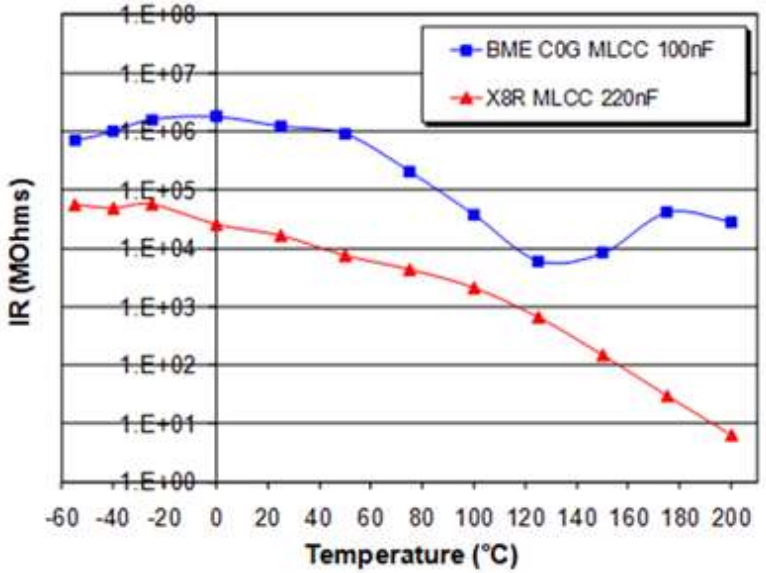
	Ni BME C0G 3640 Prototypes			Commercial Cu PLZT
	#1	**#2**	**#3**	
Dielectric Strength (V/µm)	100	110	120	27

- Ni BME C0G has higher dielectric strength even in thin active layers
- Use more active layers for high capacitance

Electrical Properties

	Ni BME C0G 3640 Prototypes			Commercial Cu PLZT
	#1	**#2**	**#3**	
Capacitance (nF)	227	343	487	310
DF (%)	0.0080	0.0117	0.0110	0.618
IR @ 25°C (GΩ)	458	277	242	16.5
IR @ 125°C (GΩ)	7.42	6.47	6.24	5.10

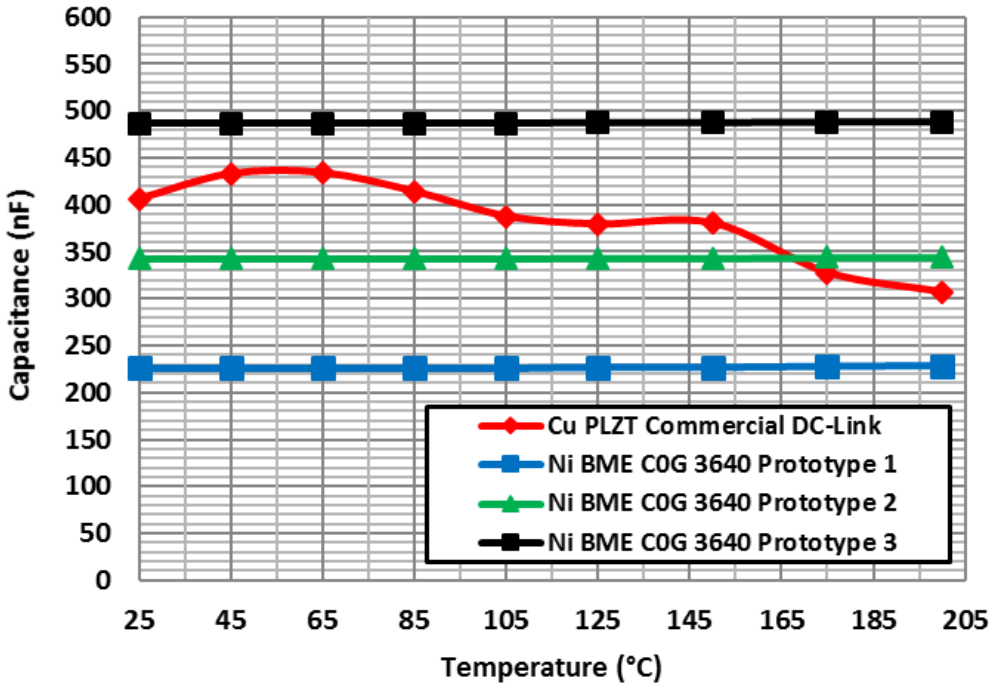
- The Commercial Cu PLZT capacitor is labeled as 1µF part but is only 310nF at $1V_{RMS}$ at 1kHz
- Ni BME C0G has far lower DF and IR does not decrease further on increasing temperature > 125°C [2]:



[2] X. Xu, A. S. Gurav, P. M. Lessner and C.A. Randall, "Robust BME Class-1 MLCC for Harsh Environment Applications", IEEE Transactions on Industrial Electronics, Vol. 50, No. 7, July 2011, pp. 2636-43.

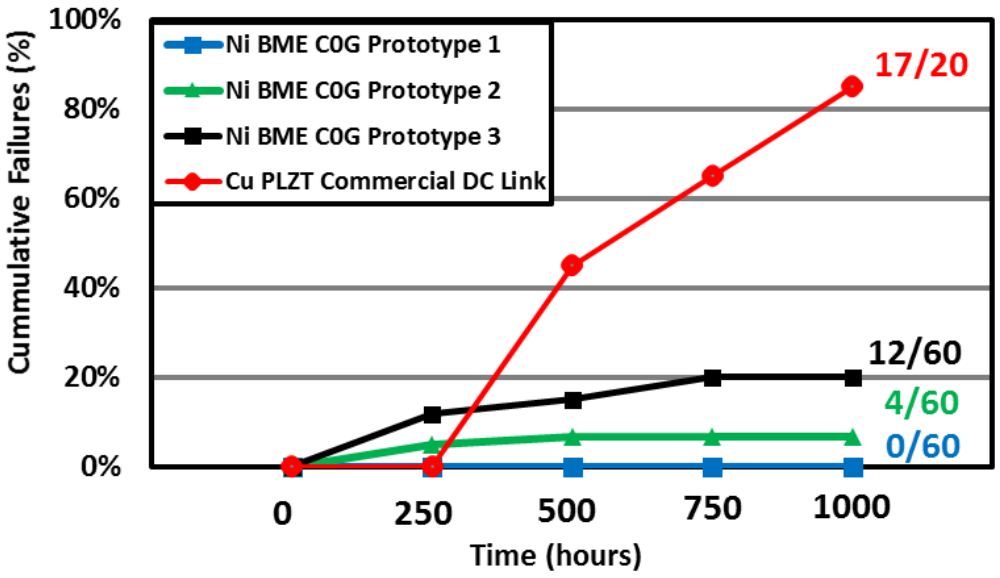
Capacitance at 500V$_{DC}$ from 25ºC to 200ºC

- Capacitance increases with applied DC voltage in anti-ferroelectric (AFE) type dielectrics like PLZT
- 500V$_{DC}$ is more representative of the operational conditions in DC-Link applications
- Capacitance varies significantly with temperature for the PLZT capacitor increasing to a peak value of 447nF
- There is hardly any change in capacitance over this temperature range for the C0G MLCC - in this respect they behave similar to film capacitors

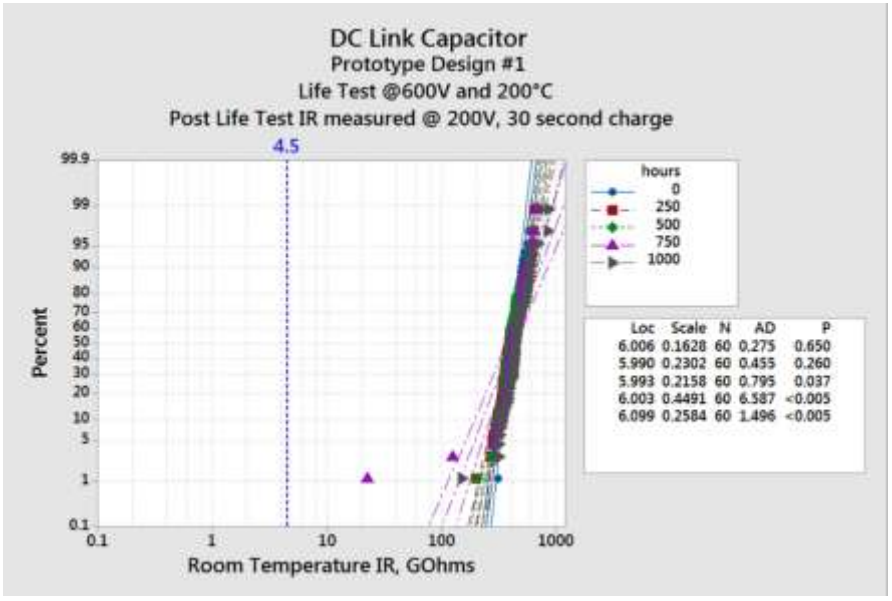


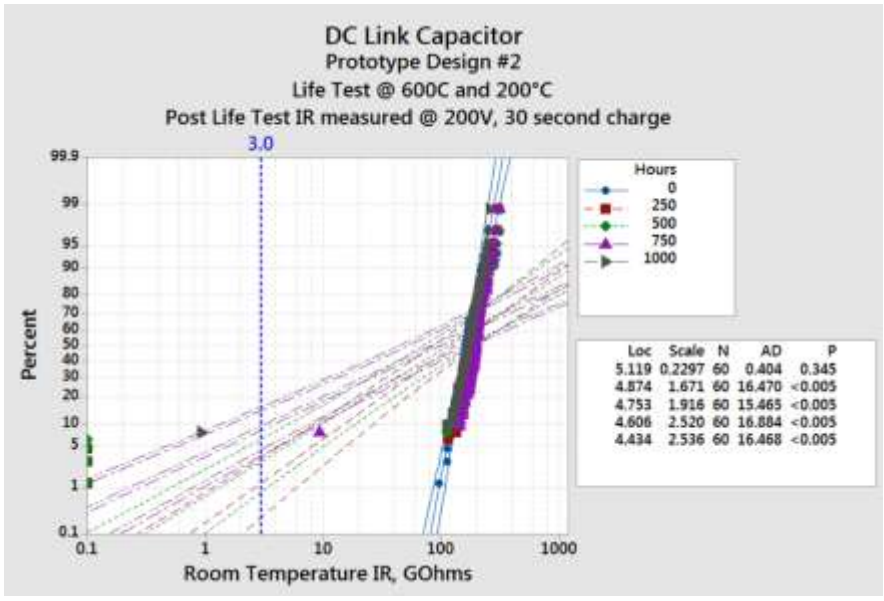
Reliability, Accelerated Life Testing 600V$_{DC}$ & 200^{o}C

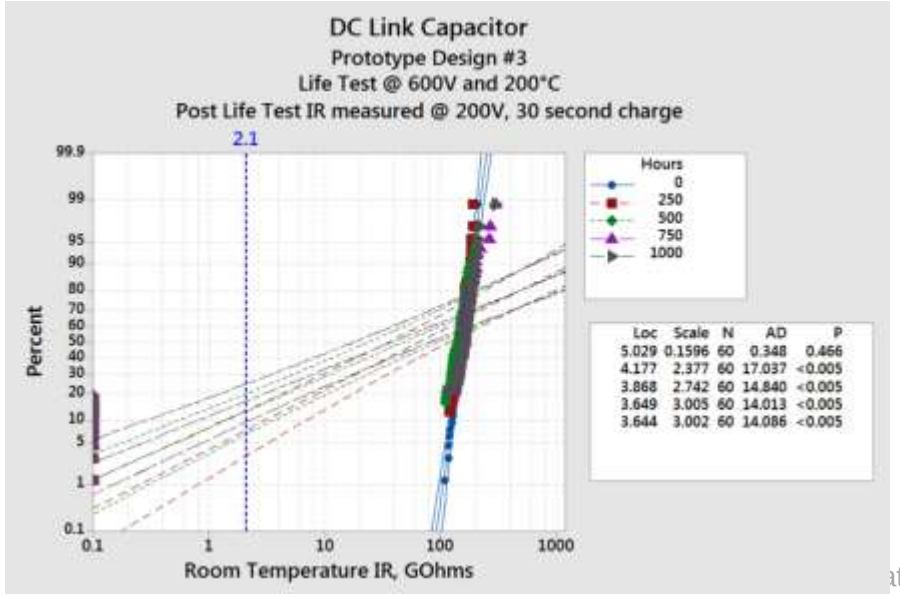
- The failure rate at 750hours of the commercial capacitor is higher than reported in the literature [1] but no failures after 250hours is consistent with this data
- The C0G 3640 prototypes #2 & #3 only had early failures at 250hours.
- No failures were detected in the 3640 Prototype #1 through 1000hours of testing
- Further testing multiple batches underway to rate for 500V$_{DC}$ & 150^{o}C

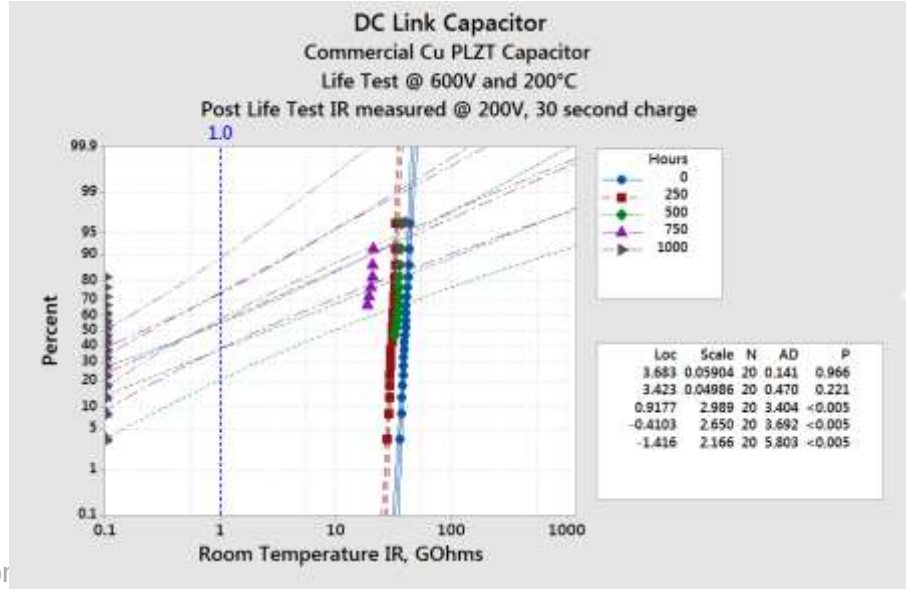


Reliability, Accelerated Life Testing 600V$_{DC}$ & 200°C, IR Weibull





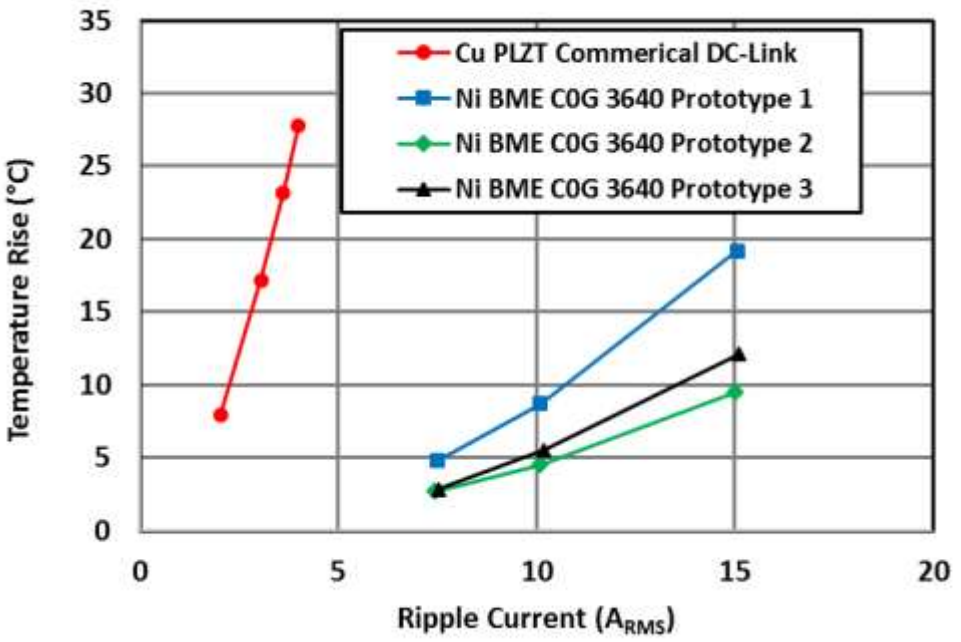




Current Handling Capability

Temperature Rise from Ambient @ 100kHz

- Temperature of the Cu PLZT capacitor increases relatively rapidly compared to the C0G Ni BME capacitors.
- Lower dissipation factors of the C0G results in a lower temperature rise. This is not unexpected since the power dissipated is related by:



$$P = i^2 d/2\pi f C$$

P = power dissipated

i = current

d = dissipation factor

f = frequency

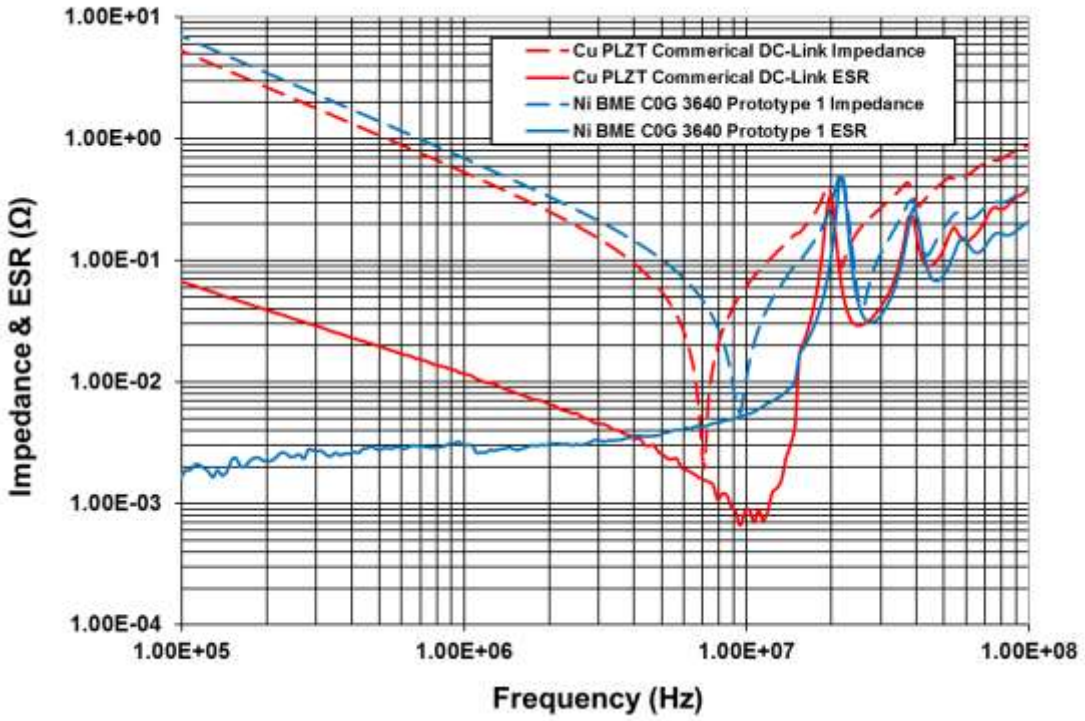
C = capacitance

- Also; **$P = i^2 ESR$** so this too should be lower

ESR, Impedance and ESL Comparisons

- < 3MHz ESR is lower for Ni BME C0G prototype #1 MLCC and self-resonant frequency is lower consistent with the lower capacitance

- ESL remains low for C0G 3640, around 0.5nH compared to 1.3nH for the PLZT commercial DC link capacitor because there are no leads in the C0G MLCC to add to the inductive loop



Power Density Figure of Merit (FOM)

- For DC Link capacitors Power Density (PD) can be calculated as follows [5]:

$PD = [C \times U_n \times I_{RMS}] / Vol$

C = max. capacitance in µF at $500V_{DC}$ up to 150^oC

U_n = DC voltage rating ($500V_{DC}$)

I_{RMS} = max. current handling at 100kHz

Vol = Volume in cm^3

Capacitor	Volume (cm^3)	C (µF)	I_{RMS} (A)	Power Density
3640 Prototype #1	0.231	0.227	15	7370
Commercial DC Link	0.347	0.447	4	2580
Commercial DC Link - *no Leads*	0.143	0.447	4	6250
Film Capacitor - *Rated 105°C*	45	200	50	110,000

No Failures (0/10) after 1000 hours @ $10A_{RMS}$ /150°C/100kHz

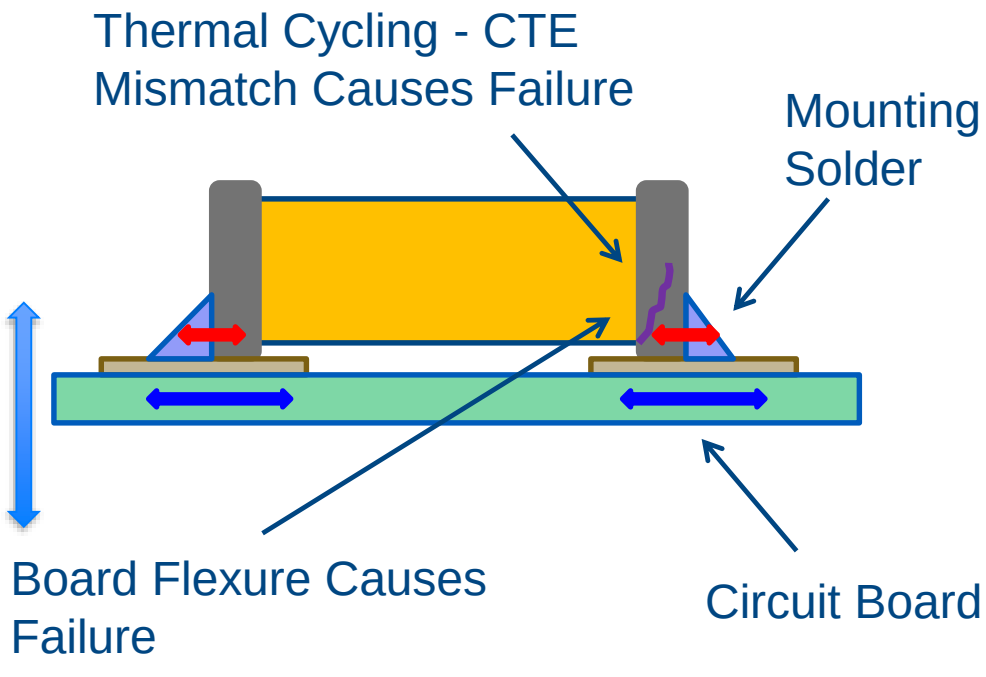
[5] P. Bettacchi, D. Montanari, D. Zanarini, D. Orioli, G. Rondelli and A. Sanua, "Power Film Capacitors for Industrial Applications", Proceedings CARTS Europe 2010, Symposium for Passive Components, Munich, Germany, pp. 1-10.

Assembly Considerations

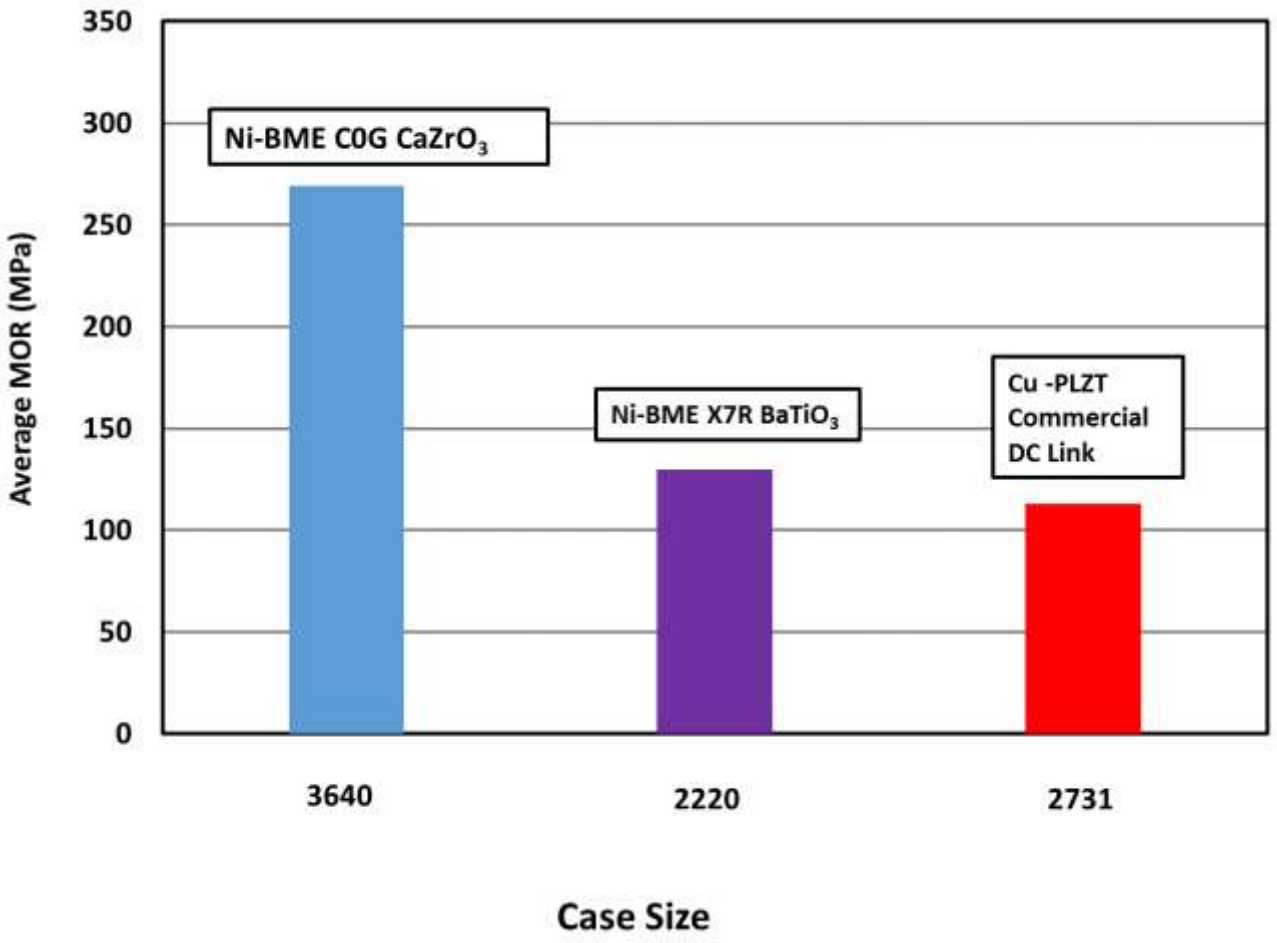
For robust performance it is desirable to have MLCC with

- High Modulus of Rupture
- High Board Flexure Capability
- No Failures during Thermal Cycling
  - Also dependent on CTE mismatch
  - C0G 8-10 PPM /^{o}C
  - FR4 14-18 PPM/^{o}C
  - Polyimide 15-19 PPM/^{o}C
  - Cu 17 PPM/^{o}C

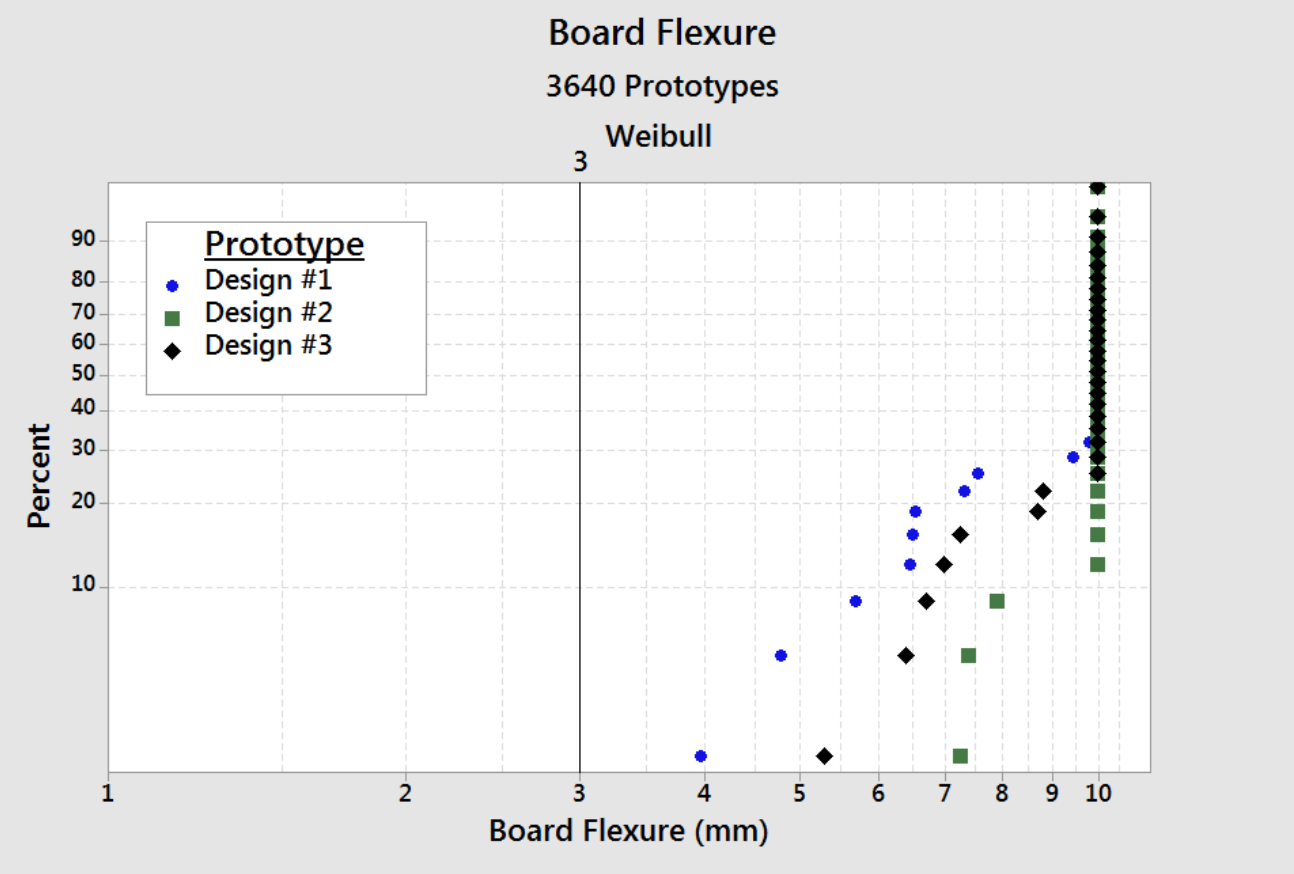
MLCC Surface Mounted on Circuit Board



Modulus of Rupture (MOR)



Board Flexure of 3640 Ni BME C0G



- Method JIS-C-6429
- 3640 flexure remains well above the 3mm limit (µStrain = 3555)
- Minimum failure recorded at 3.97mm (µStrain = 4704)

Temperature Cycling, Large Case Size Ni BME C0G, > 500V_{DC} & 200°C

Case Size	Nominal Cap. (nF)	Rated Voltage (V_{DC})	1000 Cycles -55°C to +125°C	50 Cycles -55°C to +200°C
4540	27	1500	0/231	0/50
3640	15	2000	0/154	0/100
3040	39	1000	0/154	0/100
2824	33	630	0/154	0/100

- All tests use SAC solder, FR4 board for 125°C, Polyimide for 200°C
- Cycling to 125°C by JESD22, Method JA-104
- -55°C to 200°C cycling with a 30°C/min ramp rate and 1 hour soak at each temperature

3D-Packaging Interconnects

- Transient Liquid Phase Sintering (TLPS) Materials & Processes were investigated to replace Pb-based solders [10]
- Leaded MLCC with TLPS interconnects of Cu-Sn & In-Ag had:
  - High shear capability at 300°C (useful to at least 350°C)
  - TLPS Cu-Sn leaded MLCC passed 2000 hours storage life @ 175°C, 85°C/85% humidity testing 2000 hours & 2000 cycles -40 to +175°C
- TLPS materials may be more desirable for packaging because they have low forming temperatures and higher melting temperatures but unlike solders the bonding is surface finish specific:
  - Component terminations must be compatible with the TLPS and package bonding surface
  - Temperature cycling must be evaluated

[10] ***J. Bultitude, J. McConnell and C. Shearer, "High temperature capacitors and transient liquid phase interconnects for Pb-solder replacement", Journal of Materials Science: Materials in Electronics, December 2015, Volume 26, Issue 12, pp. 9236-9242***

Conclusions

- 3640 C0G Ni MLCC prototype # 1 had no failures (0/60) in accelerated testing at 200oC, 600VDC through 1000 hours
- These C0G MLCC have low DF, very stable capacitance with temperature under bias, and higher current handling capability leading to high power density
- Larger case size C0G MLCC also have high MOR with good board flexure performance and thermal cycling capability
- C0G Ni MLCC are Pb-free and can be considered a good building block for DC Link capacitors
- TLPS materials may be considered as packaging interconnects to overcome solder limitations but are surface finish specific

Future Work

- C0G Ni MLCC are being manufactured based on the 3640 prototype #1 for qualification at 500VDC and 150°C
- Thermal cycling performance in the assembled package should be assessed to confirm interconnect integrity
- Power cycling will also need to be assessed in the final package.

Thank You!

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More Information:
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