BLE112

Preliminary Data Sheet

Friday, 28 January 2011

Version 0.91

bluegiga

VERSION HISTORY

Version	Comment
0.1	First draft
0.9	Preproduction information
0.91	Prerelease

TABLE OF CONTENTS

BLE112 *Bluetooth*® low energy single mode module

DESCRIPTION

BLE112, *Bluetooth* low energy single mode module is a single mode device targeted for low power sensors and accessories.

BLE112 offers all *Bluetooth* low energy features: radio, stack, profiles and application space for customer applications, so external processor is needed. The module also provides flexible hardware interfaces to connect sensors, simple user interfaces or even displays directly to the module.

BLE112 can be power directly with a standard 3V coin cell batteries or pair of AAA batteries. In lowest power sleep mode it consumes only 400nA and will wake up in few hundred microseconds.

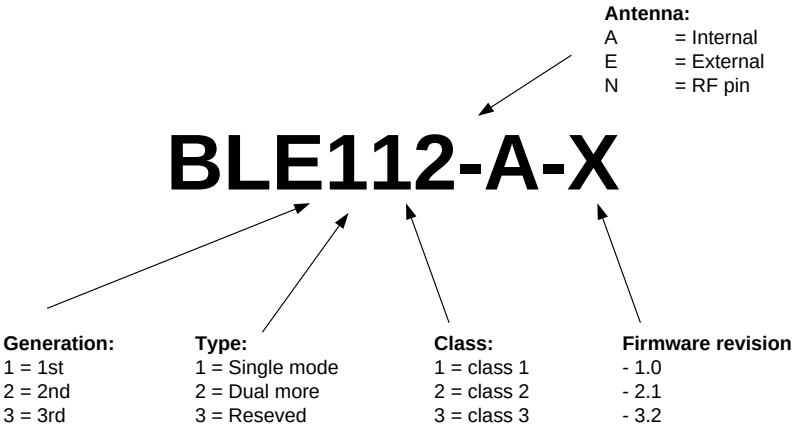
APPLICATIONS:

- Heart rate sensors
- Pedometers
- Watches
- Blood pressure and glucose meters
- Weight scales
- Key fobs
- Households sensors and collector devices
- Security tags
- Wireless keys (keyless go)
- Proximity sensors
- HID keyboards and mice
- Indoor GPS broadcasting devices

KEY FEATURES:

- *Bluetooth v.4.0*, single mode compliant
  - Supports master and slave modes
  - 4+ simultaneous connection in master mode
- Integrated *Bluetooth* low energy stack
  - GAP, GATT, L2CAP, SMP
  - *Bluetooth* low energy profiles
- Radio performance
  - TX power: +3 dBm to -23dBm
  - RX sensitivity: -87dBm to -93dBm
- Ultra low current consumption
  - Transmit: 27mA (0 dBm)
  - Sleep mode 3: 0.4uA
- Programmable 8051 processor for embedding full applications
- *Bluetooth* end product, CE, FCC and IC and Telec qualified

1 BLE112 Product numbering



*) TBD

Available products and product codes

Product code	Description
BLE112-A-v1	BLE112 with integrated chip antenna and software version 1.0
BLE112-N-v1	BLE112 with RF pin and software version 1.0
BLE112-E-v1	BLE112 with U.FL connector and software version 1.0

2 Pinout and Terminal Description

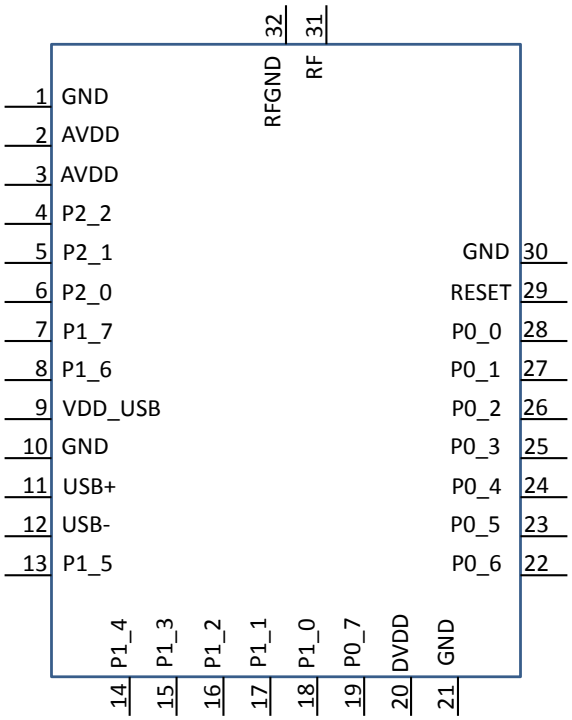


Figure 1: BLE112

	PIN NUMBER	PAD TYPE	DESCRIPTION
RESET	29		Active low reset.
GND	1, 10, 21, 30	GND	GND
RF	31	RF (*	RF output/input for BLE112-N. With BLE112-A and BLE112-E donot connect.
RFGND	32	GND	RF ground. Connected to GND internally to the module. With BLE112-A and BLE112-E leave floting or connect to a solid GND plane.
DVDD	20	Supply voltage	Supply voltage 2V - 3.6V
AVDD	2, 3	Supply voltage	Supply voltage 2V - 3.6V
VDD_USB	9	Supply voltage	Supply voltage 2V - 3.6V

*) RF pin is not connected in BLE112-A and BLE112-E. To use RF pin with BLE112-B please see the design guide.

Table 1: Supply and RF Terminal Descriptions

PIN NUMBER	PIN NAME	FUNCTION	DESCRIPTION
4	P2_2	DC	Debug clock
5	P2_1	DD	Debug data
6	P2_0	T	ADC trigger
		Timer 4	Timer 4 channel 0 capture/compare
7	P1_7	SPI_MISO	SPI data input/output (*
		UART_RX	UART data input
		Timer 3	Timer 3 channel 1 capture/compare
8	P_6	SPI_MOSI	SPI data input/output (*
		UART_TX	UART data output
		Timer 3	Timer 3 channel 0 capture/compare
11	USB+	USB+	USB data plus
12	USB-	USB-	USB data minus
13	P1_5	SPI_MOSI	SPI data input/output (*
		SPI_CLK	SPI clock (*
		UART_RTS	UART request to send output
		UART_TX	UART data output
		OBSSEL5	Radio control signal for external LNA, PA or switch
14	P1_4	SPI_MISO	SPI data input/output (*
		SPI_SS	SPI slave select (*
		UART_RX	UART data input
		UART_CTS	UART clear to send input
		Timer 3	Timer 3 channel 1 capture/compare
		OBSSEL4	Radio control signal for external LNA, PA or switch
15	P1_3	SPI_CLK	SPI clock (*
		UART_RTS	UART request to send output
		Timer 3	Timer 3 channel 0 capture/compare
		OBSSEL3	Radio control signal for external LNA, PA or switch
16	P1_2	SPI_SS	SPI slave select (*
		UART_CTS	UART clear to send input
		TIMER 1	Timer 1 channel 0 capture/compare
		OBSSEL2	Radio control signal for external LNA, PA or switch
17	P1_1	TIMER 1	Timer 1 channel 1 capture/compare
		TIMER 4	Timer 4 channel 1 capture/compare
		OBSSEL1	Radio control signal for external LNA, PA or switch
18	P1_0	TIMER 1	Timer 1 channel 2 capture/compare
		TIMER 4	Timer 4 channel 0 capture/compare
		OBSSEL0	Radio control signal for external LNA, PA or switch
19	P0_7	ADC_A7	Analog to digital converter input
		TIMER 1	Timer 1 channel 3 capture/compare
22	P0_6	ADC_A6	Analog to digital converter input
		TIMER 1	Timer 1 channel 4 capture/compare

Table 2: Terminal Descriptions

*)BLE112 is configurable as either SPI master or SPI slave

PIN NUMBER		FUNCTION	DESCRIPTION
23	P0_5	ADC_A5	Analog to digital converter input
		Comparator +	Analog comparator positive input
		SPI_CLK	SPI clock (*
		SPI_MISO	SPI data input / output (*
		UART_RTS	UART request to send output
		UART_RX	UART data input
		TIMER 1	Timer 1 channel 3 capture/compare
24	P0_4	ADC_A4	Analog to digital converter input
		Comparator -	Analog comparator negative input
		SPI_SS	SPI slave select (*
		SPI_MOSI	SPI data input / output (*
		UART_CTS	UART clear to send input
		UART_TX	UART data input
		TIMER 1	Timer 1 channel 2 capture/compare
25	P0_3	ADC_A3	Analog to digital converter input
		SPI_MOSI	SPI data input / output (*
		SPI_CLK	SPI clock (*
		UART_TX	UART data output
		UART_RTS	UART request to send output
		TIMER 1	Timer 1 channel 1 capture/compare
26	P0_2	ADC_A2	Analog to digital converter input
		OPAPM_O	Operational amplifier output
		SPI_MISO	SPI data input / output (*
		SPI_SS	SPI slave select (*
		UART_RX	UART data input
		UART_CTS	UART clear to send input
		TIMER 1	Timer 1 channel 0 capture/compare
27	P0_1/LED1	ADC_A1	Analog to digital converter input
		OPAPM_-	Operational amplifier negative input
28	P0_0/LED2	ADC_A0	Analog to digital converter input
		OPAPM_+	Operational amplifier positive input

Table 3: Terminal descriptions

*)BLE112 is configurable as either SPI master or SPI slave

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Rating	Min	Max	Unit
Storage Temperature	-40	85	°C
AVDD,DVDD, VDD_USB	-0.4	3.6	V
Other Terminal Voltages	VSS-0.4	VDD+0.4	V

Table 4: Absolute Maximum Ratings

3.2 Recommended Operating Conditions

Rating	Min	Max	Unit
Operating Temperature Range	-40	85	°C
AVDD, DVDD, VDD_USB	2.0	3.6	V

*) VDD_PA has an effect on the RF output power.

Table 5: Recommended Operating Conditions

4 Physical Dimensions

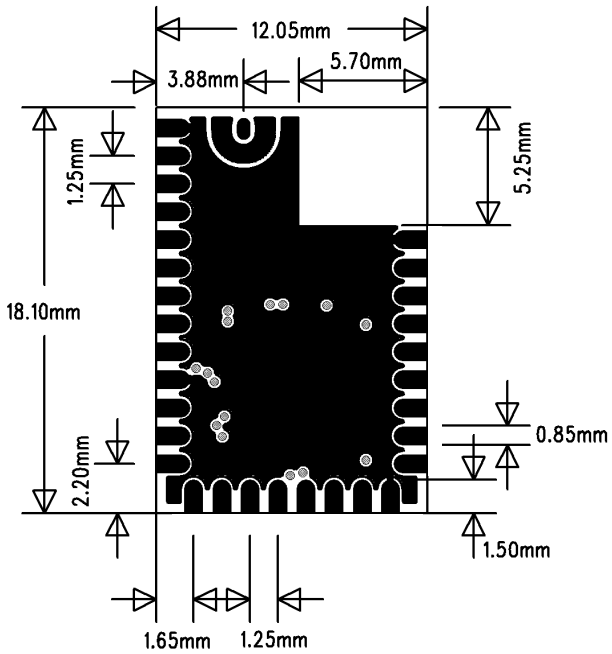


Figure 2: Physical dimensions and pinout (top view)

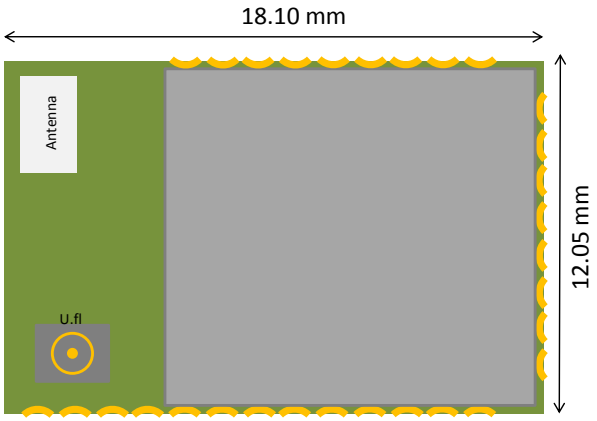


Figure 3: Physical dimensions (top view)

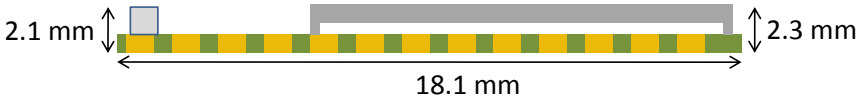


Figure 4: Physical dimensions (side view)

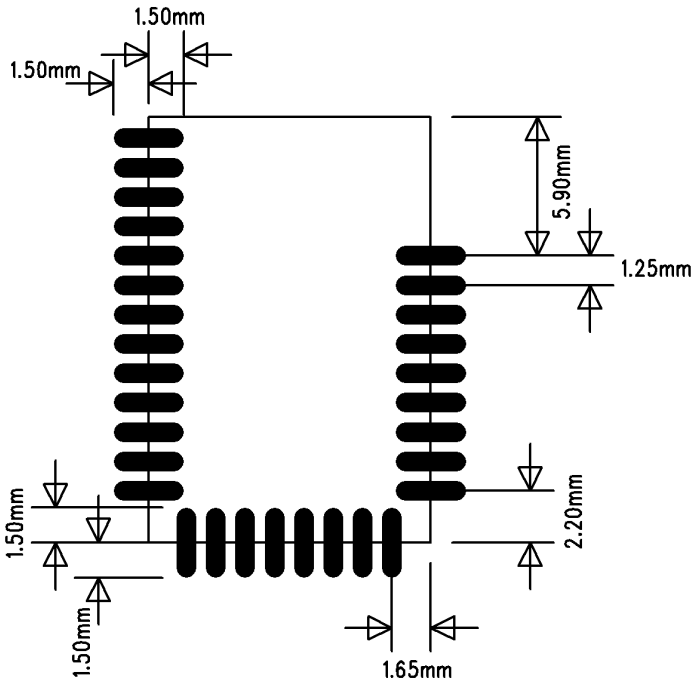


Figure 5: Recommended land pattern for BLE112-A and BLE112-E

5 Layout Guidelines

5.1 BLE112-A

For optimal performance of the antenna place the module at the corner of the PCB as shown in the figure below. Do not place any metal (traces, components, battery, …) within the clearance area of the antenna. Connect all the GND pins directly to a solid GND plane. Place the GND vias as close to the GND pins as possible. Use good layout practices to avoid any excessive noise coupling to signal lines or supply voltage lines.

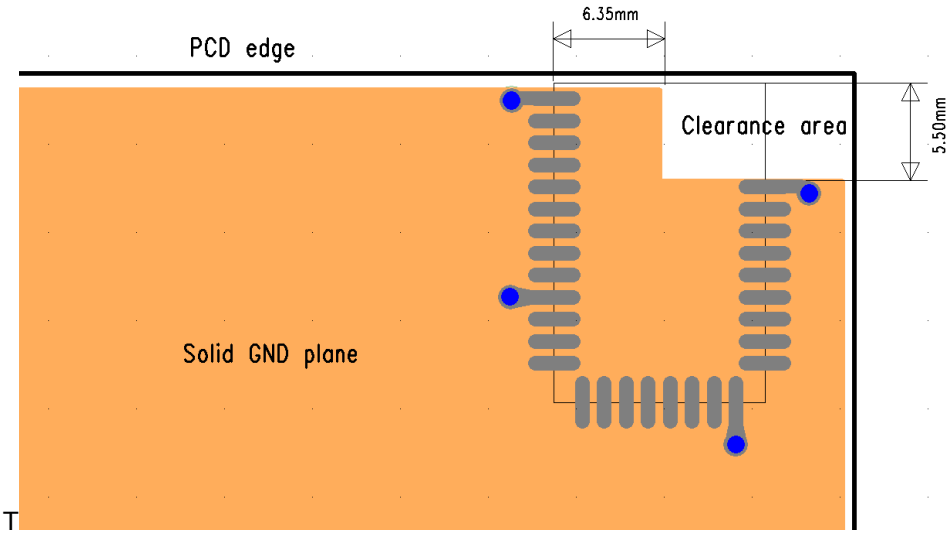


Figure 6: Recommended layout for BLE112-A

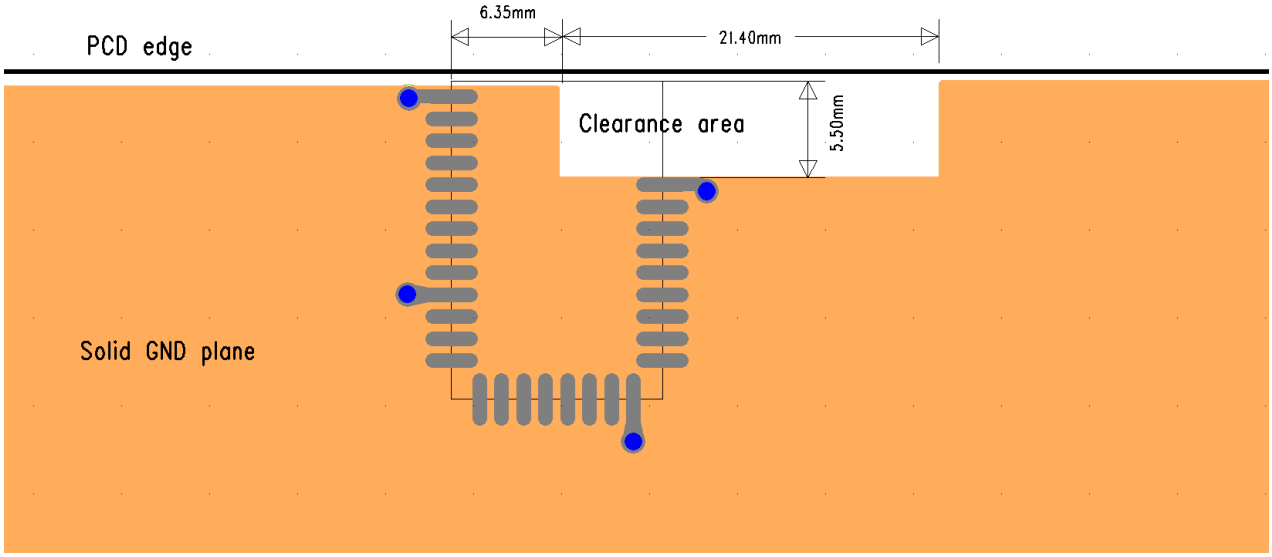


Figure 7: Example layout for BLE112-A with the module at the long edge of the PCB

6 Block diagram

BLE112 is based on TI's CC2540 chip. Embedded 32 MHz and 32.678 kHz crystals are used for clock generation. Matched balun and low pass filter provide optimal radio performance with extremely low spurious emissions. Small ceramic chip antenna gives good radiation efficiency also when the module is used in layouts with very limited space.

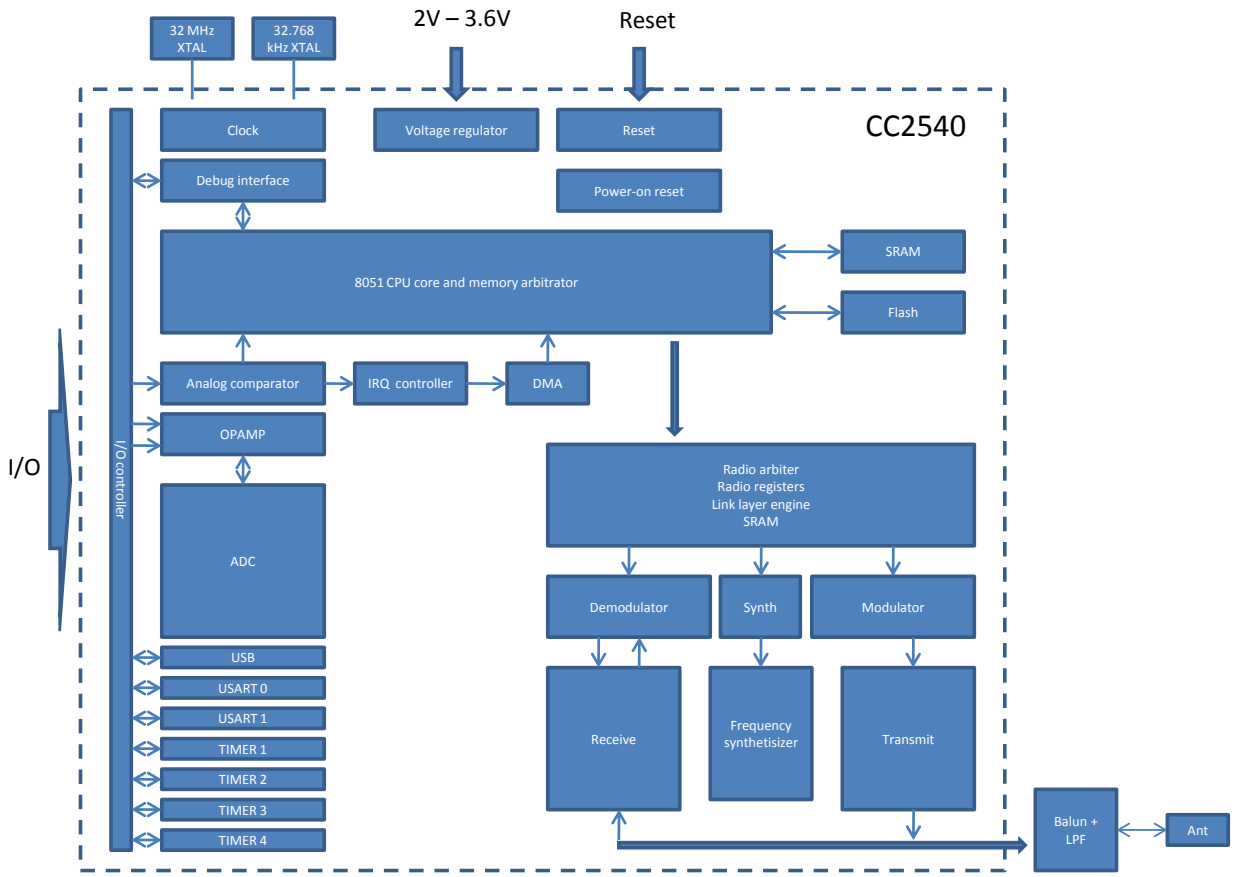


Figure 8: Simplified block diagram of BLE112

CPU and Memory

The 8051 CPU core is a single-cycle 8051-compatible core. It has three different memory access busses (SFR, DATA, and CODE/XDATA), a debug interface, and an 18-input extended interrupt unit.

The memory arbiter is at the heart of the system, as it connects the CPU and DMA controller with the physical memories and all peripherals through the SFR bus. The memory arbiter has four memory-access points, access of which can map to one of three physical memories: an SRAM, flash memory, and XREG/SFR registers. It is responsible for performing arbitration and sequencing between simultaneous memory accesses to the same physical memory.

The SFR bus is a common bus that connects all hardware peripherals to the memory arbiter. The SFR bus also provides access to the radio registers in the radio register bank, even though these are indeed mapped into XDATA memory space.

The 8-KB SRAM maps to the DATA memory space and to parts of the XDATA memory spaces. The SRAM is an ultralow-power SRAM that retains its contents even when the digital part is powered off (power modes 2 and 3).

The 128/256 KB flash block provides in-circuit programmable non-volatile program memory for the device, and maps into the CODE and XDATA memory spaces.

Peripherals

Writing to the flash block is performed through a flash controller that allows page-wise erasure and 4-bytewise programming.

A versatile five-channel DMA controller is available in the system, accesses memory using the XDATA memory space, and thus has access to all physical memories. Each channel (trigger, priority, transfer mode, addressing mode, source and destination pointers, and transfer count) is configured with DMA descriptors that can be located anywhere in memory. Many of the hardware peripherals (AES core, flash controller, USARTs, timers, ADC interface, etc.) can be used with the DMA controller for efficient operation by performing data transfers between a single SFR or XREG address and flash/SRAM.

Each CC2540 contains a unique 48-bit IEEE address that can be used as the public device address for a *Bluetooth* device. Designers are free to use this address, or provide their own, as described in the *Bluetooth* specfication.

The interrupt controller services a total of 18 interrupt sources, divided into six interrupt groups, each of which is associated with one of four interrupt priorities. I/O and sleep timer interrupt requests are serviced even if the device is in a sleep mode (power modes 1 and 2) by bringing the CC2540 back to the active mode.

The debug interface implements a proprietary two-wire serial interface that is used for in-circuit debugging. Through this debug interface, it is possible to erase or program the entire flash memory, control which oscillators are enabled, stop and start execution of the user program, execute instructions on the 8051 core, set code breakpoints, and single-step through instructions in the code. Using these techniques, it is possible to perform in-circuit debugging and external flash programming elegantly.

The I/O controller is responsible for all general-purpose I/O pins. The CPU can configure whether peripheral modules control certain pins or whether they are under software control, and if so, whether each pin is configured as an input or output and if a pullup or pulldown resistor in the pad is connected. Each peripheral that connects to the I/O pins can choose between two different I/O pin locations to ensure flexibility in various applications.

The sleep timer is an ultralow-power timer that uses an external 32.768-kHz crystal oscillator. The sleep timer runs continuously in all operating modes except power mode 3. Typical applications of this timer are as a real-time counter or as a wake-up timer to get out of power modes 1 or 2.

A built-in watchdog timer allows the CC2540 to reset itself if the firmware hangs. When enabled by software, the watchdog timer must be cleared periodically; otherwise, it resets the device when it times out.

Timer 1 is a 16-bit timer with timer/counter/PWM functionality. It has a programmable prescaler, a 16-bit period value, and five individually programmable counter/capture channels, each with a 16-bit compare value. Each of the counter/capture channels can be used as a PWM output or to capture the timing of edges on input signals. It can also be configured in IR generation mode, where it counts timer 3 periods and the output is ANDed with the output of timer 3 to generate modulated consumer IR signals with minimal CPU interaction.

Timer 2 is a 40-bit timer used by the *Bluetooth* low energy stack. It has a 16-bit counter with a configurable timer period and a 24-bit overflow counter that can be used to keep track of the number of periods that have transpired. A 40-bit capture register is also used to record the exact time at which a start-of-frame delimiter is received/transmitted or the exact time at which transmission ends. There are two 16-bit timer-compare registers and two 24-bit overflow-compare registers that can be used to give exact timing for start of RX or TX to the radio or general interrupts.

Timer 3 and timer 4 are 8-bit timers with timer/counter/PWM functionality. They have a programmable prescaler, an 8-bit period value, and one programmable counter channel with an 8-bit compare value. Each of the counter channels can be used as PWM output.

USART 0 and USART 1 are each configurable as either an SPI master/slave or a UART. They provide double buffering on both RX and TX and hardware flow control and are thus well suited to high-throughput full-duplex applications. Each USART has its own high-precision baud-rate generator, thus leaving the ordinary timers free for other uses. When configured as SPI slaves, the USARTs sample the input signal using SCK directly instead of using some oversampling scheme, and are thus well-suited for high data rates.

The AES encryption/decryption core allows the user to encrypt and decrypt data using the AES algorithm with 128-bit keys. The AES core also supports ECB, CBC, CFB, OFB, CTR, and CBC-MAC, as well as hardware support for CCM.

The ADC supports 7 to 12 bits of resolution with a corresponding range of bandwidths from 30-kHz to 4-kHz, respectively. DC and audio conversions with up to eight input channels (I/O controller pins) are possible. The inputs can be selected as single-ended or differential. The reference voltage can be internal, AVDD, or a single-ended or differential external signal. The ADC also has a temperature-sensor input channel. The ADC can automate the process of periodic sampling or conversion over a sequence of channels.

The operational amplifier is intended to provide front-end buffering and gain for the ADC. Both inputs as well as the output are available on pins, so the feedback network is fully customizable. A chopper-stabilized mode is available for applications that need good accuracy with high gain.

The ultralow-power analog comparator enables applications to wake up from PM2 or PM3 based on an analog signal. Both inputs are brought out to pins; the reference voltage must be provided externally. The comparator output is connected to the I/O controller interrupt detector and can be treated by the MCU as a regular I/O pin interrupt.

RF front end

RF front end includes combined matched balun and low pass filter, and ceramic chip antenna with matching network. Optimal matching combined with effective low pass filter provides extremely low in-band spurious emissions and harmonics. Optionally as a module assembly variant RF can be traced either to an embedded u.fl connector or to the RF pin of the module.

7 Certifications

BLE112 is compliant to the following specifications.

7.1 Bluetooth

BLE112 Bluetooth low enerfy module is *Bluetooth* qualified and listed as a controller subsystem and it is Bluetooth compliant to the following profiles of the core spec version v.4.0

7.2 FCC

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) this device may not cause harmful interference, and

(2) this device must accept any interference received, including interference that may cause undesired operation.

FCC RF Radiation Exposure Statement:
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure compliance. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Note:

When using BLE112 the end product must display an exterior label with the following detail incorporated:
“Contains Transmitter Module FCC ID: QOQBLE112”

7.3 CE

BLE112 meets the requirements of the standards below and hence fulfills the requirements of EMC Directive 89/336/EEC as amended by Directives 92/31/EEC and 93/68/EEC within CE marking requirement.

- EMC (immunity only) EN 301 489-17 V.1.3.3 in accordance with EN 301 489-1 V1.8.1
- Radiated emissions EN 300 328 V1.7.1

7.4 Industry Canada (IC)

BLE112 meets Industry Canada's procedural and specification requirements for certification.

Industry Canada ID: 5123A-BGTBLE112

7.5 Qualified Antenna Types for BLE112

This device has been designed to operate with the antennas listed below, and having a maximum gain of 2 dB. Antennas not included in this list or having a gain greater than 2 dB are strictly prohibited for use with this device. The required antenna impedance is 50 ohms.

Qualified Antenna Types for WT41-N	
Antenna Type	**Maximum Gain**
Dipole	2.2 dBi

Table 6: Qualified Antenna Types for BLE112-N

Any antenna that is of the same type and of equal or less directional gain as listed in table 14 can be used without a need for retesting. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that permitted for successful communication. Using an antenna of a different type or gain more than 2.2 dBi will require additional testing for FCC, CE and IC. Please, contact support@bluegiga.com for more information.

8 Contact Information

Sales: sales@bluegiga.com

Technical support: support@bluegiga.com
http://techforum.bluegiga.com

Orders: orders@bluegiga.com

Head Office / Finland:

Phone: +358-9-4355 060
Fax: +358-9-4355 0660

Street Address:

Sinikalliontie 5A
02630 ESPOO
FINLAND

Postal address:

P.O. BOX 120
02631 ESPOO
FINLAND

Sales Office / USA:

Bluegiga Technologies, Inc.
3235 Satellite Boulevard, Building 400, Suite300,
Duluth, GA, 30096, USA
Phone: +1 770 291 2181
Fax: +1 770 291 2183

Sales Office / Hong Kong:

Unit 10-18, 32/F, Tower 1, Millennium City 1
388 Kwun Tong Road, Kwun Tong, Kowloon, Hong Kong
Phone: +852 3972 2345
Fax: +852 3972 2211