

Applications of 1EDNx550 single-channel low-side EiceDRIVER™ with truly differential inputs

About this document

Scope and purpose

This application note shows the potential of the 1EDNx550 EiceDRIVER™ family of gate drivers with truly differential inputs. It is intended to be used in SMPS characterized by large shifts in the ground potential line. The target applications of the 1EDNx550 are described with practical examples of usage as support.

Intended audience

The document is intended for designers with entry-level technical knowledge related to SMPS, MOSFET drivers and superjunction (SJ) transistors.

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Introduction

1 Introduction

The operation state of a conventional single-channel gate driver is determined by its PWM input voltage referenced to its ground level, as shown in Figure 1. The typical threshold voltages for a TTL-compatible input solution are listed below:

- $V_{IN_LH} = 2\text{ V} \rightarrow V_{IN} \geq V_{IN_LH}$: on-state
- $V_{IN_HL} = 0.8\text{ V} \rightarrow V_{IN} \leq V_{IN_HL}$: off-state

The microcontroller generates the PWM signal with “0” and “1” voltage levels referenced to its own ground potential. A shift between the control IC ground voltage and the driver ground voltage can occur due to voltage drops on the line. The input level interpretation of the driver is affected, leading to unpredictable behavior of the MOSFET with undesirable consequences for the system reliability.

The 1EDNx550 gate driver is designed to handle this problem and is a robust solution in applications with AC ground-shift up to $\pm 150\text{ V}$. The 1EDNx550 has fully differential control inputs and its behavior exclusively depends on the voltage difference between the input signals; the operation state of the driver is independent from its ground voltage.

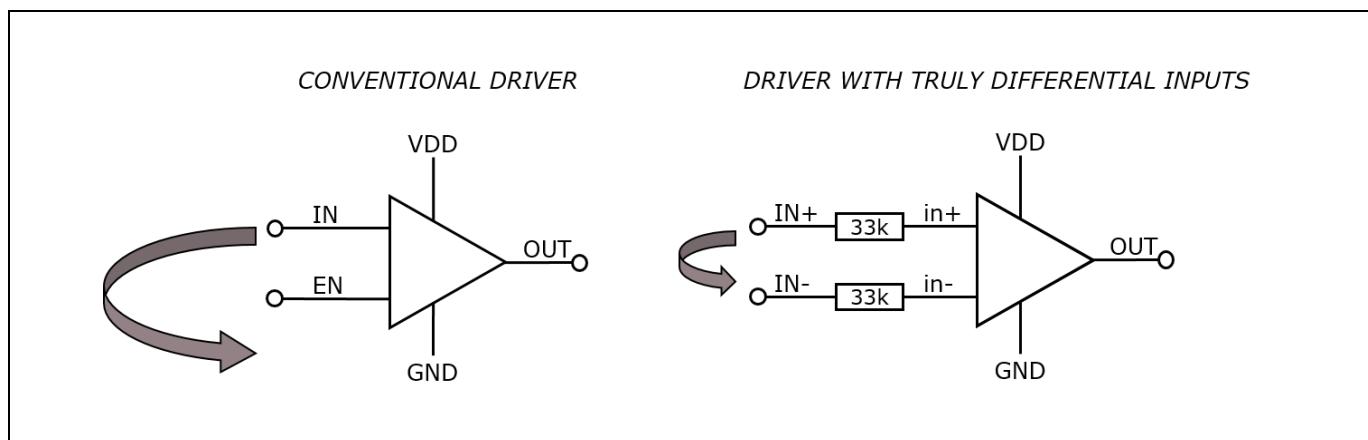


Figure 1 Conventional gate driver vs gate driver with truly differential input

The connection, shown in Figure 2, of the input pin IN^- to the microcontroller ground guarantees the proper reading of the PWM signal. This connection, in the PCB layout, must be symmetrical to the wiring between the input pin IN^+ and the PWM pin of the microcontroller; a similar dynamic common noise, generated by the parasitic inductance of the wirings, is guaranteed on the differential pins of the driver.

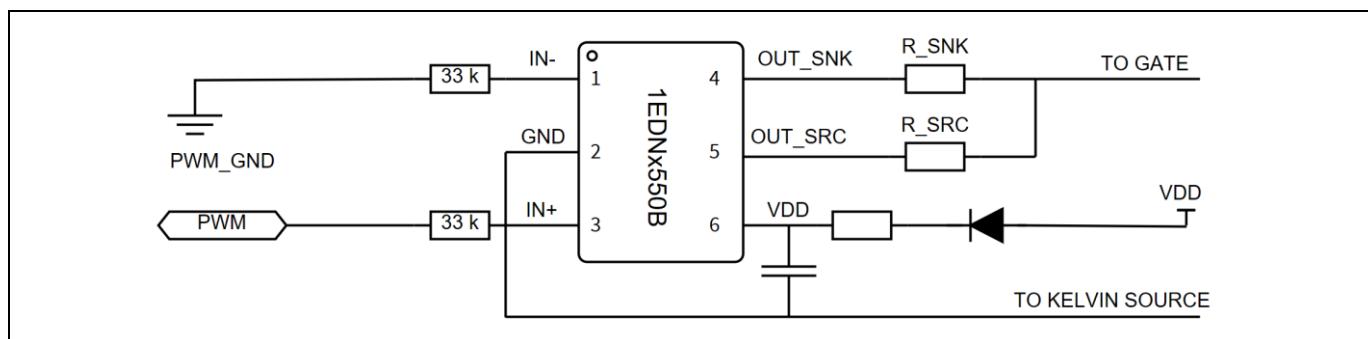


Figure 2 Schematic of the recommended usage of the 1EDNx550 driver

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Introduction

The input common noise must be scaled to a value that can be processed within the LV CMOS circuit of the driver. Two identical resistors must be always connected to the differential inputs and their choice must follow the relation above:

$$R_{IN} = (10.9V_{CC} - 3) \text{ k}\Omega \quad (1.1)$$

Where V_{CC} is the “1” level voltage of the control IC. A typical V_{CC} equal to 3.3 V requires 33 k Ω resistors.

A differential stage with a second-order low-pass filter is integrated into the driver, as shown in Figure 3, and is involved in the rejection of the high-frequency common noise.

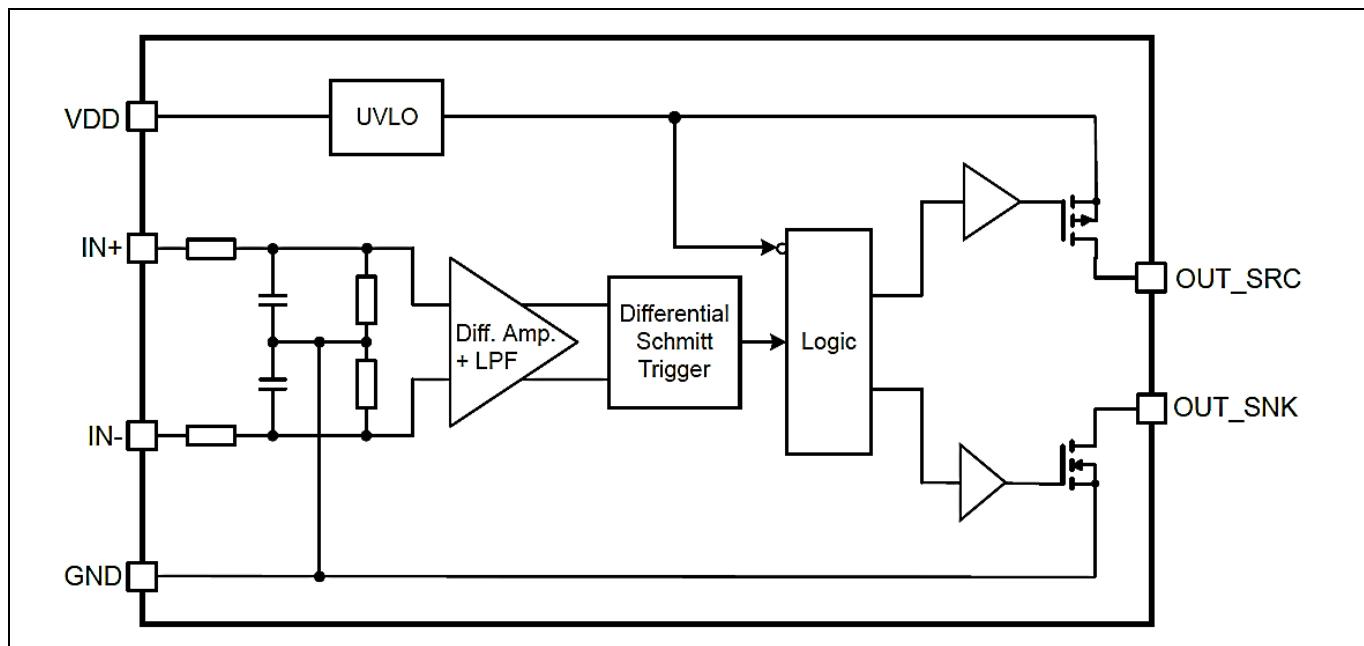


Figure 3 Internal structure of the 1EDNx550 gate-driver IC

The Schmitt trigger built into the 1EDNx550 introduces a hysteresis window equal to 0.2 V on the input-level interpretation. The operating states of the truly differential input driver are listed below:

- $V_{IN+} - V_{IN-} \geq 1.7 \text{ V}$: on-state
- $V_{IN+} - V_{IN-} \leq 1.5 \text{ V}$: off-state

The capability of 1EDNx550 to withstand AC ground-shifts is shown in Figure 4. An Infineon evaluation board has been used; this has been done purposely to test the driver and it is able to produce, through an internal ringing generator, AC shifts up to 108 V.

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Introduction

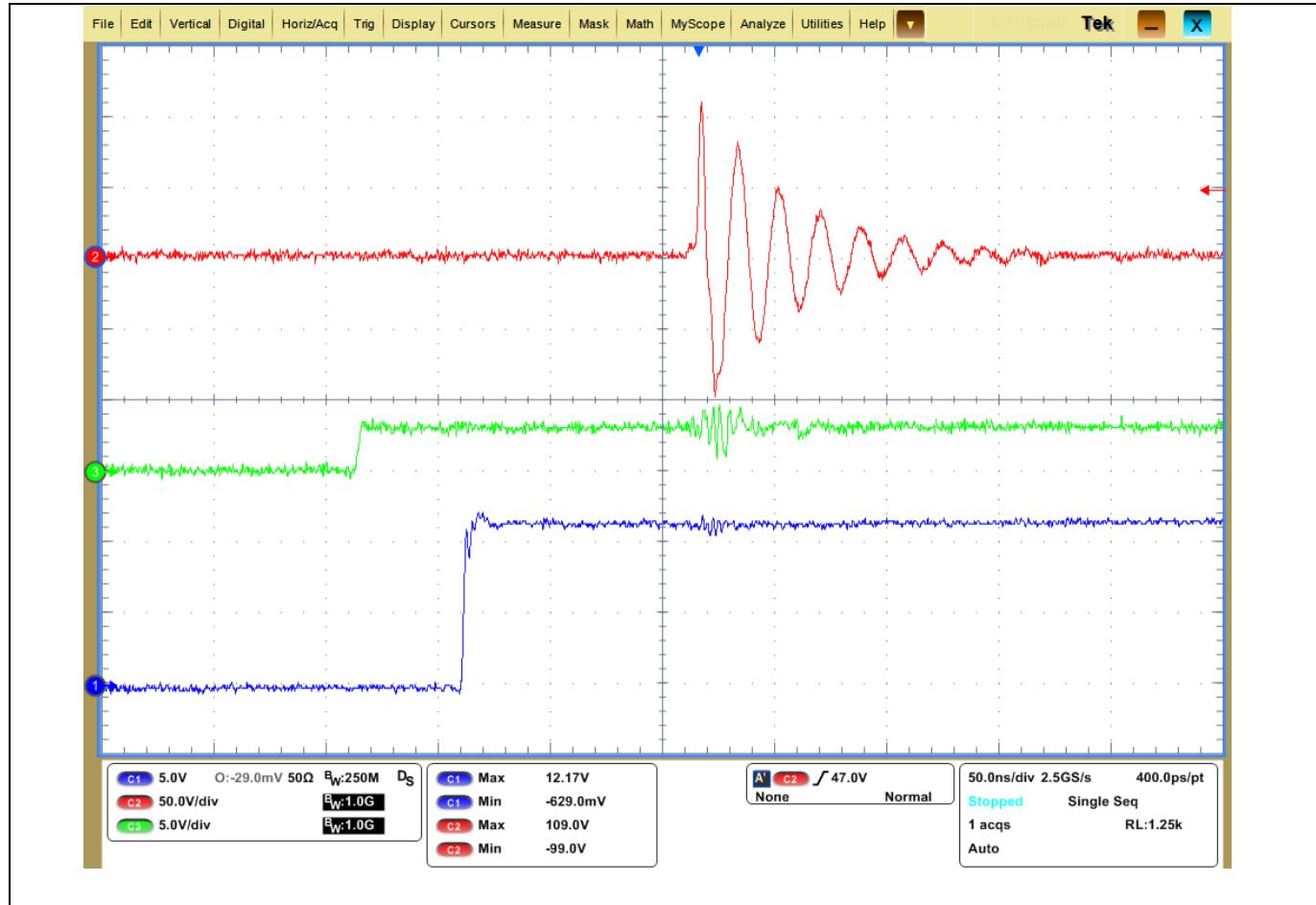


Figure 4 AC ground-shift robustness of the 1EDNx550 driver – in red the AC shift between the driver GND and the control stage GND, in green the driver PWM input signal, in blue the driver output signal

2 Application for PFC boost with Kelvin source 4-pin CoolMOS™

In a typical TO-220/247 package the parasitic source inductance assumes significant values in the range of 10 μ H. This leakage inductance is involved in the gate loop and negatively influences the performances through the increase of the turn-on switching losses and the generation of ringing on the MOSFET.

SMPS applications with strict efficiency constraints exploit the 4-pin CoolMOS™ devices to exclude the parasitic source inductance from the gate-driving loop. They use the additional Kelvin source terminal, which is available as source of the driving circuitry and is characterized by a very low parasitic inductance.

The main challenge with the driving of 4-pin devices is to handle the offset between the Kelvin source potential and the ground voltage of the microcontroller. The shift occurs during the transitions of the MOSFET when high values of $\frac{di_D}{dt}$ cause a significant voltage drop on the source parasitic inductance shown in Figure 5. The system ground voltage resonates, creating an AC shift with the driver ground.

Commonly isolated drivers are used to avoid the shifted interpretation, mentioned in Chapter 1, of the driver input signal. As shown in Figure 5, the secondary ground GND2 is connected to the Kelvin source potential. The input signal is processed by the driver primary side and proper operation of the driver is ensured, connecting the primary ground GND1 to the microcontroller ground.

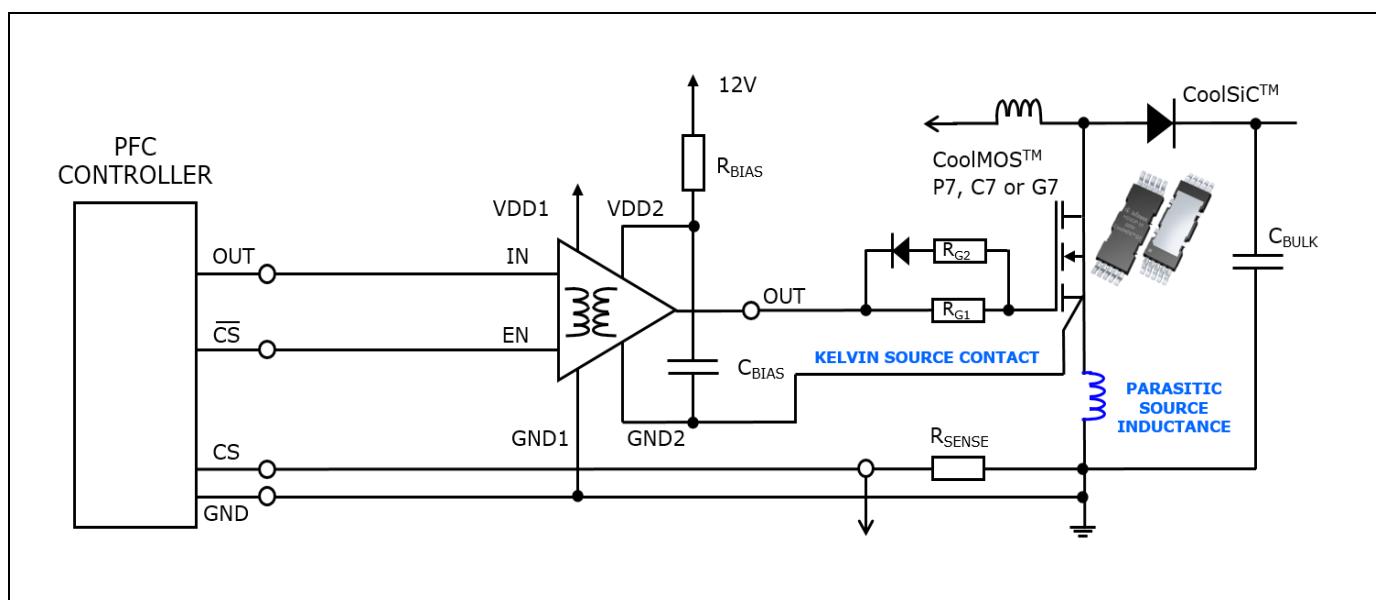


Figure 5 Driving solution for 4-pin CoolMOS™ devices based on isolated gate drivers

The single-channel isolated drivers, providing isolation values higher than 1 kV, are an over-specified solution in a wide range of applications. Realized with two chips, this solution is bulky and expensive.

The 1EDNx550 is a valid alternative and overcomes the limitations of an isolated driver. As shown in Figure 6, its ground pin is connected to the Kelvin source terminal and the AC shift is handled by the driver differential stage.

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Application for PFC boost with Kelvin source 4-pin CoolMOS™

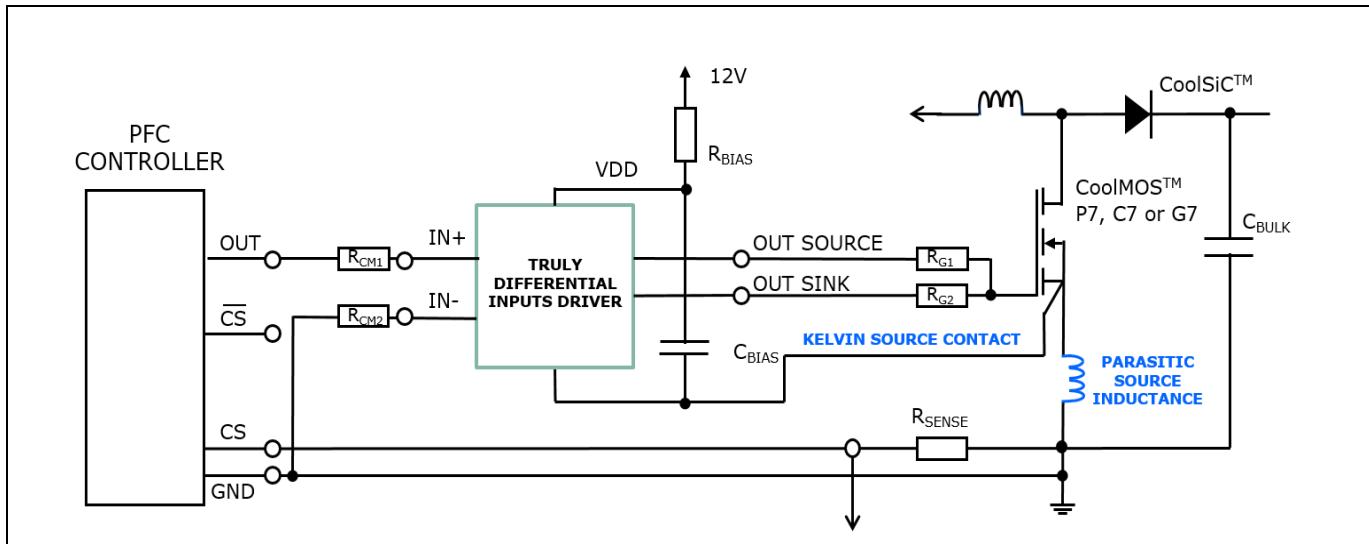


Figure 6 Driving solution for 4-pin CoolMOS™ devices based on the 1EDNx550 gate driver

In a PFB-boost application with 4-pin devices, the 1EDNx550 is a low-cost driving solution compared to the isolated driver. It is realized with a single die and requires a smaller package (SOT-23 compared to the DSO-8 of a typical single-channel isolated driver), also leading to an increase in the system power density.

The functionality of the 1EDNx550 in a 4-pin CoolMOS™-based application has been tested using the 2.5 kW PFC-boost evaluation board from Infineon visible in Figure 7.



Figure 7 1EDN7550 driver in the 2.5 kW PFC evaluation board with 4-pin CoolMOS™ - Highlighted in yellow the 4-pin device and in blue the 1EDN7550B

3 Application for single-layer PCBs or un-optimized PCBs

As well as the source parasitic inductance produced by the MOSFETs package, some SMPS layouts can experience an additional and significant leakage inductance on the ground path. Linked to the ground connection between the control IC and the driver, as shown in Figure 8, it generates a voltage drop during the transitions due to the change in the i_D current. Consequently, the ground voltage of the driver resonates, introducing an AC shift with the microcontroller ground.

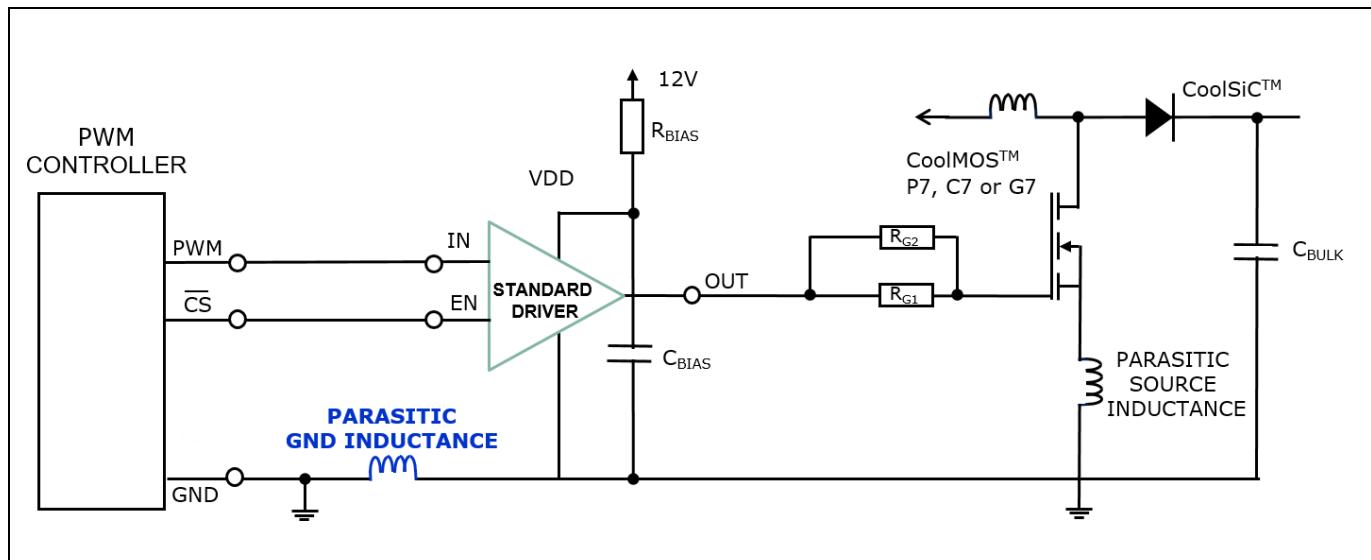


Figure 8 Conventional driving in a 3-pin MOSFET based boost converter

The 1EDNx550 provides a robust solution in such applications. Its usage is shown in Figure 9 and ensures the proper driving of the MOSFET.

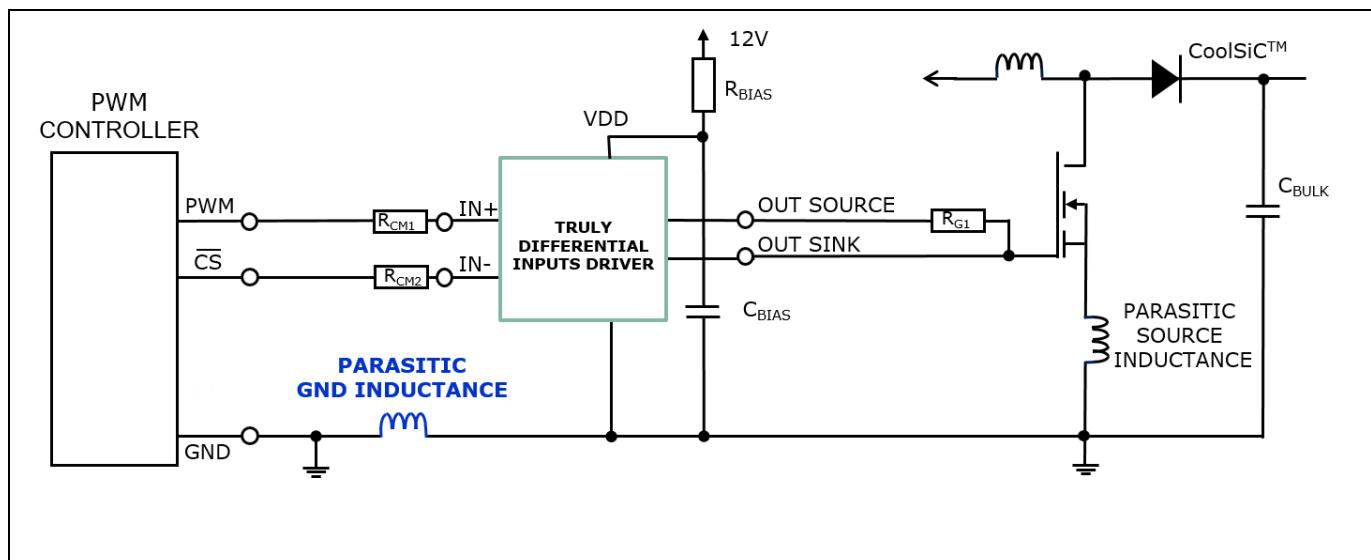


Figure 9 1EDNx550 based driving solution in a boost converter characterized by significant parasitic inductance on the GND path

The use of the 1EDNx550 is suggested in circuits where long wirings are used to connect the microcontroller and the driver. Some examples are listed below:

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Application for single-layer PCBs or un-optimized PCBs

1. Un-optimized or complex layouts
2. Control IC on external daughter card
3. Single-layer PCBs

In the latter case the AC shift on the ground path is made worse by the limited area of the available copper planes that leads to a weak shielding of the noise.

4 Application for high-side driving in half-bridge configurations up to 84V

The 1EDNx550 is designed to drive low-side MOSFETs in applications with AC ground-shift between the control IC and the driver. However, its properties also make it suitable for use in half-bridge or full-bridge configurations, as shown in Figure 10.

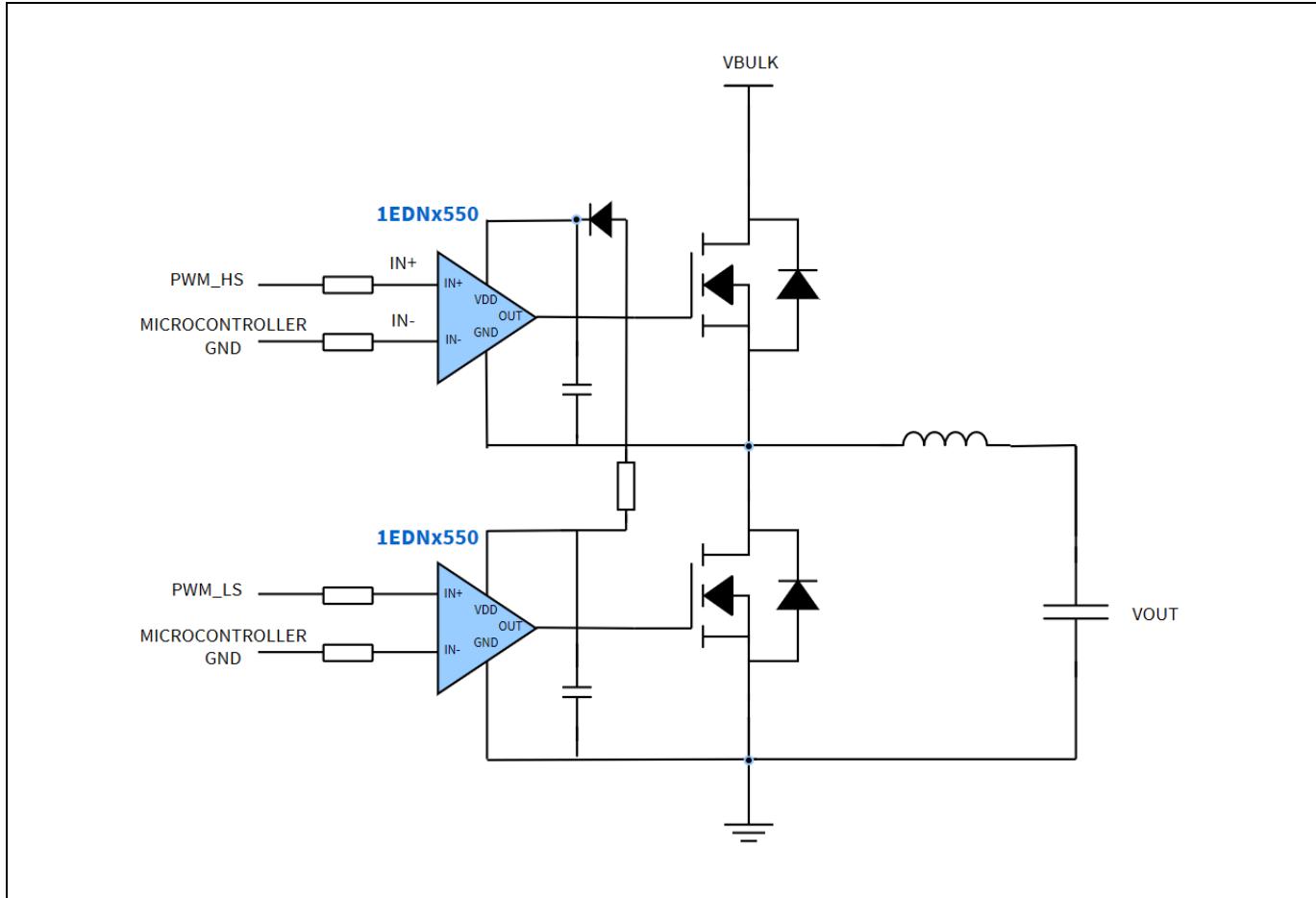


Figure 10 1EDN7550 based driving of the high-side MOSFET in a half-bridge buck converter

The 1EDNx550 can effectively drive high-side devices, replacing the common level shifters, in LV applications free of isolation requirements.

In the half-bridge structure in Figure 10 a DC offset equal to VBULK occurs between the ground of the high-side driver and the microcontroller ground. The differential behavior of the 1EDNx550 enables it to handle a floating ground up to 84 V.

Common applications are buck converters, full-bridge converters and synchronous rectifiers with a maximum input voltage of 84 V.

The functionality of the 1EDNx550 as a high-side driver has been tested in the 48 V input M1000011001 half-bridge buck converter evaluation board, designed purposely to do this, in Figure 11.

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Application for high-side driving in half-bridge configurations up to 84V

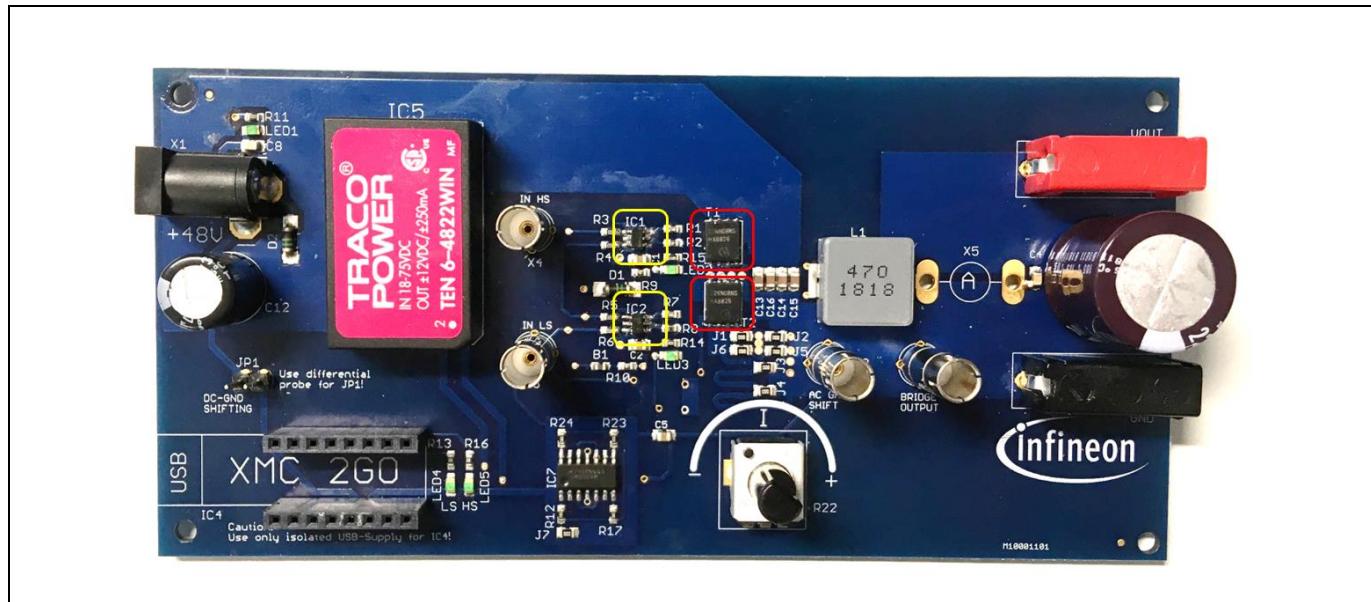


Figure 11 Top view of the M10000850 buck converter evaluation board – Highlighted in yellow the 1EDN8550B used as LS and HS drivers, in red the LS and HS MOSFETs

As well as the possibility of testing the 1EDNx550 robustness to DC ground shifts, the demo board provides additional features to create different AC ground-shift scenarios.

The high-side driver capability of the 1EDNx550 is demonstrated by the half bridge waveforms in Figure 12.

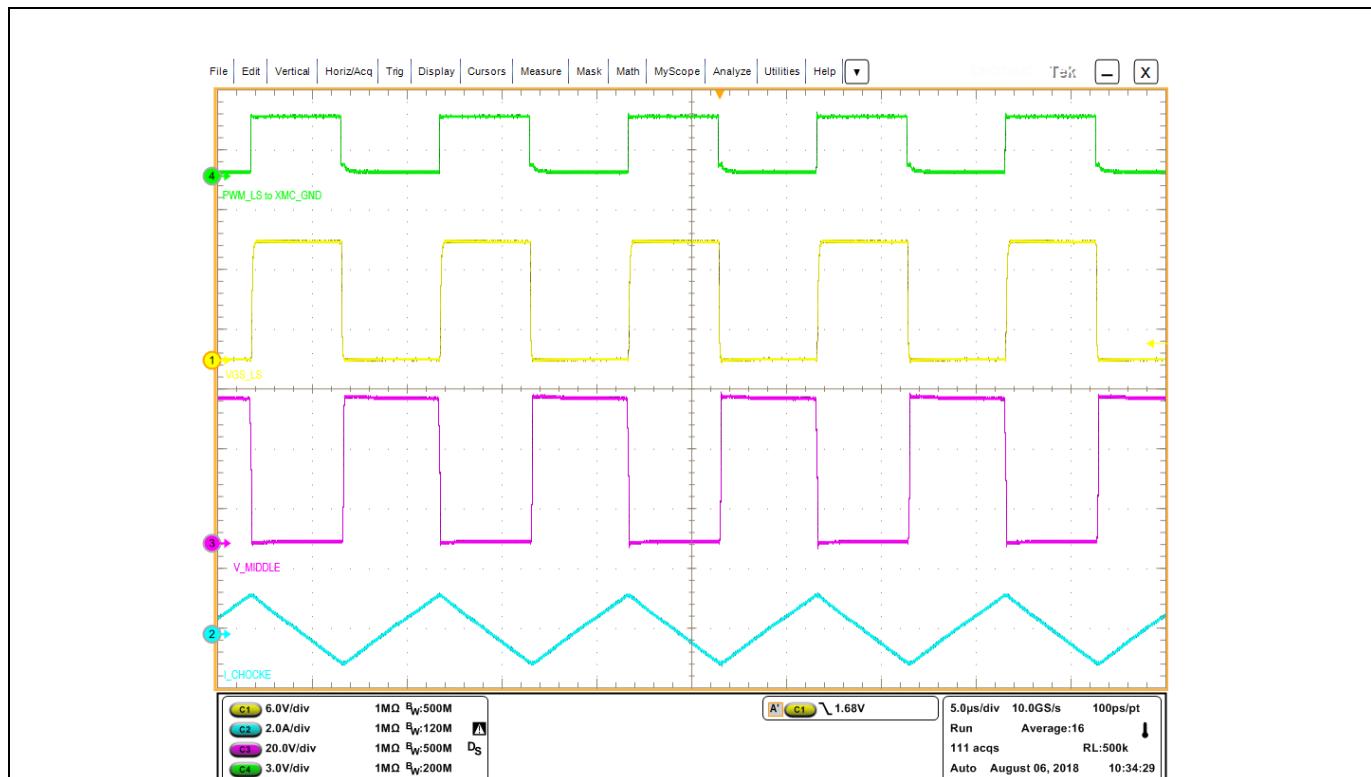


Figure 12 DC ground-shift robustness of the 1EDN8550 driver in the M1000011001 Half Bridge evaluation board – low-side PWM signal in green, low-side gate-to-source voltage in yellow, half-bridge middle node voltage in magenta, output inductor current in cyan

Layout guidelines

5 Layout guidelines

It is well-known that the layout of a fast-switching power system is a critical task with strong influence on the overall performance. Therefore, there are a huge number of rules, recommendations, guidelines, tips and tricks to finally achieve a proper system layout.

With 1EDNx550 one of the central layout problems, namely the design of the grounding network, has become much less critical due to the highly reduced sensitivity of the differential concept with respect to ground voltage differences. So layout rules can be restricted to the following rather simple and evident ones:

- place input resistors R_{IN} close to the driver and make layout of input signal path as symmetric as possible;
- use a low-ESR decoupling capacitance for the VDD supply and place it as close as possible to the driver;
- minimize power loop inductance as the most critical limitation of switching speed due to the resulting unavoidable voltage overshoots.

A layout recommendation for the input path is given in Figure 13.

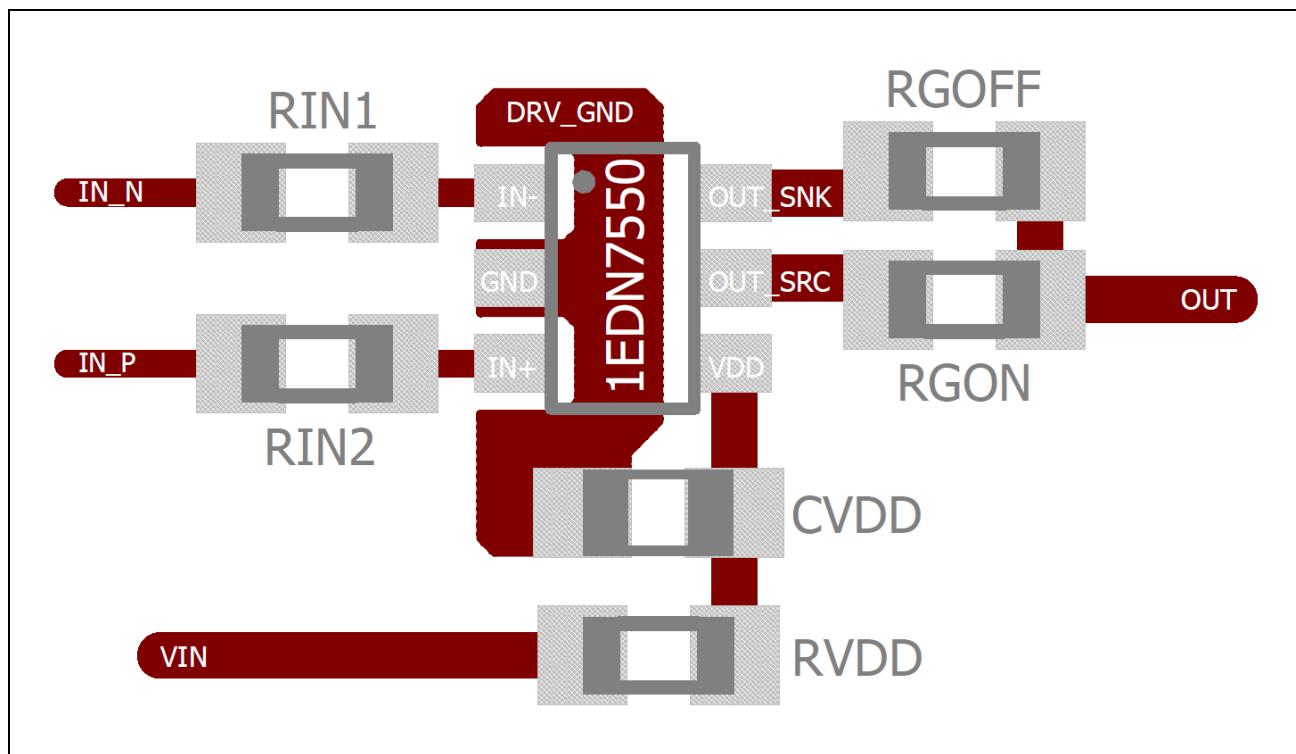


Figure 13 Layout guidelines

6 References

[1] [AN_201408_PL11_027_EVAL_2.5KW_CCM_4PIN](#) – 2.5 kW PFC evaluation board with CCM PFC controller ICE3PCS01G

Revision history

7 Revision history

Document version	Date of release	Description of changes

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