AN5026
Application note

VIPower M0-7 H-bridges

Introduction

The VIPower M0-7 H-bridge family of fully integrated and protected H-bridges are designed to drive low or medium power automotive DC motors.

Each device in the family contains the monolithic double high side driver and two low side chips.

The following features render these devices ideal for numerous DC motor applications (e.g., door locks, washer pumps, fans, mirrors, etc.) in the rigorous automotive environment:

- integrated logic for driving each MOS according to clockwise or anticlockwise motor rotation and braking
- possibility to employ PWM at 20 kHz for speed control
- embedded protections against electrical or thermal stress
- state of the art “MultiSense” diagnostic in ON and OFF state.

The purpose of this hardware design guide is to provide a comprehensive tool kit for design engineers to better understand M0-7 H-bridge behavior and the application usage context, as well as to facilitate embedding the design.

Contents

List of tables

List of figures

1 General items

The VIPower M0-7 H-bridges are built with same technology blocks featuring common functionality and a unique analogue diagnostic feedback pin. The individual devices, featuring specific $R_{ds(on)}$ (R_{ONHS} + R_{ONLS}) values for different load ranges, are listed below:

- VNH7040AY: 40 mΩ typical in a PowerSSO-36 TP package
- VNH7070AS / VNH7070BAS: 70 mΩ typical in a SO-16L package
- VNH7100AS / VNH7100BAS: 100 mΩ typical in a SO-16L package

1.1 Pin description

The M0-7 H-bridges are designed to be housed in the tiny 16-lead S0-16 plastic package and the 36-lead PowerSSO-36 package with three additional exposed pads on the surface for high thermal conductivity to the PCB, significantly increasing the power that can be managed by the device.

1.2 Common pins for all VNH7XXX devices

- **INA, INB**: voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. A logic high level on INA turns high side A (HSA) on; logic high level on INB turns high side B (HSB) on
- **PWM**: voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. A logic high level turns one or both the low side drivers on, depending on the state of INA, INB pins. A square wave signal up to 20 kHz can be used on this pin for motor speed control.
- **Vcc**: power leads are connected internally to the two HS drains and must be connected to the battery track of the application.
- **GNDA, GNDB**: connected internally to the LSA, LSB sources and also represent the ground reference of the device logic.

1.3 Additional pins for devices in SO-16N package

- **OUTA, OUTB**: these output power pins are connected to the external load. The OUTA leads are internally shorted to the sources of the HSA PowerMOS and the drains of the LSA PowerMOS; likewise for OUTB, HSB and LSB. All OUTA and OUTB leads must be connected to corresponding leads to ensure uniform distribution of the load current in the device.
- **SEL0**: voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. A logic high level lets the device sense, through the CS output, the current flowing in the HSA or a fault relevant to the Output A; likewise for logic low, HSB and Output B. This pin also allows the CS to signal an open load or stuck to battery.
- **CS**: the multiplexed analog sense output pin:
  - delivers a current proportional to the HSA output current if SEL0 is set high; likewise for HSB if SEL0 is set low
  - develops a voltage flag for a failure on the relevant output in the ON state as well as the OFF state

1.4 Additional pins for devices in PowerSSO-36 TP package

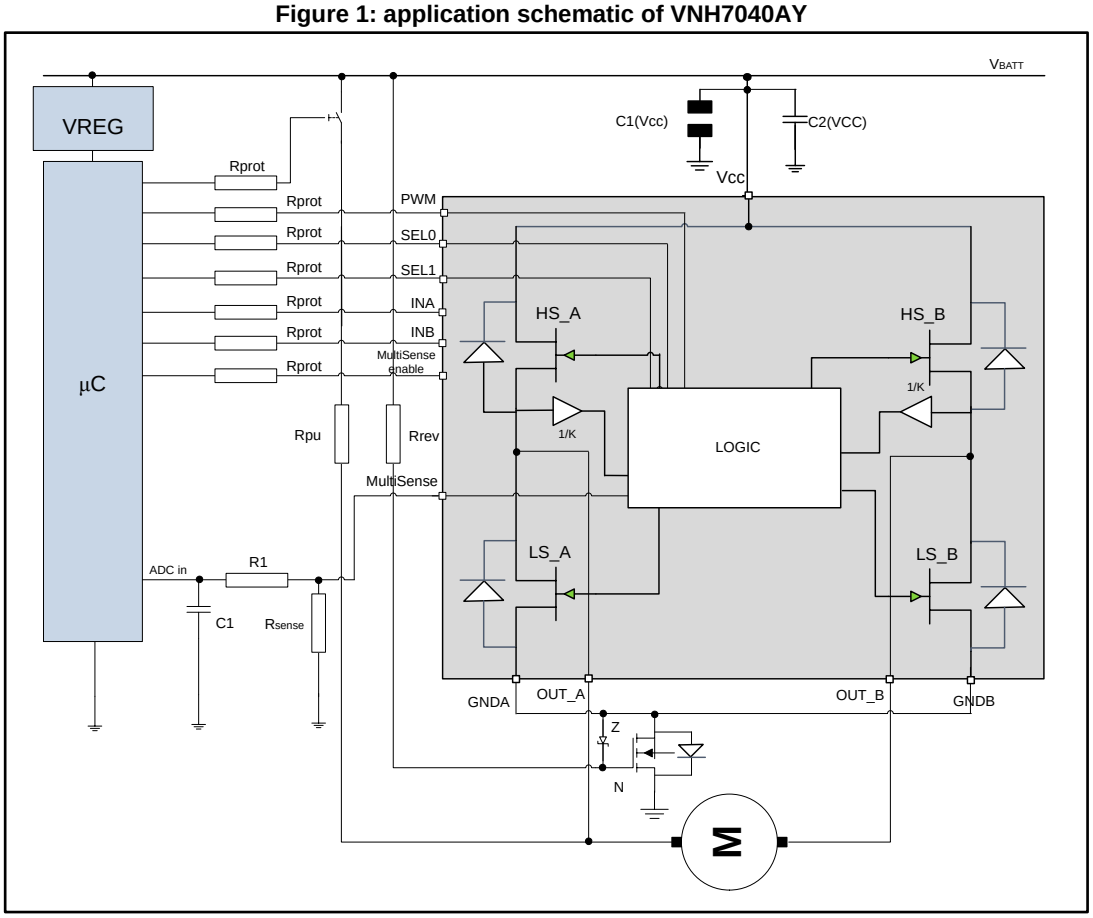
- **DRAIN_LSA, SOURCE_HSA and DRAIN_LSB, SOURCE_HSB**: output power pins which must be shorted to corresponding pins on the PCB and connected to an external load terminal. This connection is the clockwise terminal and counter-clockwise of the bi-directional DC Motor for the A side and B side, respectively.

Alternatively, if the device implements a two half H-bridge topology, the positive terminal of the mono-directional motor placed on branch A or branch B.

- **MultiSense**: the multiplexed analog sense output pin:
  - delivers a current proportional to the HSA or HSB output current according to the settings SEL0 = high or low and SEL1= low
  - in combination with SEL1 = low and SEL0 = high or low settings, it develops a voltage flag in case of failure on the relevant output in the ON state as well as the OFF state
  - In combination with SEL1= high and SEL= high or low settings, it develops a voltage signal proportional to the high side chip temperature or Vcc voltage
- **SEL0, SEL1**: voltage controlled input pins with hysteresis, compatible with 3 V and 5 V CMOS outputs. They act as Multiplexer input pins thus:
  - In the ON state: when SEL1 is low and SEL0 is high, they allow sensing the current flowing in the HSA or a fault relevant to the Output A through the MultiSense output; likewise for SEL0 low, HSB and Output B.
  - In the OFF state: When SEL1 is low and SEL0 is high, they allow monitoring of the voltage level of $DRAIN\_LS_A$, $SOURCE\_HS_A$ to detect and signal an open load or an output stuck to Vcc through the MultiSense output; likewise for SEL0 low, $DRAIN\_LS_B$, $SOURCE\_HS_B$
  - Both in ON or OFF state: two combinations allow the MultiSense pin to develop a signal proportional to the high side driver chip temperature (SEL0=low, SEL1=high) or to the Vcc voltage (SEL0=SEL1=high)
- **MultiSense_EN**: voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. A logic high level enables the MultiSense output reading. A logic low level sets the MultiSense output to high impedance.

1.5 Basic application schematic

Figure 1: application schematic of VNH7040AY



- **Rprot**: resistors are placed in series with digital inputs (INA, INB, SEL0, SEL1, PWM, and MultiSense_EN) to limit the current in the input structures and in the microcontroller output structures to a safe value during transient and reverse battery conditions. An appropriate value is 1k.
- **Rsense**: converts the current sense output current, which is proportional to the load current, into a voltage which can be read by the A/D converter of the microcontroller. The magnitude of Rsense should ensure an appropriate resolution range and granularity to monitor nominal current as well as detecting open load and overload events. A typical value is around 1 kΩ (see *Section 5.1.4: "Dimensioning the Rsense resistor"*). Rsense should not be lower than 765 Ω in order to sustain reverse battery polarity.
- **R1, C1**: an RC low pass-filter placed across the Rsense resistor to suppress HF noise. The time constant of this filter (RxC) should be long enough to suppress noise and short enough to allow MultiSense signal stabilization taking into account multiplexer delay and settling times in case of a shared microcontroller A/D port. C1 should be placed close to the MCU A/D input and its ground connection should be at the same potential as the ground of the A/D reference.R1 should be 10 kΩ and also limits the A/D input pin current.
- **C1(Vcc)**: this capacitor is used to suppress high energetic voltage transients developed, for instance, when the motor rotates and the OUTPUTs enter tristate conditions due to a battery line cut-off (see *Section 3.2.2: "Design verification checks"* and *Section 3.2.3: "Overview of capacitor C1(Vcc) assessment"*).

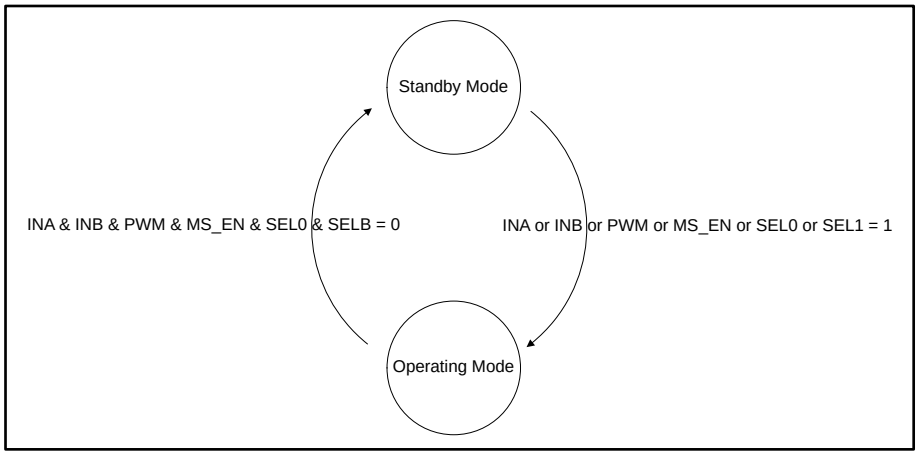
- **C2 (Vcc)**: the C2 capacitor helps suppress voltage transients that originate from other actuators connected in parallel and sharing the same battery line. This capacitor is only able to suppress low energetic short transient pulses and HF noise at the Vcc pin (see *Section 3.2.2.2: "C2(Vcc) capacitive filter on the IC supply line"*).
- **Rpu**: The pull up resistor is used for the open load detection of the OFF state (see *Section 5.1.11: "Open load detection in off-state"*).One Rpu is sufficient for a full H-bridge configuration. Two Rpu are required for a two half (one for each half) H-bridge configuration
- **N, Rrev and Z**: represent the reverse battery network. The N-MOS with source connected to the ground pins of VNH7XXX and drain on Power GND provides reverse battery and battery negative fast transient protection. Its gate needs to be connected through Rrev = 100 kΩ resistor to the battery track and a Zener diode Z is required between its gate and source to clamp the gate voltage during positive transients on the battery track (see *Section 3: "External protections"*).

1.6 Operating modes

The VNH7XXX H-bridges have the following main states (see *Figure 2: "H-bridge operating modes"*):

1. Operating mode: occurs when at least one of the input signals is set to logic level high. This condition includes the OFF state of both low side and high side MOSFETs (i.e., INA = INB = PWM = 0 V). The device current consumption from the Vcc pin in the OFF state is a few mA (indicated as I_S “off state-no-stanby” in the datasheet).
2. Standby Mode: occurs when all input signals pins (INA, INB, PWM, SEL0, SEL1, MultiSense_EN) are set to low. The current drawn by the bridge is 1µA max. from -40 °C to 85 °C in this mode. After the last input pin has been set to zero, the H-bridge only enters standby mode after a t_{D_stby} delay given in the datasheets (see *Section 5.1.8: "Entering standby-mode after an OVL event"*) to avoid triggering accidental standby due to the rapid commutation of all input pins to zero level. The device exits the standby condition when any of the IN, PWM, MultiSense_EN or SELx pins is set high.

Figure 2: H-bridge operating modes

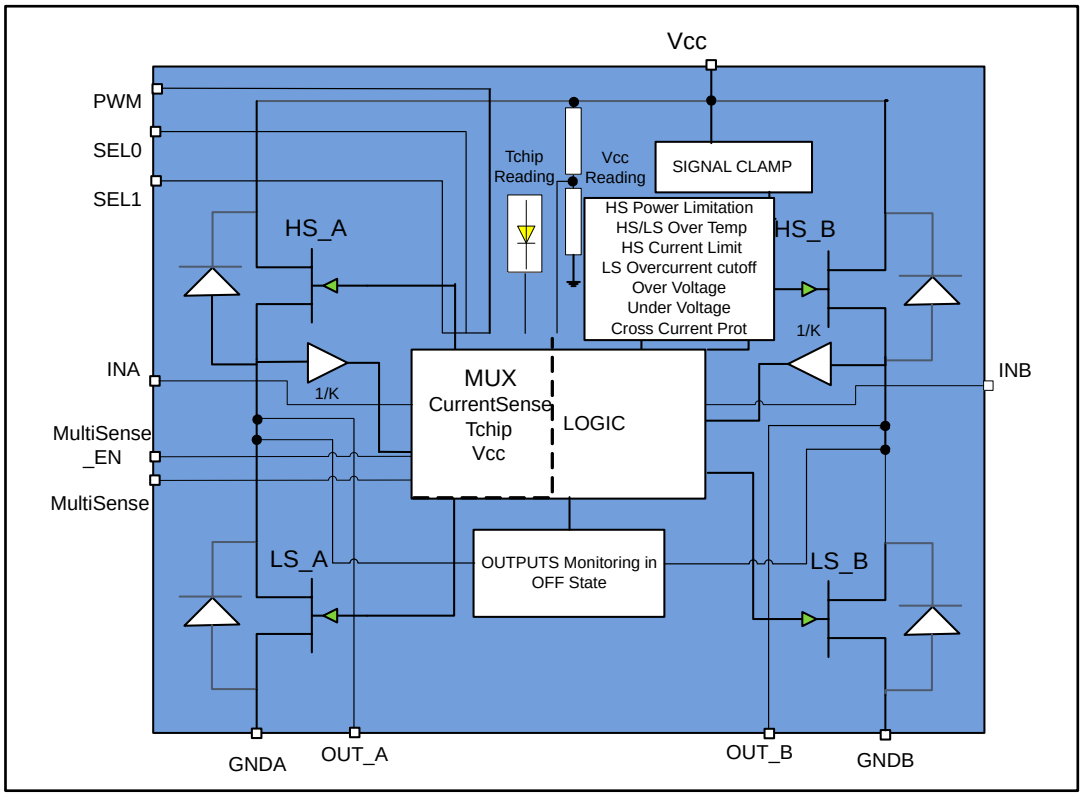


2 Embedded protections

VIPower M0-7 H-bridge drivers integrate advanced protection functions to protect both the power stage and the load. A Power MOSFET must be protected against overvoltage, overcurrent and over temperature events outside the safe operating area.

Typical overvoltage protection involves a clamp that allows switching on the PowerMOS during exposure to the stress. The Power MOSFET is current protected by a current limiter block or current latch circuitry. The Power MOSFET is protected against high temperature events both by thermal shut down and by a power limitation block that limits the junction temperature gradient with the time.

Figure 3: simplified internal blocks of a H-Bridge in PowerSSO-36 package



2.1 Protection against overvoltage

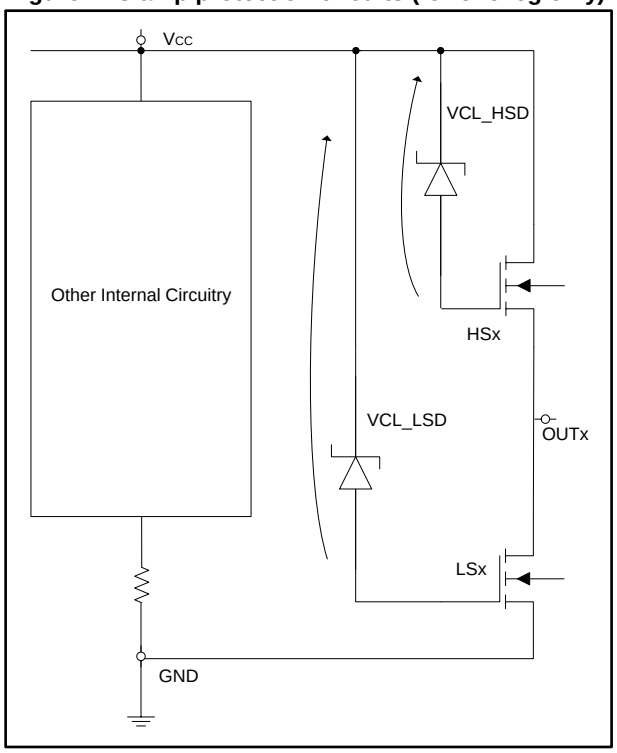
2.1.1 Overvoltage clamp

The device is protected against voltage transients on V_{CC} (e.g., ISO7637/2 transients) via the combination of the HS and LS power clamps (indicated in the datasheet as V_{CL_HS} and V_{CL_LS} respectively). As soon as a voltage transient higher than V_{CL_HS} = V_{CL_LS} occurs on V_{CC}, the LS is forced to work in the ohmic region while the HS is forced to work in the linear region. Therefore, the component subjected to the highest dissipation is the HSx.

For negative transients applied across the device supply pin terminals, most of the current flows through the PowerMOS body diodes. It is not limited by anything other than the pulse generator intrinsic resistance.

External circuitry is normally used to protect the device against such events.

Figure 4: Clamp protection circuits (for one leg only)



2.1.2 Device behavior with respect to ISO7637/2-2:2011(E) and ISO16750 standards

The table below describes the device performance with tests applied to VNH7XXX only, without components and accessed through V_{CC} and GND terminals only.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as: *"The function does not perform as designed during the test but returns automatically to normal operation after the test"*.

During negative pulses (1 and 3a) the energy is transmitted through the series of body diodes of the HS and LS and the clamp signal circuit.

Table 1: ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	U s(1)		min	max	
1	III	-112 V	500 pulses	0.5 s		2 ms, 10 Ω
2a	III	+55 V	500 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	IV	-220 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	IV	+150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4 (2)	IV	-7 V	1 pulse			100 ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	U_S (1)		min	max	
Test B - (3)		40 V	5 pulse	1 min		400 ms, 2 Ω

Notes:

(1) U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.

(2)Test pulse from ISO 7637-2:2004(E).

(3) With 40 V external suppressor referred to ground (-40°C < T_j < 150 °C).

2.1.3 Device behavior after a load dump

Load dump refers to the disconnection of the vehicle battery from the alternator while the battery is being charged. The bridges are subjected to pulses simulating this condition, according to ISO165750-2 (see *Figure 6: "Examples of waveforms relevant to ISO pulse 5b (load dump) applied to a VNH7XXX"*, where I_{MOV} is the current flowing in the external transil during the pulse).

Figure 5: Pulse waveform for ISO165750-2 test

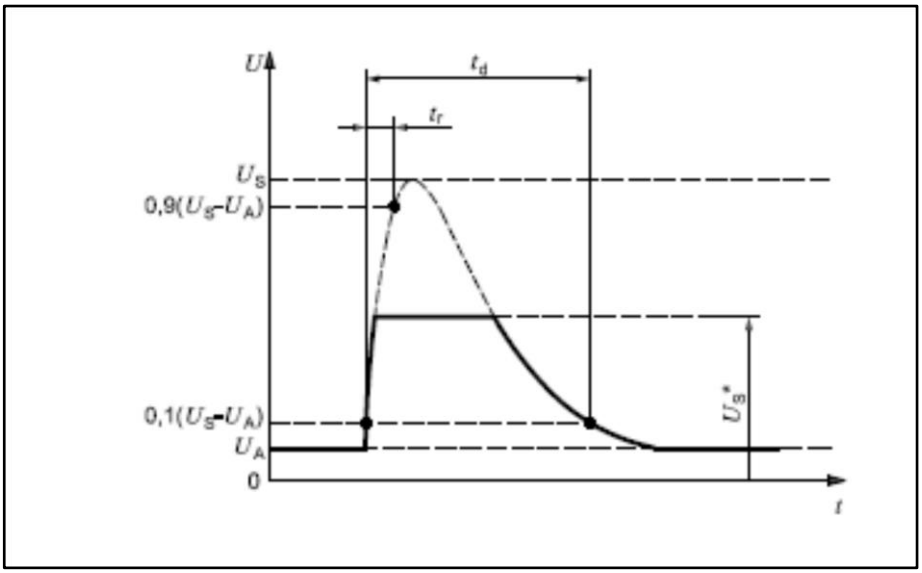
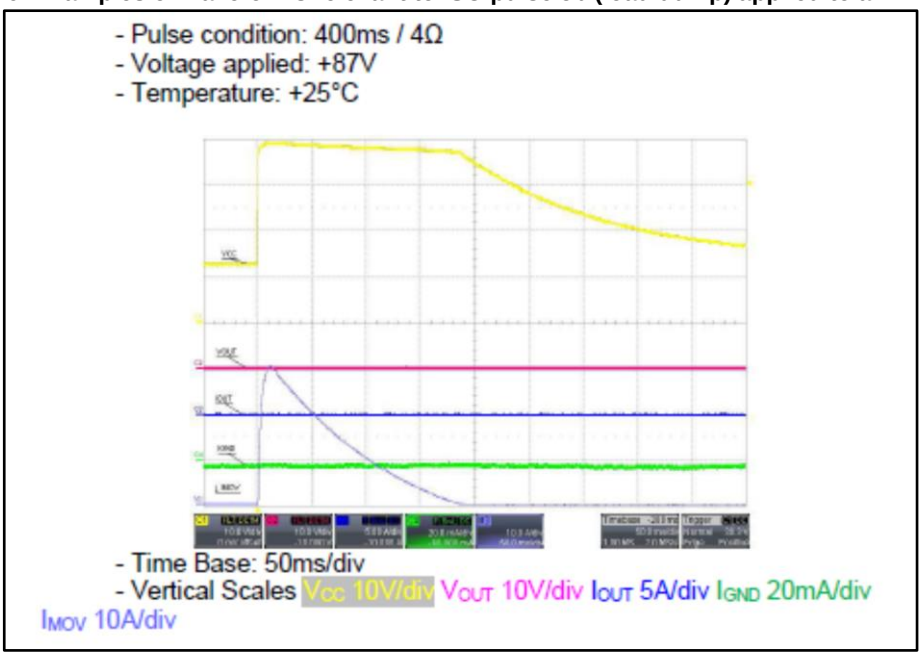


Figure 6: Examples of waveforms relevant to ISO pulse 5b (load dump) applied to a VNH7XXX



The PowerMOS energy of the LS and HS is not given in the datasheet since the device is intended to be used in H-bridge driver configuration. The inductive energy of the load in fact normally re-circulates in the PowerMOS body diodes.

External components like filtering capacitors on Vcc are necessary when the battery transients exceed those listed in the tables for ISO7637-2 and ISO 16750-2 (see *Section 3: "External protections"*).

2.2 Undervoltage protection

This function shuts down the device when battery voltage V_{BAT} is lower than V_{USD} (given in the datasheet) with an active high signal acting directly on the LS and HS gates, turning them off.

This protection validates the internal supply as soon as it is able to supply all logic blocks appropriately:

- For V_{CC} decreasing from 13.5 V, the device is turned off at about 2.5 V; current sense is disabled from about 2.9 V V_{CC}.
- Normal behavior resumes when V_{BAT} reaches V_{USD} + $V_{USDhyst}$.

The undervoltage condition is not considered a fault condition so it is not reported by the diagnostic.

- As V_{CC} rises, the device is typically turned on at 2.8 V.
- Current sense starts to operate at about 3 V.

Parameters which represent undervoltage behavior are given in the datasheet:

- V_{USD} is the maximum shutdown voltage when V_{CC} is decreasing
- V_{USD_reset} is the level which turns on the bridge when V_{CC} is increasing3
- V_{USD_hyst} is the typical hysteresis of the two voltages.

2.3 Loss of VCC and loss of GND

2.3.1 GND disconnection

Following GND disconnection, the device can stop normal operation (motor rotation control) but it must end up in a safe operating state with no motor activation.

2.3.1.1 Device GND pin disconnection

This can occur due to physical defects in PCB soldering.

Any H-bridge in an SO-16N package has four different GND pins, or 10 GND pins in a PowerSSO-36 TP package. These are split in two pairs, where each is connected to the relevant LS source.

A soldering issue causing all GND pins to be disconnected from the PCB is quite unlikely and, even if does occur, all four PowerMOS are switched off.

The device resumes normal operation once GND is reconnected.

2.3.1.2 Disconnection of the module GND line

If the module GND line that supplies the VNH7xxx is disconnected, the device switches off immediately, as shown in the following figure.

As the H-bridge Power elements are OFF, any residual motor energy is dissipated in the external IC components, especially the capacitor on the V_{CC} pin. This is charged and must be properly dimensioned (see *Section 3.2.5.2: "Capacitors on VNH7XXX Outputs (C(OUT)) and on Vcc (C2(Vcc))"*).

Figure 7: GND loss (INA, Iout, Vbatt, Vsense)

In the figure above, where the device is alternatively driven clockwise and counter-clockwise:

- red arrow: the device stops operation immediately after GND disconnection
- white arrow: device restarts normal operation as the GND line is reconnected

2.3.2 Loss of battery connection

Similar considerations are applicable to the battery where multiple pins (exposed pad included for PowerSSO-36 TP) are connected to the V_{CC} signal.

2.3.2.1 Battery line disconnection

When battery disconnection occurs, the device V_{CC} voltage starts to decrease since the bulk capacitor energy is used to supply the motor.

Figure 8: Battery loss (INA, Iout, Vbatt, Vsense)

- red arrow: motor operation stops as the V_{CC} undervoltage threshold is reached
- white arrow: operation restarts once battery is reconnected

External precautions are necessary to avoid the load energy increasing voltage V_{CC} above V_{CLAMP}, which may damage the device.

2.4 Short-circuit protection

Short-circuit events are signaled by the diagnostic CS pin (MultiSense in VNH7040AY). In fault conditions, Vsense is pulled high to VsenseH on the selected leg (through SEL0 input signal).

2.4.1 Short-circuit on device outputs to car ground

For output shorted to GND, the High Side in the ON state is the stressed element in the VNH7XXX and the drain current rises well above nominal levels.

When the I_{LIMH} threshold is reached, an embedded current limiter intervenes to protect the HS PowerMOS against dangerous current density. In this condition, the High Side PowerMOS works in the saturation region and dissipates high power due to simultaneous high voltage and high current.

At this point, the power limitation block circuit, designed to limit the fast thermal transients in the device to improve device lifetime, intervenes. It monitors the difference between the temperature read by a case temperature sensor embedded in the logic and the junction temperature measured by a sensor in the PowerMOS.

If the HS PowerMOS junction temperature exceeds the case temperature by about 60°C, the HS latches itself off.

The HS is protected against absolute maximum junction temperature (datasheet symbol T_{TSD_HS}) by the overtemperature thermal shutdown block.

In summary, the HS has the following protection circuits:

- Current Limiter: triggering of this protection is not signaled by CS (MultiSense) and does not cause device latch off
- Power Limitation circuit: triggering of this protection is signaled by CS (MultiSense) and causes device latch off
- Overtemperature shutdown circuit: triggering of this protection is signaled by CS (MultiSense) and causes device latch off

In the figure below, the device terminal A is shorted to GND and then switched on.

Figure 9: Power Limitation event (VINA, VoutA, Vsense(SEL0=1), Iout=Ihsd)

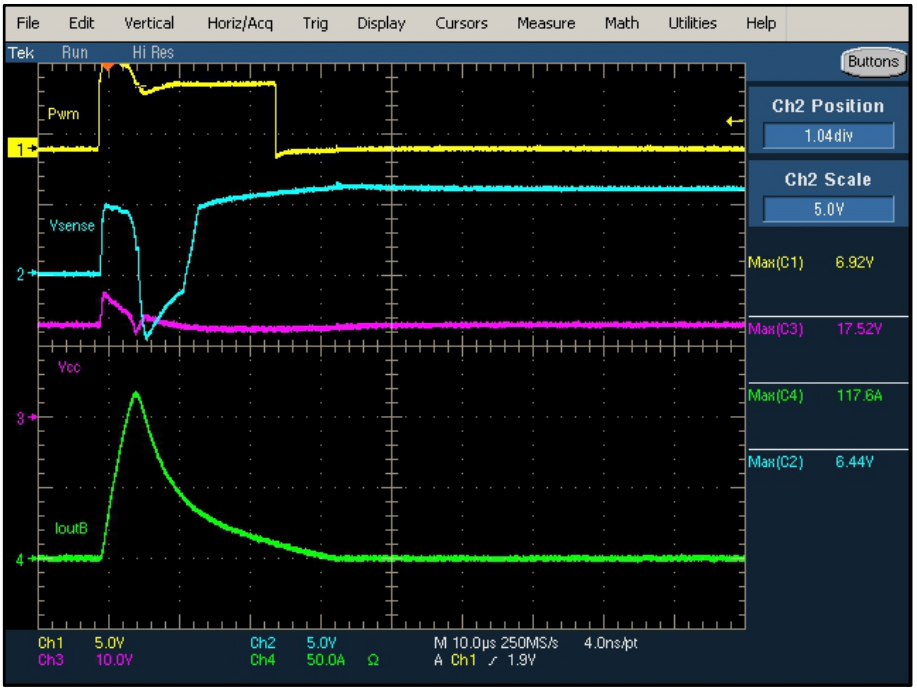
2.4.2 Short to Vcc protection

For output shorted to V_{CC}, the Low Side in the ON state is the stressed element in the VNH7XXX and the drain current rises well above nominal levels in the device. In this case, the LS has a double protection depending on whether the short-circuit is hard or resistive.

2.4.2.1 Hard short-circuit

In a hard short-circuit (few mΩ resistance), as soon as the current through the low side MOSFET exceeds the I_{SD_LS} shutdown current, the device is switched off after a certain filtering time (indicated as t_{SD_LS} in the datasheets) and it latches. The fault condition is then detected by the diagnostic.

Figure 10: VNH7070BAS short to Vcc event (CH1=VPWM, CH2=Vsense(SEL0=0), CH3=Vcc, CH4=Ivcc, INA=1, INB=0



A filtering time (datasheet symbol T_{SD_LSD}) after the LS current reaches its threshold helps avoid unwanted Low Side latching at switch-on when, for example, filtering capacitors are placed on the VNH7XXX OUTPUTs.

Just before LSx switch-on, the corresponding OUTx is at battery voltage. When the LSx is switched on, the output filtering capacitor is subjected to rapid voltage variation and a consequent current spike.

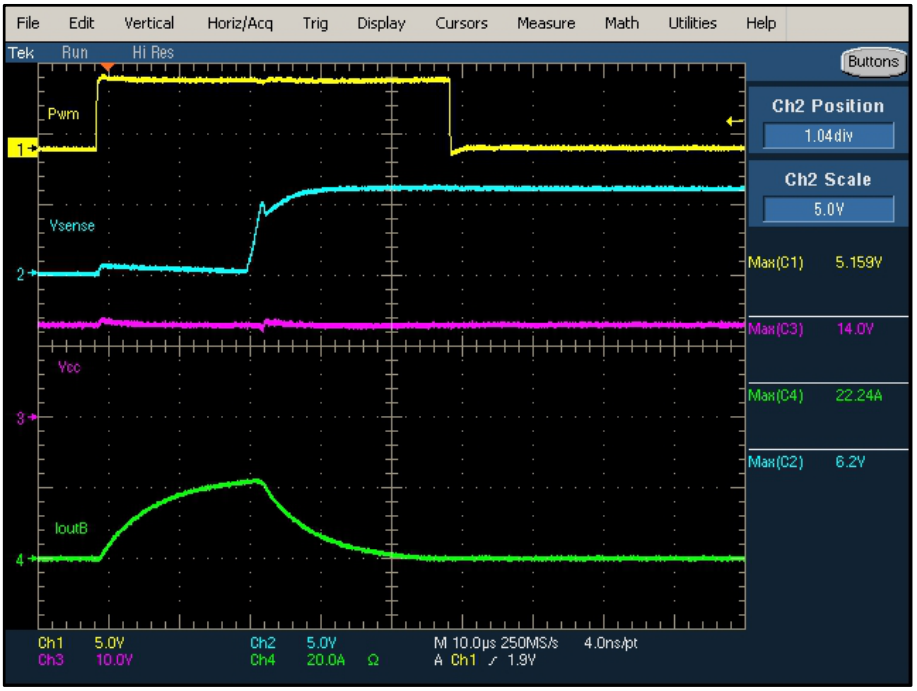
Depending on capacitor size and LS switch-on time (t_f in datasheet), this current spike can reach I_{SD_LS}, which is why this protection needs to be filtered out.

2.4.2.2 Resistive (soft) short-circuit - overload

In a resistive short-circuit, the current through the low side MOSFET doesn't reach I_{SD_LS}, but the temperature rises to the LS thermal shutdown level, causing the device to switch off and latch; this fault is detected by the diagnostic.

In the figure below, the device terminal A is before shorted to V_{BAT} and then the LSA is switched on.

Figure 11: VNH7070BAS short to Vcc event (CH1=VPWM, CH2=Vsense(SEL0=0), CH3=Vcc, CH4=Ivcc INA=1, INB=0



In summary, the Low Side has the following protection circuits:

- Shutdown low side current: triggering of this protection is signaled by CS (MultiSense) and causes device latch off
- Overtemperature shutdown circuit: triggering of this protection is signaled by CS (MultiSense) and causes device latch off

The VNH7XXX enters standby mode if all logic pins (INA, INB, SEL0 and PWM) are at low logic level. The aim of standby is to minimize I_s device current consumption while the module is idle.

At device power on from standby mode, it is recommended to toggle either INA, INB, SEL0, SEL1 or MultiSense EN out of STBY mode and then toggle PWM with a delay of at least 20 µs. This avoids overly stressing the LS in case of permanent short-to-battery.

The device behavior in case of short-circuit to V_{BAT} is influenced by the initial state:

- starting from the STBY condition, the internal logic needs around 20 µs to detect the short to V_{BAT} and turn off the LS, during which time the device operating current is well above I_{SD_LS}. The characteristics of the short-circuit (stray inductance and resistance) play a key role in limiting the current slope and following the max. peak current because of the 20 µs delay time.
- starting from a condition other than STBY, the internal logic detects the fault immediately after the built-in filtering time (t_{SD_LS}), turning off the LS at a lower peak current.

2.4.3 Short-circuit across the load

A hard short-circuit across the load latches due to the triggering of the overload current shutdown protection of the PowerMOS with the lowest value. The VNH7XXX bridges are designed with the High Side current limitation (I_{LIM_H}) lower than the Low Side shutdown current (I_{SD_LS}).

2.4.3.1 Short-circuit is applied so that HSA is switched on while the LSB is already on

In the following figure, at the HS switch on V_{DS}, HS = V_{CC} – V_{outA} ~ V_{BAT}, meaning that the whole battery voltage is across the HS terminals. In this condition, the HS dissipates a lot of power deriving from I_{LIMH} x $V_{BAT,}$ while the power dissipation inside the LS is much less as the LS V_{DS} is well below 1 V.

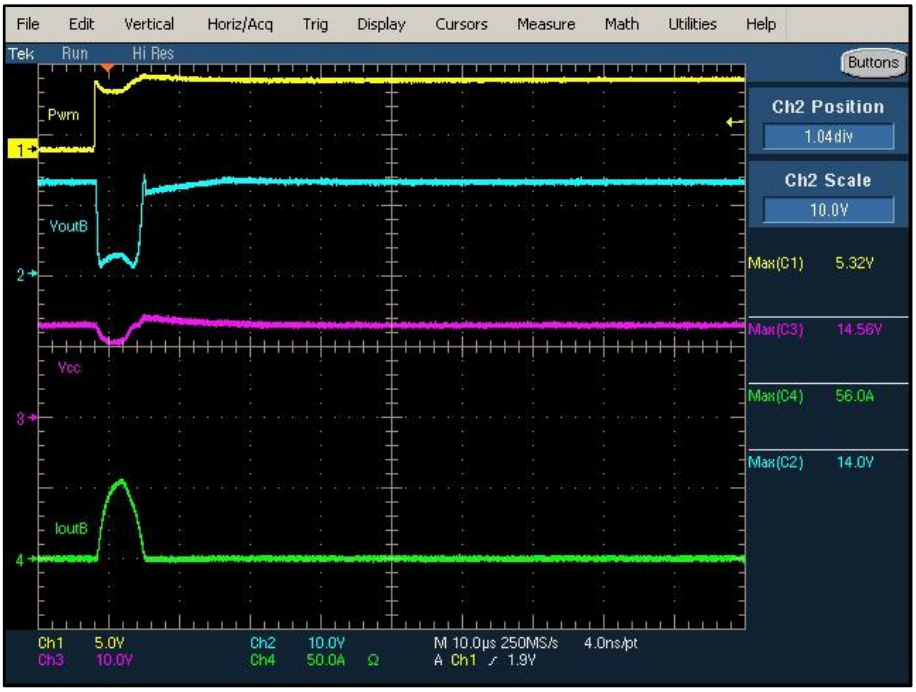
As the HS is in high dissipation, either power limitation or thermal shut down circuit will latch the device off.

Figure 12: VNH7040AY short across load event (HSA switched on while LSB is already ON)

2.4.3.2 Short-circuit is applied so that LSB is switched on while the HSA is already on

In this second case, the device latches due to LS protection triggering (I_{SD_LS} reached).

Figure 13: VNH7040AY short across the load event (LSB switched on while HSA is ON)



2.4.3.3 Short circuit occurs when HSA and LSB are both on

In this third case, the overshoot of the HSA current limiter lets the LSB reach its shutdown current protection I_{SD_LSD} and cuts off of the short-circuit current by latching the device off.

2.5 Cross conduction suppression

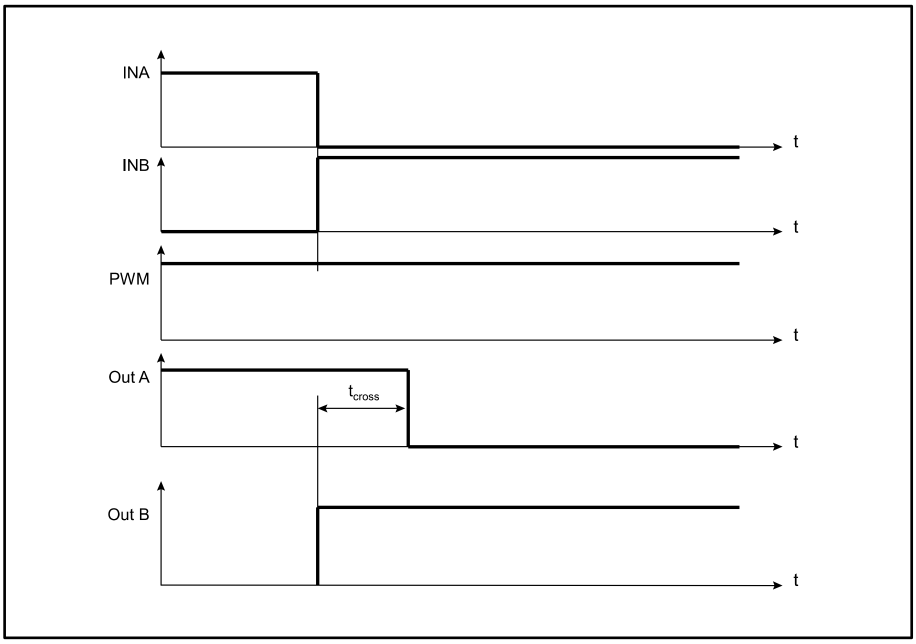
In normal operation, an H-bridge drives a motor in two directions: clockwise (HSB on, LSA on) and counter clockwise (HSA on, LSB on). It cannot switch both PowerMOS of the same leg on at the same time as this causes a short to GND battery event (cross conduction event).

To avoid this behavior, the VNH7XXX ICs implement specific logic:

- when INA is toggled high, the complemented signal immediately turns off the LSA MOSFET before the charge pump circuitry has had time to switch on the HS MOSFET; likewise for INB and LSB.This protection takes advantage of the switching time difference between the Low Side MOSFET and the High Side MOSFET; due to the charge pump circuitry, the HS switch has slower turn-on/turn-off times compared to the LS MOSFET.
- when INA is toggled low, HSA switch off is slower than LSA switch on, so a delay (t_{cross} of about 150 µs) is added to ensure LSA switch on after HSA switch off; likewise for INB, HSB and LSB.Therefore, t_{cross} is longer than the HS switch off time ($t_{d(off)}$).

The figure below shows a change of direction from HSA and LSB in on state to HSB and LSA in on state, and indicates the t_{CROSS} delay before the LSA is turned on (delay time for turning on of HSB is not shown)

Figure 14: cross current delay



The M0-7 H-bridge drivers are designed to avoid shoot-through during operation in PWM, even in adverse ambient conditions.

In the figure below, the High Side is in the DC condition (HSA is on, HSB is off), while the Low Side is toggling as per the PWM signal.

Figure 15: Vbatt=13.5V, TJ=25°C, Duty Cycle 50%, DC MOTOR (CH1=VPWM, CH2=Vcc, CH3=I(Vcc), CH4=Imotor)

The current peaks on V_{CC} are due to the intrinsic HS diode recovery time.

The VNH7XXX devices are immune to shoot-through, a typical dynamic issue in bridge topology. As soon as any LS is switched on by a PWM signal, a negative dv/dt is applied to the High Side of the same leg output.

Potentially, this dv/dt is coupled through the High Side C_{GS} capacitance to its gate (C_{GD} and C_{GS}). Depending on the HS gate-source pull down impedance, current may flow from battery to ground, resulting in extra power dissipation (the impact of which can be significant at high frequencies) and hazardous conditions for the device. This problem is avoided by design in the VNH7XXX bridge.

3 External protections

3.1 Reverse polarity protection

A common problem in the automotive environment is damage when car battery terminals are connected incorrectly.

H-bridge ICs in VIPower technology include two parasitic p-n diodes from GND to the supply voltage pin V_{CC} (2 x V_f ~ 1.5 V). An inverse supply voltage would allow high current to flow through these diodes and damage the device.

Electronic safeguards involving passive or active reverse polarity protection need to ensure that any reverse current flow and reverse bias voltage is low enough to prevent damage to internal electronics.

Reverse polarity protection strategies can be:

- active or passive
- on battery line (V_{CC} terminal) or on GND line (GND terminal)

Four possible reverse battery protection solutions are summarized in the following table.

Table 2: Reverse battery protection designs

Reverse battery protection design	Protection type	Connection
Schottky Diode	Passive	Vcc
P-channel MOSFET	Active	Vcc
Reverse FET	Active	Vcc
N-channel MOSFET	Active	GND

3.1.1 Diode in series with battery line

3.1.1.1 Protection behavior

Normal operation (positive battery voltage)

All load current flows through the diode, which must be chosen so as not to allow the junction temperature to exceed the maximum. Here it is the formula to apply:

Equation 1

$$\mathrm{DT_j} = \mathrm{T_{j(D)max}} - \mathrm{T_{amb,max}} < \mathrm{P} \cdot \mathrm{R_{thj-amb}}$$

Where:

- $T_{amb,max}$ is the maximum module temperature
- $R_{thj-amb}$ is the thermal resistance (junction to ambient) for the device and mounting use

Power dissipation is given by:

Equation 2

$$P = V_{TO} * I_{F(AV)} + rd \cdot I^2_{F(RMS)}$$

Where:

- $I_{F(AV)}$ = maximum average forward current
- $I_{F(RMS)}$ = RMS forward current
- rd (small signal diode resistance) and V_{TO} depend on the special characteristics of the diode and can be extracted from the diode datasheet.

Behavior during reverse battery polarity

The diode is off once polarity is inverted; no current can flow in this state other than the rated leakage reverse current.

The diode breakdown voltage V_z must be higher than the reverse battery voltage value (typ.: 16 V). An important aspect is the peak reverse voltage limit of the Schottky diode. If we consider the maximum repetitive reverse voltage of the diode:

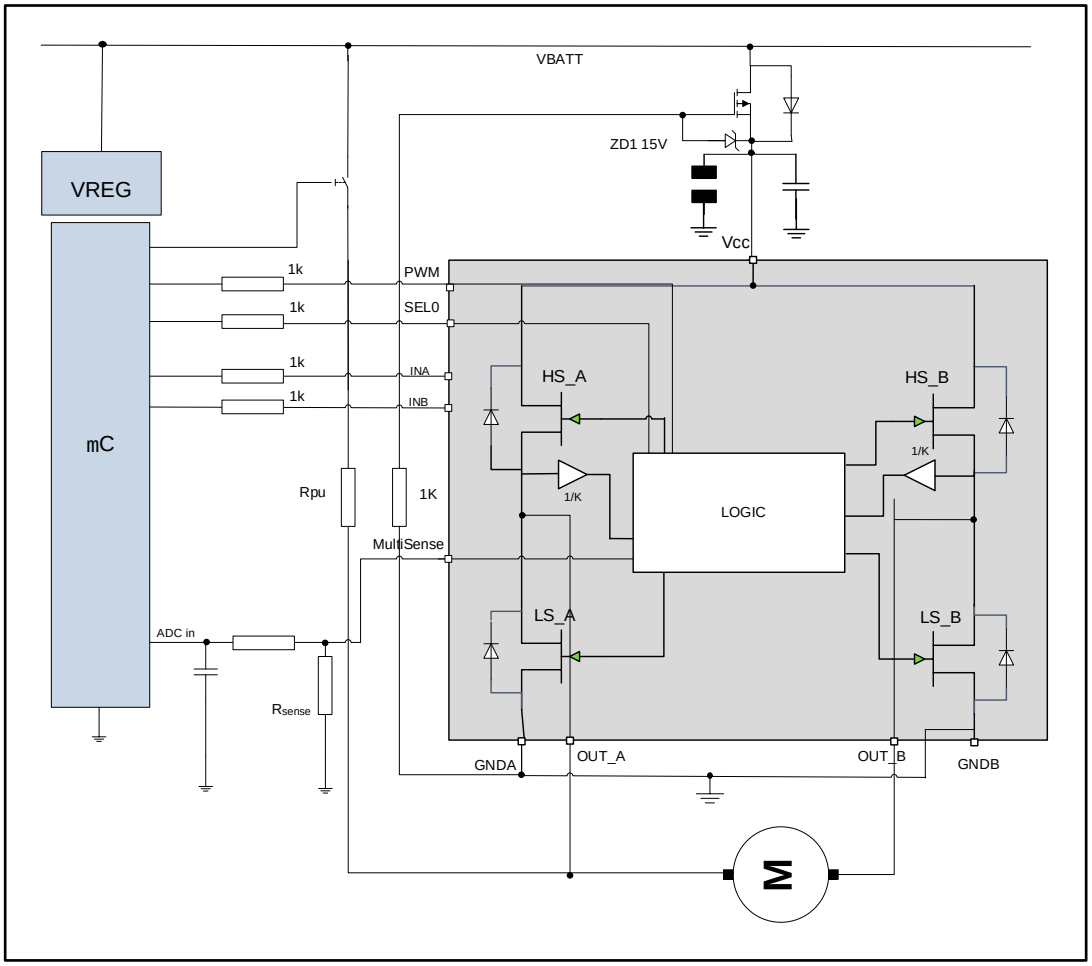
- V_{RRM} > 100V for “ISO 7637-2:2004(E)” pulse 1 Test level IV
- V_{RRM} > 150V for “ISO 7637-2:2011(E)” pulse 1 Test level IV.

During the negative ISO7637-2 transients, the motor is supplied by the electrolytic filtering capacitor on V_{CC}.

The advantage of a Schottky diode over a standard diode is a very low voltage drop in the forward direction, hence power dissipation is reduced. This solution can be used for low current motors.

3.1.2 P-channel MOSFET in the Vcc line

Figure 16: Reverse battery protection with P-channel MOSFET



3.1.2.1 Protection behavior

Normal operation (positive battery voltage)

After the power-up phase when the P channel MOSFET body diode is forward-biased, a negative gate-source voltage switches on the P channel MOSFET.

Behavior during reverse battery polarity

The P channel MOSFET is switched off since its gate-source voltage is positive (voltage drop over the Zener diode); no current can flow in this state.

3.1.2.2 External component selection

Zener diode ZD1 is dimensioned on the basis of:

- Vz above the nominal battery voltage to avoid high module standby current;
- Vz must be below the P- Ch PowerMOS gate-source voltage absolute maximum rating;
- Power rating enough to handle the current in case of load dump event.

The resistor between gate and GND limits the current through the Zener diode at supply voltages higher than the Zener voltage and limits the charging or discharging current of the gate.

This resistor, together with the gate capacitance of the P-channel MOSFET, also determines the turn-off time when exposed to fast negative transients or abrupt reverse polarity according to LV 124: 2013-06 standard.

1 kΩ appears to be a good compromise between minimizing the charging/discharging current and ensuring a fast turn-off time.

As the P-channel MOSFET also carries the load current, it needs to be properly dimensioned to handle the whole load current.

A capacitor could be placed between Gate and Source of the P-channel MOSFET.

The RC filter composed of the 1 kΩ resistor and the capacitor can be dimensioned to be transparent against the fast negative pulses ISO 7637-2:2004(E) pulse 1 test level IV, keeping the reverse polarity protection circuitry switched ON.

Main PowerMOS parameters ($R_{ds(on)}$, $V_{(BR)DSS}$, V_{gs_th}):

The maximum P-channel V_{gs_th} is given at the minimum battery voltage.

The P channel $R_{ds(on)}$ must be such that power dissipation is kept low enough to keep the junction temperature below the rated maximum (150 °C).

Equation 3

$$DTj = Tj_{Pch\_max} - T_{amb\_max} = R_{ds(0N)max} * I^2_{motor\_RMS\_max}$$

Where:

- $T_{amb,max}$ is the maximum module temperature
- $I_{motoravg\_max}$ is average motor current calculated at the maximum battery voltage.

The P channel MOSFET breakdown voltage ($V_{(BR)DSS}$) must be higher than the reverse battery voltage value (typ. 16 V).

If no low pass filter is placed on the P channel gate, any negative ISO transient opens the P channel MOSFET. The motor is then supplied by the electrolytic filtering capacitor on V_{CC}.

A standard logic MOSFET is normally recommended for noise immunity issue.

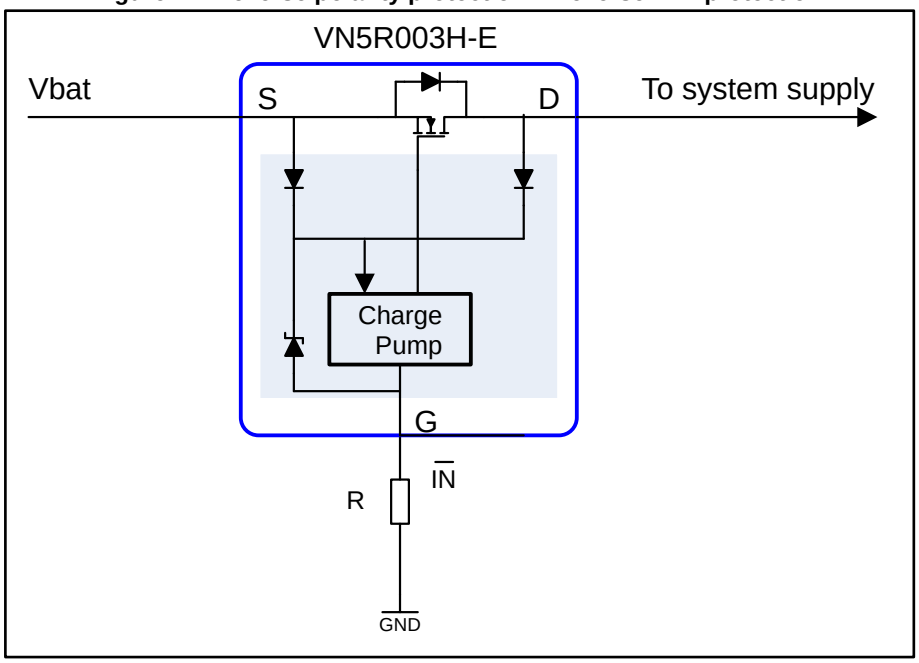
The Zener diode clamps the Gate of the MOSFET to its Zener voltage and protects it against overvoltage.

The same reverse battery protection can be shared among several bridges connected to the battery.

3.1.3 Dedicated ST Reverse FET solution

The VN5R003H-E device uses VIPower™ technology by ST to provide reverse battery protection for an electronic module. It consists of an N-channel MOSFET and driver circuit, two power pins (Drain and Source) and a control pin (IN_NOT).

Figure 17: Reverse polarity protection – Reverse FET protection

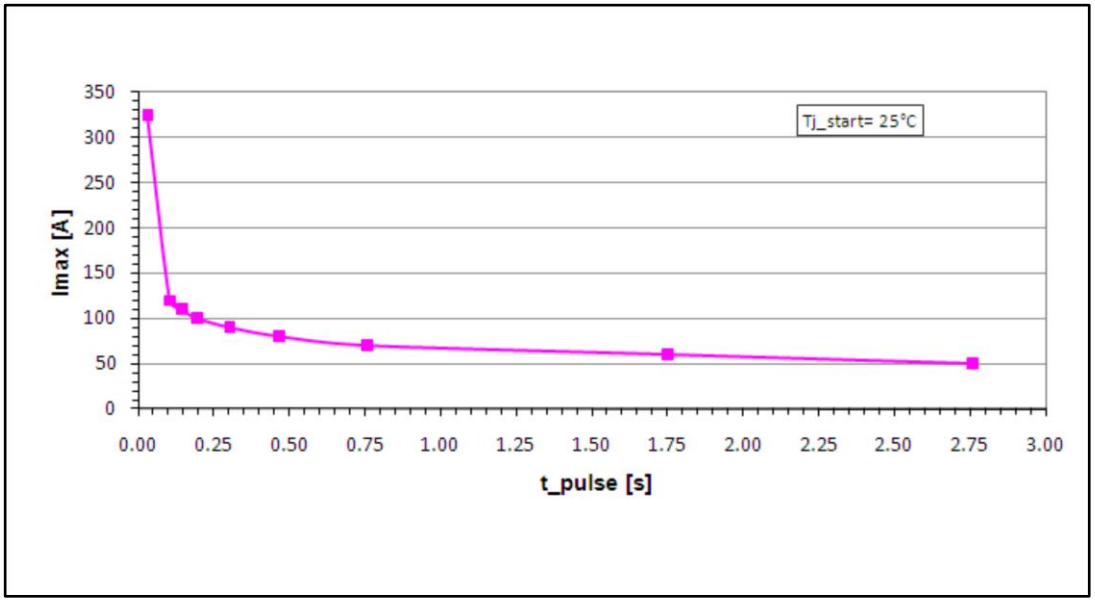


Once the IN_NOT voltage is pulled low, the device is turned ON. The internal charge pump allows the PowerMOS gate to rise above the battery voltage to make it function in ohmic region. When IN_NOT is left open, device is in the OFF state and behaves like a power diode between the source and drain pins.

During a reverse battery polarity event, the charge pump stops operation, causing the PowerMOS to switch off. In normal operation, the VN5R005 dissipates power given by the battery current multiplied by its $R_{ds(on)}$.

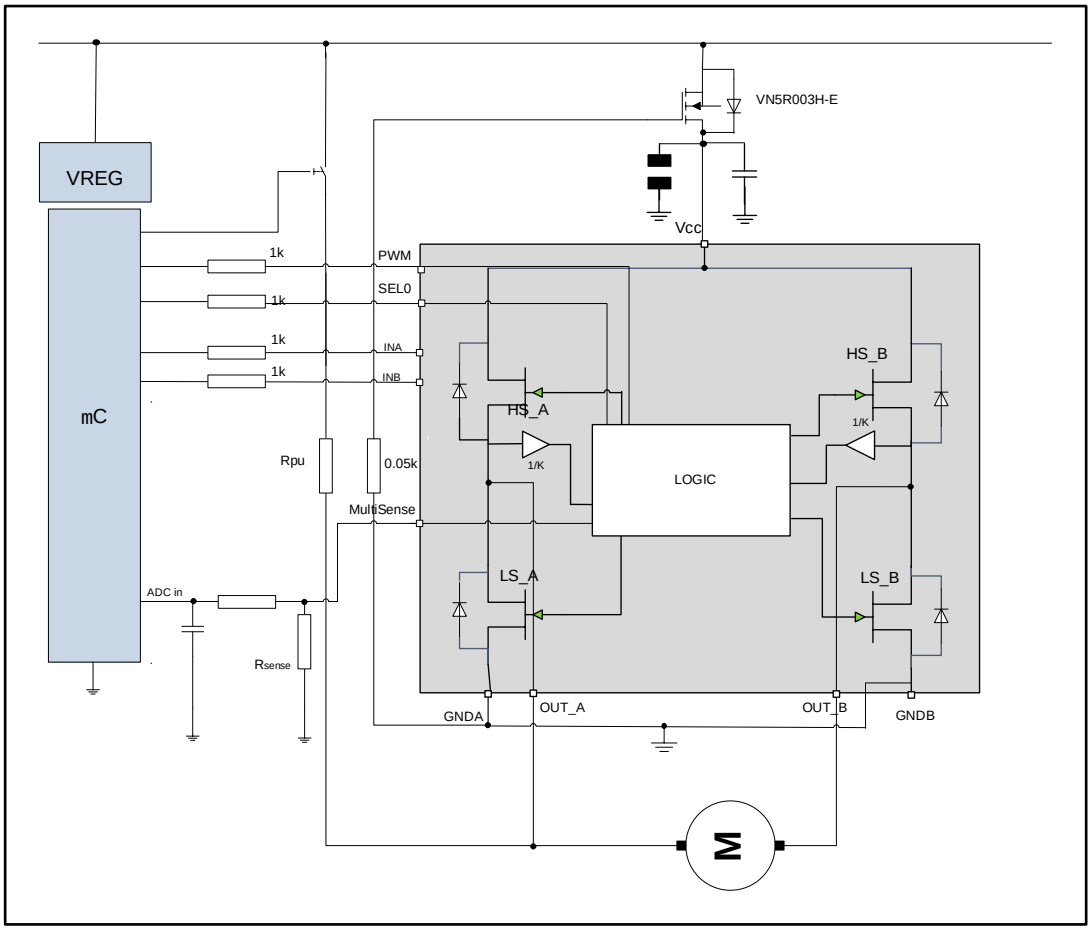
The figure below shows the safe operating area and the maximum pulsed drain current the device is able to manage during normal operation (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 mm, Copper areas: minimum pad lay-out and 2 cm²)

Figure 18: Maximum current versus duration time of VN5R003H-E



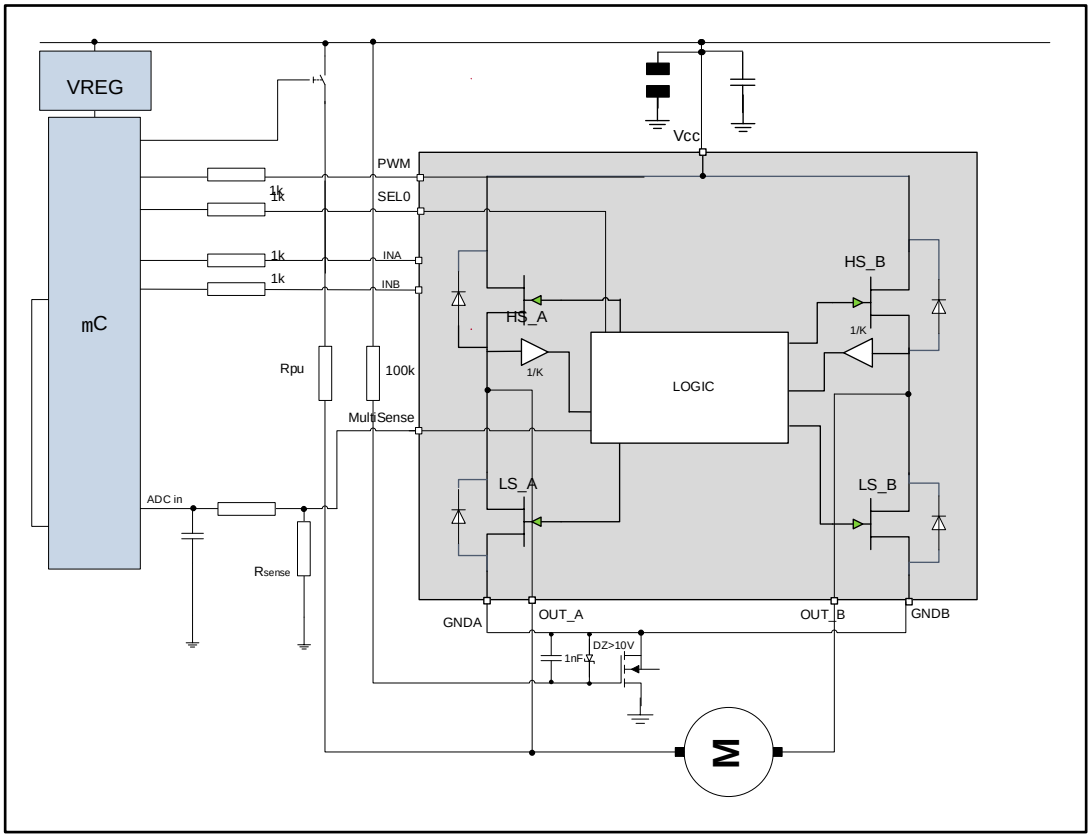
The VN5R003H-E is able to handle ISO 7637-2 2004 pulses with R (IN_NOT) > 5 Ω. Its performance was evaluated using the circuit schematic below.

Figure 19: Application schematic with VN5R003H-E



3.1.4 N-channel MOSFET connected to module ground

Figure 20: Reverse battery protection with N-channel MOSFET



3.1.4.1 Protection behavior

Normal operation (positive battery voltage)

After the power-up phase ,when the N channel MOSFET body diode provides the GND to the motor control IC, the zener diode DZ plus the resistor generate enough gate-source voltage to switch on the N-MOSFET.

Reverse battery polarity condition

The N-Channel is switched off since its gate voltage is low; no current can flow in this state.

The series resistor R_g between V_{CC} and N channel MOSFET gate limits the current through the Zener diode at supply voltages higher than the Zener voltage and limits the charging/discharging current of the gate.

This resistor, together with the gate capacitance of the N channel Power MOSFET, determines the turn-off time when the module is exposed to fast negative transients or abrupt reverse polarity according to the LV 124: 2009-10 standards.

A good tentative value for R_g could be a few tens of kilohms, considering that a long turn-off time could cause high power dissipation for both the LS and this N-channel Power MOSFET used as reverse battery.

A capacitor, C_g, might be placed between Gate and Source of the N channel Power MOSFET. The RC filter formed by R_g and C_g can be dimensioned to be transparent against the fast negative pulses ISO 7637-2:2011(E) 3a, keeping the reverse polarity protection circuitry switched on.

The time constant (R_gxC_g) must be longer than the pulse 3a length (0.1 µs) but smaller than the pulse 1 length (2 ms).

3.1.4.2 External component selection

The zener diode must be dimensioned based on the following considerations:

- V_Z above the nominal battery voltage to avoid high module standby current;
- V_Z must be below the N-Ch PowerMOS gate-source voltage absolute maximum rating;
- Power rating enough to handle the current in case of load dump event.

Main PowerMOS parameters ($R_{ds(on)}$, $V_{(BR)DSS}$, V_{th}):

The N-Ch $R_{ds(on)}$ must be such that power dissipation is kept low enough to ensure that the junction temperature remains below the rated maximum (150 °C).

Equation 4

$$DTj = Tj_{Nch\_max} - T_{amb\_max} = R_{ds(0N)max} * I^2_{motor\_RMS\_max}$$

Where:

- $T_{amb,max}$ is the maximum module temperature
- $I_{motor\_RMS\_max}$ is average motor current calculated at the maximum battery voltage.

The N-channel PowerMOS breakdown voltage ($V_{(BR)DSS}$) should be higher than the maximum negative transient peak voltage of ISO 7637:2-2011(E) or its energy capability in avalanche must be high enough to handle the transient pulse energy.

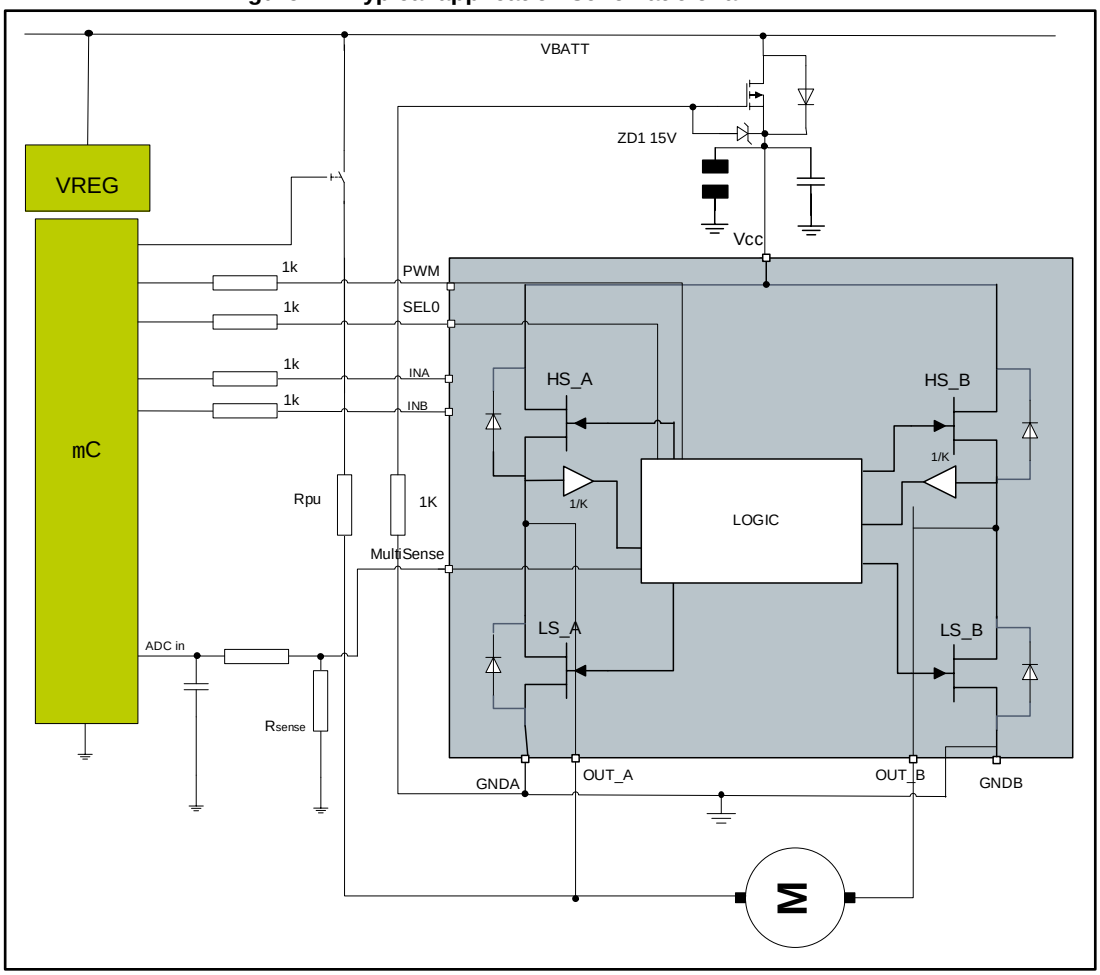
The N-channel PowerMOS must be large enough to handle ISO7637/2 pulse 1 level IV energy.

A standard logic MOSFET is normally recommended for noise immunity issue.

3.2 DC motor control application considerations

The typical application schematic of a M0-7 H-bridge is given below.

Figure 21: Typical application schematic of a VNH7XXX



3.2.1 H-bridge device application considerations

Mechanically commutated motors with brushes (DC motors) are driven by half bridge or by full-bridge (H-bridge) power switch configurations.

High-current and high frequency applications like motor control need to address the effect of parasitic inductors. Inappropriate handling of these inductors can lead to EMC issues (conducted and radiated high RF noise emission), erratic behavior and IC device failure.

Any interconnection inside the device (wire bonding) of the car wiring and in the module (vias, PCB traces) introduces stray inductances. Switching of inductive current causes overvoltages across its terminals as per the formula:

Equation 5

$$V_L = -L \cdot dI_L/dt$$

Where:

- V_L is the voltage across the inductor
- L the inductor itself
- I_L is the current flowing through

Any high current variation leads to an overvoltage.

Moreover, according to the formula:

Equation 6

$$E_L = 0.5L \cdot I^2$$

Any inductor stores some energy that, when inductor current is stopped, is discharged or transferred to the structures connected to the inductor terminals. This energy must be managed to avoid unexpected failure of the structures connected to the inductor.

3.2.2 Design verification checks

3.2.2.1 C1(Vcc) capacitive filter on the supply line

This electrolytic capacitor keeps the voltage ripple at the V_{CC} pin of the IC below a predefined value during operation in PWM at high frequency. This ripple should be kept below 3 V peak to peak.

The capacitive value of an electrolytic capacitor depends on the V_{CC} DC voltage and the module ambient temperature.

Capacitor selection must involve consideration of the ESR value, which can degrade the filtering capability of the capacitor if too high. This capacitor must be placed as close as possible to the device V_{CC} and GND pins to minimize trace inductance.

3.2.2.2 C2(Vcc) capacitive filter on the IC supply line

This ceramic capacitor must absorb all fast transients between the V_{CC} pin and GND pin. The value can be determined from CISPR25 conducted emission measurements on the battery line.

This capacitor must be placed as close as possible to the IC supply pin (V_{CC}) and ground terminals with minimal PCB trace length to minimize the trace inductance.

3.2.2.3 Ripple on Vcc caused by motor inductance

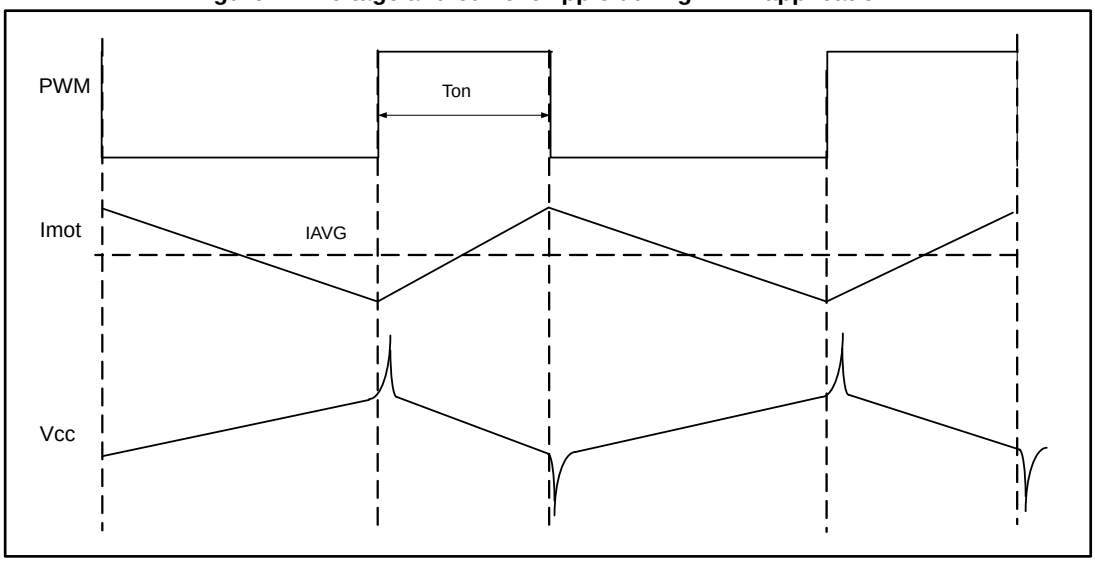
In the steady state with the motor driven by PWM, the motor current is the sum of:

1. an average value (I_{MAVG}) - provided by the car battery
2. a ripple current ($I_{Mripple}$ peak-to-peak) - provided by the bulk capacitor(s) placed across the motor control IC

The battery provides energy to the motor when either HSA /LSB or HSB /LSA are on (T_{on}, on phase of the whole PWM period).

Below are the typical waveforms:

Figure 22: Voltage and current ripple during PWM application



In the following considerations, it is assumed that the motor average current is provided by the battery, whilst the ripple current is provided by the bulk capacitor.

In the worst case assumption that the system formed by the H-bridge IC and the bulk capacitor is decoupled from the battery by the wire stray inductance, the energy provided by the supply bulk capacitors during T_{on} is identical to the power provided to the DC motor.

The characteristic equation of a DC motor is:

Equation 7

$$V_{batt} = R_{motor} \cdot I_{motor} + L_{motor} \cdot \frac{dI_{motor}}{dt} + BEMF = V_{motor,avg} + V_{motor,ripple}$$

Where:

Equation 8

$$V_{motor,avg} = R_{motor} \cdot I_{avg} + BEMF$$

If we neglect the drop on the motor resistance R_{motor} in the above equation, we derive the following formula:

Equation 9

$$Vmotor,ripple \cong Lmotor * \frac{dImotor}{dt}$$

Therefore the current ripple during t_{ON} can be simplified according to the following equation:

Equation 10

$$I_{motor,ripple} = \frac{\left(V_{batt} - V_{motor,avg}\right)}{L_{motor}} \cdot T_{on}$$

Where:

Equation 11

$$V_{motor,avg} = \frac{T_{on}}{T} . V_{batt}$$

If we consider a linear increase of the motor current, the charge required by the bulk capacitor to supply the motor is:

Equation 12

$$DQ = 0.5 \cdot T_{on} \cdot I_{motor,ripple}$$

At this point, the $C_{(Vcc)}$ must be:

Equation 13

$$C1_{(Vcc)} > \frac{DQ}{DV_{CC}}$$

This equation helps to define the right $C1_{(Vcc)}$ capacitor for the chosen ripple allowed on V_{CC}.

By applying the previous four formulas, we finally derive:

Equation 14

$$C1_{(Vcc)} > \frac{0.5 \cdot T_{on}^2 \cdot V_{batt} \cdot \left(1 - \frac{T_{on}}{T}\right)}{L_{motor} \cdot DV_{CC}}$$

The maximum pulse length (t_{on}) is determined by the PWM frequency and duty cycle (in *Equation 14*, the maximum $C1(V_{CC})$ is obtained at 67% duty cycle. The capacitor value in case of loads which require 20 kHz PWM is relatively low in comparison to the value needed to face other possible applicative conditions described below.

3.2.2.4 Ripple on Vcc caused by stray wiring inductance during sudden current variation

During motor operation in PWM, the battery current is continuously stopped and restarted.

The ripple on V_{CC} depends on:

- the stray inductance between the IC V_{CC} and the battery itself
- the maximum speed at which the LS is switched on and off
- the maximum motor load current in the worst case environmental conditions.

The voltage variation across the stray inductance is:

Equation 15

$$DV_{CC} = -L_{stray} \left(\frac{dI_{motor}}{dt}\right)$$

Where L_{stray} is the stray inductance between V_{batt} and device V_{CC} and dt is either the t_{fall} or the t_{rise} of the LS working in PWM.

The filtering capacitor on V_{CC} must be dimensioned by taking in account the balance of energy between the one stored in the L_{stray} and the one stored in the $C_{(VCC)}$.

If we consider that the stray inductance energy is transferred instantaneously to the bulk capacitor (thus neglecting the LS switching times), the following equation applies:

Equation 16

$$0.5 \cdot L_{stray} \cdot I_{motor}^2 = 0.5 \cdot C1_{(Vcc)} \cdot DV_{CC}^2$$

Assuming:

Equation 17

$$\mathrm{DV_{CC,max}} = \mathrm{V_{CC\_AMR}} - \mathrm{V_{batt\_max}}$$

Where V_{CC_AMR} is given in the datasheet Absolute Maximum Rating table.

This yields:

Equation 18

$$C1_{(VCC)} > \frac{L_{stray} \cdot I_{motor}^2}{DV_{CC,max}^2}$$

3.2.2.5 Ripple on Vcc in current switch off due to short to battery and short to ground

All VIPower H-bridges have the Low Side shut-down current (I_{LS_SD} in datasheets), so in short-circuits to battery, the LS switches off as soon as the LS current reaches the current cut-off value.

Depending on the stray inductance of the short-circuit, the energy stored in it must be dissipated in the structures connected to the stray inductor terminals.

Because of the H-bridge structure, a positive pulse on the LS drain is transferred to the IC supply pin (V_{CC}).

The capacitive filtering on V_{CC} helps to absorb this inductive energy.

Even here, we must balance the energy thus:

Equation 19

$$0.5 \cdot L_{stray\_sc} \cdot {I_{SD\_LS,max}}^2 = 0.5 \cdot C1_{(VCC)} \cdot DV_{CC,max}^2$$

Where:

- L_{stray_sc} is the short-circuit stray inductance
- $I_{SD\_LS,max}$ is the Low Side shut-down current

- $DV_{CC,max} = V_{CC,max} – V_{CC,initial}$ with $V_{CC,max}$ representing the Absolute Maximum Rating of the device.

By imposing that $DV_{CC,max} = V_{CC\_AMR} – V_{batt\_max}$ (where the V_{CC_AMR} is given in the datasheet Absolute Maximum rating table), this yields:

Equation 20

$$C1_{(VCC)} > \frac{L_{stray\_sc} \cdot I^2_{SD\_LS,max}}{DV^2_{CC,max}}$$

The same considerations can be applied in case of short-circuits to ground. In the H-bridge IC, the High Side has both current limitation and thermal shut down features. The worst case energy discharge event is the one that occurs at the maximum current limitation value ($I_{lim,h}$). The formula is:

Equation 21

$$0.5 \cdot L_{stray} \cdot I^2_{limh} = 0.5 \cdot C1_{(Vcc)} \cdot DV^2_{CC,max}$$

By imposing that $DV_{cc,max} = V_{cc\_AMR} – V_{batt\_max}$ (V_{cc_AMR} from the datasheet Absolute Maximum rating table), we derive:

Equation 22

$$C1_{(Vcc)} > \frac{L_{stray} \cdot I^2_{limh}}{DV^2_{CC,max}}$$

3.2.2.6 Ripple on Vcc due to sudden battery disconnection with motor fully energized

In this condition, the motor energy must be absorbed by the bulk capacitors to avoid reaching the H-bridge IC breakdown voltage and consequent failure due to excessive energy levels. The applicable formula is:

Equation 23

$$E_{motor} = 0.5 \cdot C1_{(Vcc)} \cdot DV^2_{CC,max}$$

By imposing that $DV_{cc,max} = V_{cc\_AMR} – V_{batt\_max}$ (V_{cc_AMR} from the datasheet Absolute Maximum Rating table), we derive:

Equation 24

$$C1_{(Vcc)} > \frac{E_{motor}}{0.5 \cdot DV^2_{CC,max}}$$

3.2.2.7 Vcc drop with risk of undervoltage event at motor current in-rush

Device V_{CC} is normally inductively decoupled from the car battery positive due to:

1. battery cable with stray inductance powering the IC
2. inductance of the Pi filter if present

The motor start current is much higher than nominal current to overcome mechanical inertia (in-rush current) and generate movement.

$C1_{(Vcc)}$ must be large enough to provide at least part of the energy required by the motor in order to avoid unwanted undervoltage events.

Equation 25

$$dI_{motor,inrush} = C1_{(Vcc)} \cdot \frac{DV_{CC}}{dt}$$

Given $DV_{CC} = V_{batt,min} - V_{USD\_max}$, then:

Equation 26

$$C1_{(Vcc)} > \frac{dI_{motor,inrush} \cdot dt}{V_{batt,min} - V_{USD\_max}}$$

All of the above formulas set the conditions that $C1_{(Vcc)}$ must fulfil to guarantee proper device operation.

3.2.2.8 Vcc variation because of fast ISO7637/2 ISO transients (pulses 3a, 3b)

Some reverse battery protection topologies allow transfer of voltage transients directly to device V_{CC}.

The fast transients according to ISO7637/2 are:

1. 3a, level IV, max. negative voltage = -220 V, pulse length= 0.1 µs, series resistance= 50 Ω; this pulse causes sudden V_{CC} voltage drop of roughly 100 ns
2. 3b, level IV, max. positive voltage = +150 V, pulse length= 0.1 µs, series resistance = 50 Ω; This pulse causes a sudden overvoltage that could trigger the H-bridge IC Power clamp in case of no filtering capacitor on the V_{CC} line.

A filtering capacitor $C2_{(Vcc)}$ of a few tens of nF is enough to smooth the effect of the above pulses and avoid triggering any protections as well as device malfunction.

3.2.3 Overview of capacitor C1(Vcc) assessment

Table 3: Overview of capacitor C1(Vcc) assessment

Applicative condition	Formula to apply to get $C1_{(Vcc)}$	Applied criteria
Section 3.2.2.3: "Ripple on Vcc caused by motor inductance"	*Equation 14*	DV_{CC} = maximum allowed peak to peak voltage (e.g., 3 V)
Section 3.2.2.4: "Ripple on Vcc caused by stray wiring inductance during sudden current variation"	*Equation 18*	L_{stray} is the stray inductance from battery to device (included any eventual inductance of Pi-filter); $DV_{cc,max} = V_{cc\_AMR} - V_{batt\_max}$(1)
Section 3.2.2.5: "Ripple on Vcc in current switch off due to short to battery and short to ground"	*Equation 20*	L_{stray_sc} is the stray inductance of the short-circuit path; $I_{SD\_LS,max}$ is the maximum low side cutoff current (given in the datasheet); $DV_{cc,max} = V_{cc\_AMR} - V_{batt\_max}$(1)
	Equation 22	L_{stray} is the stray inductance from battery to device (included any eventual inductance of Pi-filter); I_{LIM_H} is the maximum high side current limitation (given in the datasheet); $DV_{cc,max} = V_{cc\_AMR} - V_{batt\_max}$(1)
Section 3.2.2.6: "Ripple on Vcc due to sudden battery disconnection when the motor fully energized"	*Equation 24*	E_{motor} is the total energy of the motor (kinetic and inductive). $DV_{cc,max} = V_{cc\_AMR} - V_{batt\_max}$(1)
Section 3.2.2.7: "Vcc drop with risk of undervoltage event at motor current in-rush"	*Equation 26*	Dt_{motor_inrush} is the rise time of the motor in-rush current; V_{USD_max} is the maximum undervoltage shutdown threshold (given in the datasheet)

Notes:

(1)V_{cc_AMR} is given in the datasheet Absolute Maximum Rating table

To prevent dangerous overvoltages or undervotages on the battery connection for the H-Bridge, all the above conditions should be fulfilled.

Example: Dual washer pump motor driven by VNH7040AY

During ON state, PWM 20 kHz is applied.

The following VNH7040AY parameters are applied:

- V_{CC_AMR} = 38 V
- I_{LIM_HSD} = 70A Maximum
- I_{SD_LS} = 84 A Maximum
- V_{USD} = 4 V Maximum
- T_{ON}/T=0.67; T_{ON} = 33.5 µs

The following DC motor parameters are applied:

- L_{motor} = 100 µH
- I_{motor} = 10 A Maximum
- $DI_{motor,inrush}$ = 26 A Maximum
- $Dt_{motor,inrush}$ = 1 µs
- E_{motor} = 33.5 mJ (Energy of the motor before battery disconnection)

The following application parameters are applied:

- $V_{batt,min}$ = 7 V
- $V_{batt,max}$ = 26 V (for example jump start)
- DV_{CC} = 3 V (max peak to peak voltage)
- L_{stray} = 5 µH
- L_{stray_sc} = 3 µH

The limitation of V_{CC} ripple during PWM caused by motor inductance (*Equation 14*) yields:

$$C1(Vcc) > \frac{0.5 * Ton^2 * Vbatt,max * \left(1 - \frac{Ton}{T}\right)}{Lmotor * DVcc} = 16.05\mu F$$

Limitation of V_{CC} ripple caused by wiring stray inductance due to sudden current variation (*Equation 18*) yields:

$$C1(Vcc) > \frac{Lstray * Imotor^2}{DVcc,max^2} = 3.47\mu F$$

Limitation of V_{CC} peak at LS switch off in the event of short of OUT to battery (*Equation 20*), yields:

$$C1(Vcc) > \frac{Lstray\_sc * I^2_{SD\_LS,max}}{DVcc,max^2} = 147\mu F$$

Limitation of V_{CC} peak at HS switch off in the event of short of OUT to ground (*Equation 22*), yields:

$$C1(Vcc) > \frac{Lstray * I^2_{SLIM\_HSD,max}}{DVcc,max^2} = 170\mu F$$

Limitation of Vcc peak during sudden battery disconnection with energized motor (*Equation 24*), yields:

$$C1(Vcc) > \frac{Emotor}{0.5 * DVcc,max^2} = 470\mu F$$

Limitation of V_{CC} drop at motor inrush (*Equation 26*), yields:

$$C1(Vcc) > \frac{dImotor,inrush * dt}{Vbatt,min - V_{USD\_max}} = 8.7\mu F$$

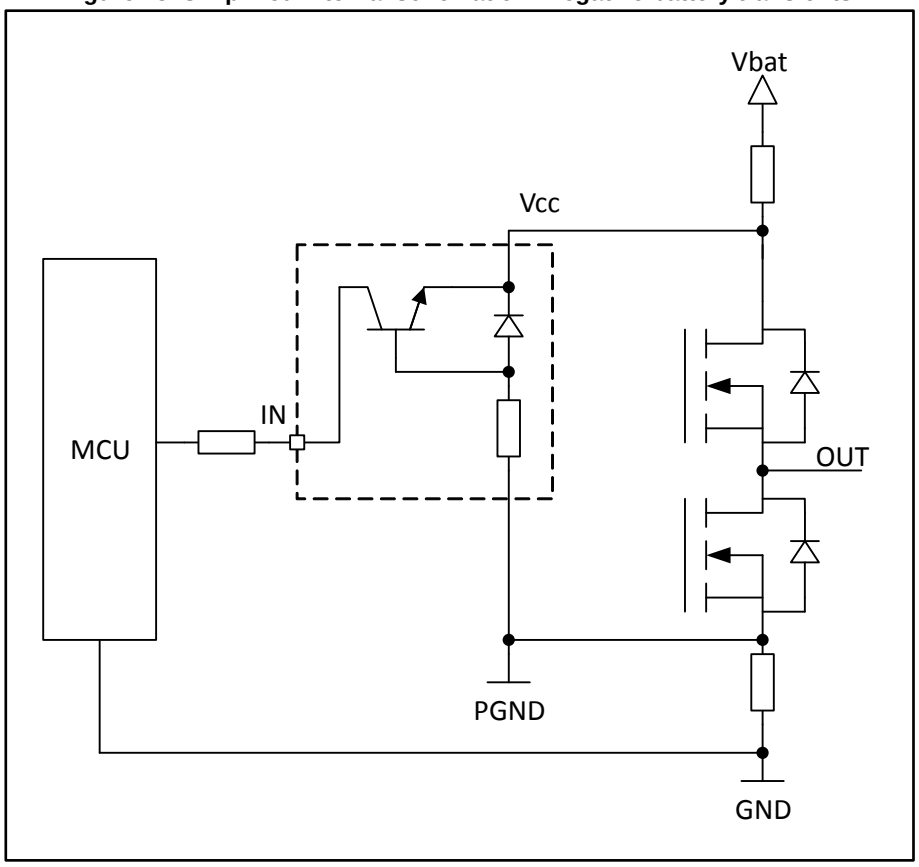
The worst case condition in this example is the battery disconnection with energized motor, since all other applicative events require a smaller C1(V_{CC}). Every applicative condition, DC motor type and VNH7XX choice should take into account the above-mentioned conditions.

3.2.4 Protection resistors (INA, INB, PWM and SEL0)

When negative transients are applied to V_{CC}, the control pins are pulled negative to approximately -2 x Vf ~ -1.5 V where this latter is the voltage drop across the PowerMOS antiparallel intrinsic diodes.

During such an event, the npn parasitic bipolar transistor present in each logic pin enters saturation mode (see the following figure).

Figure 23: simplified internal schematic in negative battery transients



This bipolar saturation current may rise higher than the maximum MCU I/O current and cause MCU failure (latch-up event).

VNH7XXX digital input protection resistors (typ. 1 KΩ) are therefore mandatory.

The value of these resistors is a compromise between the current absorbed by the HS I/Os in high logic state and the latch-up limit of microcontroller I/Os:

Equation 27

$$\frac{1.5V}{\mathrm{I_{latchup}}} \leq R_{prot} \leq \frac{\mathrm{V_{OH\mu C,min}} - \mathrm{V_{IH,min}}}{\mathrm{I_{INHmax}}}$$

Where:

- $I_{latchup}$ is the maximum latch-up current of the microcontroller
- $V_{OH\mu C,min}$ is the minimum high state voltage of the microcontroller output
- $V_{IH,min}$ is the minimum input high level voltage of the VNH7XXX (given in the datasheet)
- $I_{INH,max}$ is the maximum input current of VNH71XXX (given in the datasheet)

In summary, the above protection resistors are recommended in case of VNH7XXX failure with potential high voltage in the digital inputs; negative ISO transients (worst case based on the ISO7637/2, ed. 2011 is -150 V) applied to the Vcc pin.

This event is heavily influenced by the reverse battery protection topology and is only applicable when the reverse battery network is connected to the device ground.

3.2.5 Rejection of conducted and radiated electromagnetic emissions

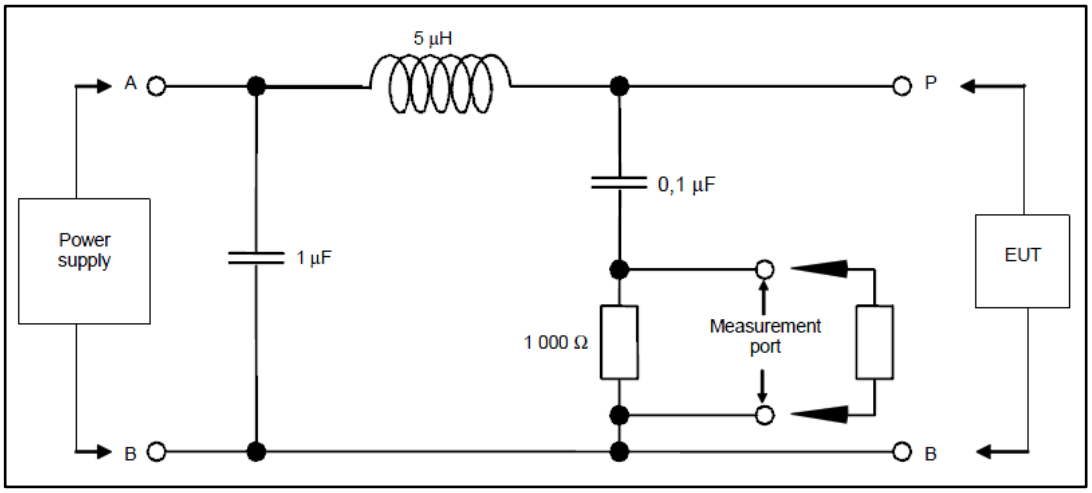
A device or system generates noise which is injected into connection lines or radiated, potentially affecting the performance of other devices or systems connected to the same lines and placed close to it.

To limit the effect of this noise, its amplitude must be lower than EMC limits contained in specific technical reference documentation:

- Standard reference CISPR25 (conducted emissions on V_{batt}, radiated emissions at system level)
- Standard reference IEC 61967/4 (conducted emissions on Outputs using 1 Ω/150 Ω method)
- Standard reference IEC 61967/2 (radiated emissions using TEM-Cell method and wideband TEM-cell method -150 KHz to 8 GHz).

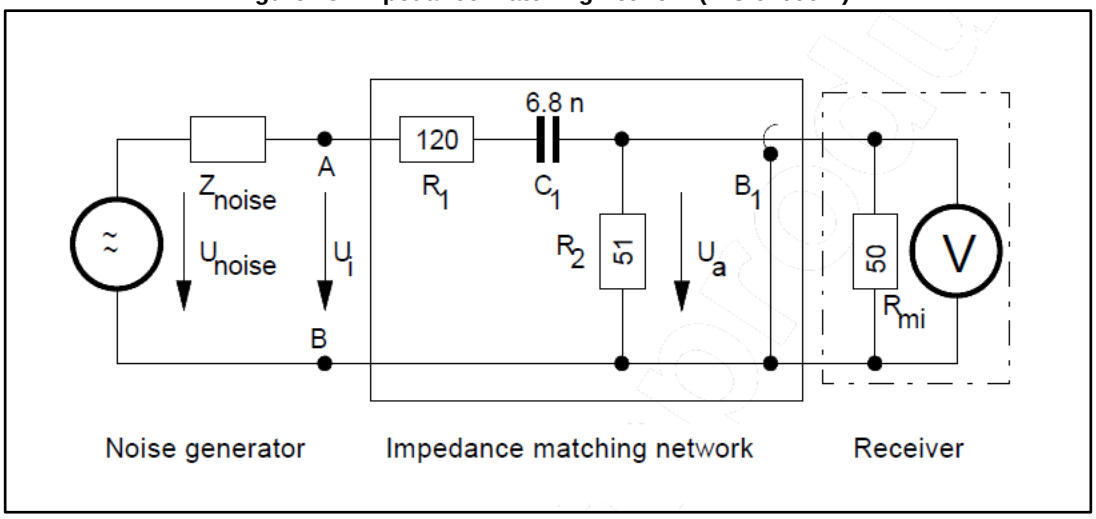
For conducted emissions on Vbatt, a specific artificial network (AN) called line impedance stabilizing network (LISN), is used to couple the measurement instrument (spectrum analyzer) with the V_{batt} line. The figure below shows the LISN schematic for the CISPR25 standard.

Figure 24: LISN setup - CISPR25



For conducted emissions on system outputs (e.g., V_{CC} line or VNH7XX outputs), the 150 Ω measurement method (IEC 61967/4) is commonly used. To perform measurements, the impedance matching network figured below is required.

Figure 25: Impedance matching network (IEC 61000-4)



One or multiple configurations can be chosen for input signals, PWM frequency, duty cycle percentage and output loads. The final configuration is usually the one closer to the common operating condition of the DUT. The type (shielded or unshielded) and length of wire may affect performance of the DUT either with respect to the CISPR25/IEC 61967/4 standard (conducted emissions) or the IEC 61967/2 standard (radiated emissions).

3.2.5.1 Pi-filter dimensioning

Conducted emission measurements may reveal levels of RF noise injected into the battery line above the required limits. The best solution in this case is to add a Pi filter in series with the dedicated battery line.

$C1_{(Vcc)}$ can be considered as part of the normally used Pi filter and its capacitance is calculated with formulas explained in previous chapters.

The resonance frequency of the $L_{(Vcc)}$ and $C_{(Vbatt)}$ filter is:

Equation 28

$$fr = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{(Vcc)} \cdot C_{(Vbatt)}}}$$

The equation for the $L_{(Vcc)}$, C(Vbatt) filter transfer function Vout/Vin:

Equation 29

$$\frac{V_{out}}{V_{in}} = \frac{\frac{1}{j\omega C_{(Vbatt)}}}{j\omega L_{(Vcc)} + \frac{1}{j\omega C_{(Vbatt)}}}$$

Where V_{in} is the device $V_{CC,}$ while V_{out} is the V_{batt} as the filter is intended to cut the noise generated by the H-bridge while operating in PWM. Artificial network (LISN to couple spectrum analyzer with DUT) impedance and internal resistance of V_{batt} are considered negligible.

According to transfer function given above, $L_{(Vcc)}$ $C_{(Vbatt)}$ filter attenuation in dB can be expressed as:

Equation 30

$$Att._{dB} = 20 * log\left|\frac{Vout}{Vin}\right| = 20 * log\left|\frac{\frac{1}{j\omega C(Vbatt)}}{j\omega L(Vcc) + \frac{1}{j\omega C(Vbatt)}}\right|$$
$$= 20 * log\left|\frac{1}{1 - 4 * \pi^2 * f^2 * L(Vcc) * C(Vbatt)}\right|$$
$$\cong 20 * log\left|\frac{1}{4 * \pi^2 * f^2 * L(Vcc) * C(Vbatt)}\right|$$

Where, considering frequencies whose attenuation values, in absolute value, are generally higher or equal to 40dB, we can suppose:

$$1 \ll 4 * \pi^2 * f^2 * L(Vcc) * C(Vbatt)$$

Selection criteria for the input power inductor $L_{(Vcc)}$ include inductance value, rated current, series resistance, power rating (internal temperature rise) and size.

The power dissipated inside the inductor depends on the typical DC resistance R_{DCR} and worst case input RMS current:

Equation 31

$$P_{L_{(Vcc)}} = R_{DCR} \cdot {I_{(vcc)}}^2$$

Taking the criteria into account, $L_{(Vcc)}$ is generally in the range of 1 µH to 30 µH.

According to general conducted EMC rules or specific customer requirements, minimum noise attenuation in dB can be chosen at a given frequency (generally the lower value in the measurement frequency range).

Starting from the selected $L_{(Vcc)}$ value and required noise attenuation level, we can express $C_{(Vbatt)}$ as:

Equation 32

$$C_{(Vbatt)} = \frac{1}{L_{(Vcc)}} \cdot \left(\frac{10^{-\frac{Att._{dB}}{40}}}{2 \cdot \pi \cdot f}\right)^2 = \frac{1}{L_{(Vcc)}} \cdot \left(\frac{10^{\frac{|Att._{dB}|}{40}}}{2 \cdot \pi \cdot f}\right)^2$$

The real attenuation of the PI filter made of the $L_{(Vcc)}$ and $C_{(Vbatt)}$ components just dimensioned is actually lower than the value calculated in *Equation 30*. This mainly due to the equivalent series resistance (ESR) of $C_{(Vbatt)}$, called ESR.

To determine the attenuation of the real filter, given that

$$1 \ll 4 * \pi^2 * f^2 * L(Vcc) * C(Vbatt)$$

we use the formula:

Equation 33

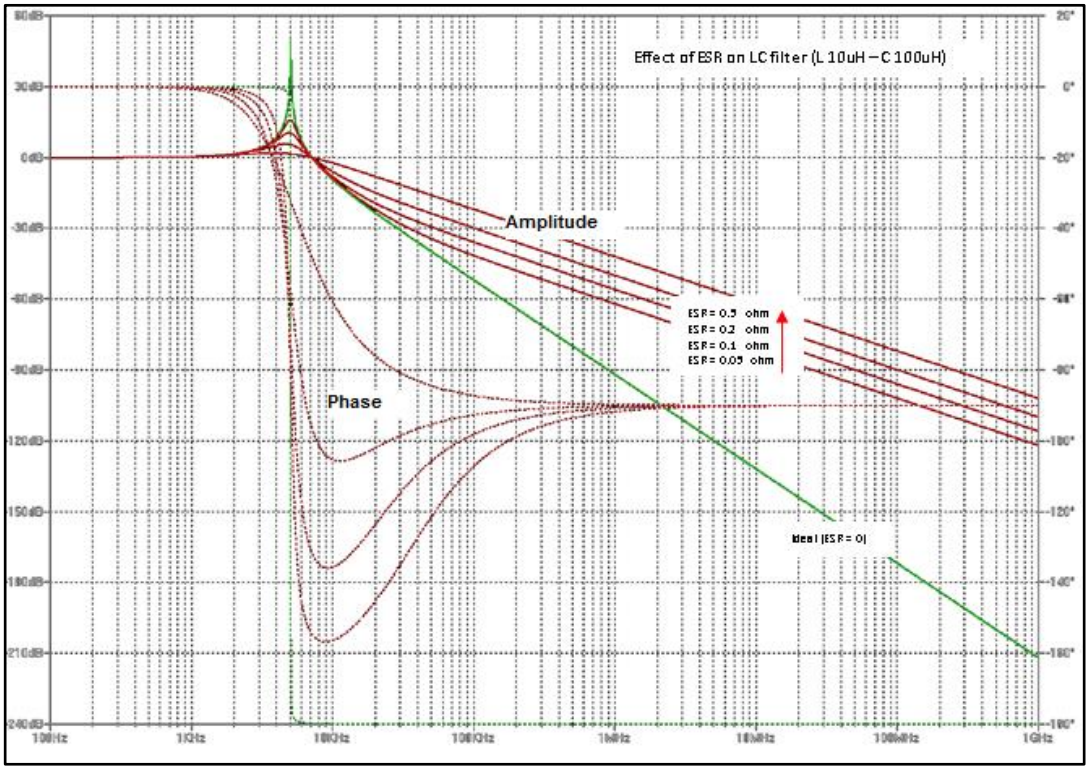
$$Att._{dB} = 20 \cdot log \sqrt{\frac{1}{1 + w^2 \cdot L \cdot C \cdot \frac{w^2 \cdot L \cdot C - 2}{1 + w^2 \cdot ESR^2 \cdot C^2}}}$$

Where:

- ω=2.π.f
- $L=L_{(Vcc)}$
- $C=C_{(Vbatt)}$
- $ESR=ESR_{C(Vbatt)}$

The figure below illustrates the effect of rising ESR and compares the ideal and real cases for a filter where $L_{(Vcc)}$ = 10 µH and $C_{(Vbatt)}$ = 100 µF. The ESR acts as a damping resistor which partially compensates the resonance effect.

Figure 26: Attenuation diagram of Pi-filter with different ESR



Below we can see an example regarding the benefit we can obtain introducing PI filter on the Vbatt line. Without a filter the CISPR25 spectrum (compared to customer limits TL965EN VW) is above class4 limit mask in almost all frequency ranges; by adding a PI filter, dimensioned as written in *Equation 32*, emissions on battery line decrease significantly.

The filter is dimensioned considering that a real attenuation of -50dB minimum at 150 kHz frequency is required, bearing in mind that the theoretical and real attenuation are different because of the ESR.

A simplified schematic and component values are shown in *Figure 27: "Simplified schematic and component values"*.

By setting for example $L_{(Vcc)}$ = 6µH inductance and taking into account *Equation 32* where we considered the theoretical Attenuation of -70dB, we calculated a capacitance value of 593 µF for $C_{(Vbat)}$ capacitor. Using a commercial capacitor with a capacitance of 470 µF, we obtain through *Equation 30* about -68 dB theoretical attenuation instead of -70 dB.

Figure 27: Simplified schematic and component values

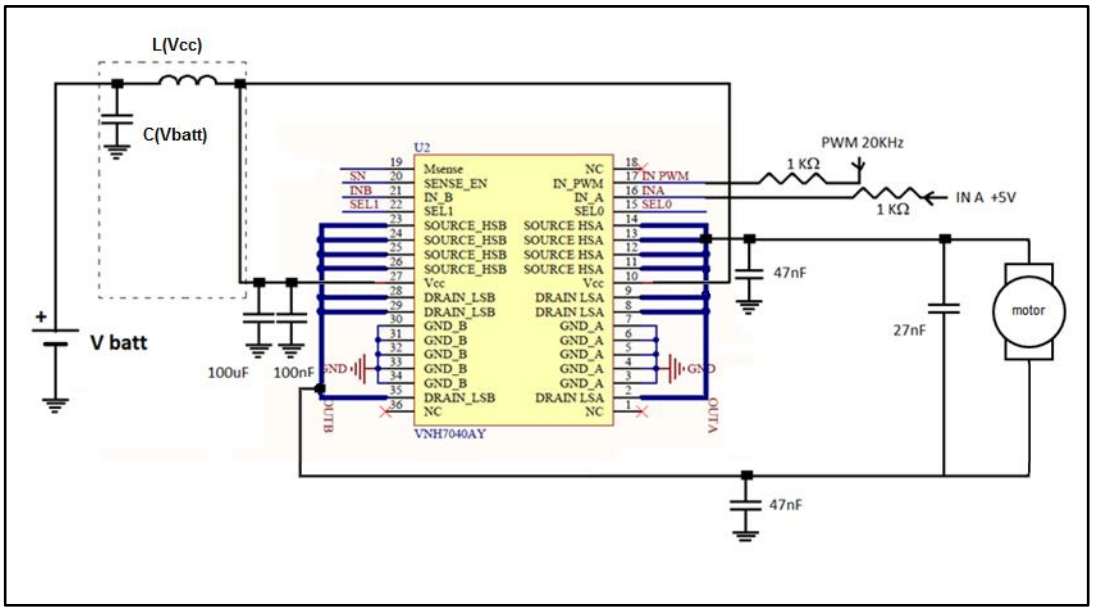
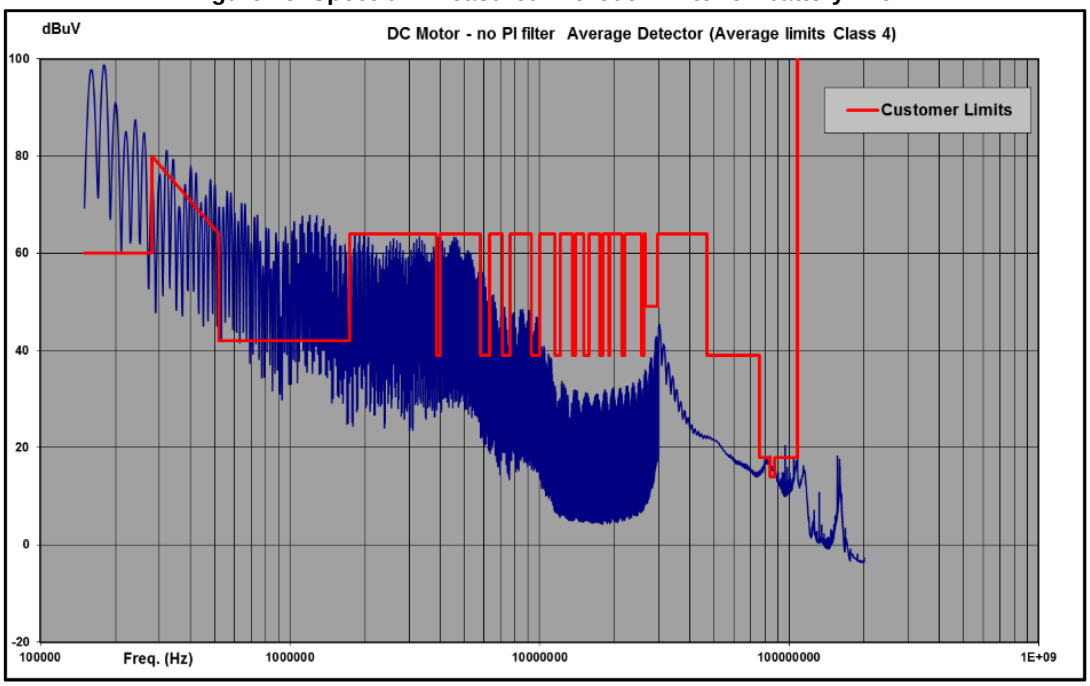


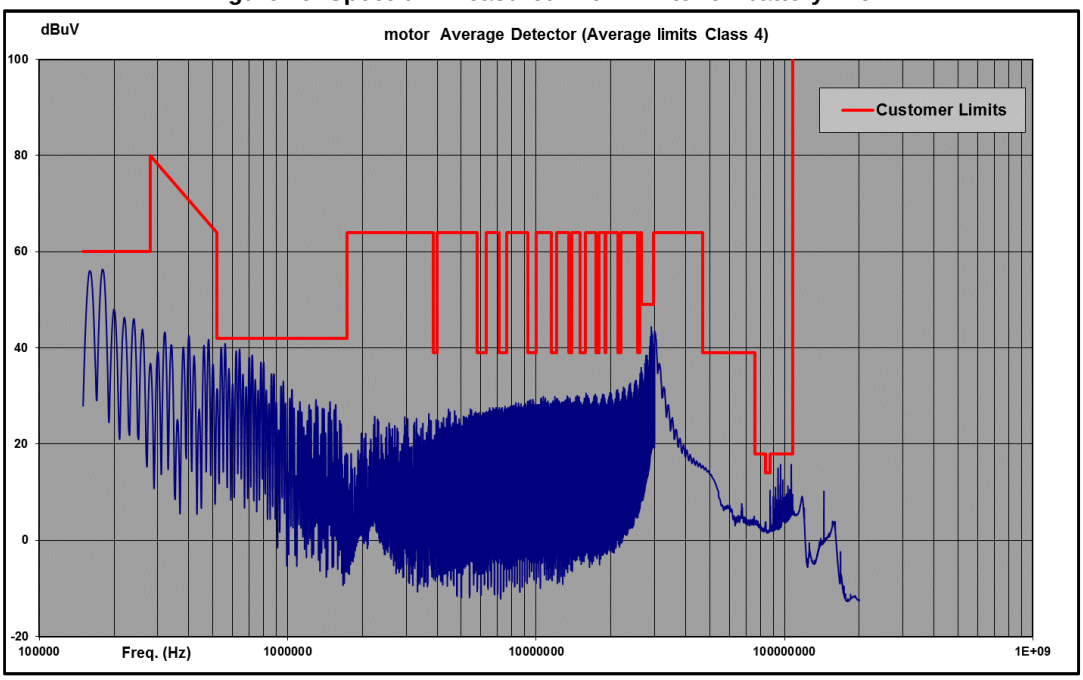
Figure 28: Spectrum measured without PI filter on battery line



The above figure shows the spectrum measured without putting the filter on battery line, while the figure below shows the spectrum with a PI filter on the battery line.

We can see emissions are about 50 dB lower in low frequency range. This allows the spectrum to be below the class4 limit mask.

Figure 29: Spectrum measured with PI filter on battery line



As shown in the two figures, the real attenuation as the absolute value, is 20 dB lower than the theoretical one due to ESR of $C_{(Vbat)}$, about 50 mΩ in this case.

In case the real filter does not fulfill the attenuation specification, we can dimension the filter by assigning a higher theoretical attenuation in *Equation 32*, in order to compensate the ESR value and repeating the verification through *Equation 33*.

3.2.5.2 Capacitors on VNH7XXX Outputs (C(OUT)) and on Vcc (C2(Vcc))

Ceramic capacitors on the VNH7XXX outputs help improve application EMI and ESD performance. Their values depend on the PWM frequency, on the inductive energy in place and on the motor wires.

During motor control in PWM, EM disturbance is injected into the VNH7XXX output pins either due to the antenna effect in car wiring or due to motor brushes. Capacitors on outputs create a path to GND for those disturbances, thus avoiding their return to V_{batt}.

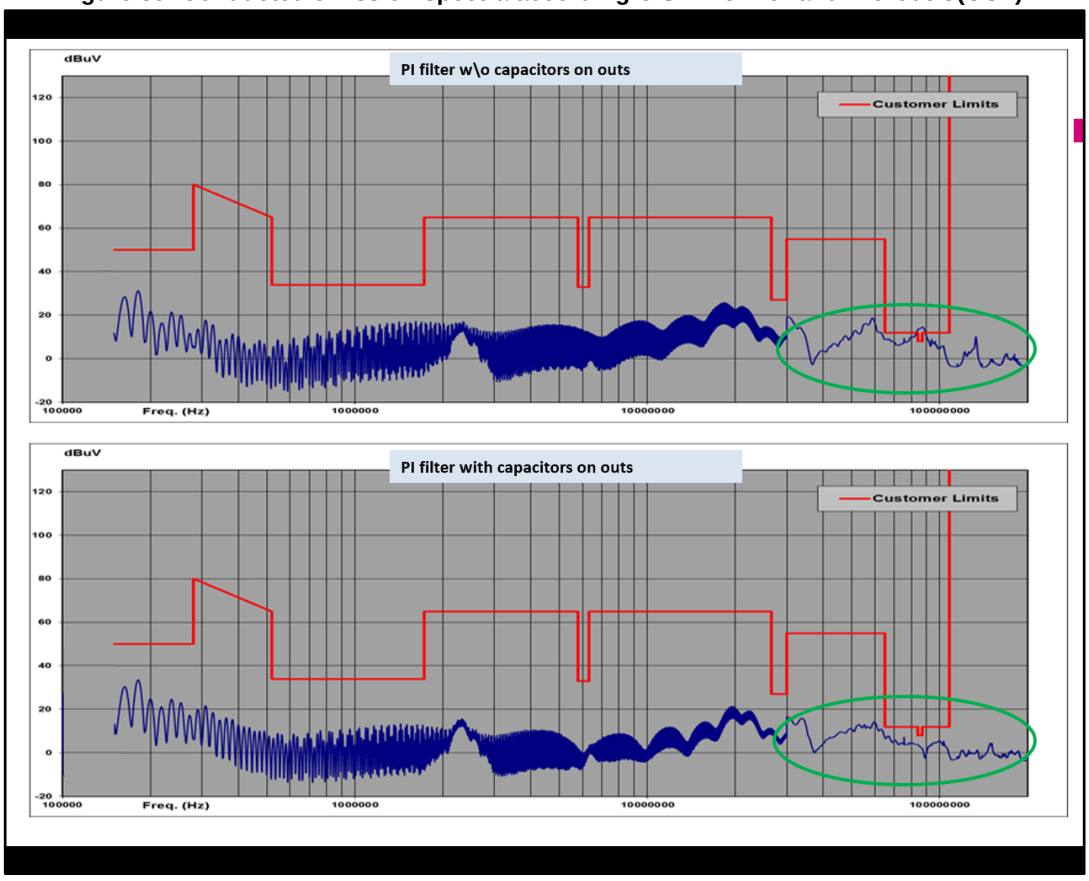
They also smooth falling and rising edges of output waveforms, which benefits emissions at high frequencies (reducing emissions conducted on batt).

Capacitor values between 47 nF and 100 nF are recommended: values below this have little effect and values above don't provide any further benefits and may negatively affect output waveforms and increase switching losses.

$C2_{(Vcc)}$ values between 47 nF and 100 nF are also recommended for similar reasons.

The following VNH7040AY spectra with and without $C_{(OUT)}$ highlights the beneficial effect of the output capacitor at high frequencies.

Figure 30: Conducted emission spectra according CISPR25 with and without C(OUT)



3.2.6 PCB layout considerations

In an H-bridge driver, high current paths and low current paths are all near each other. Alternating current (ac) paths carry spikes and noise, high direct current (dc) produces significant voltage drops and low current paths are sensitive to noise.

We can group the signals thus:

- High frequency and high current (i.e., H-bridge outputs)
- Digital at low frequency (Like INX signals)
- Digital at high frequency (like PWM signals)

A PCB floor plan is important to minimize current loop areas and arrange the power components so that the current flows smoothly, avoiding sharp corners and narrow paths. This helps reduce parasitic capacitance and inductance, therefore, eliminating ground bounce.

The best performance in terms of parasitic inductance and EMC can be reached with a 3- or 4-layer PCB with a dedicated GND plane that improves filtering efficiency.

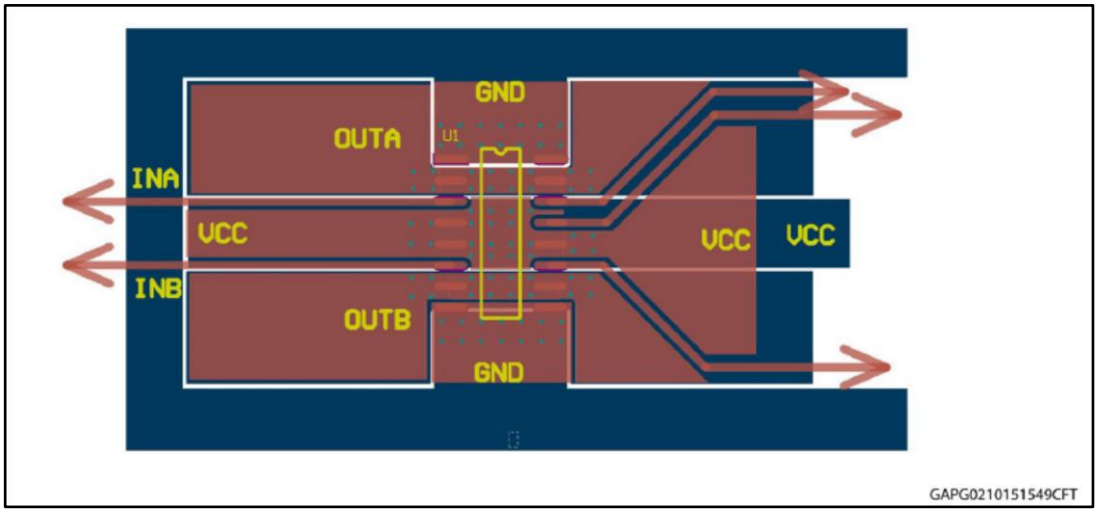
All filtering capacitors (mainly $C1_{(Vcc)}$ and $C2_{(Vcc)}$) must be placed as close as possible to the device terminals to keep the parasitic inductors of the PCB-wires as low as possible.

To keep the RF noise from the DC motor low and reach good immunity from ESD, the $C_{(OUT)}$ and $C_{(Vbatt)}$ capacitors must be placed on the board connector and directly soldered to the module GND usually in star connection with all possible ground signals (Digital GND, Analog GND and Power GND).

The best ESD performance can be achieved by putting an ESD filtering component like a transil or ceramic capacitor as close as possible to the connector pin and well-grounded by via to the ground plane.

A multilayer PCB is better than a 2-layer PCB for heat dissipation. For improved thermal and electrical conduction, a 2-ounce-or-higher copper thickness may be used in place of the standard 1 ounce. Several PGND planes connected together with vias also help.

Figure 31: Optimized connection between Drain LS and Source HS and GND_A and GND_B connection (symmetrical connection)



4 Load and device compatibility

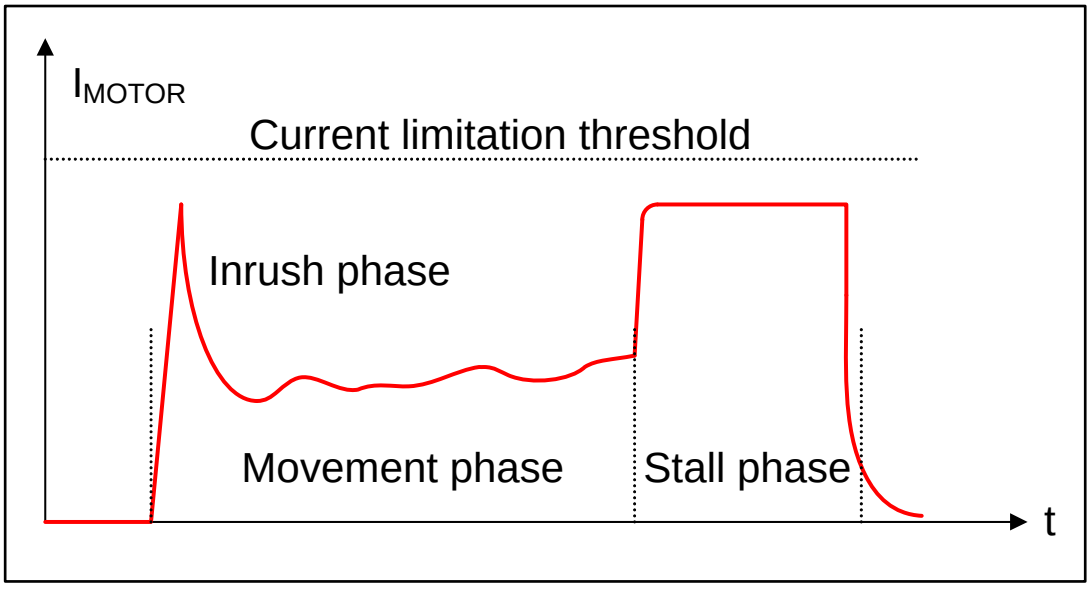
Matching the right motor driver device with the motor influences the operational behavior and lifetime of the device.

Embedded protections like current limitation, current shutdown, power limitation and over temperature shutdown never intervene during normal device operation, only during anomalous, transitory fault conditions.

In general we can recognize three phases of motor current demand.

- **Inrush phase**: the motor drive device can deliver above-nominal current for a short time to provide peak torque to start the motor; the peak torque of the starting motor determines peak current inrush current of the starting motor
- **Movement phase**: a moving motor draws less current; it is generally the desired motor operation phase
- **Stall phase**: the motor loses its movement speed and current becomes maximal. The current is limited by the armature winding resistance only

Figure 32: Generic motor current profile



4.1 Protections summary

4.1.1 PowerMOS High Side protections

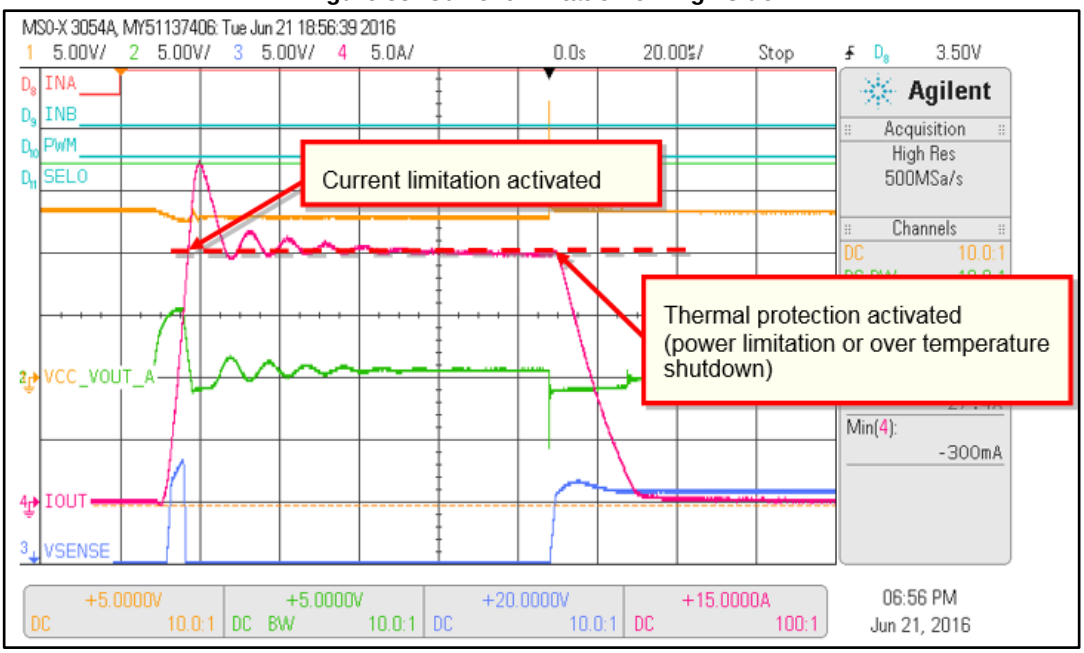
- **Current limitation (ILIMH)** – this protection limits the maximum current flowing over the activated Power MOS
- **Power limitation** – when the monitored difference between junction and case temperature rises above the threshold, Power MOS is shut down.
- **Junction overtemperature** – when the junction temperature (sensor is positioned close to Power MOS) threshold is breached, the Power MOS is shut down.

The following example depicts motor load switching on the VNH7070AS high side:

1. the motor inrush current exceeds the threshold limit
2. the high side Power MOS limits the current supplied to the load
3. the high (limited) current flowing though the Power MOS increases its temperature to above the threshold

4. a further power limitation or overtemperature protection is triggered
5. the Power MOS is deactivated, signaled by the VSENSE_H level on the MultiSense output

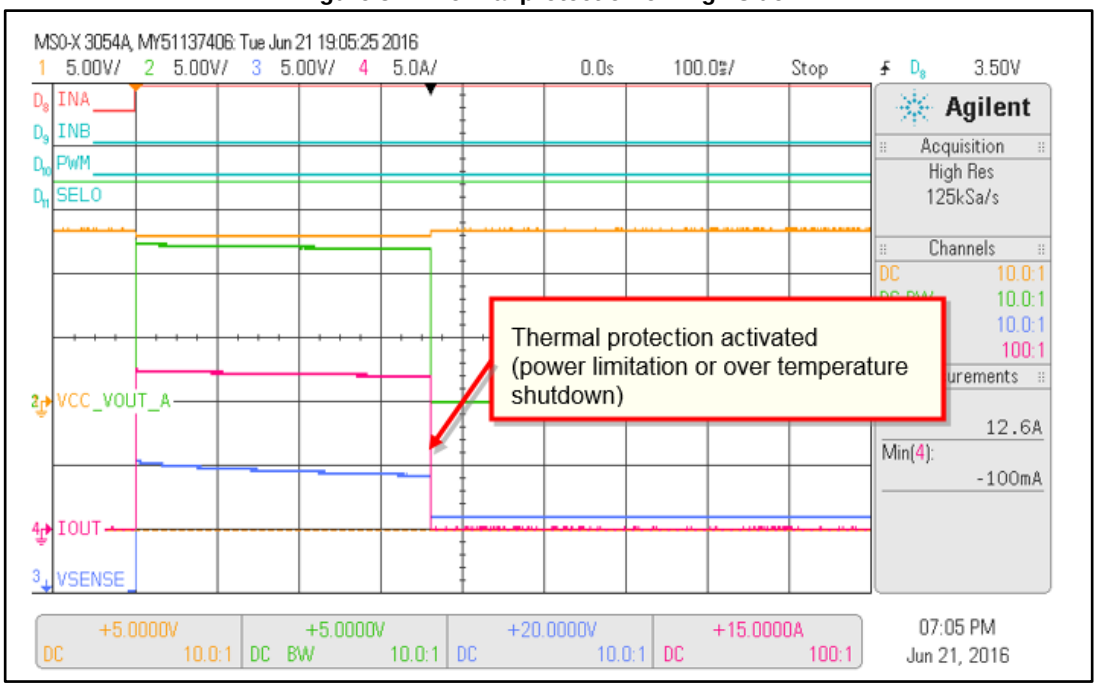
Figure 33: Current limitation on high side



The next example shows:

1. the current threshold on the high side Power MOS is not reached
2. power dissipation on the high side still triggers the thermal protection triggering
3. output is deactivated and fault state is signaled by VSENSE_H

Figure 34: Thermal protection on high side



4.1.2 PowerMOS Low Side protections

- **Junction over temperature** – exceeding absolute threshold on junction temperature sensor (positioned close to Power MOS) causes Low Side Power MOS latch off.
- **Overcurrent detector** – exceeding the shutdown current (I_{LS_SD}) flowing through low side Power MOS causes its latch off.

The following example shows:

1. an overload on the low side that exceeds the maximum current threshold
2. the Power MOS is shut down

Figure 35: Overload on low side

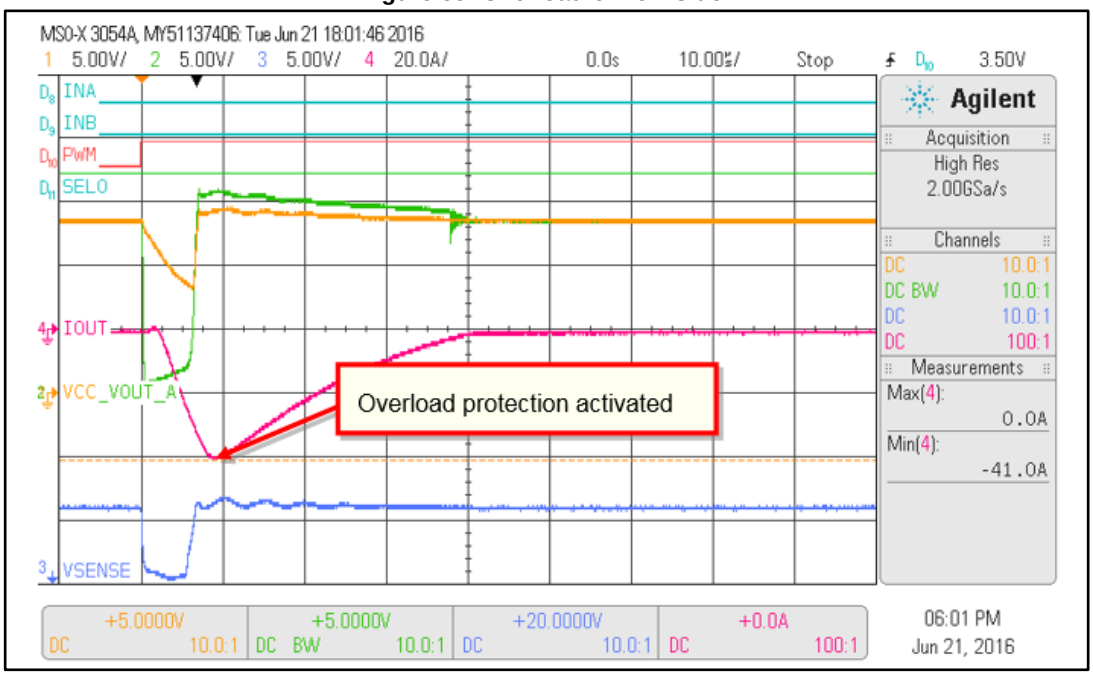
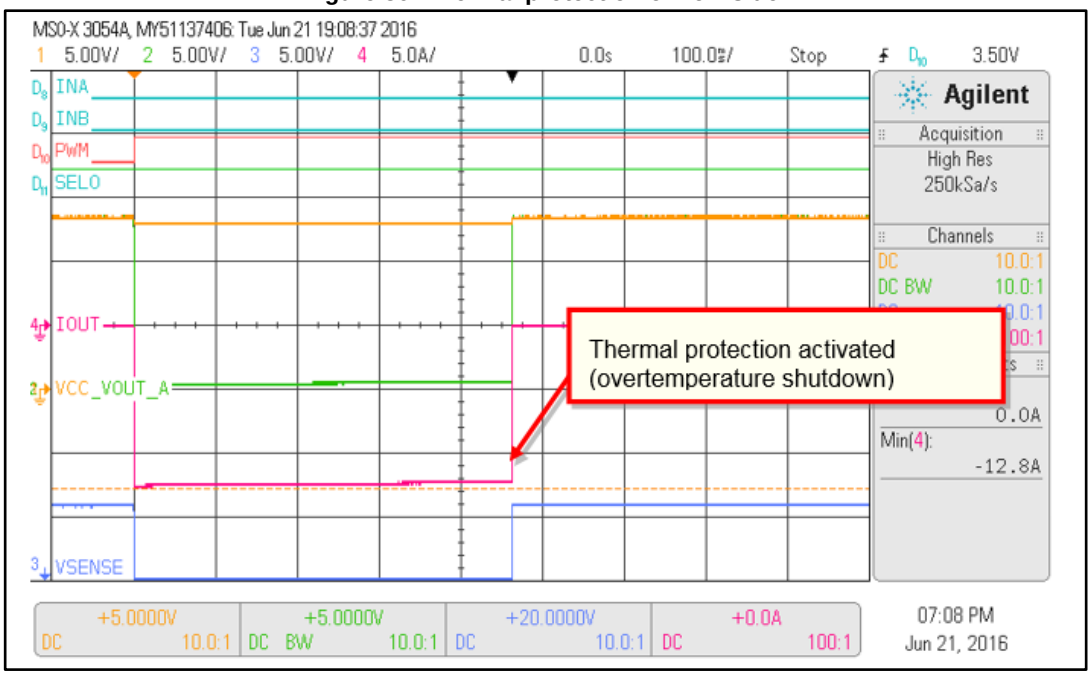


Figure 36: Thermal protection on low side



During the motor inrush and movement phases, none of the protections should be activated. If motor parameters are not compatible with the device and one or more protections are triggered, device control will be interrupted.

4.1.3 Motor phases and protections

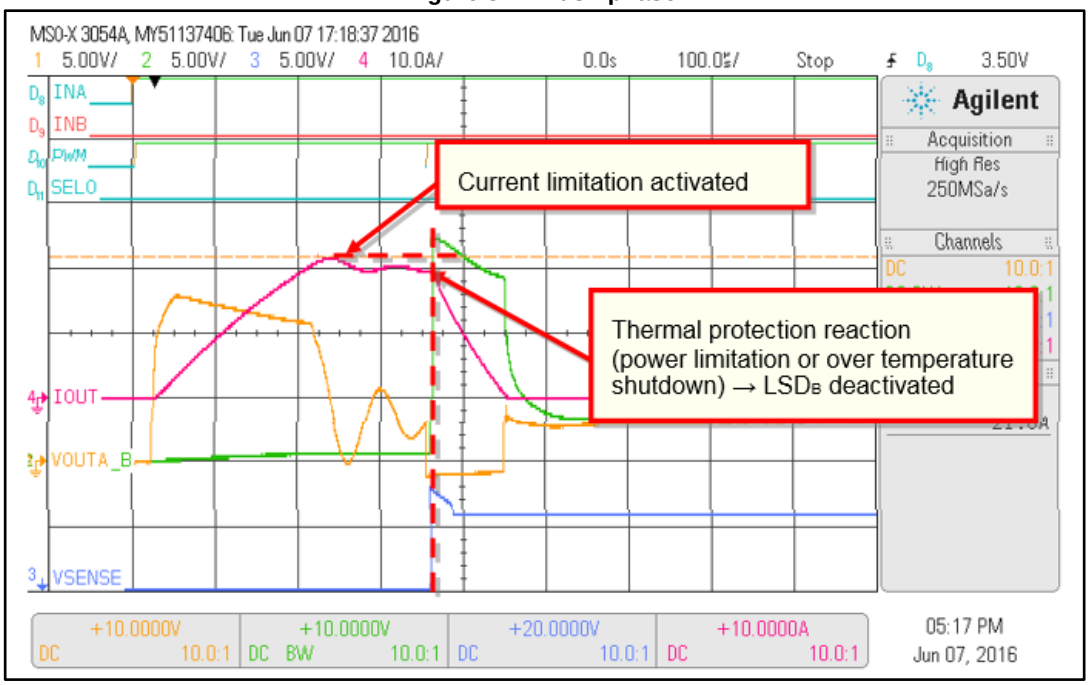
4.1.3.1 Inrush phase

During the inrush phase (where the main parameters are the inrush current and time) the current peak should not activate **any of** the low side overcurrent protections, high side power limitations or high side and low side over temperature triggers.

The figure below shows an example of underestimated motor load driven by a VNH7070BAS:

1. HS_A and LS_B are active
2. the current flowing through the load rises to the current limitation threshold
3. the current is limited to the threshold level
4. before the inrush phase has elapsed, the thermal protection deactivates the LS_B
5. the error is signaled by the MultiSense output by VSENSE_H level

Figure 37: Inrush phase

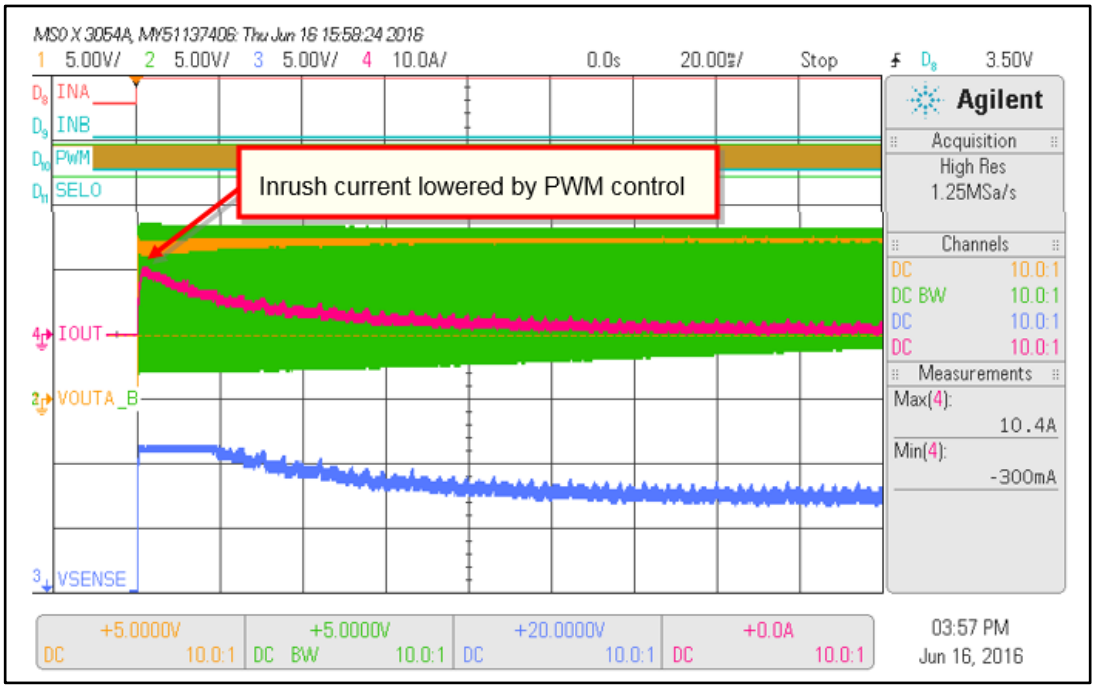


To achieve a smooth motor start during the inrush phase (by limiting inrush current), PWM control can be applied over the H-bridge PWM pin.

The figure below shows motor activation with PWM mode control (duty cycle 50%):

1. the maximum current over the motor load during the inrush phase gets limited
2. the motor activation phase is accordingly prolonged
3. none of the protections are activated and motor is started successfully

Figure 38: Motor activation with PWM



4.1.3.2 Movement phase

When the motor reaches the movement phase, it typically draws less current than the inrush current. The duration of the movement phase is important because energy dissipated in the high and low side Power MOS increases overall temperature, which may trigger temperature protections (power limitation or over temperature shutdown).

If speed reduction or regulation is required, PWM control can also be applied (all protections are active during this type of control).

The approximate dissipated energy in the H-bridge can be estimated thus (assuming motor current is more or less constant):

Equation 34: Power dissipation on activated high side

$$P_{ONHS}[W] = R_{ONHS} * I^2_{RMS\_MOT}$$

Where:

- R_{ONHS} = static resistance on high side
- I_{MOT} = steady current of activated load (motor)

Equation 35: Power dissipation on activated low side (active state only while output driven in PWM mode)

$$P_{ONLS}[W] = R_{ONLS} * I^2_{RMS\_MOT} * DutyCycle$$

Where:

- R_{ONLS} = static resistance on low side
- I_{MOT} = steady current of activated load (motor)
- DutyCycle = PWM active state of low side

Equation 37: Switching losses for inductive load on low side

$$P_{SWITCHINGLS}[\mathrm{W}] = \frac{1}{2}(V_{CC} + \mathrm{V}_F) * I_{RMS\_MOT} * (t_R + t_F) * f$$

Where:

- V_{CC} = power supply voltage
- V_F = high side free-wheeling diode forward voltage, (typically 0.7 V)
- I_{MOT} = steady current of activated load (motor
- t_R = datasheet value rise time
- t_F = datasheet value fall time
- f = low side switching frequency

Equation 38: Power losses in high side (during free-wheeling)

$$P_{SWITCHING\_HS}[\mathrm{W}] = \mathrm{V}_F * I_{RMS\_MOT} * (1 - DutyCycle)$$

Where:

- V_F = high side free-wheeling diode forward voltage typically (0.7 V)
- I_{MOT} = steady current of activated load (motor)
- DutyCycle = PWM active state of low side

4.1.3.3 Stall phase

In the stall phase, the current reaches its maximum level given by the armature winding resistance, leading to increased power dissipation. During this phase, the device is subject to similar stresses as during the inrush phase, so it is desirable to shorten the stall time and thus reduce power dissipation.

It is up to the application to detect stalls (e.g., through MultiSense output diagnostics) and turn the outputs OFF.

In order to properly match device with the motor load, additional aspects have to be considered:

- In the case of load repetitive activations (e.g., door-lock motor control), the number of cycles and the delay between consecutive activations must be taken in account (influencing the device temperature)
- PWM application influences the inrush current and power losses (switching losses) during activation of the device. A permanent application of PWM at 20 kHz, for example, to modulate the speed, significantly increases the Power dissipation in the corresponding Low Side as well as in the High Side (due to recirculation of the inductive current in the body diode during OFF state)
- The PCB layout should be designed to minimize thermal impedance

4.1.4 Other aspects of device and motor load compatibility

For repetitive load activations (e.g., door lock control), the number of cycles and the delay between consecutive activations must be considered (influencing the device temperature).

PWM application influences the inrush current and power losses (switching losses) during activation of the device. A permanent application of PWM at 20 kHz to, for example, modulate the speed, increases power dissipation in the relevant low side as well as the high side (due to recirculation of the inductive current in the body diode during OFF state).

PCB layout should be optimized in order to lower thermal impedance.

5 MultiSense operation

An analog monitoring output called MultiSense is used for M0-7 H-bridge diagnostics. It multiplexes several analogue signals, controlled by the SELx and MultiSense_EN pins.

Depending on the device family, the following signals are provided:

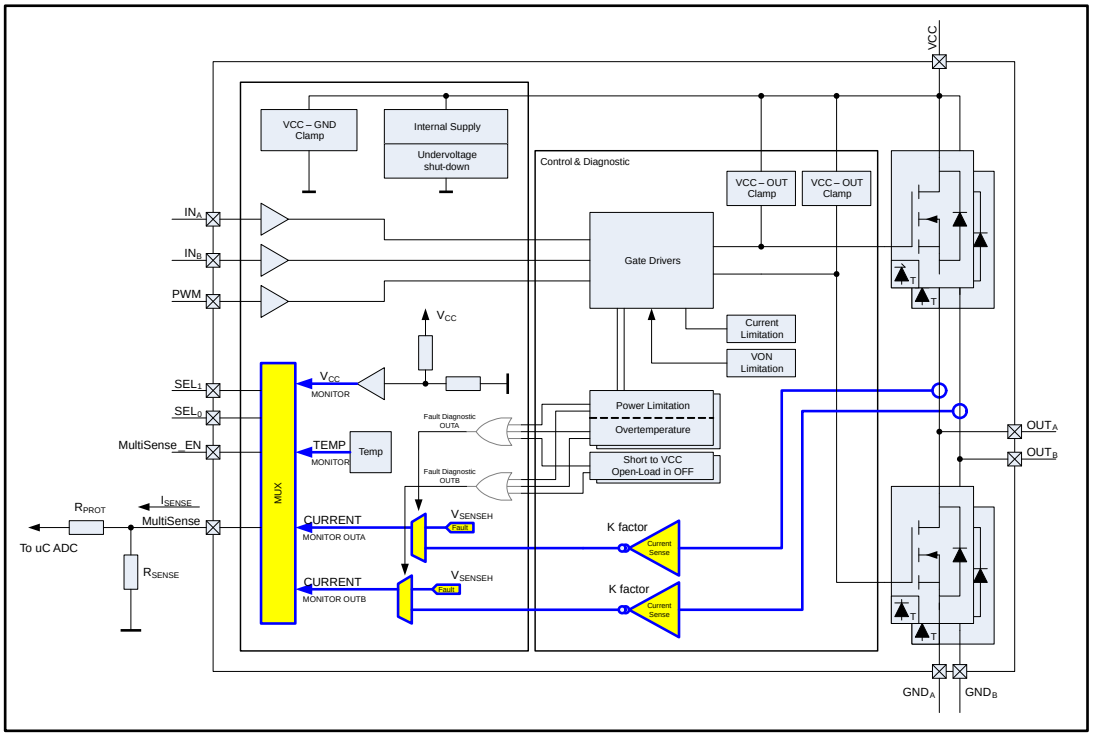
- **Current monitor**: delivers current proportional to the ON state of the high side driver (HSA or HSB) according to the selection pin SEL0 (SEL0=H selects HSA, SEL0=H selects HSB) and SEL1=L for VNH7040AY. A failure on the relevant output in ON or OFF states triggers a voltage flag.
- **Vcc voltage**: scaled monitor of V_{CC}
- **Case temperature**: scaled chip temperature

On top of these signals, the MultiSense enters high impedance when:

1. MultiSense_EN = 0 (for VNH7040AY); this condition is necessary to enter standby mode.
2. During current mode with a current flowing in the load (for VNH7040AY SEL1=L), whenever the OFF state high side driver is selected via the SEL0 pin (SEL0=H and INA=L or SEL0=L and INB=L).
3. When Output A falls below V_{OUT_MSD} typical 5 V (datasheet parameter) while HSA is switched on and HSA protection is not triggered; likewise for Output B and HSB.
4. During the Brake to GND condition, when no low side protection is triggered

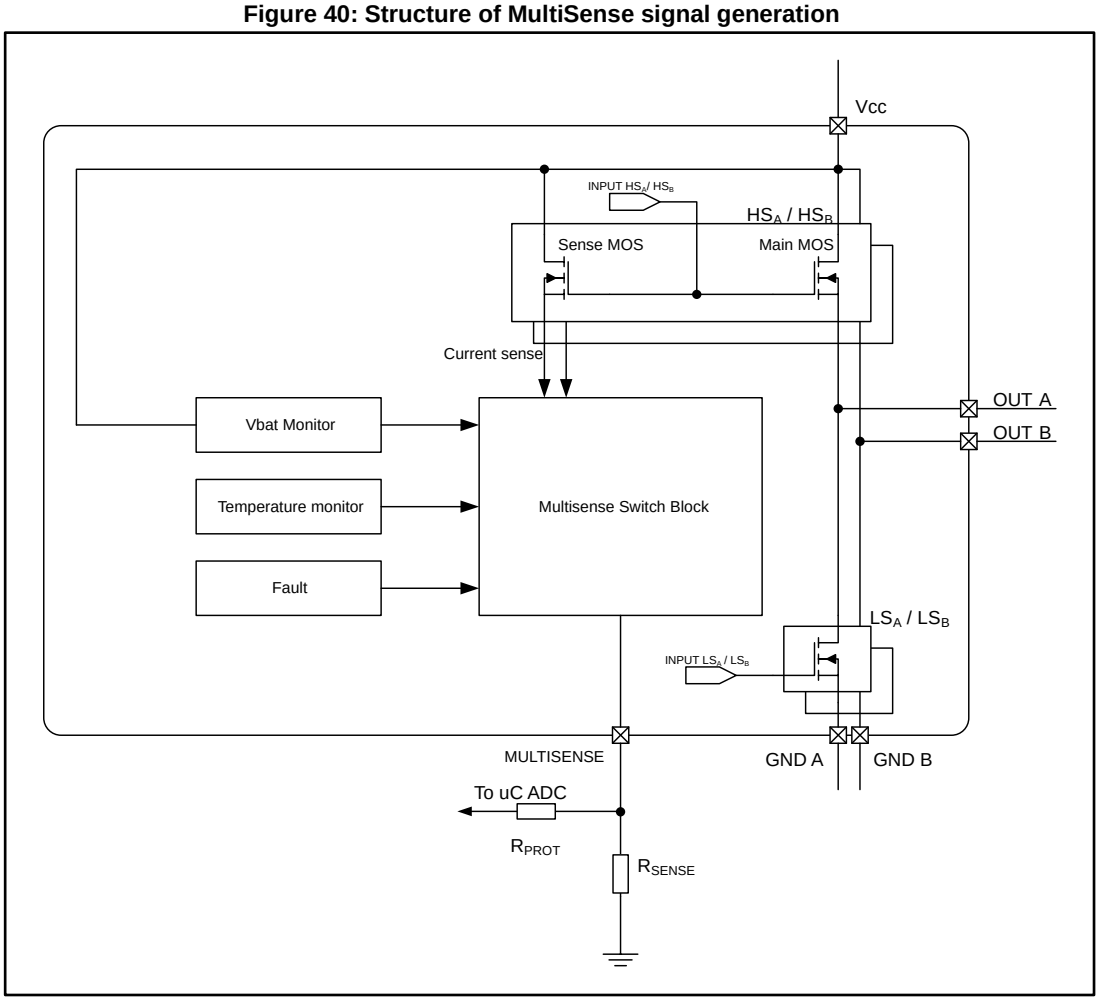
The different modes of the MultiSense pin are given in combination with the other device inputs in *Table 4: "MultiSense control truth table"*.

Figure 39: M0-7 driver with analog current sense



5.1 Current sense - principle of MultiSense signal generation

Figure 40: Structure of MultiSense signal generation



In General, the MultiSense output signal operates for V_{CC} < 28 V

Table 4: MultiSense control truth table

Digital pins						MultiSense output
INA	INB	PWM	MultiSense_EN (1)	SEL1 (1)	SEL0	
X	X	X	0	X	X	Hi-Z
X	1	X	1	0	0	Current Monitoring HS_B
X	0	X				Hi-Z
1	X	X	1	0	1	Current Monitoring HS_A
0	X	X				Hi-Z
	X	X		1	0	T_CHIP (HS) Monitoring(1)
X	X	X	1	1	1	Vcc Monitoring(1)

Notes:

(1)Valid for H-Bridge in PowerSSO-36 TP only

Current monitor: during no fault conditions ($V_{OUT} > V_{OUT\_MSD}$ -see datasheet value), the current flowing through the main high side MOS is mirrored through Sense-MOS. Sense-MOS is a scaled down copy of the main MOS according to a defined geometric ratio. Current is passed through the MultiSense switch block, fully decoupling MultiSense signal from the output current.

During the Bridge ON state, whenever a protection is triggered and the bridge is in current mode (e.g., for VNH7040AY, SEL1=L), the internal logic sets the MultiSense output in fault mode with a constant voltage VSENSE_H signal.

Temperature, VCC monitor: the internal logic is switched to voltage output mode, applying an output voltage that corresponds with the temperature or V_{CC} sensor, depending on the selected signal.

5.1.1 Current monitor

MultiSense output is set to current monitor mode via SEL0, SEL1, MultiSense_EN; see *Table 4: "MultiSense control truth table"*); it can provide:

- **Current during normal operation**: proportional to the load current flowing over the activated high side, selected by SEL0 according to the known ratio, K. This current can be easily converted to a voltage by using an external sense resistor, allowing continuous load monitoring and abnormal condition detection.
- **Diagnostics flag in fault conditions**: delivering fixed voltage V_{SENSEH} (with a certain current capability) in case of:
  - fault condition on activated high side (in ON state) triggered by power limitation, overtemperature protection, where MultiSense output is selected by SEL0 to high side in fault state
  - fault condition on activated low side (in ON state) triggered by overcurrent shutdown, overtemperature protection, where MultiSense output is selected by SEL0 to the same leg (of high side) where low side is in fault state
  - short-circuit to VCC on OUT in OFF state (INA = INB = PWM = L) selected by SEL0; for the H-bridge in the S016N package, special care must be taken for the OUTB (SEL0 = L) because the fixed voltage is available only before device enters its standby mode after T_{D_STDBY} (because all control signals are set to L)
  - in the configuration of half bridge (load connected between OUT and ground), when open load appears on OUT in OFF state (selected by SEL0) with activated external pull-up resistor. Such condition causes effect similar to the short-circuit to V_{CC} on leg in OFF state (mentioned in above case, output voltage exceeds open load threshold V_{OL})
- **Diagnostic flag during NO fault conditions**: delivering fixed voltage (V_{SENSEH}) in following configuration: full bridge in OFF state (load connected between OUTA and OUTB, INA = INB = PWM = 0), applying activated external pull-up resistor on the leg which is opposite to the monitored one by MultiSense output (pull-up on OUTB while SEL0 =1; or pull-up on OUTA while SEL0 = 0). Attention must be paid to the configuration where external pull-up is applied on OUTA, SEL0 = 0, as the device enters standby mode after T_{D_STDBY}

5.1.2 Normal operation (MultiSense_EN = 1, output active, corresponding SEL0,1 set)

While device is operating in normal conditions (no fault intervention), the V_{SENSE} can be calculated thus:

Equation 39: Current provided by MultiSense output

$$I_{SENSE} = \frac{I_{OUT}}{K}$$

Equation 40: Voltage on R_{SENSE}:

$$V_{SENSE} = R_{SENSE} I_{SENSE} = R_{SENSE} \frac{I_{OUT}}{K}$$

Where:

V_{SENSE} is the voltage measurable on R_{SENSE} resistor

I_{SENSE} is the current provided from MultiSense pin in current output mode

I_{OUT} is the current flowing in the selected high side

K factor represents the ratio between Power MOS cells and Sense MOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying ratio between I_{OUT} and I_{SENSE}.

5.1.3 Current Sense voltage and current saturation

During current monitoring, the voltage on the MultiSense pin has a certain voltage depending on load conditions and R_{SENSE} (e.g., default MultiSense voltage at nominal load current assumed to be 2.5 V).

Particular care must be taken to use an appropriate R_{SENSE} to ensure linearity over the load current range to be monitored (see *Section 5.1.4: "Dimensioning the Rsense resistor"*). Current monitoring via MultiSense is in fact guaranteed up to a maximum MultiSense voltage of 5 V (defined V_{SENSE_SAT} min. in VNH7x datasheets)

5.1.3.1 MultiSense voltage saturation

The VNH7070AS R_{SENSE} is selected so that V_{SENSE} = 2.5 V at I_{OUT} = 3.5 A

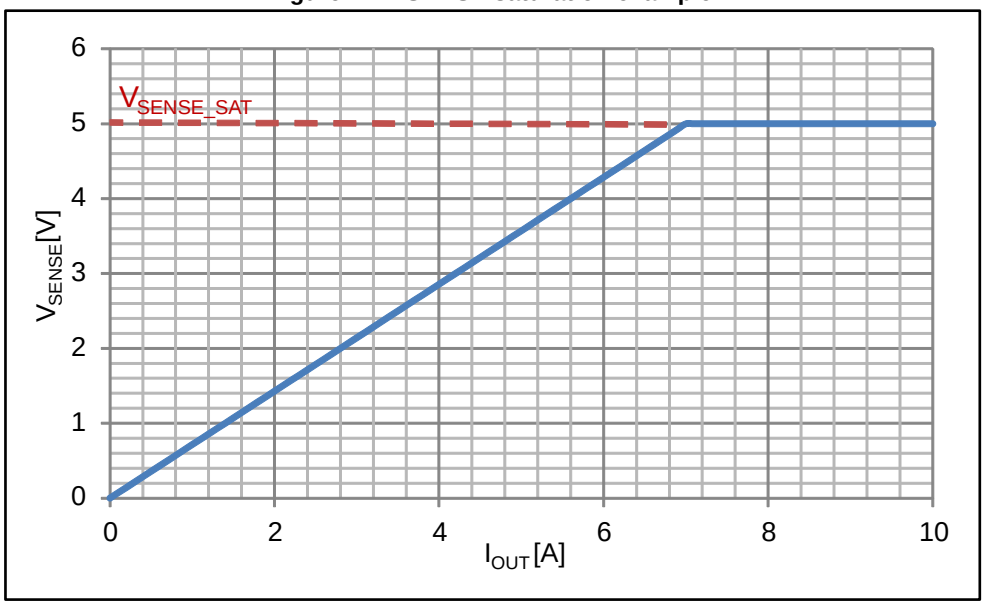
Considering (for simplicity)

K_2 @ 3.5 A = 1540 (typ.) → I_{SENSE} = 2.273mA → R_{SENSE} = 1100

Given a datasheet V_{SENSE_SAT} min. 5 V, the maximum I_{SENSE} = 5V / 1100 Ω = 4.55 mA to maintain linearity and, assuming that K_2 remains constant, the maximum I_{OUT} ~ 7 A.

Therefore, with the selected R_{SENSE}, any load current greater than 7 A produces the same V_{SENSE}, as shown below.

Figure 41: VSENSE saturation example



The current mirror output must also not reach saturation, which would again cause I_{SENSE} to no longer to be proportional to I_{OUT}. This normally happens when the maximum current from the current mirror is reached and corresponds with the minimum value of the datasheet parameter I_{SENSE_SAT} min.

5.1.3.2 MultiSense current saturation

The VNH7070AS R_{SENSE} is selected so that V_{SENSE} = 2.5 V at I_{OUT} = 3.5 A

Considering an overload current of 6 A at 4 V of MultiSense pin analog voltage, and I_{SENSE_SAT} = 4.6mA min.:

Equation 41

$$R_{SENSE} > \frac{V_{SENSE}}{I_{SENSE\_SAT\_MIN}} = \frac{4V}{4.6mA} \doteq 870\Omega$$

The following two figures show a VNH7070AS MultiSense plot.

Two different low R_{SENSE} values are connected to the MultiSense pin and relevant linearity range of V_{SENSE} versus I_{OUT} is highlighted.

- I_{SENSE_SAT} is approximately 7.5 mA, which corresponds with a maximum current that can be monitored of about 11 A.
- R_{SENSE} = 220 Ω

Figure 42: VNH7070AS VSENSE with rising IOUT versus time with RSENSE = 220 Ω

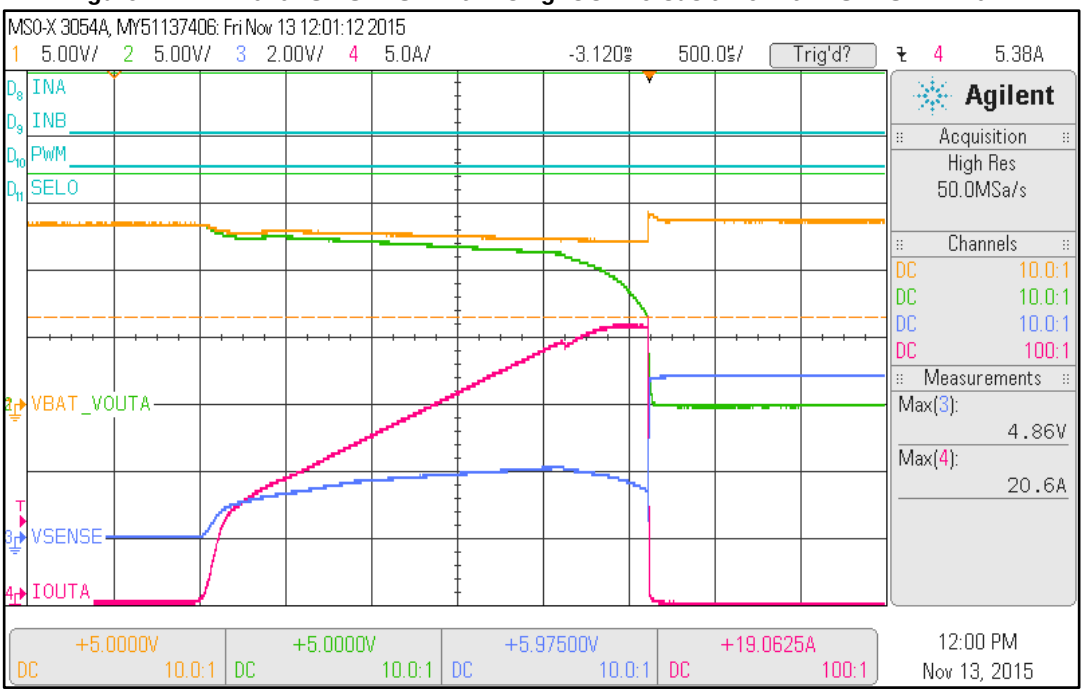
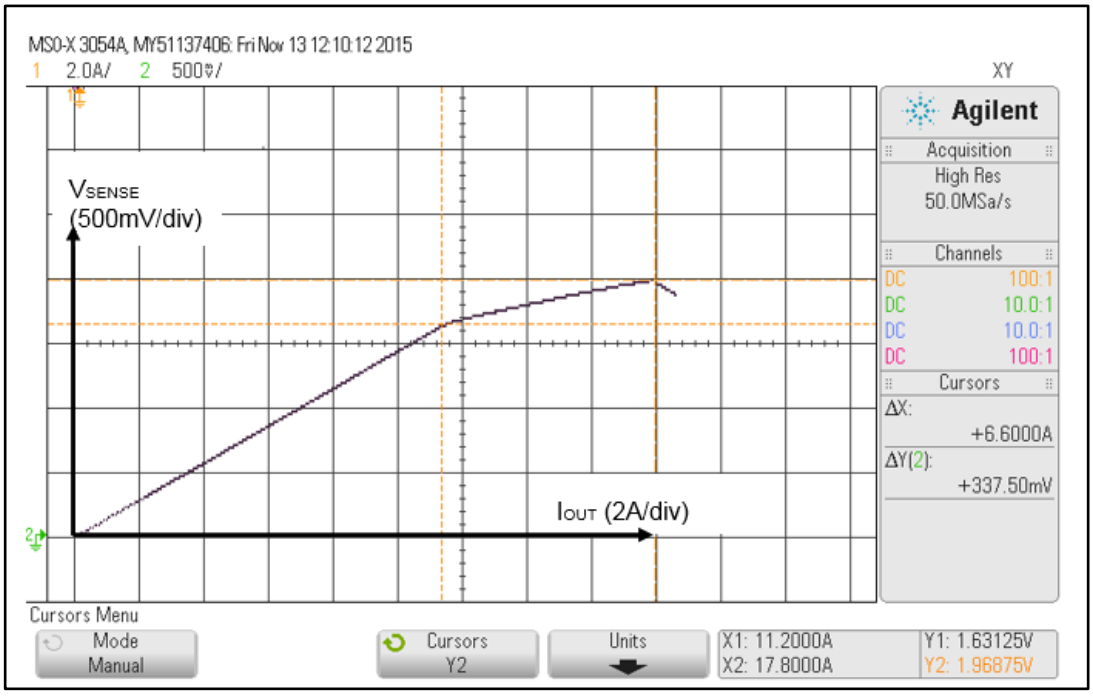


Figure 43: Corresponding VNH7070AS XY plot (VCC = 14 V) on OUTA



- R_{SENSE} = 470 Ω

Figure 44: VNH7070AS VSENSE with increasing IOUT versus time with RSENSE = 470 Ω

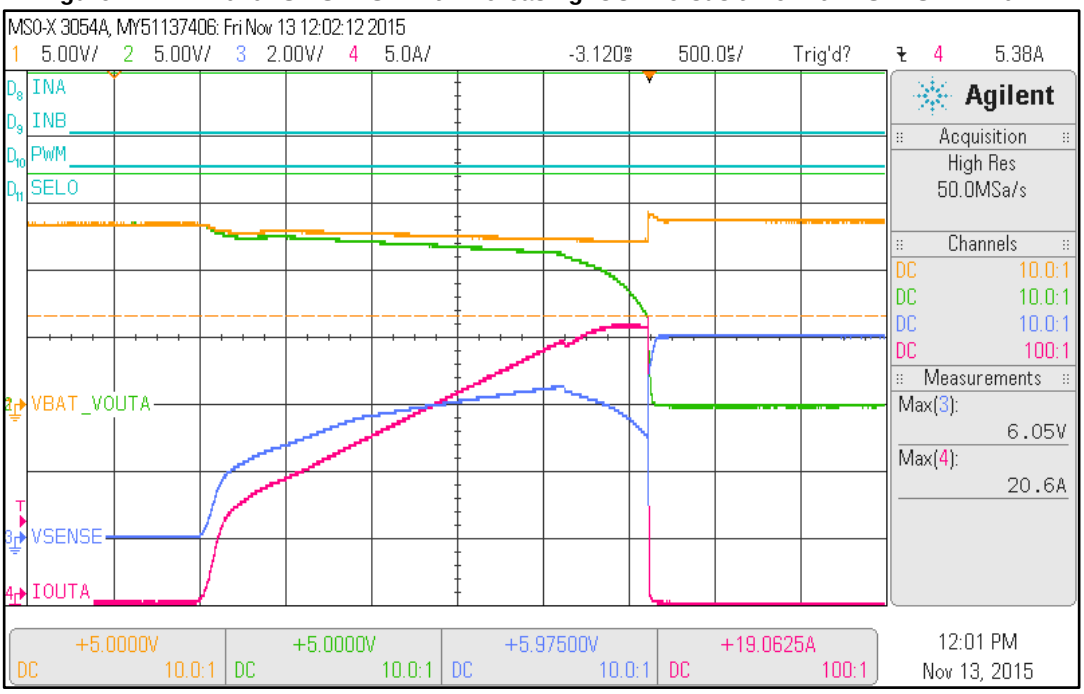
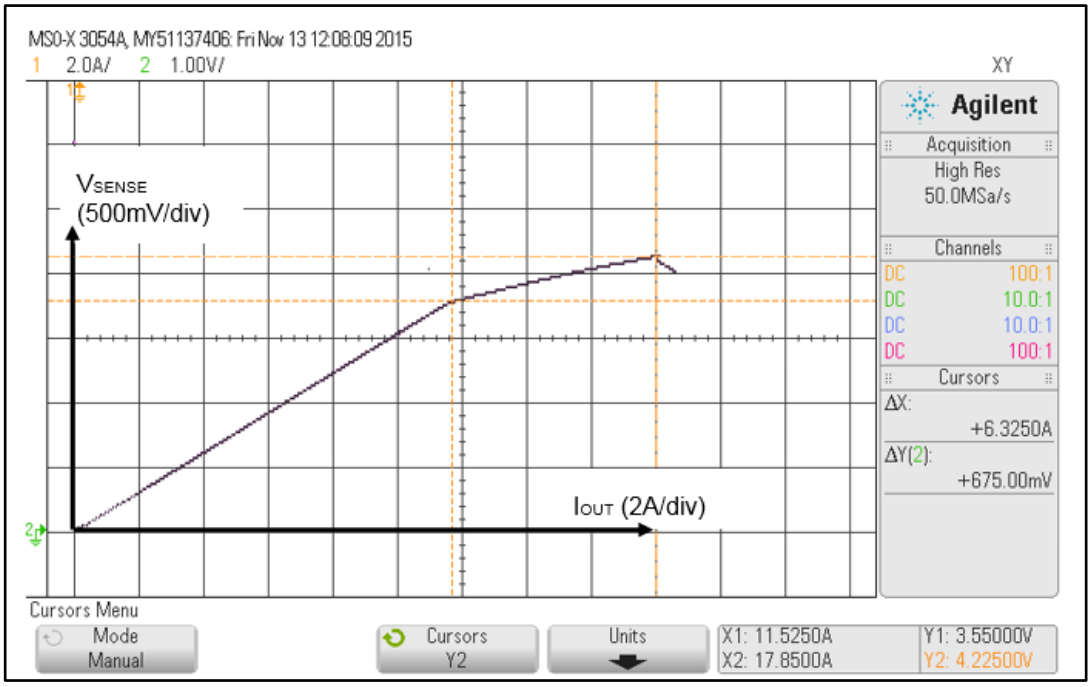


Figure 45: Corresponding XY plot (VCC = 14 V) on OUTA



V_{SENSE_SAT} and I_{SENSE_SAT} minimum values are guaranteed for the minimum V_{CC} voltage in which all K factor limits are guaranteed (7 V in datasheets) and maximum operating junction temperature (150°C in datasheets) which represent worst case conditions for the maximum load current to be monitored.

The following two figures show plots extracted from experimental data measured on VNH7070AS at 25 °C for V_{SENSE_SAT} and I_{SENSE_SAT}, respectively.

R_{SENSE} = 47K

Figure 46: Behavior of VSENSE_SAT vs VCC

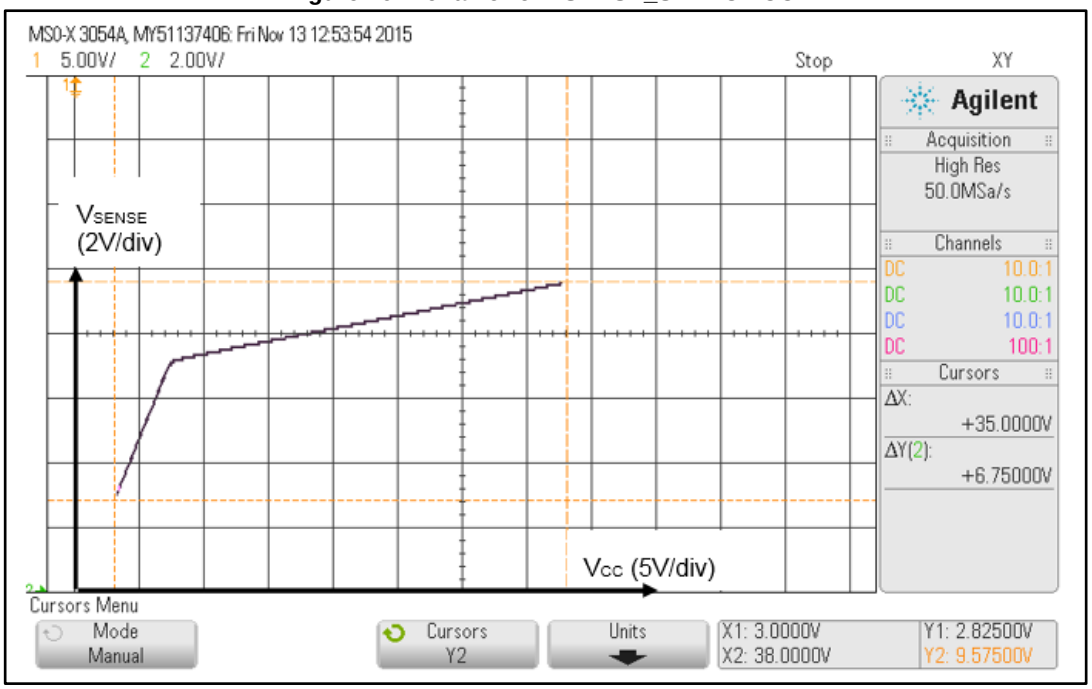
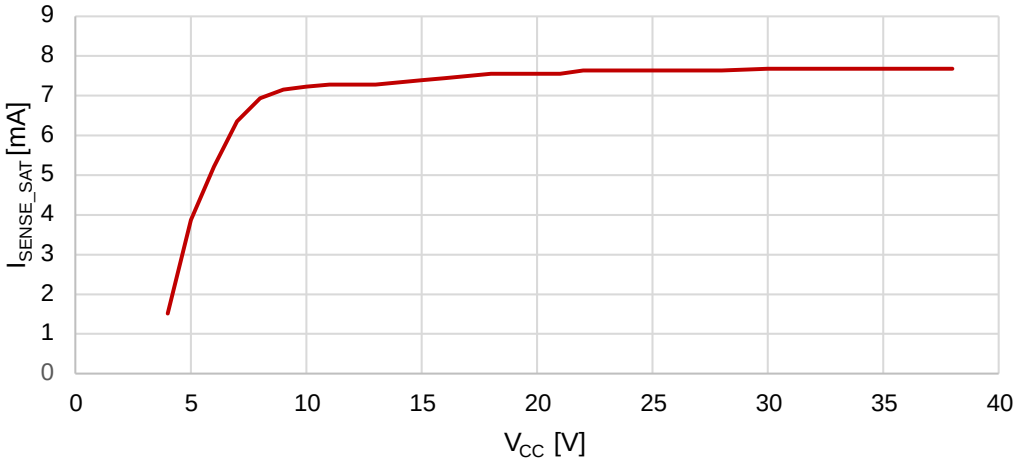


Figure 47: Behavior of ISENSE_SAT vs VCC



I_{SENSE_SAT} drops rapidly when V_{CC} is below 10 V approx. For V_{CC} > 7 V battery level, we can consider the minimum value of I_{SENSE_SAT} (given in datasheet).

The MultiSense current monitoring linear behavior is featured down to V_{CC} = 4.5V and for V_{SENSE} < V_{CC} -1.5 V (even though relevant specification limits in datasheets are no longer guaranteed).

5.1.4 Dimensioning the Rsense resistor

In normal operating conditions, the following equation applies

Equation 42: Relationship between I_{OUT} and V_{SENSE}

$$V_{SENSE} = R_{SENSE} I_{SENSE} = R_{SENSE} \frac{I_{OUT}}{K} [V]$$

The sense resistor value can be calculated from the above equation given the intended voltage at the ADC with the nominal load current and the typical K factor of the device.

The sense resistor value implies the following design considerations:

To avoid reaching MultiSense voltage saturation V_{SENSE_SAT} under normal operating conditions with the maximum load current I_{OUT_MAX} that can be monitored, R_{SENSE} must satisfy the following equation:

Equation 43

$$R_{SENSE} < K_{MIN} \frac{V_{SENSE\_SAT\_MIN}}{I_{OUT\_MAX}} [V]$$

Below this maximum current, the linearity of MultiSense is guaranteed. R_{SENSE} must be larger if a lower maximum load current needs to be read.

Under normal operating conditions, the maximum sense voltage that can be read with the given R_{SENSE} must be higher than a certain ADC threshold:

Equation 44

$$R_{SENSE} > \frac{V_{SENSE\_MAX}}{I_{SENSE\_SAT\_MIN}}$$

Where V_{SENSE_MAX} is the maximum voltage that the ADC has to read at the maximum monitored load current. This value can be 5 V or less, which is the usual maximum operating range of the ADC.

To differentiate a normal operating condition from a fault condition (where H-bridge protection applies MultiSense output to current limited voltage mode), the MultiSense pin must develop a voltage above the V_{SENSEH} (in datasheet, V_{SENSEH} = 6V typ.):

Equation 45

$$R_{SENSE} > \frac{V_{SENSE\_H\_MIN}}{I_{SENSE\_H\_MIN}}$$

Finally, the current sense resistor must protect the MulitSense pin in case of reverse battery. During this event, for monolithic devices, an intrinsic diode between MultiSense

and V_{CC} pins is forward biased and the resulting current must be limited. This I_{SENSE} value is 20 mA for VNH7070AS, therefore the minimum R_{SENSE} to protect the MultiSense pin in case of reverse battery (supposing a static condition of V_{CC} = -16 V) is:

Equation 46

$$R_{SENSE} > \frac{-V_{CC} - V_F}{I_{SENSE\_REV\_MAX}} = \frac{16V - 0.7V}{20mA} = 765$$

R_{SENSE} must therefore fulfill two conflicting conditions to ensure linearity under normal operating conditions:

1. avoid MultiSense pin current saturation (increase R_{SENSE})
2. avoid MultiSense pin voltage saturation (decrease R_{SENSE})

R_{SENSE} must also be such that normal operation (linear mode V_{SENSE} proportional to load current) can be distinguished from a fault condition (constant voltage generator developing V_{SENSEH} across the R_{SENSE}).

In chip temperature and V_{CC} monitoring mode, the MultiSense is a voltage source with limited current. In this case, however, current saturation is higher than I_{SENSE_SAT}, so linearity in T_{CHIP} and V_{CC} reading is respected with the minimum R_{SENSE} which fulfills the second condition.

The following two figures plot the empirical VNH7070AS data under typical conditions for the T_{CHIP} and V_{CC} monitor versus R_{SENSE}, respectively.

Figure 48: MultiSense in T CHIP mode behavior versus R SENSE for VNH7040AS at V CC = 14V and T C = 25°C

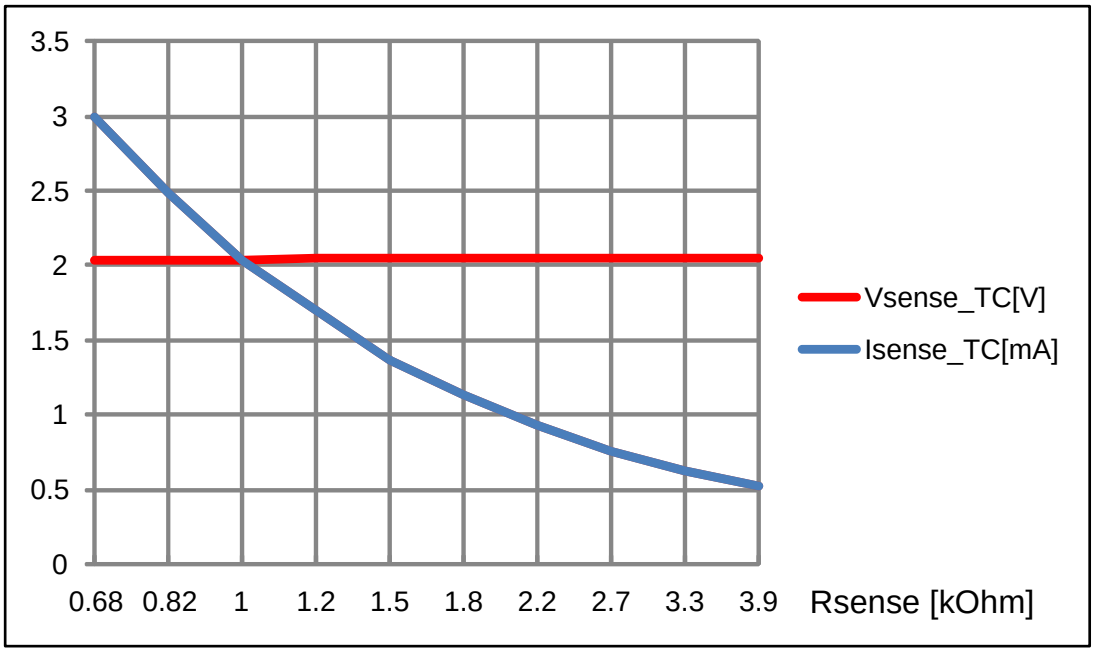
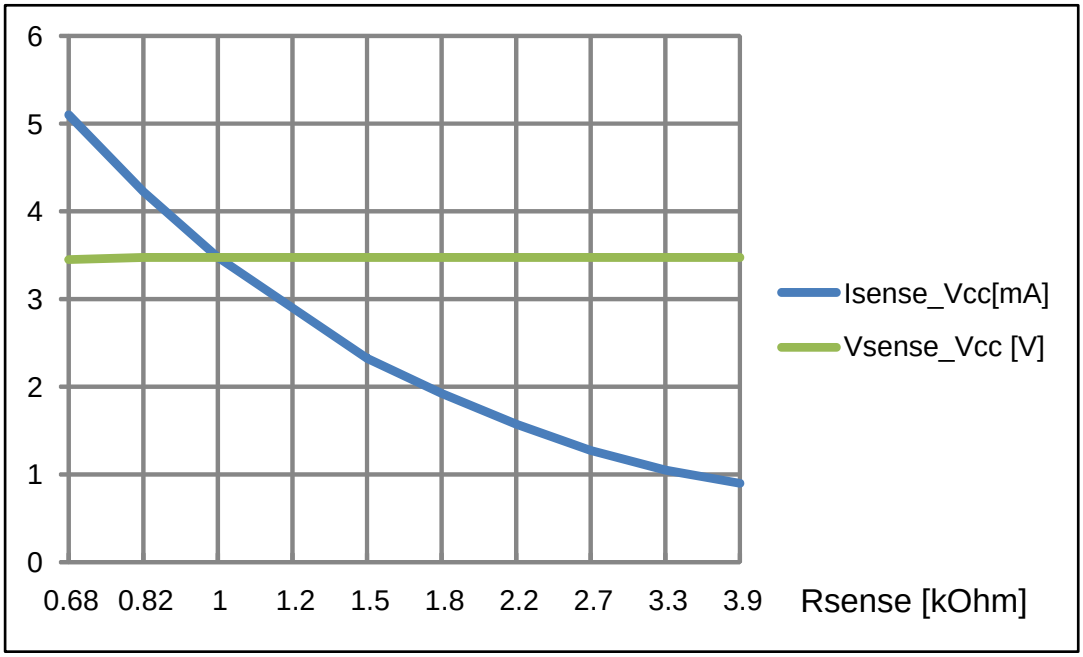


Figure 49: MultiSense in Vcc mode behavior versus R SENSE for VNH7070AS at V CC = 14V and T C = 25°C



5.1.4.1 Rsense calculation example

Consider the VNH7070BAS (70 mΩ H-bridge) with a nominal load current I_N = 3A for an intended V_{SENSE} = 2 V and typical K_2 = 1540 (from datasheet).

From *Equation 42*,

$$R_{SENSE} = K\frac{V_{SENSE}}{I_{OUT}} = 1540\frac{2}{3} = 1026\Omega$$

Supposing that the maximum load current the ADC has to monitor in linearity is twice the nominal current, then:

I_{OUT_MAX} = 6 A at V_{SENSE_MAX} = 4 V.

This means that neither V_{SENSE_SAT} nor I_{SENSE_SAT} must be reached and a voltage above 5 V must be issued in fault conditions.

We can verify that R_{SENSE} is appropriate by applying *Equation 43* to *Equation 46*:

$$R_{SENSE} < K_{3\_MIN}\frac{V_{SENSE\_SAT\_MIN}}{I_{OUT\_MAX}}1357\frac{5}{6} = 1131$$

$$R_{SENSE} > \frac{V_{SENSE\_MAX}}{I_{SENSE\_SAT\_MIN}} = \frac{4V}{4.6mA} = 870\Omega$$

$$R_{SENSE} > \frac{V_{SENSE\_H\_MIN}}{I_{SENSE\_H\_MIN}} = \frac{5V}{10mA} = 500$$

$$R_{SENSE} > \frac{-V_{CC} - V_F}{I_{SENSE\_REV\_MAX}} = \frac{16V - 0.7V}{20mA} = 765\Omega$$

Hence the chosen sense resistor of 1 kΩ is appropriate.

5.1.5 Impact of output voltage on MultiSense output

Current sense operation for load currents nearing limit thresholds is not guaranteed or predictable. Indeed, the current limiter can cause the output voltage to drop significantly, down to almost 0 V in the event of a hard short-circuit.

As the whole circuit is referenced to V_{OUT}, ambiguous and unreliable current values could derive from the MultiSense under such conditions.

To bring the MultiSense to a defined state, a dedicated circuit section shuts down the current sense circuitry when V_{OUT} drops below the V_{OUT_MSD} threshold (typically 5 V).

Therefore, in normal operation, current sense works properly inside the defined border conditions.

For a given device, I_{SENSE} is a single value monotonic function of I_{OUT} as long as the maximum V_{SENSE} (*Section 5.1.3.1: "MultiSense voltage saturation"*) or I_{SENSE} (*Section 5.1.3.2: "MultiSense current saturation"*) saturation are not reached; i.e., there is no possibility of having the same I_{SENSE} for different I_{OUT} values within the given range.

5.1.6 Current sense in overload condition (failure flag indication)

Faults caused by power limitation, overtemperature, open load or short to V_{CC} in the OFF state are indicated by the MultiSense pin being internally switched to a current-limited voltage source pulled to the V_{SENSEH} level.

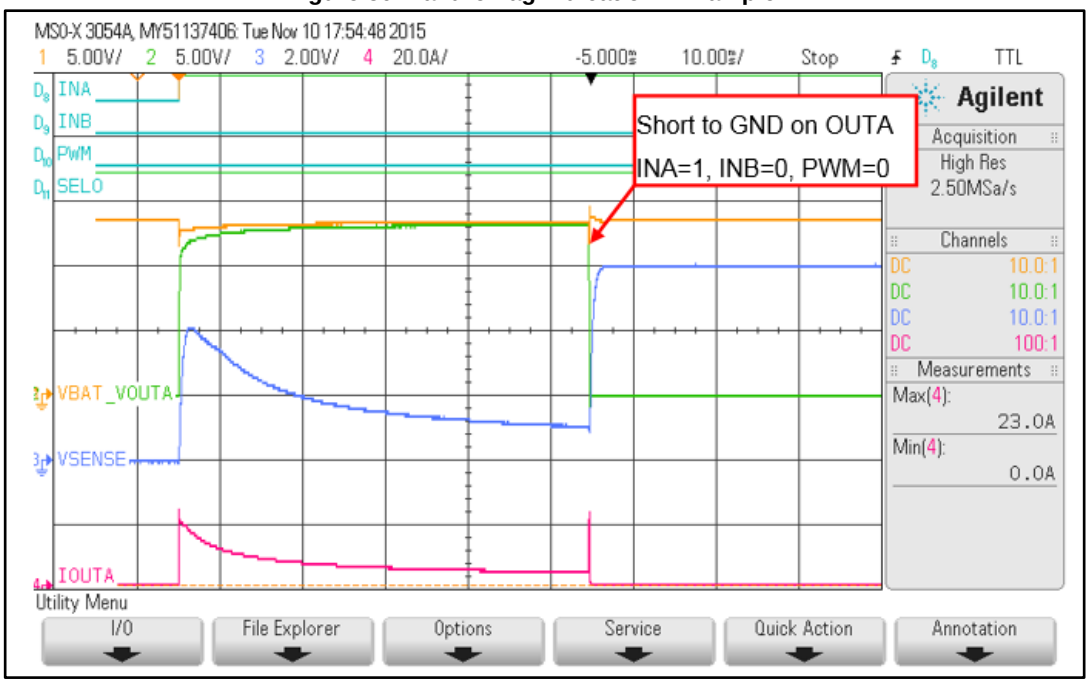
Conditions causing MultiSense being switched to V_{SENSEH} include:

- Current flowing in activated high side triggers power limitation protection, junction temperature exceeds overtemperature threshold or short-circuit to GND (MultiSense output is enabled by MultiSense_EN, selected to OUT with activated high side by SEL0, SEL1).
- Current flowing in activated low side output triggers cut-off current protection (I_{OUT} >I_{SD_LS}), or junction temperature exceeds overtemperature shutdown threshold (MultiSense output is enabled by MultiSense_EN and selected to OUT corresponding with activated low side by SEL0, SEL1).
- Voltage on OUT pin in OFF state (INA = INB = PWM = L) exceeds VOL threshold; e.g., short-circuit to VCC (MultiSense output is enabled by MultiSense_EN and selected to output by SEL0, SEL1 with mentioned output voltage). Special care must be taken for H-bridge in the S016N package for the OUTB (SEL0 = L) because the fixed voltage is only available until the device enters its standby mode after T_{D_STDBY} (because all control signals are set to L). The MultiSense output, in these events is controlled in such a way as to develop at least a voltage of V_{SENSEH} (given in the datasheet) across the external sense resistor.

The current sourced by MultiSense in this condition is in any case limited to I_{SENSEH} (given in the datasheet). To allow the current sense pin to develop at least V_{SENSEH} = 5 V, a minimum sense resistor value must be set (see *Section 5.1.4: "Dimensioning the Rsense resistor"*).

The typical behavior of a M0-7 H-bridge in a hard short-circuit to GND on OUTA (INA=H, INB= L, PWM = L) is shown below for VNH7070BAS:

Figure 50: Failure flag indication - Example 4

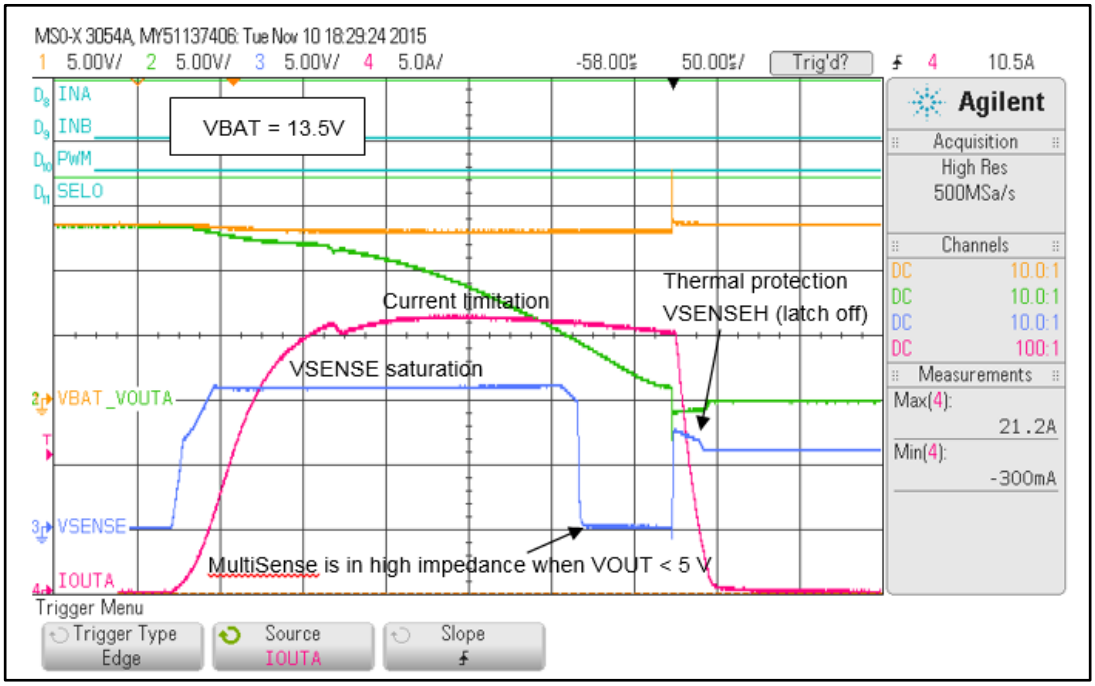


An example of a condition with progressively increasing output current (single shot ramp) from an electronic load supplied by VNH7070BAS is shown in *Figure 51: "VNH7070BAS MultiSense current monitoring with increasing overload and device latch off due to thermal protection"*.

R_{SENSE} = 10 kΩ

1. the saturation voltage V_{SENSE_SAT} is reached at about 7 A current
2. the current rises until it reaches the current limitation I_{LIM_H} threshold
3. the thermal protection then intervenes (power limitation, or the overtemperature shutdown)
4. when the output voltage drops below approximately 5 V (V_{OUT_MSD} in datasheet) the MultiSense pin goes in high impedance, until the first thermal protection is activated
5. the MultiSense pin is then reactivated and the V_{SENSEH} voltage is issued and latched
6. as INA remains active in this case, high side HSA is kept deactivated.

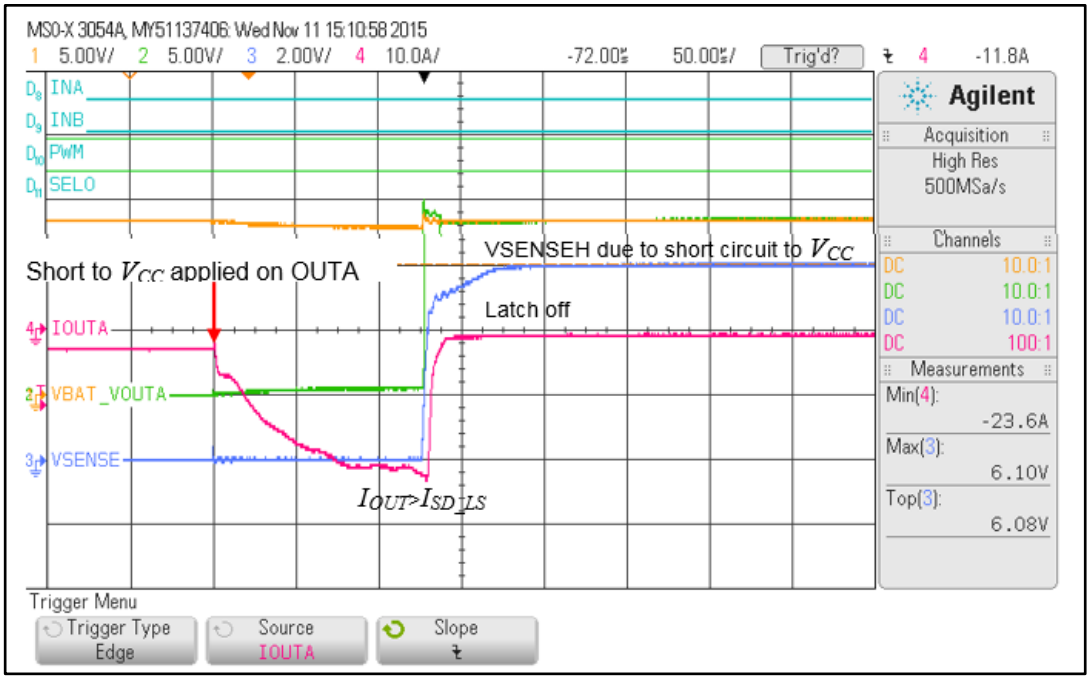
Figure 51: VNH7070BAS MultiSense current monitoring with increasing overload and device latch off due to thermal protection



The second example depicts output short-circuit to V_{CC} on activated low side driver on OUTA (INA=0 INB=0 and PWM = 1).

1. the current exceeds the shutdown threshold $I_{OUT}>I_{SD\_LS}$ or the junction temperature exceeds the overtemperature shutdown level
2. the relevant driver is latched off
3. V_{SENSEH} is signaled by the MultiSense output.

Figure 52: VNH7070BAS MultiSense current monitoring with short-circuit to V CC and device latch off due to overload protection



5.1.7 Latching and unlatching conditions

5.1.7.1 Latching conditions

The fault conditions causing latch off of the affected A or B full bridge (where OUTA or OUTB or both are put into high impedance) are:

- power limitation or overtemperature shutdown protection triggered (for example due to short-circuit to ground on OUTA or OUTB) on activated high side HSA or HSB
- activated low side LSA or LSB reaches overcurrent shutdown threshold (also referred to as cut-off current shutdown and indicated by I_{SD_LS} in the datasheet) or overtemperature condition (e.g., due to output short to V_{CC} on OUTA or OUTB).

The latch off state can be evaluated on the MultiSense output; it is necessary to select the channel corresponding with the current output monitor. The combination of INA, INB, SEL0 and SEL1 and MultiSense_EN control pin states can be used to determine the latch off state of a particular high or low side.

In general, V_{SENSEH} on the MultiSense output (in current mode) means the corresponding leg is disabled, OUTA or OUTB are in high impedance. The latch off condition continues to be signaled by V_{SENSEH} until unlatching is performed to clear the fault of the latched side and restart it.

5.1.7.2 Unlatching conditions

High side driver: to unlatch the high side driver after a latch off condition, set INA low (if HSA goes into protection mode); or set INB low (if the HSB goes into protection mode), for a minimum time $t_{LATCH\_RST\_HS}$. The high side can then be reactivated (by INA or INB set high).

Low side driver: unlatch the low side driver by setting the INA (in case the LSA goes into protection mode) high or by setting INB (in case the LSB goes into protection) high, for a minimum time $t_{LATCH\_RST\_LS}$. After such period INA or INB applying low level will re-activate low side channel again.

5.1.8 Entering standby-mode after an OVL event

To enter standby after a fault, all input pins must be set to low level for at least t_{D_SDBY} (from when the last input pin is set to low).

Suppose that a high side driver (e.g. HSA) is latched in full bridge setup. In order to leave its latch off condition, INA is set low for $t_{LATCH\_RST\_HS}$. This unlatches the high side driver and also satisfies the precondition of all INA or INB low. The device enters standby mode after t_{D_stby}.

Another scenario is when the low side driver is latched (e.g., LSB). To clear the latch off condition, the INB signal must be set from low to high. After all the input pins are set to low again, the device enters standby mode after t_{D_stby}.

To exit standby, it is sufficient to set one of the input pins (INA, INB, PWM, MultiSense_EN, SEL0, SEL1) from low to high. It is recommended in this procedure to set the PWM from low to high after any of the other input pins after a minimum 20 µs delay (to avoid overstressing the low side if there is a short-circuit between output and V_{CC})

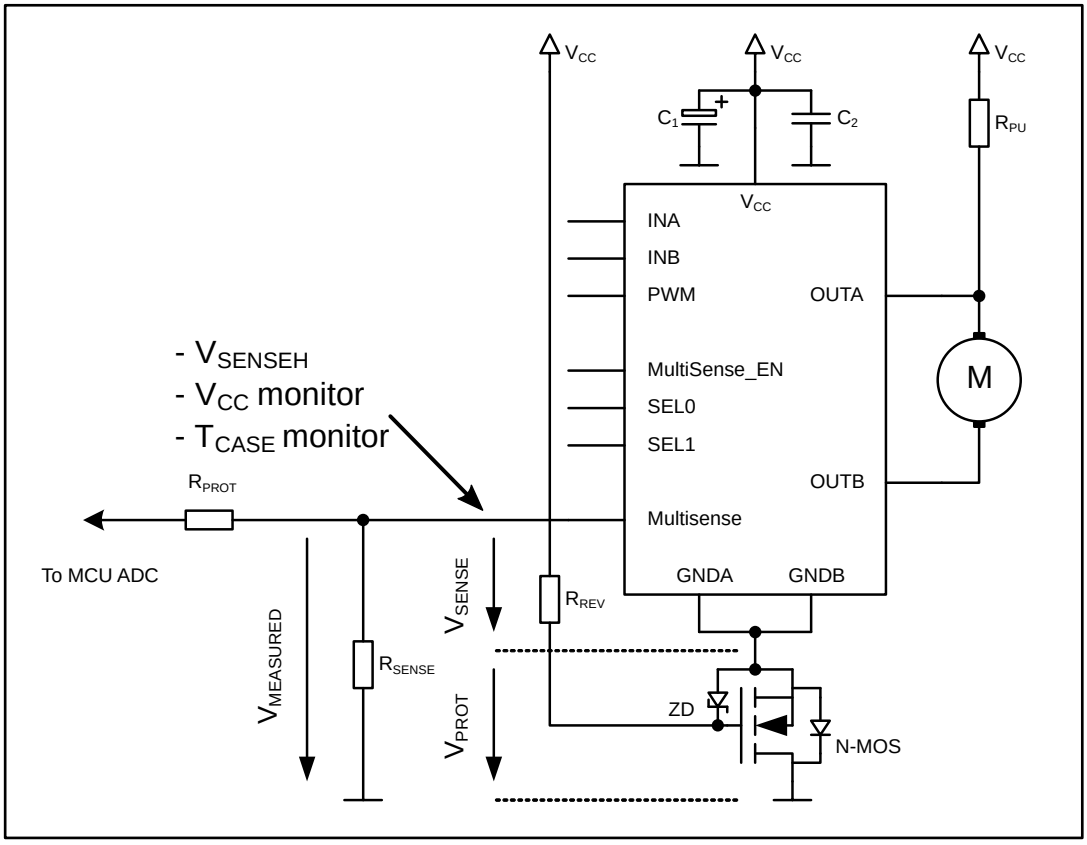
5.1.9 VNH7040AY Tcase, Vcc monitoring

The VNH7040AY device deploys full MultiSense logic implementation, which includes device case temperature and battery voltage monitoring.

MultiSense output operates in voltage mode and the output level is referred to device GND. For monolithic devices, where reverse battery protection circuitry is used on the device GND side, voltage offset is created relative to real GND potential. This offset must be considered during measurement on MCU side.

The image below shows the connection between $V_{MEASURED}$ and real V_{SENSE} signal.

Figure 53: VNH7040AY MultiSense voltage mode with GND voltage shift



5.1.9.1 Vcc monitor

The battery monitoring channel provides:

$$V_{SENSE} = \frac{V_{CC}}{4}$$

By applying the limit cases of transfer coefficients, we can determine the potential V_{CC} monitoring inaccuracy.

Considering the limit values in the VNH7040AY datasheet, and presuming all HSs and LSs are deactivated (Inx = 0, PWM = 0)

$$V_{SENSE\_VCC\_MIN} = 3.16V = \frac{13}{TRANSFER\_COEFFICIENT\_MAX}$$

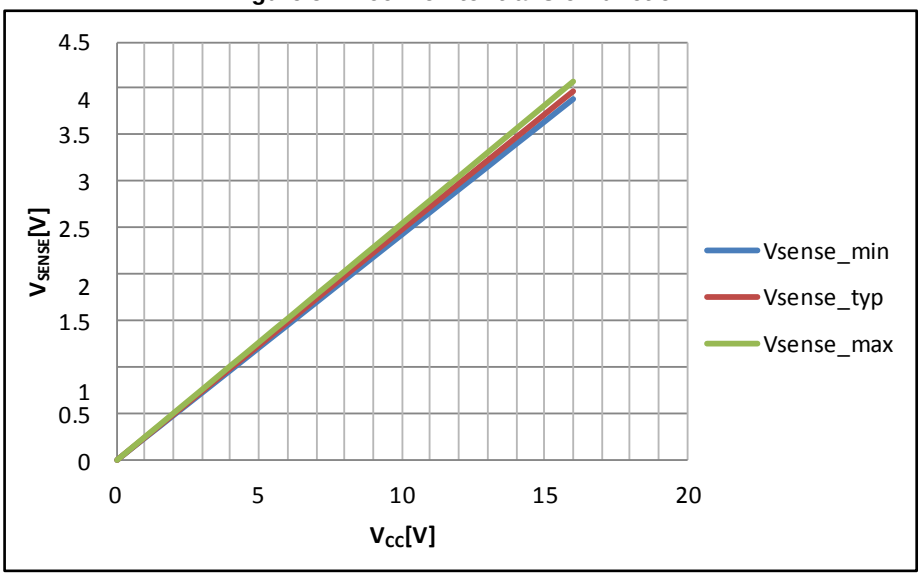
$$TRANSFER\_COEFFICIENT\_MAX = \frac{13}{3.16} = 4.114(+2.8\%)$$

Similarly,

$$V_{SENSE\_VCC\_MAX} = 3.30V = \frac{13}{TRANSFER\_COEFFICIENT\_MIN}$$

$$TRANSFER\_COEFFICIENT\_MIN = \frac{13}{3.30} = 3.939(-1.5\%)$$

Figure 54: Vcc monitor transfer function



Without calibration of voltage analogue feedback accuracy, only limited V_{CC} monitoring precision is possible.

Calibration involves measuring an operating point of a device V_{SENSE_VCC} (e.g., calibration at 13 V and 25 °C) and applying the relationship between V_{SENSE_VCC} and device temperature to determine V_{CC} with more precision.

Experimental results show an average:

$$\frac{dV_{SENSE\_VCC}}{dT_{CHIP}} \cong -70\mu V/K$$

and an average relative error

$$\frac{dV_{SENSE\_VCC}/V_{SENSE\_VCC}}{dT_{CHIP}} \cong -5.4\frac{\mu V/V}{K} for -40°C to 85°C$$

The MultiSense signal in V_{CC} mode also depends on the state of the channels; experimental results show a V_{SENSE} variation of about 3 mV when HS or LS are activated.

5.1.9.2 Case temperature monitor

The temperature coefficient is dV_{SENSE_TC}/dT ~ -5.5 mV/°C.

The case temperature monitor determines actual device temperature with temperature sensing diodes:

Equation 47: relationship between temperature and output V SENSE level

$$V_{SENSE\_TC}(T) = V_{SENSE\_TC}(T_0) + \frac{dV_{SENSE\_TC}}{dT}(T - T_0)$$

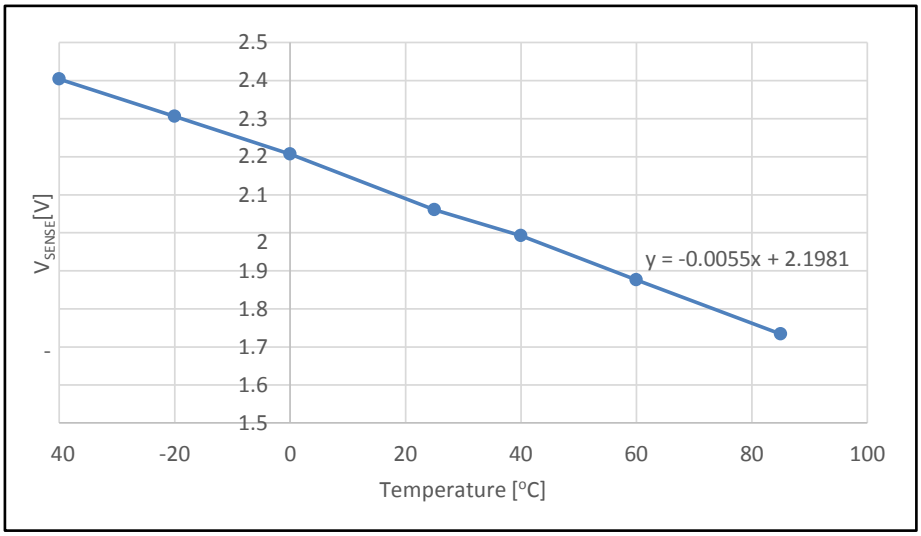
Where:

$$temperaturecoefficient = \frac{dV_{SENSE\_TC}}{dT}$$

From the datasheet, V_{SENSE_TC} typ. = 2.1 V (at 25 °C and 13 V, all channels off, R_{SENSE} = 1 kΩ), hence:

The following graph depicts result of V_{SENSE_TC} function by experimental measurement:

Figure 55: Temperature monitor transfer function



The temperature coefficient is dV_{SENSE_TC}/dT ~ -5.5 mV/°C.

The total spread of V_{SENSE_TC} at a given temperature (between -40 °C and 150 °C) varies ±85 mV, which equates to about ±15 °C in temperature precision without calibration.

Calibrating the MultiSense T_{CHIP} monitor involves measuring an operating point of a device V_{SENSE_TC} (e.g, at 13 V and 25 °C) and applying the relationship between V_{SENSE_VCC} and the battery voltage.

Experimental results show an average

$$\frac{dV_{SENSE\_VCC}}{dV_{CC}} \cong -0.5mV/V$$

Hence,

$$\frac{dT_C}{dV_{CC}} \cong 0.09\,^{\circ C}/_{V}\ from 7V to 18V$$

The MultiSense signal in V_{CC} mode also depends on the state of the channels; experimental results show a V_{SENSE} variation of about 1.2 mV when HS or LS are activated, for a positive offset of about 0.2 °C.

5.1.10 Tchip measurement example during consecutive motor activations with VNH7040AY

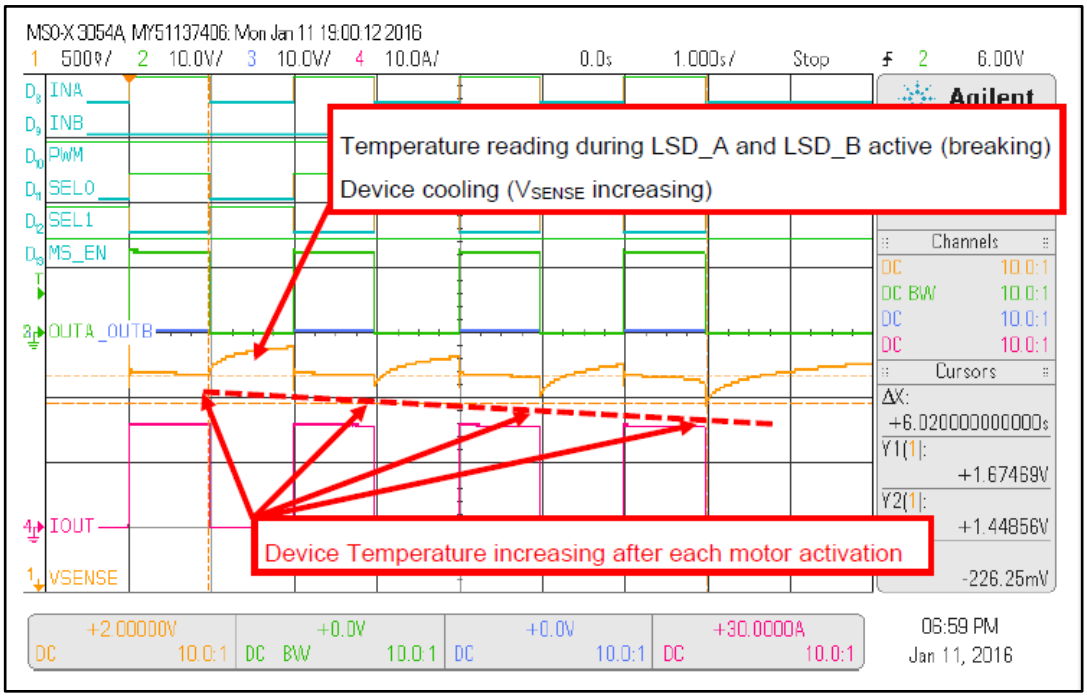
In this example, the current monitoring is applied during on state of HSA (MultiSense in configuration SEL0 = 1, SEL1 = 0).

During the turn on of LSA and LSB, the chip and motor is braked to GND: the chip temperature decreases (VSENSE increasing) as shown by Multisense output (activated TCHIP). The figure below shows the temperature decreasing during inactive state (by increasing of Multisense voltage), but after activation of all H-bridges, the overall temperature increases.

This can alert the application designer that several other activations may lead to overtemperature and consequent output Latch-off. Therefore, a software lock can be implemented to limit the number of consecutive activations.

As a load is used mirror folding motor in parallel with R = 1 Ω.

Figure 56: Temperature reading during consecutive motor activations



Applying V_{SENSE} data from the figure above and *Equation 47* for temperature calculation, we can recalculate chip temperature from MultiSense output voltage level.

Point 1 temperature (V_{SENSE1} = 1.675 V)

$$T_1 = \frac{V_{SENSE\_TC}(T) - V_{SENSE\_TC}(T_0) + \frac{dV_{SENSE\_TC}}{dT}T_0}{\frac{dV_{SENSE\_TC}}{dT}} = \frac{1.675 - 2.07 - 0.0055 * 25}{-0.0055} \doteq 97°C$$

Point 2 temperature (V_{SENSE2} = 1.449 V)

$$T_2 = \frac{V_{SENSE\_TC}(T) - V_{SENSE\_TC}(T_0) + \frac{dV_{SENSE\_TC}}{dT}T_0}{\frac{dV_{SENSE\_TC}}{dT}} = \frac{1.449 - 2.07 - 0.0055 * 25}{-0.0055} \doteq 138°C$$

So after four H-bridge activations, the device temperature increased around 41°C, and further activations would eventually cause device over temperature shutdown.

5.1.11 Open load detection in off-state

The Open Load (OL) detection in off-state operates in the condition where the device is OFF (INA, INB and PWM all set to low). The OL detection is performed by reading the CS output in case of devices in SO-16N or the MultiSense output in case of devices in PowerSSO-36 (in the latter case, by setting the MultiSense_EN = H).

A short to V_{CC} can be detected from open load condition with a pull up resistor applied over switched circuitry. Depending on application setup, the following cases can be applied:

1. **half-bridge** with separate loads on OUTA and OUTB, open load pull-up resistor R_{PU} is applied for each side; open load is indicated by VsenseeH (see *Figure 62: "Open load detection in OFF state – two half-bridge configuration"*)
2. **Full bridge** (load connected between OUTA and OUTB), only one pull-up resistor R_{PU} is sufficient; open load is indicated by high impedance of MultiSense(see *Figure 65: "Open load detection in OFF state – full-bridge configuration"*)

The following figures show the delay times for OL detection in the off state vs INA/INB and SEn settings. The relevant delay times t_{DSTKON} and t_{D_VOL} are given in the datasheets.

In H-Bridges without the MultiSense_EN pin, to perform open load diagnostics, the device must not enter Stby before it has ended the OL detection task. T_{DSTKON} is defined as the minimum delay time after the INA and INB pins (considering that PWM is already low) are set low so the device can provide a valid indication of the OL detection. Since the detection can be performed both on reading of OUTA (SEL0=H) and OUTB (SEL0=L), it is suggested to start the OFF state OL detection by keeping SEL0=H for at least the maximum T_{DSTKON} given in the datasheets. After that, SEL0 can be set low and the OL detection on OUTB can also be performed.

In the H-Bridges not having the MultiSense_EN pin, the OL detection of OUTB (after setting of SEL0 from H to L) must be done inside the T_{D_STBY} minimum value, as per the datasheet

Figure 57: Open load/short to Vcc detection in OFF state - delay after INA or INB is set from high to low

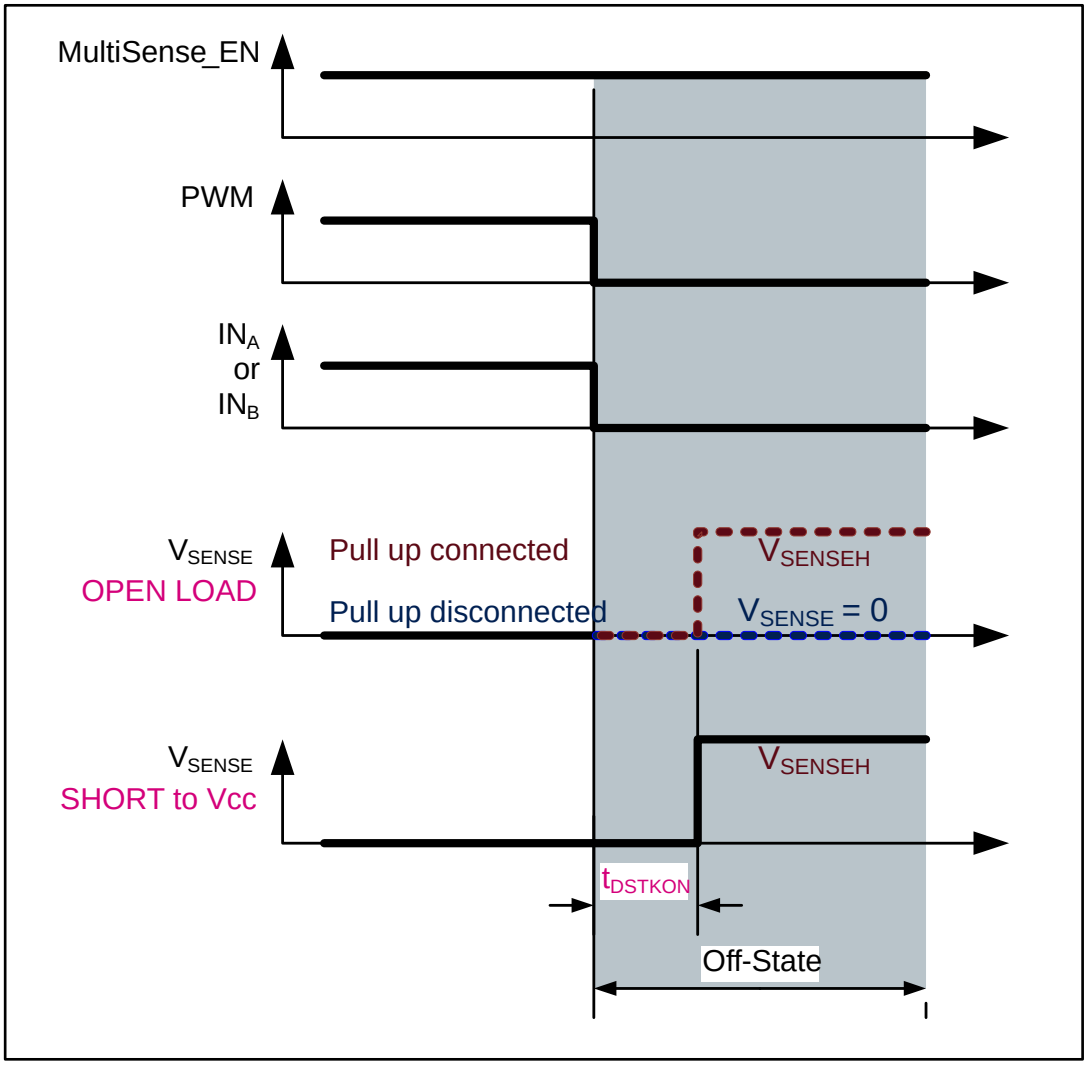


Figure 58: Open load / short to V CC detection in OFF state - delay after VOUT > VOL

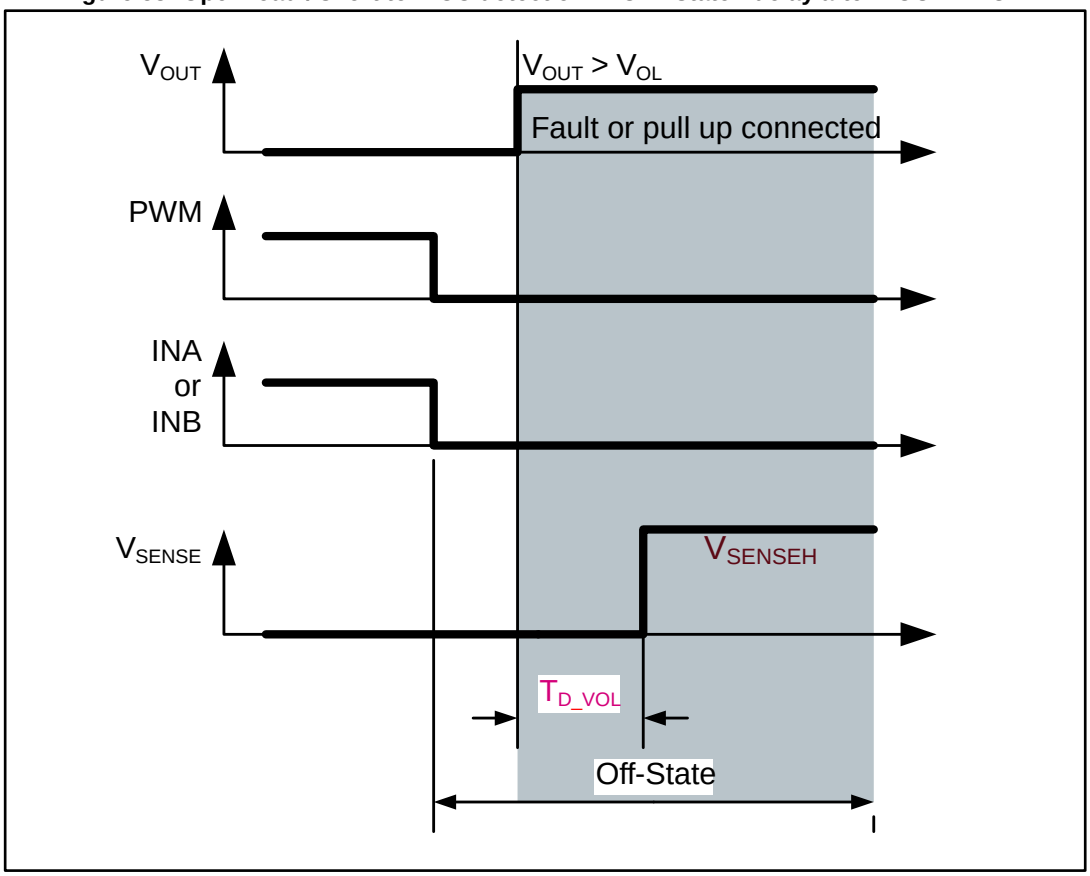


Figure 59: Open load / short to V CC detection in OFF state - delay after MULTISENSE_EN is set high to low, or all control signals set low (enter standby mode)

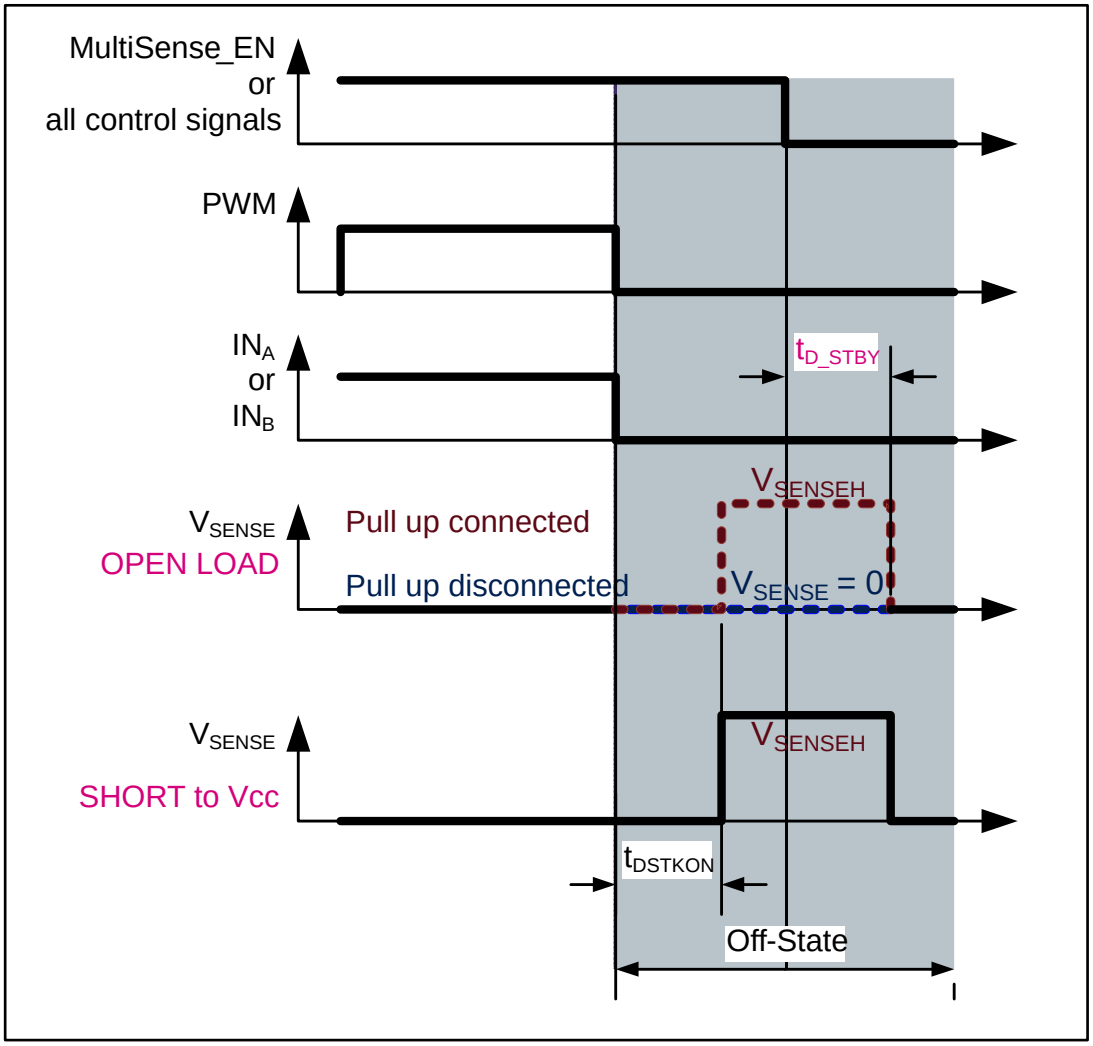


Table 5: MultiSense pin levels in off-state

Condition	Pull up	MultiSense	MultiSense_EN
Open load	Yes	0	L
		V_{SENSEH}	H
	No	0	L
		0	H
Short to V_{CC}	Yes	0	L
		V_{SENSEH}	H
	No	0	L
		V_{SENSEH}	H
Nominal	Yes	0	L
		0	H

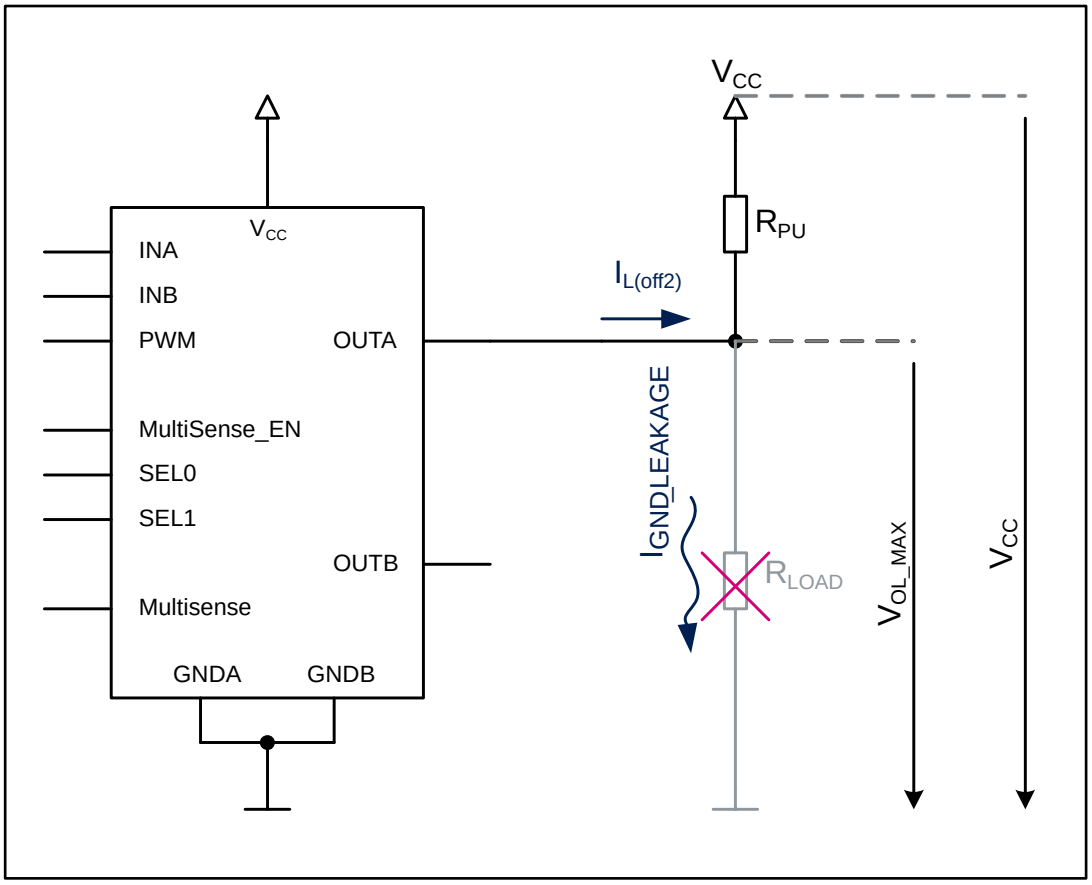
Condition	Pull up	MultiSense	MultiSense_EN
	No	0	L
		0	H

5.1.11.1 Half-bridge design considerations

Half-bridge – maximum RPU during open load

The switchable resistor R_{PU} must ensure $V_{OUT} > V_{OL\_MAX}$ (value in datasheet), considering maximum leakage current for V_{OL_MAX}, as well as additional leakage current flowing to GND (due to humidity).

Figure 60: Half-bridge – RPU calculation with no load connected (RPU on OUTA)



Resistor R_{PU} connected to V_{BAT} supply results in:

Equation 48

$$R_{PU} < \frac{V_{BAT} - V_{OL\_MAX}}{I_{GND\_LEAKAGE} - I_{L(off2)\_MIN}}$$

Given

- V_{BAT} = 7 V
- $I_{GND\_LEAKAGE}$ = 0
- $I_{L(off)}$ = -100 µA (OFF state output sink current - datasheet value)

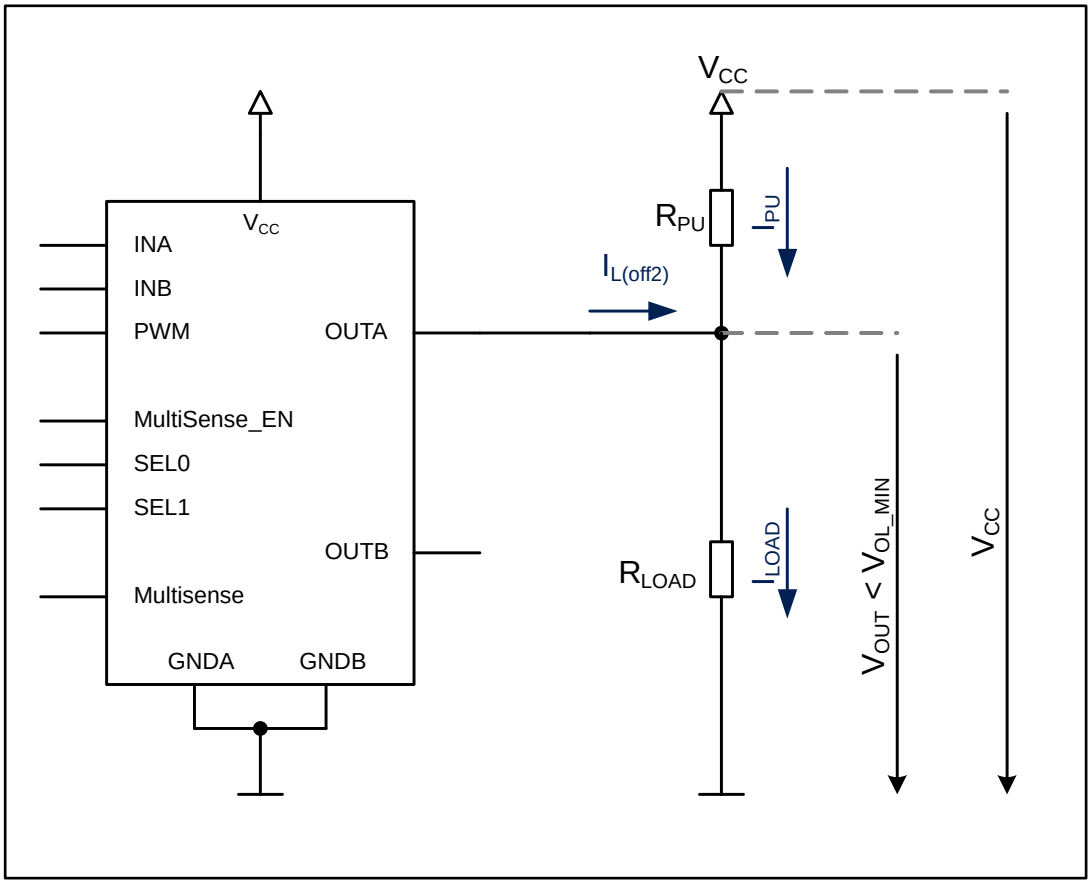
$$R_{PU} < \frac{7V - 4V}{100\mu A} = 30k\Omega$$

Hence for V_{BAT} = 7 V, R_{PU} should be less than 30 kΩ to detect an open load in the OFF state.

Half-bridge – minimum RPU while load is connected

To ensure that no OFF state open load failure flag is set when the load is connected, the minimum R_{PU} value must be evaluated.

Figure 61: Half-bridge – RPU calculation with load connected (RPU on OUTA)



Considering:

Equation 49

$$I_{LOAD} = \frac{V_{OUT}}{R_{LOAD}} = I_{L(off2)} + I_{PU}$$

and

Equation 50

$$I_{PU} = \frac{V_{BAT} - V_{OUT}}{R_{PU}}$$

then:

Equation 51

$$\frac{V_{OUT}}{R_{LOAD}} = I_{L(off2)} + \frac{V_{BAT} - V_{OUT}}{R_{PU}}; V_{OUT} < V_{OL\_MIN}$$

Results in:

Equation 52

$$R_{PU} > \frac{R_{LOAD}(V_{BAT} - V_{OL_{MIN}})}{V_{OL\_MIN} - R_{LOAD} * I_{L(off2)\_MAX}}; (I_{L(off2)\_MAX} isnegative)$$

Consider a VNH7070BAS device driving a load with the following parameters:

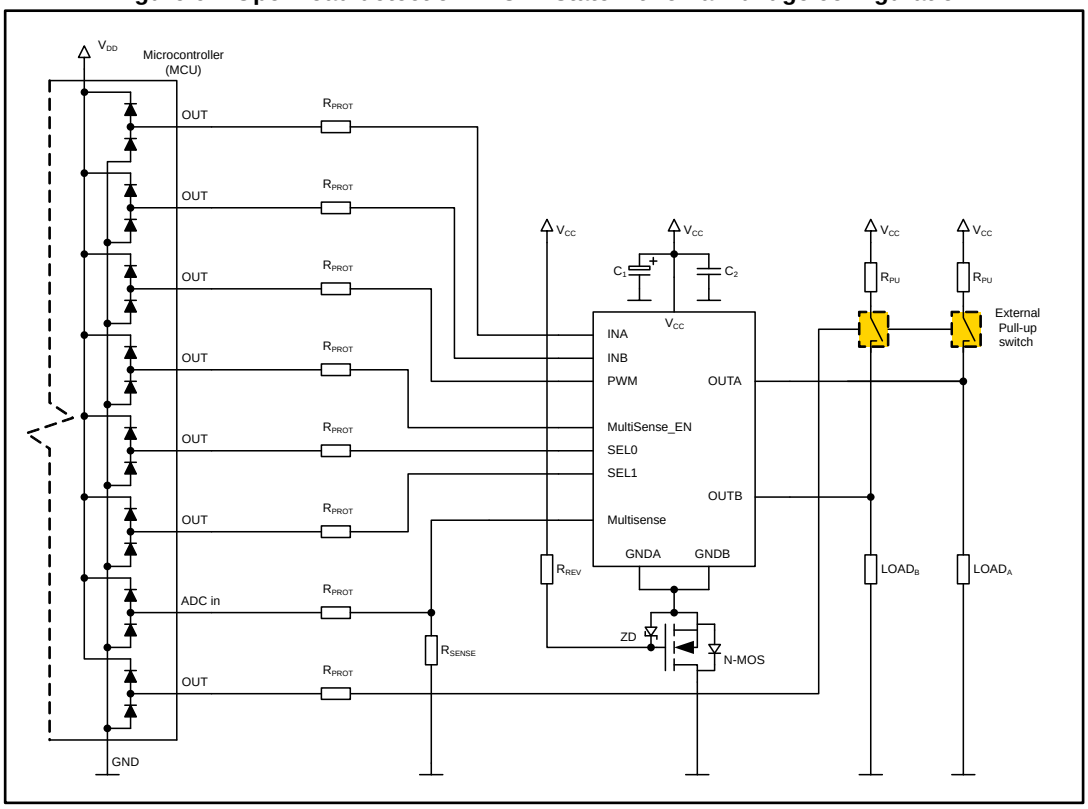
- R_{LOAD} = 4 Ω
- V_{OL_MIN} = 2 V and V_{BAT} = 18 V (worst case for battery)
- $I_{L(off2)\_MAX}$ = -15 µA

Applying *Equation 52*, the pull-up resistance in order not to generate a false OL diagnostic is:

$$R_{PU} > \frac{4\Omega(18V - 2V)}{2V - 4\Omega \cdot (-15A)} = 32\Omega$$

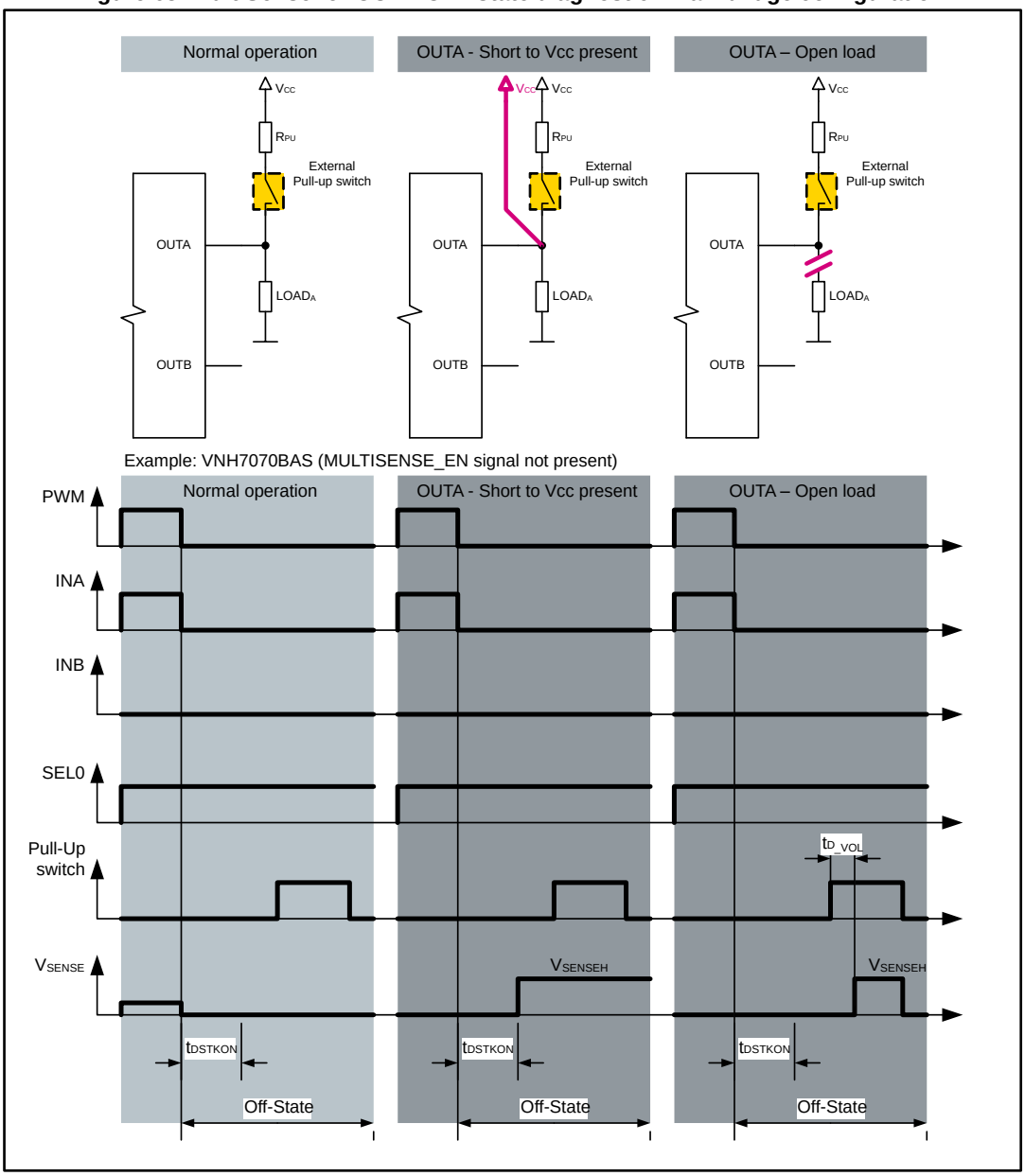
In the configuration of two half bridges, external pull-up circuits are applied for both OUTA and OUTB, open load diagnostics is done for each output separately.

Figure 62: Open load detection in OFF state – two half-bridge configuration



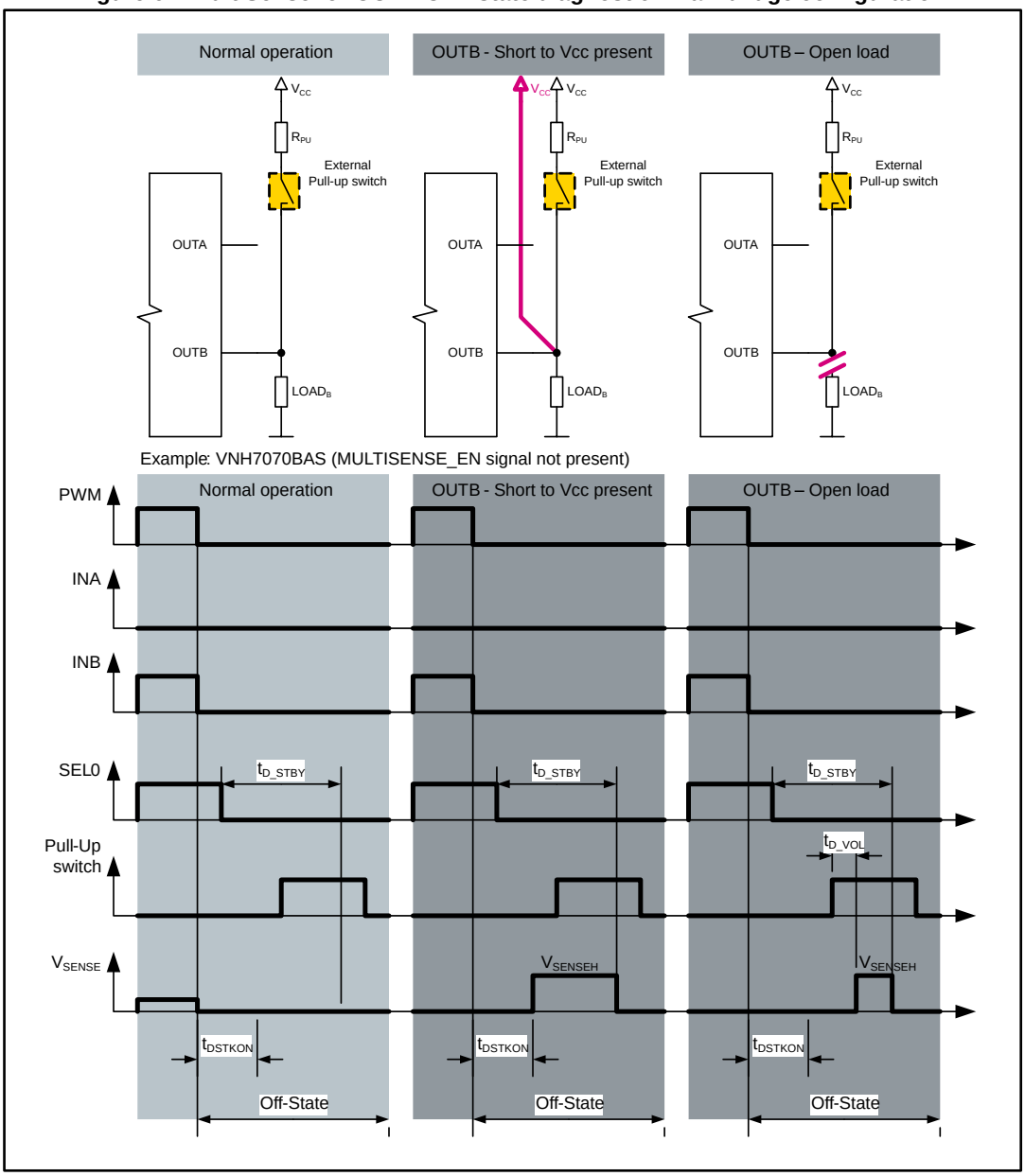
The diagnostics in the OFF state for OUTA is illustrated below.

Figure 63: MultiSense for OUTA OFF state diagnostic – half-bridge configuration



The behavior is slightly different for OUTB: the MultiSense signal is available during open load with active pull-up resistor only until standby mode is entered (after t_{D_STBY}), when all control signals set low: INA = INB = SEL0 = SEL1 = MULTISENSE_EN = L).

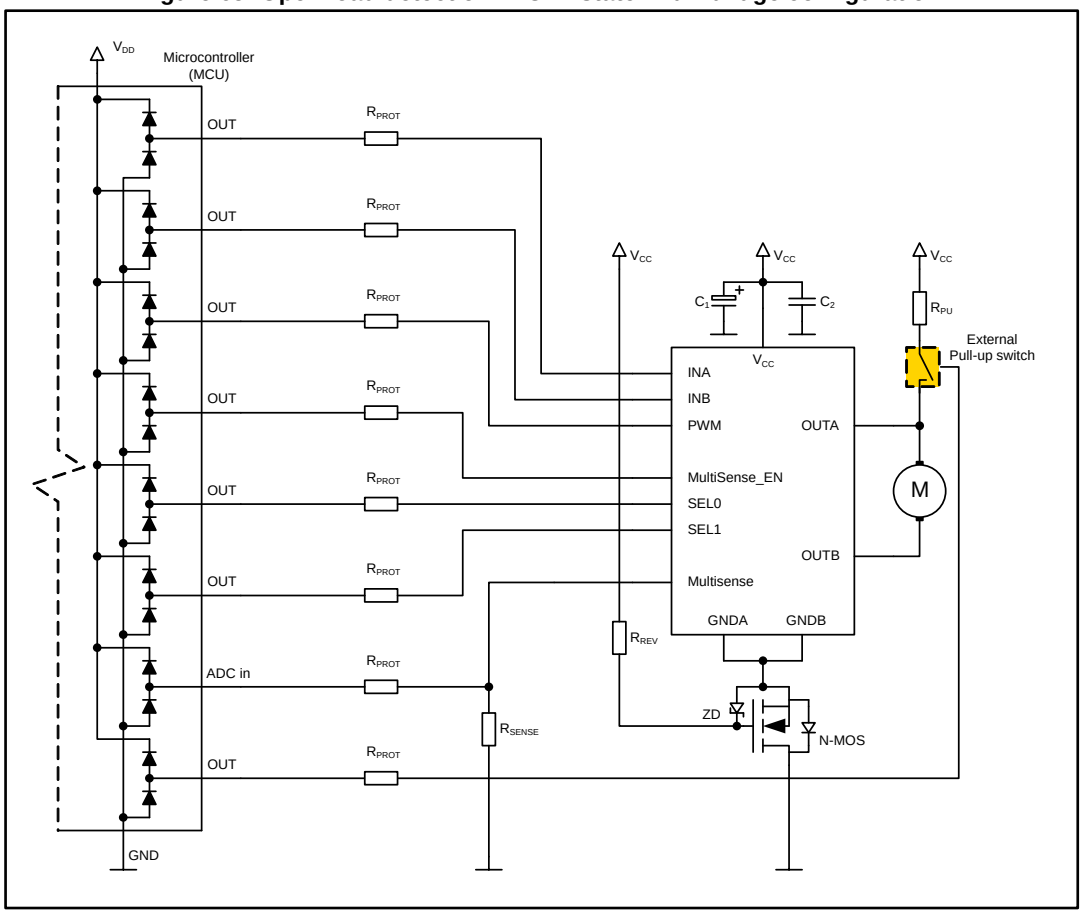
Figure 64: MultiSense for OUTB OFF-state diagnostic – half-bridge configuration



5.1.11.2 Full-bridge design considerations

The typical configuration for open load detection in full bridge topology is illustrated below.

Figure 65: Open load detection in OFF state – full-bridge configuration

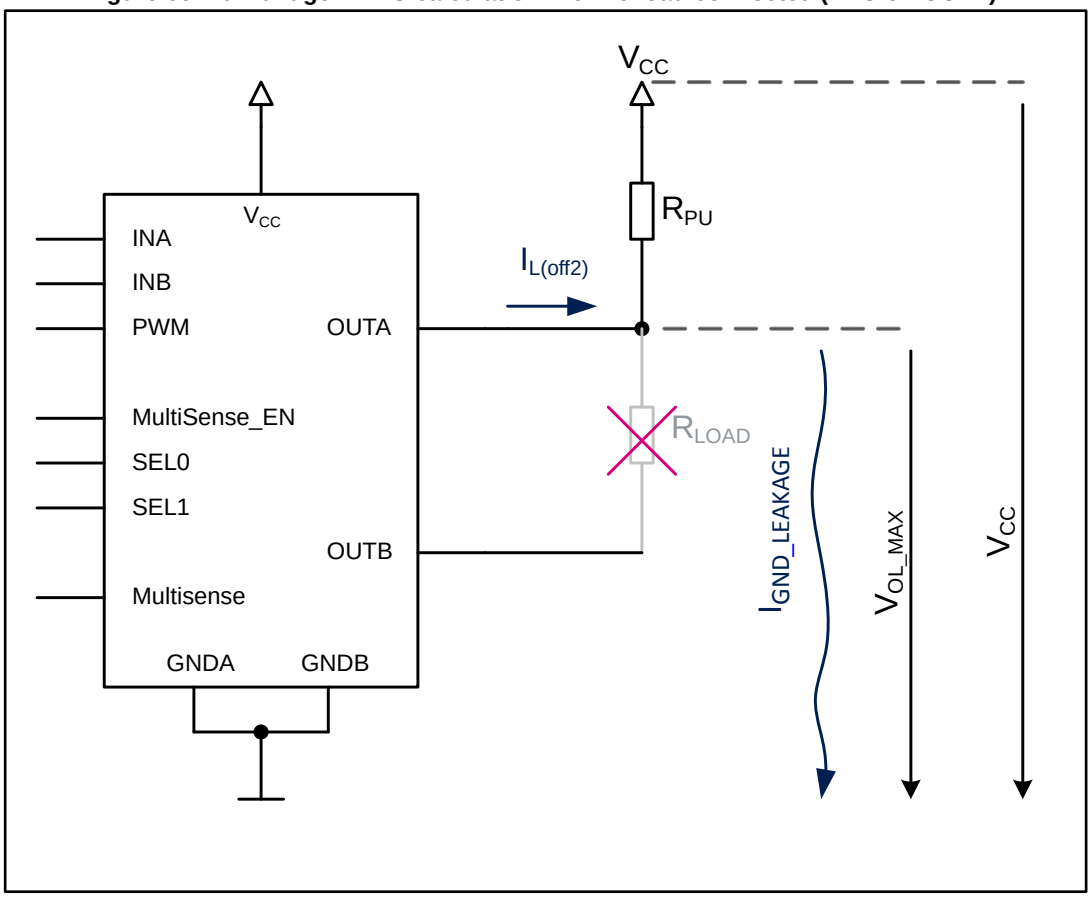


Full-bridge – maximum RPU during open load

For maximum R_{PU} calculation, the same equations for the half-bridge configuration apply.

The switchable resistor R_{PU} must ensure $V_{OUT} > V_{OL\_MAX}$ (value in datasheet), considering maximum leakage current for V_{OL_MAX}, as well as additional leakage current flowing to GND (e.g., due to humidity).

Figure 66: Full-bridge – RPU calculation with no load connected (RPU on OUTA)



Resistor R_{PU} connected to V_{BAT} supply results in:

Equation 53

$$R_{PU} < \frac{V_{BAT} - V_{OL\_MAX}}{I_{GND\_LEAKAGE} - I_{L(off2)\_MIN}}$$

Considering:

- V_{BAT} = 7 V
- $I_{GND\_LEAKAGE}$ = 0
- $I_{L(off)}$ = -100 µA – (OFF state output sink current – datasheet value)

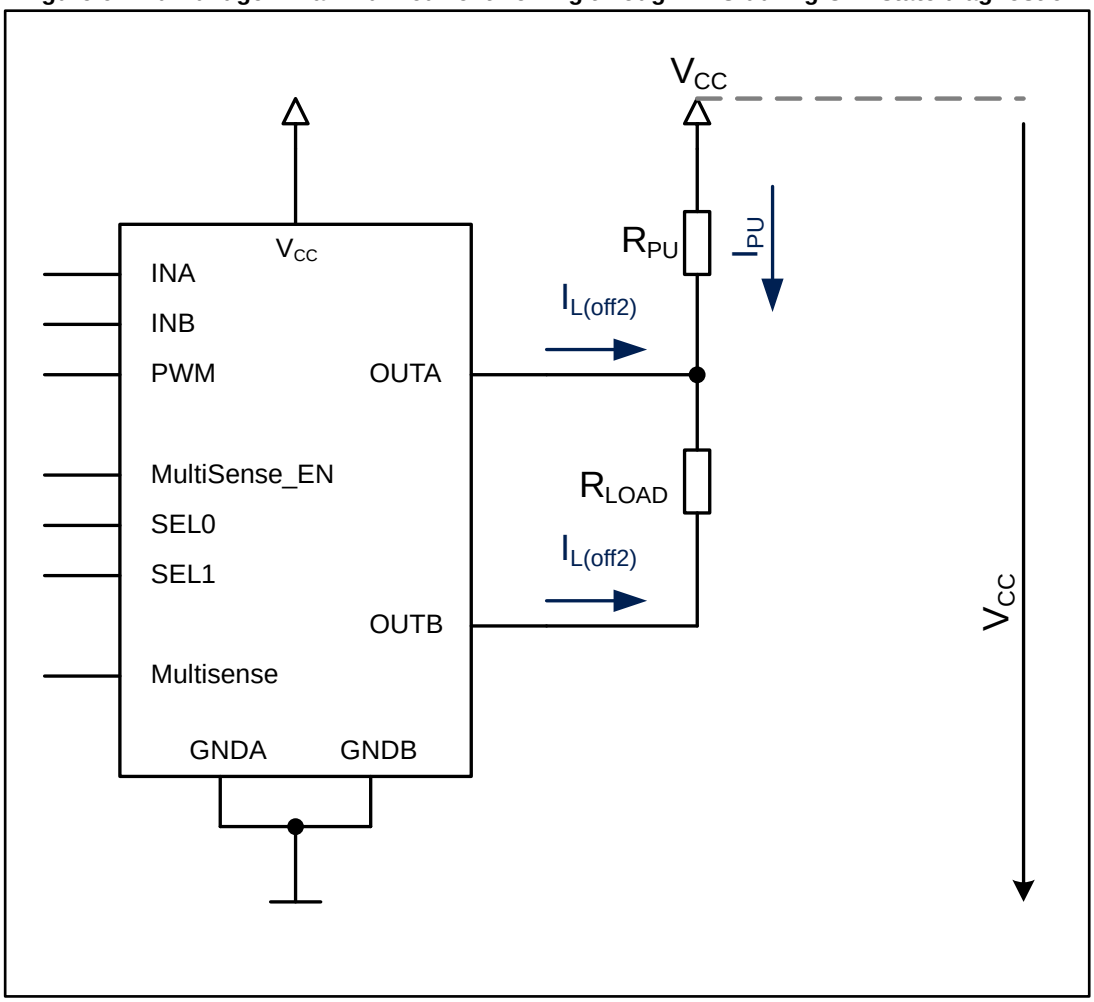
$$R_{PU} < \frac{7V - 4V}{100\mu A} = 30k\Omega$$

Hence for V_{BAT} = 7 V, R_{PU} should be less than 30 kΩ to detect an open load in the OFF state.

Full bridge - minimum RPU (only for switched pull up activated during LS active)

There is no specific minimum R_{PU} for OFF state open load detection; as both outputs are in the OFF state (HS and LS are off by INA = INB = PWM = L), the maximum current through the resistor is given by the OFF state output sink current from both outputs.

Figure 67: Full bridge – maximum current flowing through RPU during OFF state diagnostic



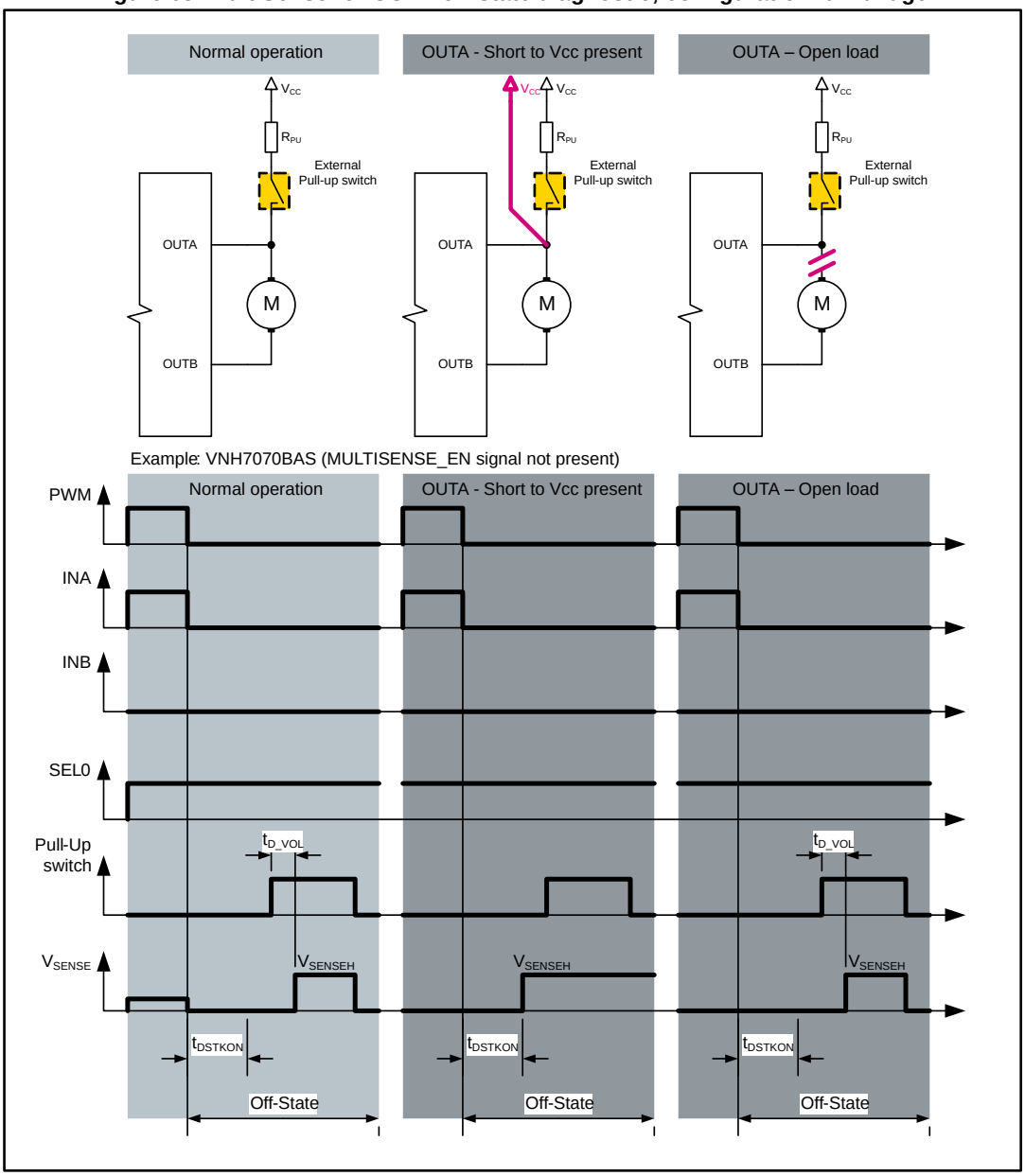
Attention is required in cases where the switched pull-up resistor would be activated during low side ON state (depicted as LS of OUTA); the maximum power dissipation must not be exceeded.

$$R_{PU} > \frac{P_{PU}}{Vcc}$$

An open load or short-circuit to V_{CC} can therefore be detected by checking the V_{SENSE} output during activated/inactivated external pull up switch.

The following figures depict particular cases applying OFF state diagnostics on OUTA with external pull-up switch.

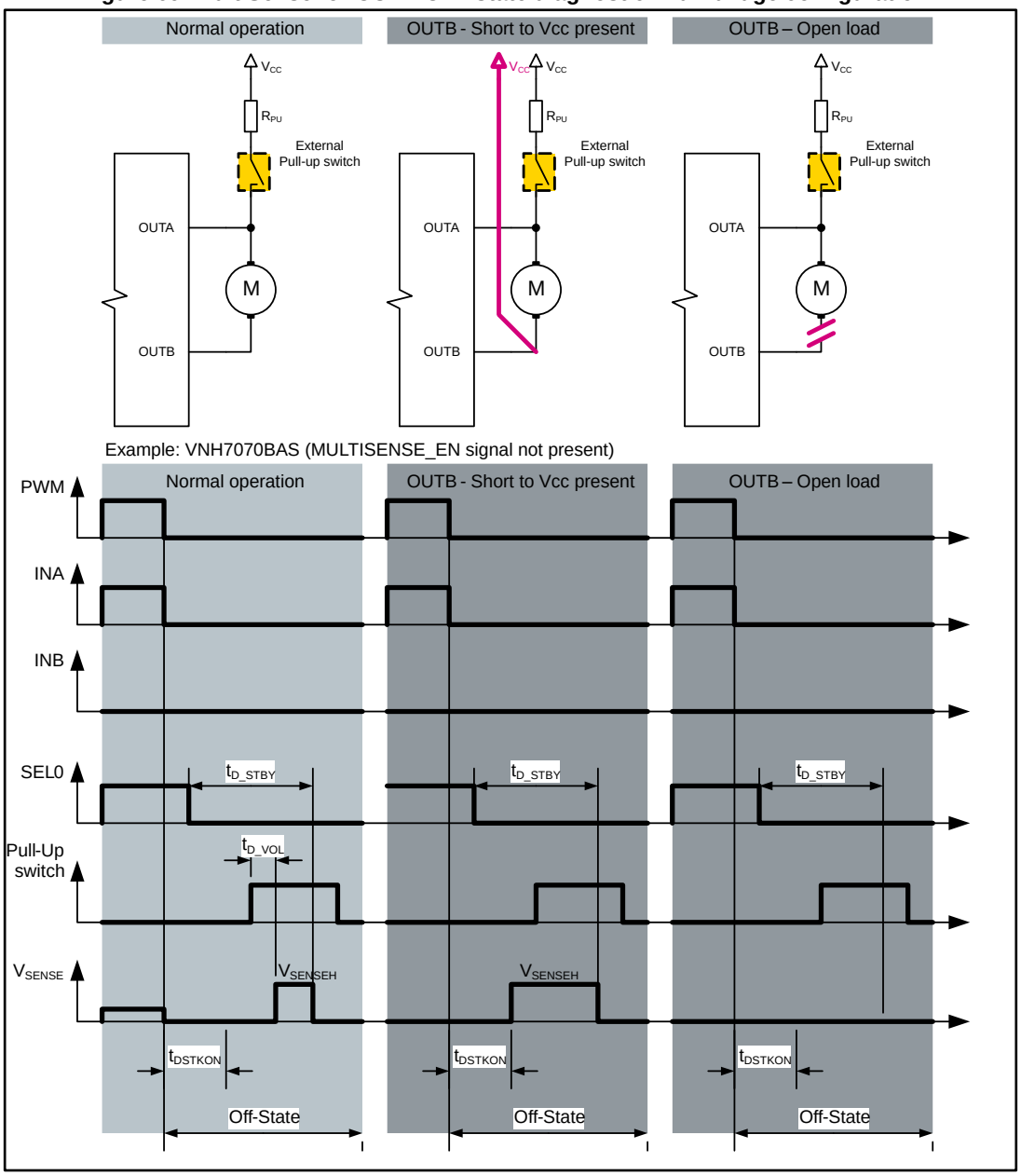
Figure 68: MultiSense for OUTA off-state diagnostic; configuration full-bridge



From the configuration where R_{PU} is connected to the same diagnosed leg depicted in the figure above, it is clearly not possible to distinguish normal operation from open load in the OFF state. It is therefore more efficient to apply V_{SENSE} reading on the output opposite to the external R_{PU}, as figured below.

For OFF state diagnostic on OUTB, take in account that if all control pins are set to low, the device enters standby mode after t_{D_STBY}. To apply diagnostics OUTB sampling of MultiSense output on VNH7070AS, VNH7070BAS, VNH7100AS, VNH7100BAS, MultiSense reading has to be applied within t_{D_STBY} after SEL0 is set low.

Figure 69: MultiSense for OUTB OFF state diagnostic – full bridge configuration



5.1.12 Summary of failure conditions

5.1.12.1 Diagnostic summary for half bridge configurations

5.1.12.1.1 Half bridge configuration in active state

Table 6: Half bridge configuration in active state - normal operation

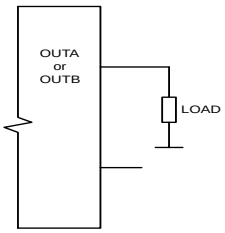
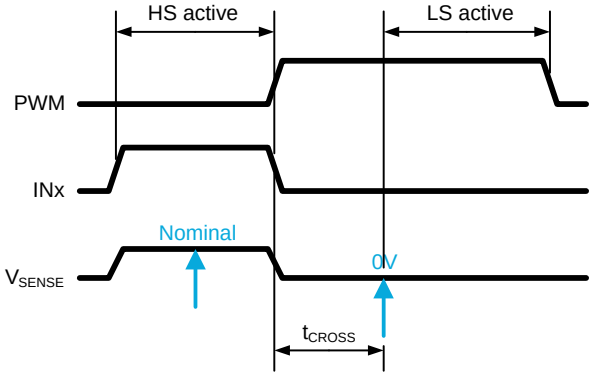
Condition	Signal	Value H = high side active L= low side active	
	IN_A or IN_B	H	L
	PWM	L	H
	Waveform sampling		
	V_{SENSE}	Nominal	0 V
	Notes	Delay time from falling edge of IN pin until LSx is activated must be considered (t_{CROSS}). SEL0 = L - monitor HSB (Load on OUTB) SEL0 = H - monitor HSA (Load on OUTA)	

Table 7: Half bridge configuration in active state - open load

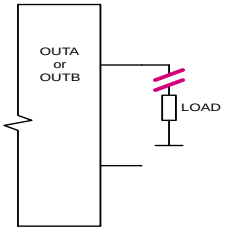
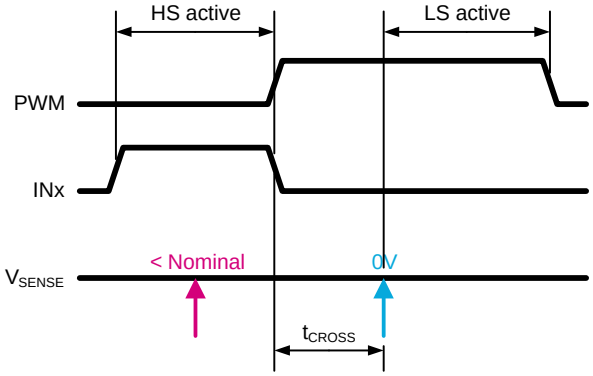
Condition	Signal	Value H = high side active L= low side active	
	IN_A or IN_B	H	L
	PWM	L	H
	Waveform sampling		
	V_{SENSE}	< Nominal	0 V
	Notes	Delay time from falling edge of IN pin until LSx is activated must be considered (t_{CROSS}). SEL0 = L - monitor HSB (Load on OUTB) SEL0 = H - monitor HSA (Load on OUTA)	

Table 8: Half bridge configuration in active state - short to VBAT

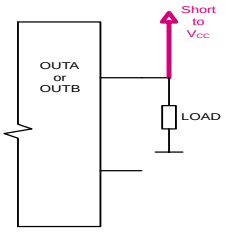
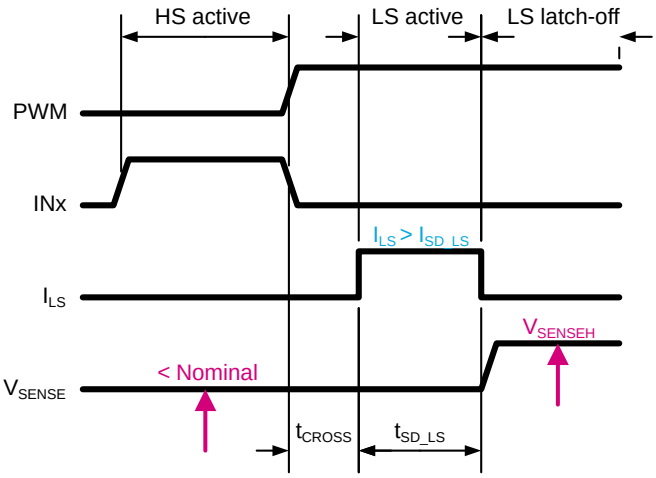
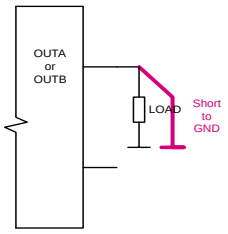
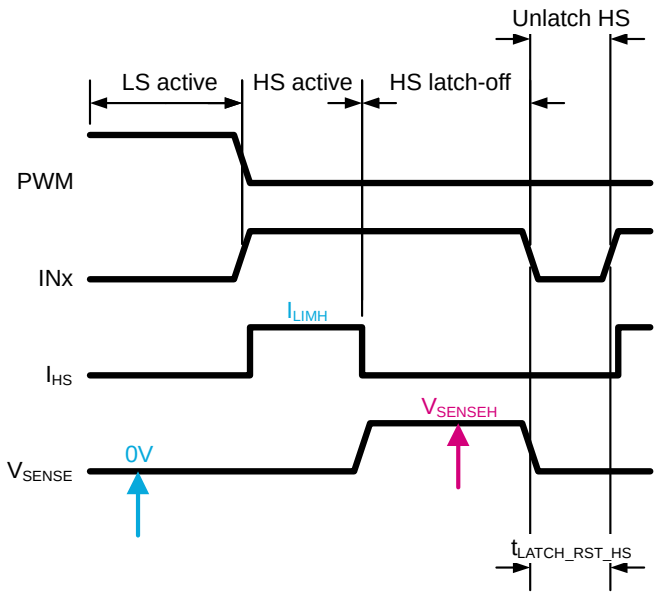
Condition	Signal	Value H = high side active L= low side active	
	IN_A or IN_B	H	L
	PWM	L	H
	Waveform sampling		
	V_{SENSE}	< Nominal	V_{SENSEH}
	Notes	Delay time from falling edge of IN pin and time to shut down output in overcurrent condition must be considered (t_{CROSS} and t_{SD_LS}). SEL0 = L - monitor LSB fault (Fault on OUTB) SEL0 = H - monitor LSA fault (Fault on OUTA)	
	IN_A or IN_B	L (Low side active)	H (High side active)
	PWM	H	L

Table 9: Half bridge configuration in active state - short to GND

Condition	Signal	Value H = high side active L= low side active	
	IN_A or IN_B	H	L
	PWM	L	H
	Waveform sampling		
	V_{SENSE}	0 V	V_{SENSEH}
	Notes	Current sense delay response time from rising edge of IN pin must be considered respectively trip time to power limitation/overtemperature shutdown whatever is longer. Output latched-off after the first intervention of power limitation or thermal shutdown. Output can be unlatched by a low level pulse on the IN pin ($t_{PULSE} > t_{LATCH\_RST\_HS}$).	

5.1.12.1.2 Half bridge configuration in OFF state

Table 10: Half bridge configuration in OFF state - normal operation

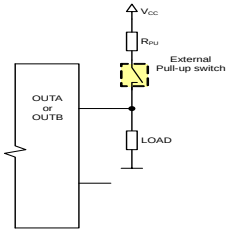
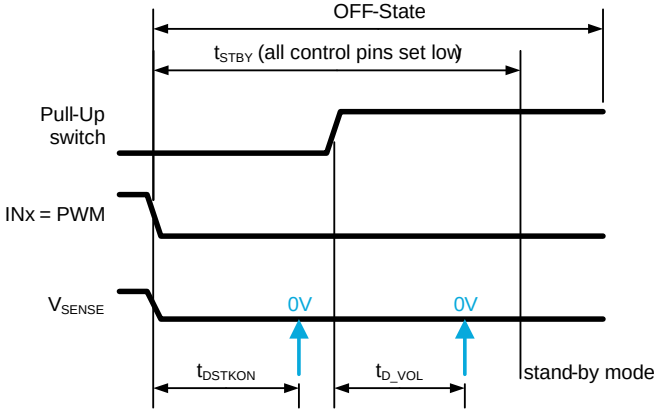
Condition	Signal	Value H = high side active L= low side active	
	IN_A or IN_B, PWM	L	L
	Pull-up switch	INACTIVE	ACTIVE
	Waveform sampling		
	V_{SENSE}	0 V	0 V
	Notes	t_{DSTKON} - delay time from falling edge of IN pin must be considered before sampling in off state t_{D_VOL} - OFF-state diagnostic delay time from rising edge of VOUT must be considered before sampling in off state with activated Pull-Up switch. By design the $t_{DSTBY} > t_{DSTKON} + t_{D\_VOL}$	

Table 11: Half bridge configuration in OFF state - open load

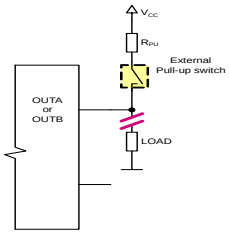
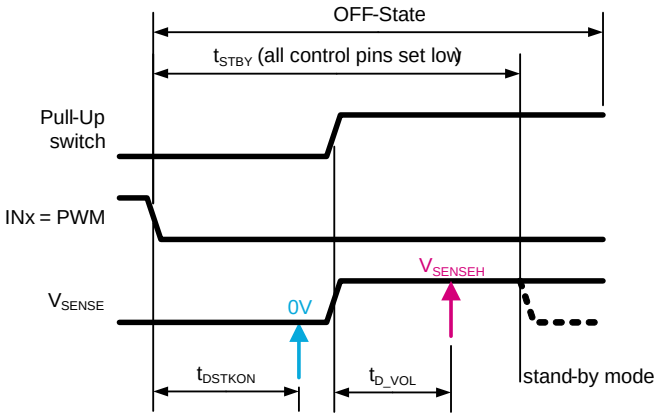
Condition	Signal	Value H = high side active L= low side active	
	IN_A or IN_B, PWM	L	L
	Pull-up switch	INACTIVE	ACTIVE
	Waveform sampling		
	V_{SENSE}	0 V	V_{SENSEH}
	Notes	t_{DSTKON} - delay time from falling edge of IN pin must be considered before sampling in off state t_{D_VOL} - OFF-state diagnostic delay time from rising edge of VOUT must be considered before sampling in off state with activated Pull-Up switch. By design the $t_{DSTBY} > t_{DSTKON} + t_{D\_VOL}$	

Table 12: Half bridge configuration in OFF state - short to VBAT

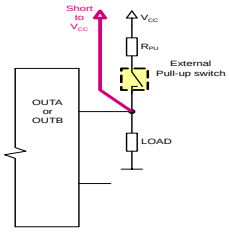
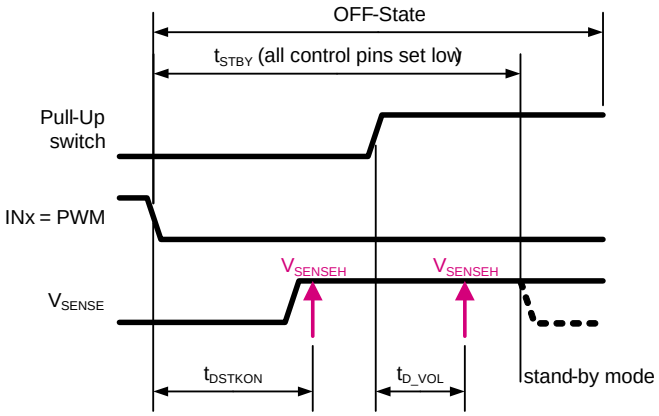
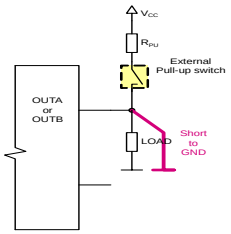
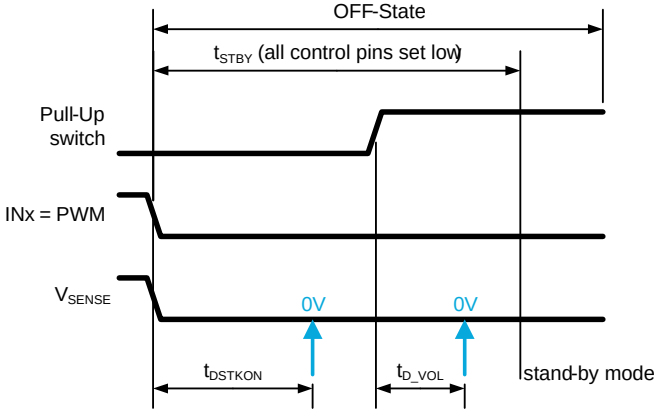
Condition	Signal	Value H = high side active L= low side active	
	IN_A or IN_B, PWM	L	L
	Pull-up switch	INACTIVE	ACTIVE
	Waveform sampling		
	V_{SENSE}	V_{SENSEH}	V_{SENSEH}
	Notes	t_{DSTKON} - delay time from falling edge of IN pin must be considered before sampling in off state t_{D_VOL} - OFF-state diagnostic delay time from rising edge of VOUT must be considered before sampling in off state with activated Pull-Up switch. By design the $t_{DSTBY} > t_{DSTKON} + t_{D\_VOL}$	

Table 13: Half bridge configuration in OFF state - short to ground

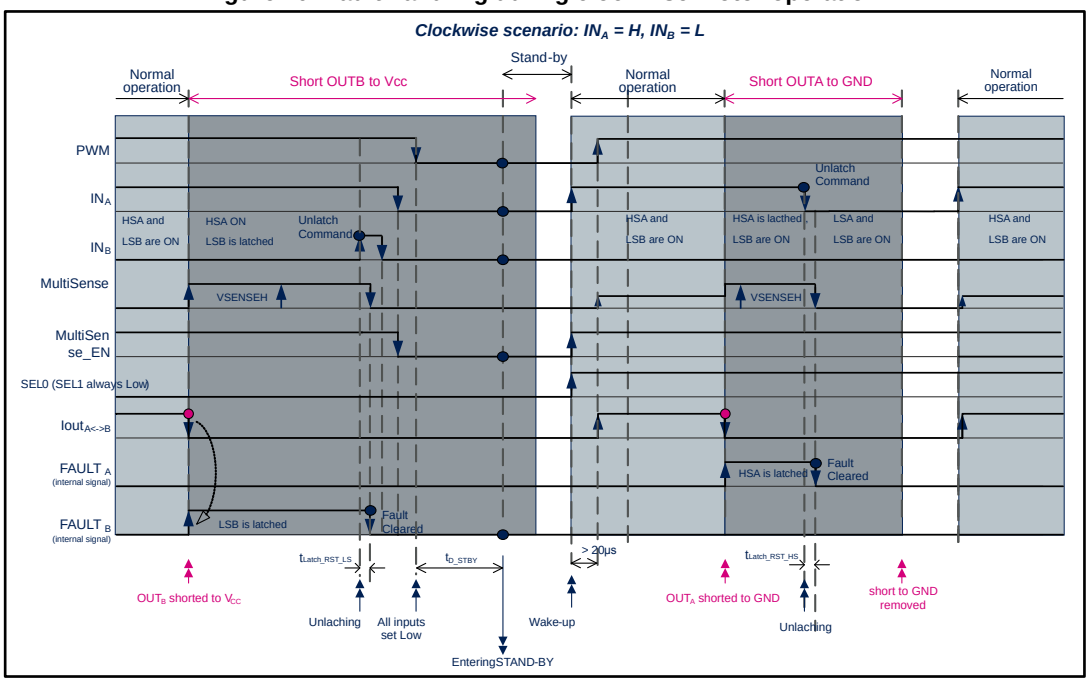
Condition	Signal	Value H = high side active L= low side active	
	IN_A or IN_B, PWM	L	L
	Pull-up switch	INACTIVE	ACTIVE
	Waveform sampling		
	V_{SENSE}	0 V	0 V
	Notes	t_{DSTKON} - delay time from falling edge of IN pin must be considered before sampling in off state t_{D_VOL} - OFF-state diagnostic delay time from rising edge of VOUT must be considered before sampling in off state with activated Pull-Up switch. By design the $t_{DSTBY} > t_{DSTKON} + t_{D\_VOL}$ Off-state diagnostic in half-bridge configuration is not capable to detect short to GND As the sampled data of V_{SENSE} are similar to normal operation (without failure).	

To perform the open load diagnostic with H-bridges with no MultiSense_EN pin, ensure the device does not enter STDBY mode. T_{DSTKON} is defined as the minimum delay time in which the IN_A and IN_B pins are set to low (considering that PWM is already low) and the device can give a valid indication of the OL detection. It is suggested to start the OFF state OL detection by keeping SEL0=H (reading of OUTA status) after the maximum T_{DSTKON} given in the datasheet, then perform the OL detection task of OUTB by setting SEL0=L. The OL detection of OUTB (setting SEL0 from H to L) must be performed within T_{D_STBY} minimum value as per datasheet.

5.1.12.2 Diagnostic summary for full bridge configurations

Fault handling in full bridge configuration is depicted below with time sequences during normal operation, short-circuit on OUTB to VCC, entering and exiting standby mode, short of OUTA to GND and returning to normal operation.

Figure 70: Fault handling during clockwise motor operation



5.1.12.2.1 Full bridge configuration in active state

Table 14: Full bridge configuration in active state - normal operation

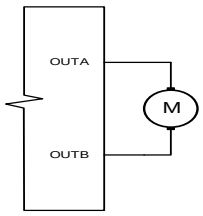
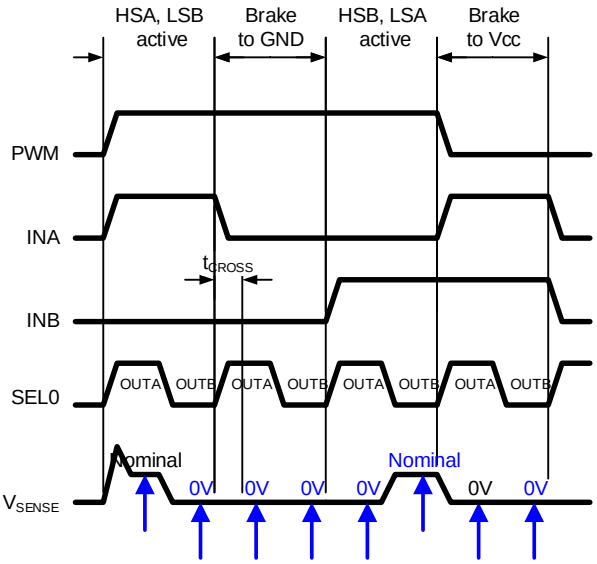
Condition	Signal	SEL0 = H	SEL0 = L
	Waveform sampling		
HSA,LSB active	V_{SENSE}	Nominal	0 V
	Notes	No error detected over the V_{SENSE}	
Brake to GND (LSA, LSB active)	V_{SENSE}	0 V	0 V
	Notes	No error detected over the V_{SENSE}	
HSB,LSA active	V_{SENSE}	0 V	Nominal
	Notes	No error detected over the V_{SENSE}	
Brake to Vcc	V_{SENSE}	0 V	0 V
	Notes	No error detected over the V_{SENSE}	

Table 15: Full bridge configuration in active state - open load

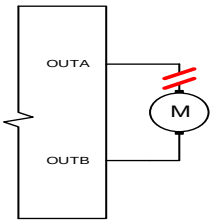
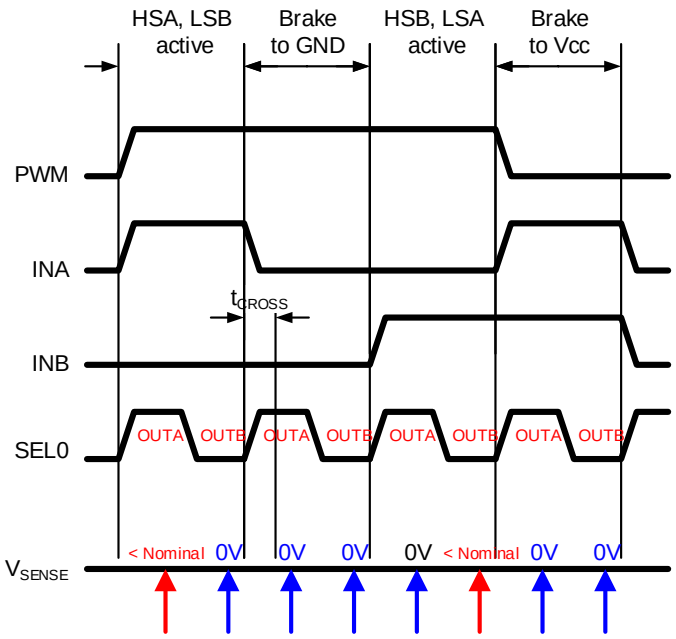
Condition	Signal	SEL0 = H	SEL0 = L
	Waveform sampling		
HSA,LSB active	V_{SENSE}	< Nominal	0 V
	Notes	Error is detectable by MultiSense configured to OUTA, where VSENSE output < Nominal	
Brake to GND (LSA, LSB active)	V_{SENSE}	0 V	0 V
	Notes	No error detected over the V_{SENSE}	
HSB, LSA active	V_{SENSE}	0 V	< Nominal
	Notes	Error is detectable by MultiSense configured to OUTB, where VSENSE output < Nominal	
Brake to Vcc	V_{SENSE}	0 V	0 V
	Notes	No error detected over the V_{SENSE}	

Table 16: Full bridge configuration in active state - Short-circuit to Vcc on OUTA

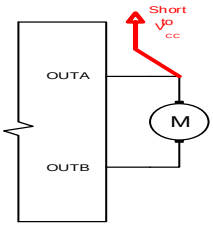
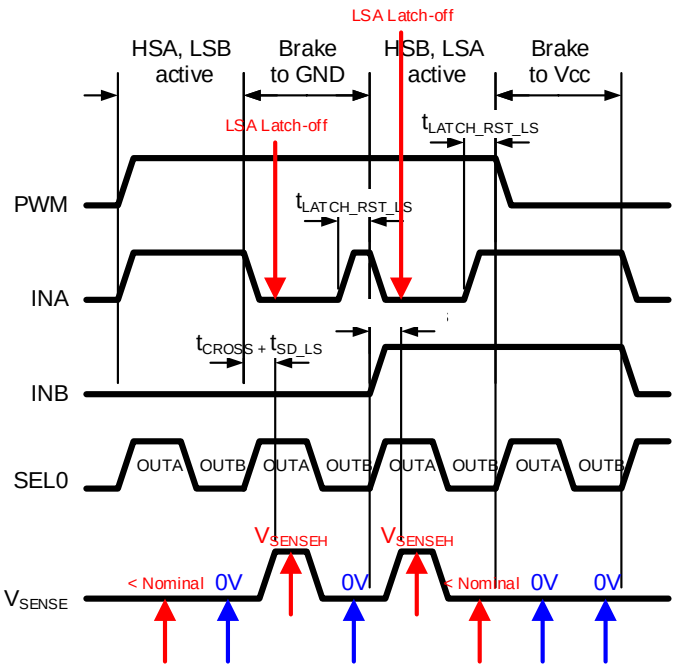
Condition	Signal	SEL0 = H	SEL0 = L
	Waveform sampling		
HSA,LSB active	V_{SENSE}	< Nominal	0 V
	Notes	Error is detectable by MultiSense configured to OUTA, where VSENSE output < Nominal	
Brake to GND (LSA, LSB active)	V_{SENSE}	V_{SENSEH}	0 V
	Notes	Delay time from falling edge of INA pin and time to shut down output in overcurrent condition must be considered (t_{CROSS} and t_{SD_LS}). LSA output latched-off after the overcurrent condition can be unlatched by a high level pulse on the INA pin (t_{PULSE} > $t_{LATCH\_RST\_LS}$). A side effect of LSA latched-off during braking to GND causes motor activation through short circuit on OUTA and active LSB	
HSB,LSA active	V_{SENSE}	V_{SENSEH}	< Nominal
	Notes	Delay time from falling edge of INA pin and time to shut down output in overcurrent condition must be considered (t_{CROSS} and t_{SD_LS}). LS output latched-off after the overcurrent condition can be unlatched by a high level pulse on the INA pin (t_{PULSE} > $t_{LATCH\_RST\_LS}$). LSA output latched-off after the overcurrent condition. The motor is braked to Vcc through the short on OUTA and active HSB.	
Brake to Vcc	V_{SENSE}	0 V	0 V
	Notes	Operation correct, no error detected over the V_{SENSE}	

Table 17: Full bridge configuration in active state - short-circuit to Vcc on OUTB

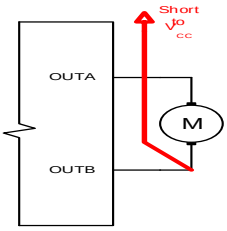
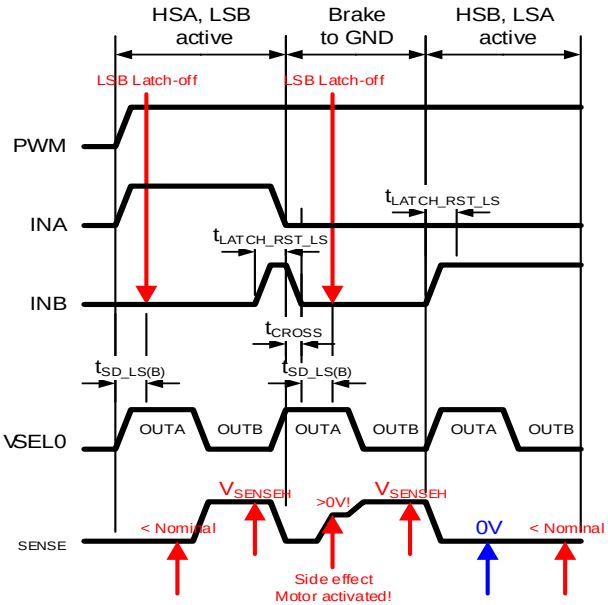
Condition	Signal	SEL0 = H	SEL0 = L
	Waveform sampling		
HSA,LSB active	V_{SENSE}	< Nominal	V_{SENSEH}
	Notes	Delay time from rising edge of PWM pin and time to shut down output in overcurrent condition must be considered (t_{SD_LS}) LSB output latched-off after the overcurrent condition can be unlatched by a high level pulse on the INB pin (t_{PULSE} > $t_{LATCH\_RST\_LS}$).	
Brake to GND (LSA, LSB active)	V_{SENSE}	>0 V	V_{SENSEH}
	Notes	Delay time from falling edge of INB pin and time to shut down output in overcurrent condition must be considered (t_{CROSS} and t_{SD_LS}). A side effect of LSB latched-off during braking to GND causes motor activation through short-circuit on OUTB and active LSA. Motor remains active until condition is detected by V_{SENSEH} on MultiSense pin configured to sense OUTB. LS output latched-off after the overcurrent condition can be unlatched by a high level pulse on the INB pin (t_{PULSE} > $t_{LATCH\_RST\_LS}$).	
HSB,LSA active	V_{SENSE}	0 V	< Nominal
	Notes	Error is detectable by MultiSense configured to OUTB, where VSENSE output < Nominal	
Brake to Vcc (not depicted on illustration)	V_{SENSE}	0 V	0 V
	Notes	Operation correct, no error detected over the V_{SENSE}	

Table 18: Full bridge configuration in active state - short-circuit to GND on OUTA

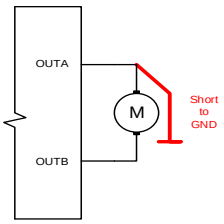
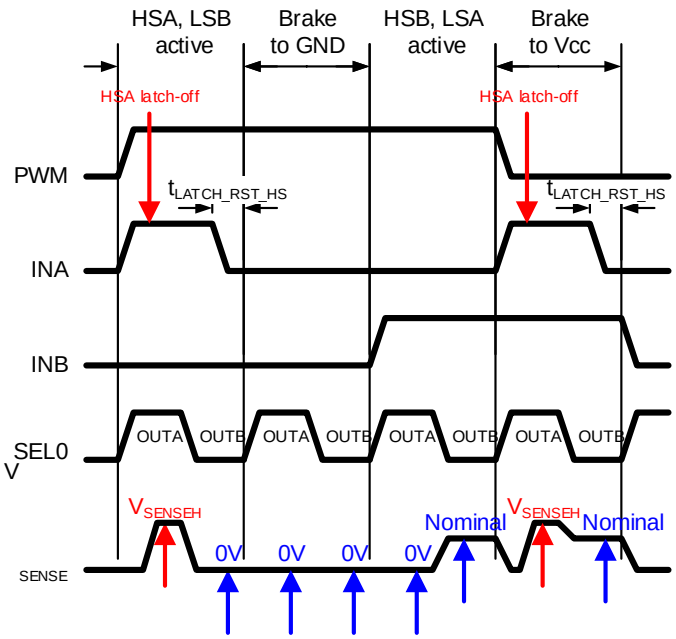
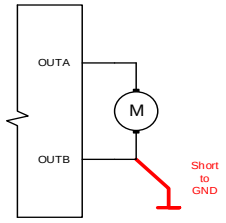
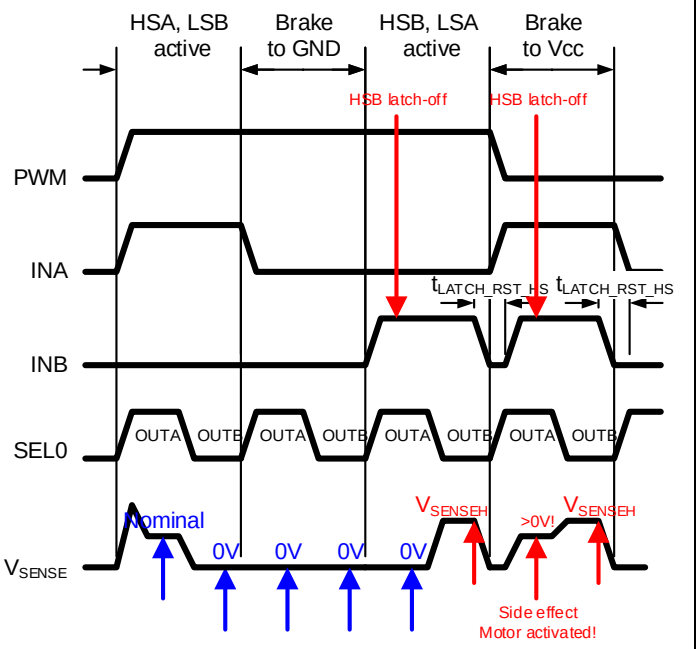
Condition	Signal	SEL0 = H	SEL0 = L
	Waveform sampling		
HSA,LSB active	V_{SENSE}	V_{SENSEH}	0 V
	Notes	Current sense delay response time from rising edge of IN pin must be considered respectively trip time to PowerLimitation/Overtemperature shutdown whatever is longer. Due to condition short to GND on the OUTA, the output voltage on OUTA is $V_{OUT} < V_{MSD}$. Consequentlythe V_{SENSE} output reports high-Z condition, until output is latched-off and V_{SENSEH} is reported. Output latched-off after the first intervention of power limitation or thermal shutdown. Output can be unlatched by a low level pulse on the INA pin ($t_{PULSE} > t_{LATCH\_RST\_HS}$).	
Brake to GND (LSA, LSB active)	V_{SENSE}	0 V	0 V
	Notes	Operation correct, no error detected over the V_{SENSE}	
HSB,LSA active	V_{SENSE}	0 V	Nominal
	Notes	Operation correct, no error detected over the V_{SENSE}	
Brake to Vcc	V_{SENSE}	V_{SENSEH}	0 V
	Notes	Current sense delay response time from rising edge of IN pin must be considered respectively trip time to PowerLimitation/Overtemperature shutdown whatever is longer. Output latched-off after the first intervention of power limitation or thermal shutdown. Output can be unlatched by a low level pulse on the INA pin ($t_{PULSE} > t_{LATCH\_RST\_HS}$). A side effect of HSA latched-off during braking to Vcc causes motor activation through short circuit on OUTA and active LSB. The condition is detected by Vsense>0 when reading OUTB Remark: In case of VNH7070AS and VNH7100AS the Vsense = High Z	

Table 19: Full bridge configuration in active state - short-circuit to GND on OUTB

Condition	Signal	SEL0 = H	SEL0 = L
	Waveform sampling		
HSA,LSB active	V_{SENSE}	Nominal	0 V
	Notes	Operation correct, no error detected over the V_{SENSE}	
Brake to GND (LSA, LSB active)	V_{SENSE}	0 V	0 V
	Notes	Operation correct, no error detected over the V_{SENSE}	
HSB,LSA active	V_{SENSE}	0 V	V_{SENSEH}
	Notes	Current sense delay response time from rising edge of IN pin must be considered respectively trip time to PowerLimitation/Overtemperature shutdown whatever is longer. Output latched-off after the first intervention of power limitation or thermal shutdown. Output can be unlatched by a low level pulse on the INB pin ($t_{PULSE} > t_{LATCH\_RST\_HS}$).	
Brake to Vcc	V_{SENSE}	>0 V	V_{SENSEH}
	Notes	Current sense delay response time from rising edge of IN pin must be considered respectively trip time to PowerLimitation/Overtemperature shutdown whatever is longer. A side effect of HSB latched-off during braking to GND causes motor activation through short-circuit on OUTB and activated HSA. Motor remains active until condition is detected by V_{SENSEH} on MultiSense pin configured to sense OUTB. Output latched-off after the first intervention of power limitation or thermal shutdown can be unlatched by a low level pulse on the INB pin ($t_{PULSE} > t_{LATCH\_RST\_HS}$).	

5.1.12.2.2 Full bridge configuration in OFF state

Table 20: Full bridge configuration in OFF state - normal operation

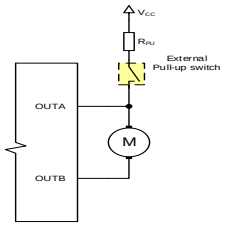
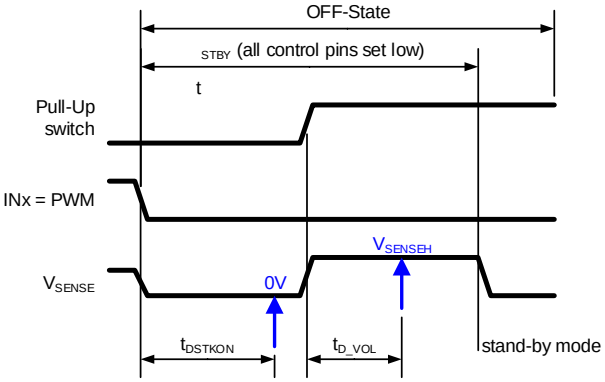
Condition	Signal	Value	
	IN_A = IN_B = PWM	L	
	Pull-up switch	INACTIVE	ACTIVE
	Waveform sampling		
	V_{SENSE}	0 V	V_{SENSEH}
	Notes	t_{DSTKON} - delay time from falling edge of IN pin must be considered before sampling in off state t_{D_VOL} - OFF-state diagnostic delay time from rising edge of VOUT must be considered before sampling in off state with activated Pull-Up switch. When all control pins are set low, t_{DSTBY} must be taken in account too, because device enters standby mode after t_{DSTBY} and V_{SENSE} output gets inactive.	

Table 21: Full bridge configuration in OFF state - open load

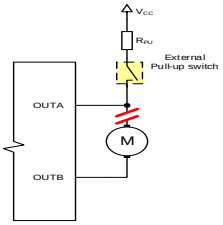
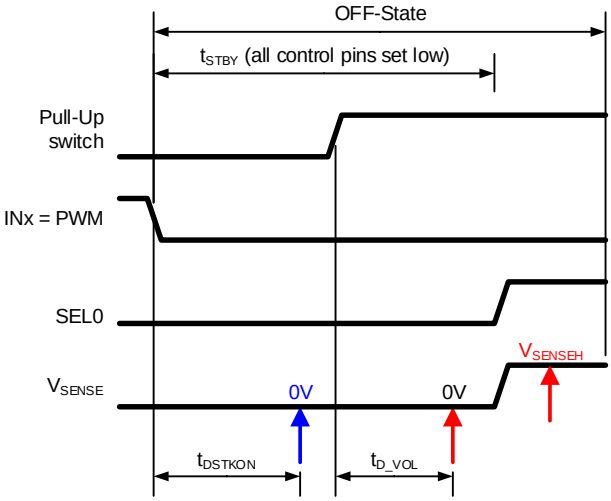
Condition	Signal	Value	
	$IN_A = IN_B$ = PWM	L	
	Pull-up switch	INACTIVE	ACTIVE
	Waveform sampling		
	V_{SENSE}	0 V	SEL0 = L → V_{SENSE} = 0V SEL0 = H → V_{SENSE} = V_{SENSEH}
	Notes	t_{DSTKON} - delay time from falling edge of IN pin must be considered before sampling in off state t_{D_VOL} - OFF-state diagnostic delay time from rising edge of VOUT must be considered before sampling in off state with activated Pull-Up switch. When all control pins are set low, t_{DSTBY} must be taken in account too, because device enters standby mode after t_{DSTBY} and V_{SENSE} output gets inactive.	

Table 22: Full bridge configuration in OFF state - short-circuit to VBAT

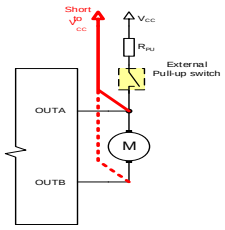
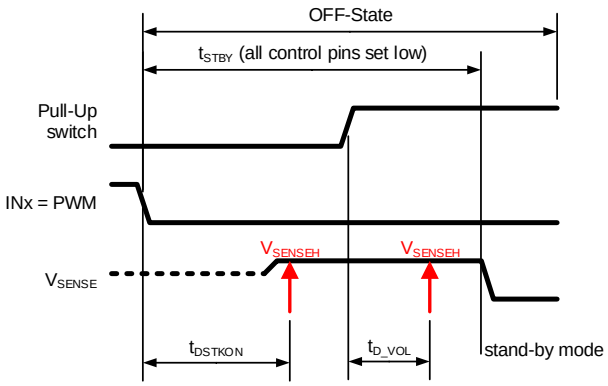
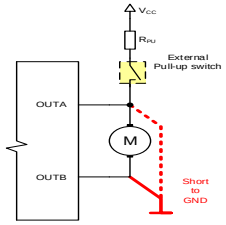
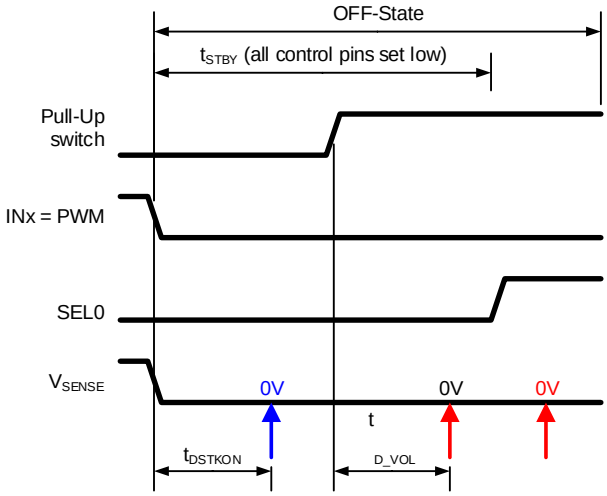
Condition	Signal	Value	
	IN_A = IN_B = PWM	L	
	Pull-up switch	INACTIVE	ACTIVE
	Waveform sampling		
	V_{SENSE}	V_{SENSEH}	V_{SENSEH}
	Notes	t_{DSTKON} - delay time from falling edge of IN pin must be considered before sampling in off state t_{D_VOL} - OFF-state diagnostic delay time from rising edge of VOUT must be considered before sampling in off state with activated Pull-Up switch. When all control pins are set low, t_{DSTBY} must be taken in account too, because device enters standby mode after t_{DSTBY} and V_{SENSE} output gets inactive.	

Table 23: Full bridge configuration in OFF state - short-circuit to GND

Condition	Signal	Value	
	IN_A = IN_B = PWM	L	
	Pull-up switch	INACTIVE	ACTIVE
	Waveform sampling		
	V_{SENSE}	0 V	SEL0 = L → V_{SENSE} = 0V SEL0 = H → V_{SENSE} = 0V
	Notes	t_{DSTKON} - delay time from falling edge of IN pin must be considered before sampling in off state t_{D_VOL} - OFF-state diagnostic delay time from rising edge of VOUT must be considered before sampling in off state with activated Pull-Up switch. When all control pins are set low, t_{DSTBY} must be taken in account too, because device enters standby mode after t_{DSTBY} and V_{SENSE} output gets inactive. Distinguishing between open load and short-circuit to GND condition can be done by sampling of V_{SENSE} for both outputs (SEL0 = L and SEL0 =H)	

5.1.13 Current sense calibration method

To increase V_{SENSE} accuracy, it is possible to reduce the K spread and eliminate the R_{SENSE} variation by adding a simple test (calibration test) at the end of the module production line.

5.1.13.1 Two point calibration method

Calibration is performed on a specific device soldered in a module forcing fixed output current and reading the V_{SENSE} to determine the K ratio below.

Equation 54

$$I_{OUT} = I_{SENSE} * K$$

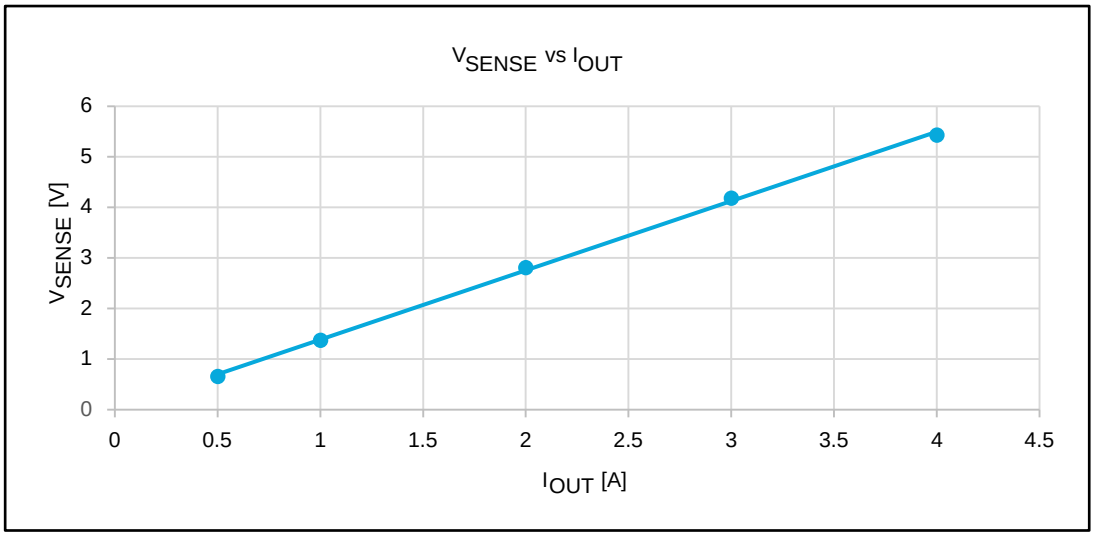
However, even if the K ratio measured in a single point eliminates the parametric spread, it doesn't eliminate the V_{SENSE} variation due to the K dependency on output current. This variation can be eliminated doing the following considerations.

Table 24: "Vsense measurements" and *Figure 71: "VSENSE vs IOUT measurement"* show V_{SENSE} measurements on a sample of VNH7070AS-E (OUTA) with R_{SENSE} = 2.2 kΩ.

Table 24: Vsense measurements

IOUT [A]	VSENSE (OUTA) [V]
0.5	0.661
1	1.376
2	2.813
3	4.189
4	5.431

Figure 71: VSENSE vs IOUT measurement



The trend is almost linear in the application range, so we can approximate the V_{SENSE} trend as:

Equation 55

$$V_{SENSE} = m * I_{OUT} + a$$

Where:

- m [Ω] is the rectangular coefficient
- a [V] is a constant

Inverting this equation it is easy to obtain a relationship in place of *Equation 53*, where the output current is calculated thus:

Equation 56

$$I_{OUT} = M * V_{SENSE} + b$$

Once M [S] and b are known, it is possible to evaluate I_{OUT} with high accuracy, leaving only the spread due to the temperature variation.

The maximum current sense ratio fluctuation is expressed in the datasheet with the parameter dK/K (maximum relative error in the full MultiSense Vcc and Tj specification range versus K at V_{CC} = 13 V and Tj = 25 °C).

5.1.13.2 Calculating M and b

To calculate M and b, two simple measurements performed at the end of the production line are required.

Fixing two reference output currents I_{REF1} and I_{REF2}, the respective V_{SENSE1} and V_{SENSE2} are measured.

These values can be stored in an EEPROM, which the microcontroller can use to calculate M and b using the following variations of *Equation 55*:

$$I_{REF1} = M * V_{SENSE1} + b$$

and

$$I_{REF2} = M * V_{SENSE2} + b$$

Solving these two equations we obtain:

Equation 57

$$M = \frac{I_{REF1} - I_{REF2}}{V_{SENSE1} - V_{SENSE2}}$$

and

$$b = \frac{I_{REF2} * V_{SENSE1} - I_{REF1} * V_{SENSE2}}{V_{SENSE1} - V_{SENSE2}}$$

5.1.13.3 Calculation example

From *Table 24: "Vsense measurements"*:

- For I_{REF1} = 1 A → V_{SENSE1} = 1.376 V and
- For I_{REF2} = 3 A → V_{SENSE2} = 4.189 V

Hence:

M = 0.711 [S]

b = 0.0217 [A]

Therefore:

$$I_{OUT} = 0.711 * V_{SENSE} + 0.0217$$

A simple algorithm can determine the values of M and b. During the EOL, the (V_{SENSE1}, I_{REF1}) and (V_{SENSE2}, I_{REF2}) pairs, or just M and b, can be stored in the microcontroller EEPROM.

Following calibration, the current sense variation is still influenced by the device temperature; the result is still affected by an error proportional to the sense current thermal drift.

This drift is given in the datasheet as dK/K and decreases with increasing output current.

For example, in the VNH7070BAS datasheet the drift is:

- ±25% at 50 mA
- ±4% at 5.5 A.

5.1.14 Paralleling of MultiSense pins with multiple H-bridges or M0-7 HSDs

The paralleling of MultiSense must take into account different device technologies (monolithic H-bridges, monolithic or hybrid HSDs) and/or supply line configurations (same or separate supply line for each H-bridge or HSD).

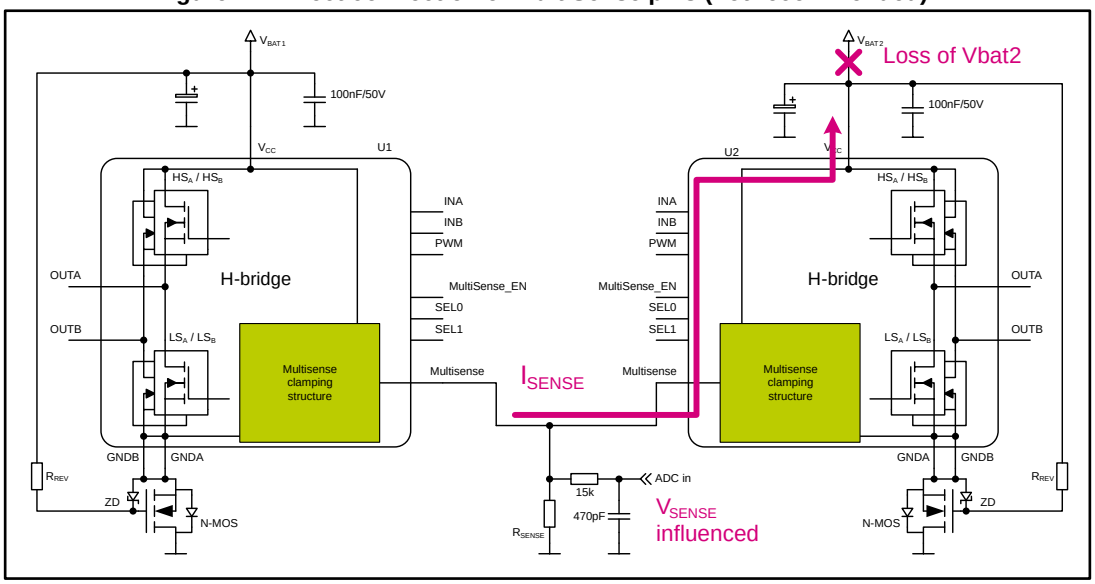
Direct connection of MultiSense pins is generally allowed when the devices are supplied from one supply line, sharing the same GND network.

In case of separate supply lines or separate GND protection networks, additional components are required to ensure safe operation under automotive conditions (ISO pulses, reverse battery, etc.).

5.1.14.1 Devices supplied from different supply lines

Paralleling of MultiSense pins of multiple H-bridges or monolithic HSDs is possible, but certain precautions are necessary if the HSDs are supplied from different supply lines.

Figure 72: Direct connection of MultiSense pins (not recommended)



The direct connection of MultiSense pins is not safe when there is:

- a negative voltage surge on V_{BAT1} or V_{BAT2}
- a positive voltage surge on V_{BAT1} or V_{BAT2} while positive pulse energy higher than the H-Bridge capability (all paralleled devices risk damage)
- the loss of VBAT1 or VBAT2

A negative voltage surge (ISO 7637-2 pulse 1, 3a) either on V_{BAT1} or V_{BAT2} is directly coupled to the MultiSense pin through the internal V_{CC}-MultiSense clamp structure. If the negative voltage on MultiSense line is big enough to activate the V_{CC}-MultiSense clamp

structure, unlimited current may flow through both MultiSense pins, leading to the malfunction or failure of one or both of the H-bridges or HSDs.

A positive voltage surge (ISO7637-2 pulse 2a, 3b) either on V_{BAT1} or V_{BAT2} together with missing GND connection can activate the V_{CC} - MultiSense clamp structure (clamp voltage similar to V_{CC} -GND clamp). If this occurs, unlimited current may flow through both MultiSense pins and cause malfunction or failure of one or both of the H-bridges or HSDs.

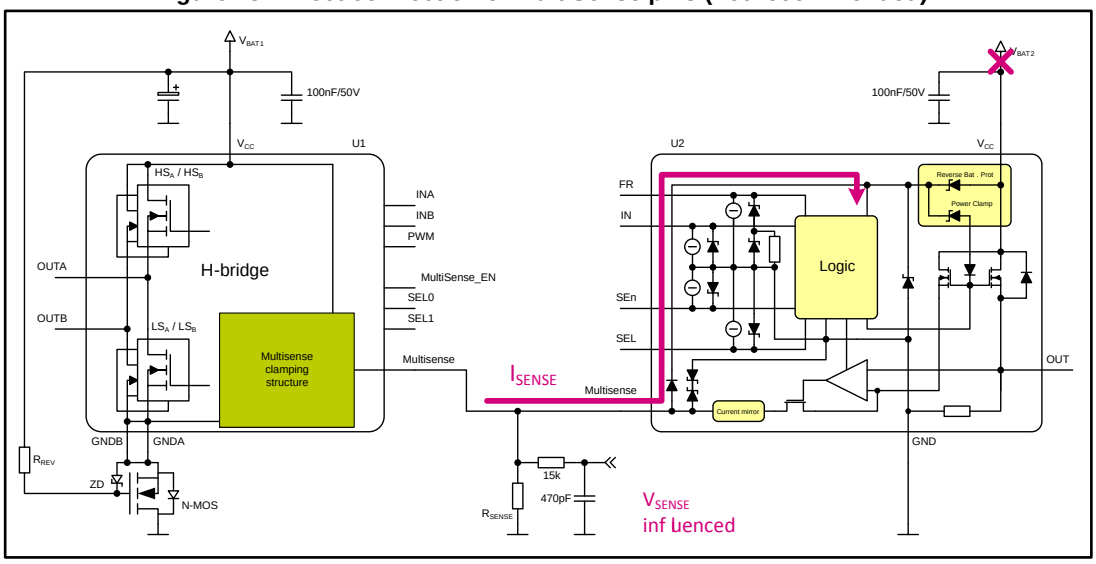
Loss of either V_{BAT1} or V_{BAT2} leads to an incorrect current sense signal. If V_{BAT2} is lost, U2 and other components connected to V_{BAT2} are supplied by U1 current sense signal through the internal V_{CC} - MultiSense clamp structure.

The voltage on MultiSense bus will therefore drop to almost 0 V and the V_{SENSE} reading will no longer be valid.

5.1.14.2 Mix of H-bridge and hybrid HSD supplied from different supply lines

Paralleling of MultiSense pins of multiple H-bridges and hybrid HSDs is possible, however certain precautions are necessary if the HSDs are supplied from different supply lines.

Figure 73: Direct connection of MultiSense pins (not recommended)



The direct connection of MultiSense pins is not safe in the event of:

- a negative ISO pulse on V_{BAT1}
- the loss of V_{BAT1} or V_{BAT2}
- the loss of GND connection

A negative voltage surge (ISO7637-2 pulse 1, 3a) on V_{BAT1} is directly coupled to the MultiSense pin through the internal V_{CC}-MultiSense clamp structure. If the negative voltage on the MultiSense line is large enough to activate the MultiSense-GND clamp structure, unlimited current could flow through both MultiSense pins and cause malfunction or even failure of one or both of the H-bridge or HSD.

Loss of V_{BAT1} or V_{BAT2} leads to the wrong current sense signal. If V_{BAT2} is lost, the U2 logic section is supplied by U1 current sense signal through the internal V_{CC} - MultiSense clamp structure. Therefore the voltage on MultiSense bus will drop and the V_{SENSE} reading will no longer be accurate.

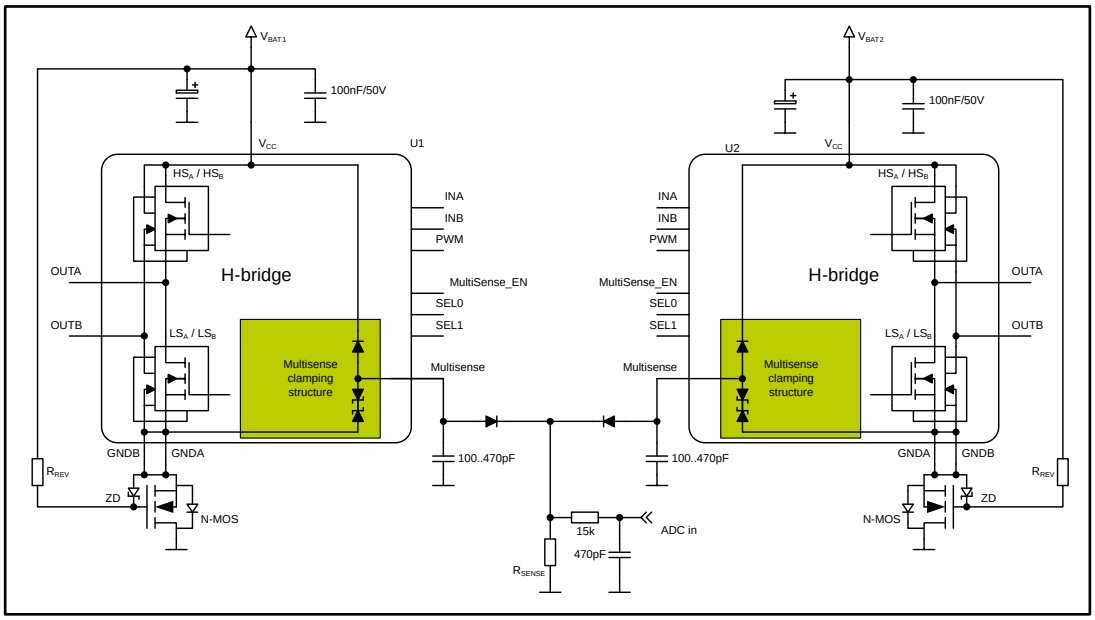
If the GND connection of one device is lost, positive as well as negative ISO pulses on the associated supply line are no longer clamped (considering no other devices connected to this supply line). If the transient voltage is large enough to activate the involved clamp

structures, unlimited current could flow between both supply lines through the MultiSense pins and cause malfunction or failure of one or both of the H-bridge or HSD.

To protect the devices during ISO pulses and ensure a valid current sense signal, we can add a diode in series to each MultiSense pin (see *Figure 74: "Safe solution for paralleling MultiSense pins"*). To suppress the rectification of noise injected in the sense line, add a ceramic filter capacitor between each CS pin and ground.

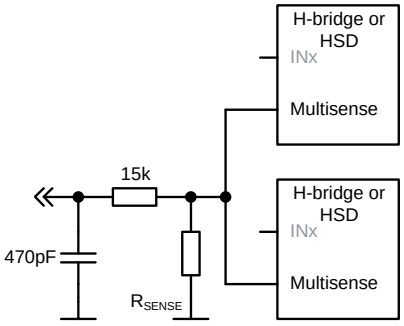
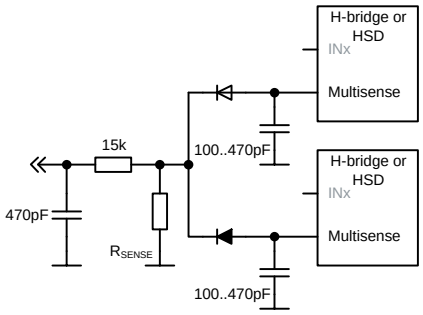
However, the voltage drop on diodes in series with MultiSense pin can have an influence on the dynamic range of current sense, temperature and current sense accuracy. There must be also taken in account voltage drop over protection diode while MultiSense output is switched in voltage mode (V_{BAT}/Temperature signal output or V_{SENSEH} fault flag).

Figure 74: Safe solution for paralleling MultiSense pins



The following table summarizes the possible combinations of HSDs with paralleled MultiSense outputs relative to the power supply network.

Table 25: Summary of MultiSense paralleling

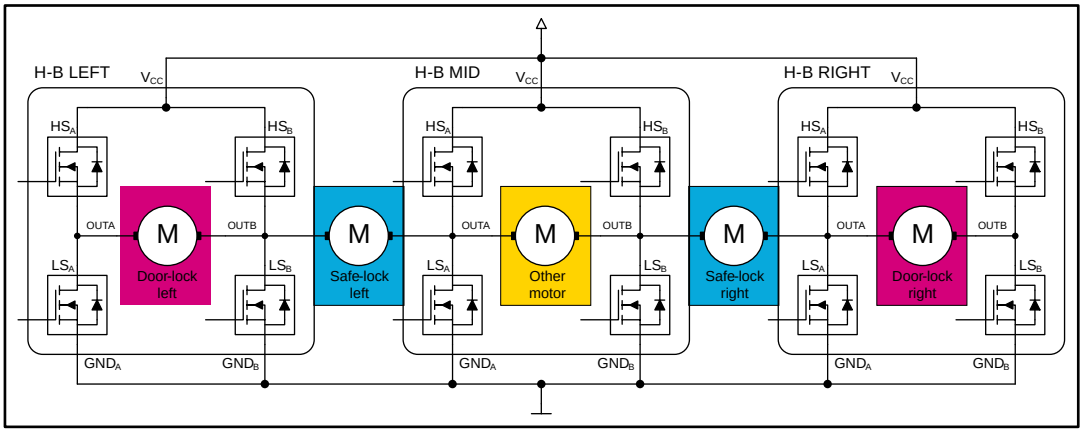
Technology	The same power supply network(VBAT + GND network)	Different supply networks(different VBAT or GND protection network)
Monolithic + Monolithic		
Monolithic + Hybrid		

6 Multi-motor configurations

In order to drive multiple loads (motors), it is possible to combine H-bridges in a cascaded configuration that require less H-bridges than the actual number of motors.

The locking system figured below illustrates how five motors can be driven in both directions by three full H-bridges.

Figure 75: Door lock system example



In the above example, every motor can be controlled independently through specific combinations of INA, INB and PWM on dedicated H-bridges. In this example, VNH7100BAS devices are considered (only SEL0 is available for MultiSense control).

In order to save time during motor transitions, multiple motors are activated at the same time; for example:

- Lock door-lock left, door-lock right
- Lock safe-lock left, safe-lock right
- Unlock safe-lock left, safe-lock right
- Unlock door-lock left, door-lock right
- “Other motor” control (remaining motors in high-Z)

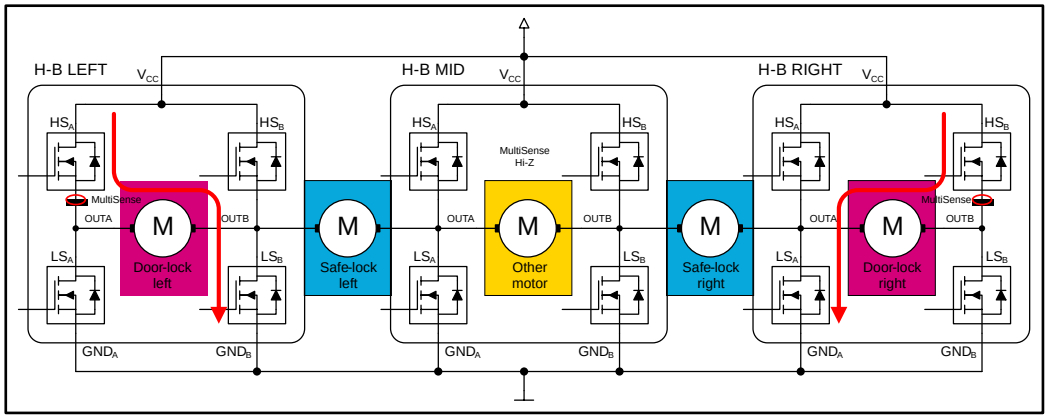
6.1 Motor activation sequences

1 **Locking door-lock left, door-lock right**:Applying signals INA=H, INB=L and PWM=H on H-B LEFT, door-lock left is activated. Simultaneously applying signals INA=L, INB=H and PWM=H on H-B RIGHT activates door-lock right as well.

Other motors are inactive as H-B MID is in high-Z mode (INA=INB=PWM=0).

Analog diagnostics applies current monitoring on HSA of H-B LEFT via SEL0=H and current monitoring on HSB of H-B RIGHT via SEL0=L.

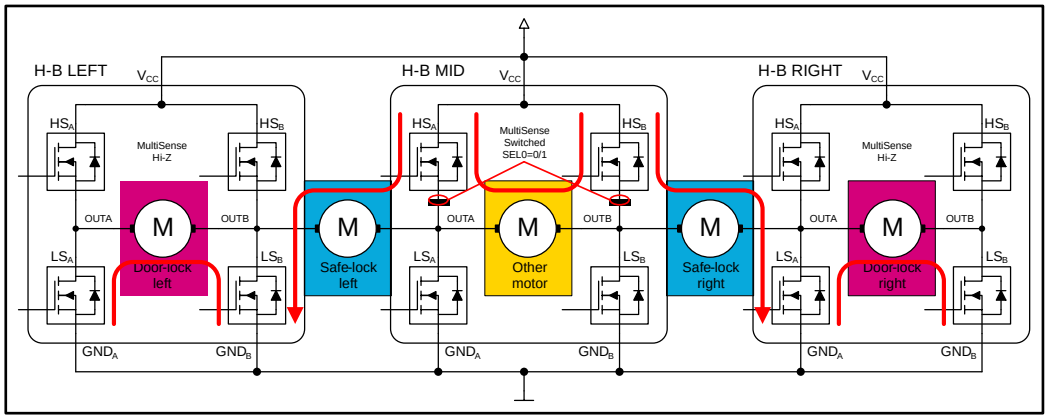
Figure 76: Locking door-lock left, door-lock right



2 **Locking safe-lock left, safe-lock right**:Applying signals INA=L, INB=L and PWM=H on H-B LEFT, door-lock left is braked to GND. Since H-B MID activates HSA by INA=H, safe-lock left is activated. Simultaneously applying signals INB=H of H-B MID and INA=L, INB=L and PWM=H on H-B RIGHT also activates safe-lock right. Door-lock right is braked to GND; central motor is braked to V_{CC}.

Alternate SEL0 between H and L during active state of both high sides (INA=INB=H) to monitor HSA and HSB of H-B MID. This is a new feature with respect to the previous VNH5xxx family of H-bridges.

Figure 77: Locking safe-lock left, safe-lock right

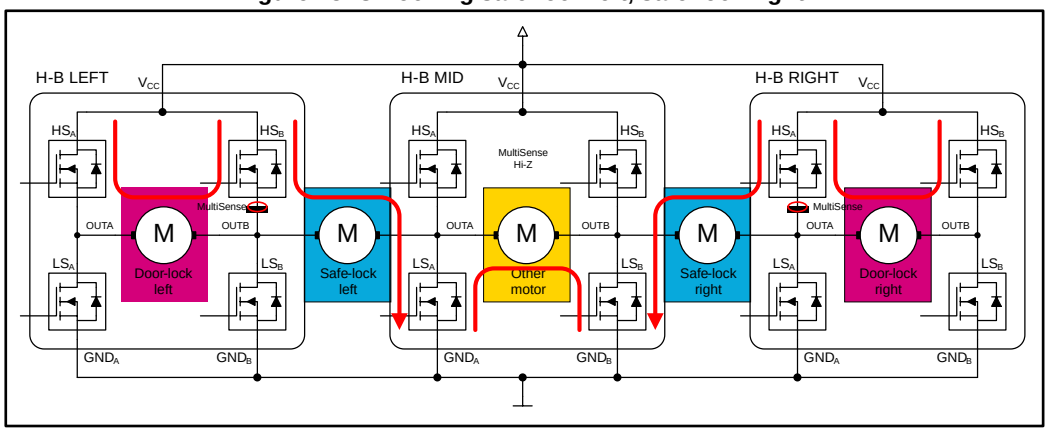


3 **Unlocking safe-lock left, safe-lock right**:Applying signals INA=H, INB=H and PWM=L on H-B LEFT, door-lock left is braked to V_{CC}. As H-B MID activates LSA by INA=L and PWM=H, safe-lock left is unlocked. Simultaneously applying signals INB=L (keeping PWM=H) of H-B MID and INA =H, INB=H and PWM=L on H-B RIGHT, safe-lock right is also unlocked. The central motor is braked to GND; door-lock right is braked to V_{CC}.

MultiSense on H-B LEFT monitors high side HSB via SEL0=L; on H-B RIGHT monitors high side HSA via SEL0=H.

Alternate SEL0 between L and H during active state of both high sides (INA=INB=H) to monitor HSA and HSB of H-B MID.

Figure 78: Unlocking safe-lock left, safe-lock right

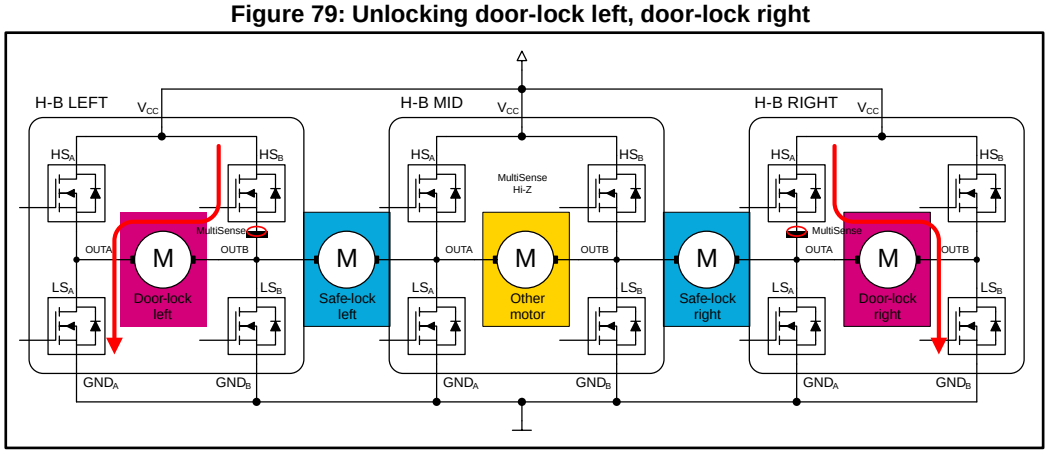


4 **Unlocking door-lock left, door-lock right**:Applying signals INA=L, INB=H and PWM=H on H-B LEFT, door-lock left is unlocked. Simultaneously applying signals INA=H, INB=L and PWM=H on H-B RIGHT, door-lock right is also activated.

The remaining motors are inactive as H-B MID is in high-Z mode (INA=INB=PWM=L).

Analog diagnostics applies current monitoring on HSB of H-B LEFT via SEL0=L and current monitoring on HSA of H-B RIGHT via SEL0=H.

Figure 79: Unlocking door-lock left, door-lock right

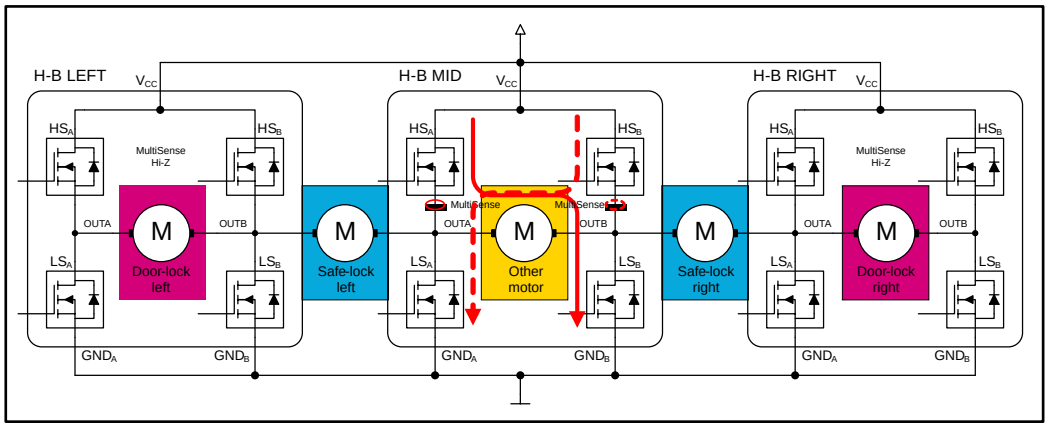


5 **Central motor separate control lock, unlock**:Only H-B MID is activated to control the central motor. H-B LEFT and H-B RIGHT are kept in High-Z mode by applying INA =INB=PWM=L.

To control the central motor in the direction of the solid red line, INA=H, INB=L and PWM=H. MultiSense monitors high side HSA via SEL0=H.

To control Central motor in the opposite direction of the dotted red line, INA=L INB=H and PWM=H are applied. MultiSense monitors high side HSB via SEL0=L.

Figure 80: Central motor control



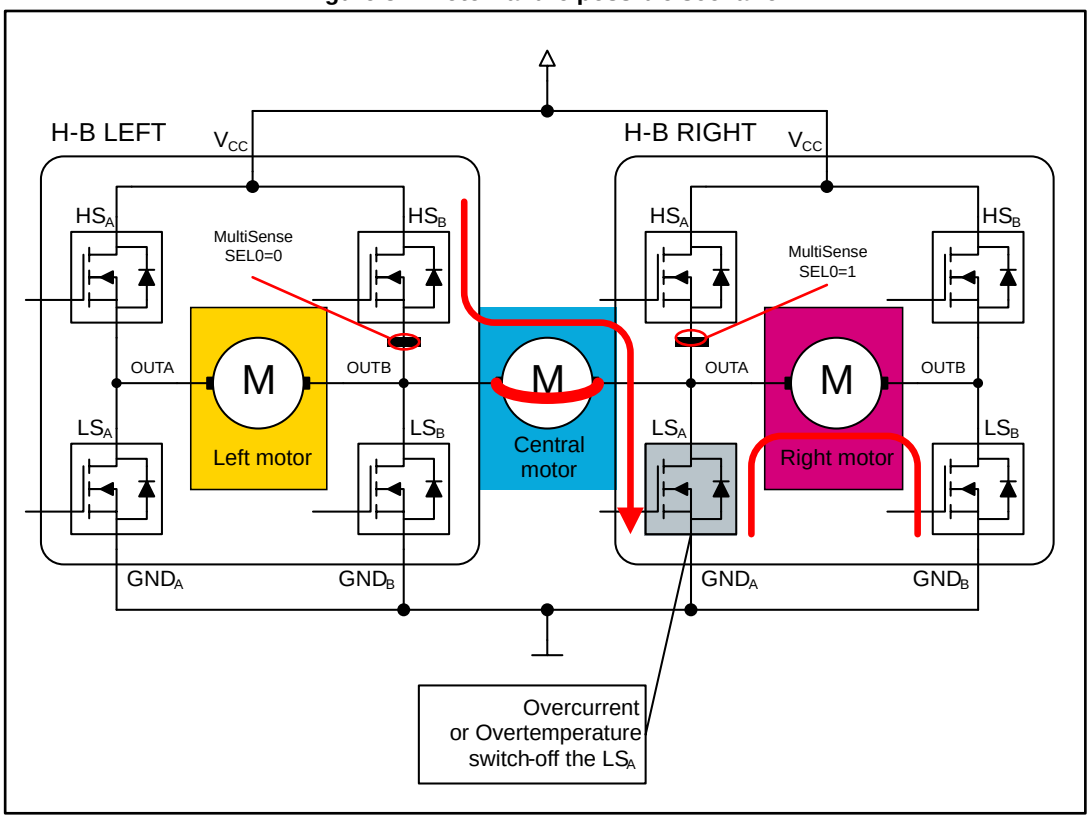
6.2 Preventing unwanted motor activation of the motor in brake state

In multi-motor configuration, an undesirable situation can occur where the motor is activated in the brake state. The following sequence shows the effect on a simplified setup.

The central motor is activated by INB=H (high side) on H-B LEFT and INA=INB=L and PWM=H (low side) on H-B RIGHT.

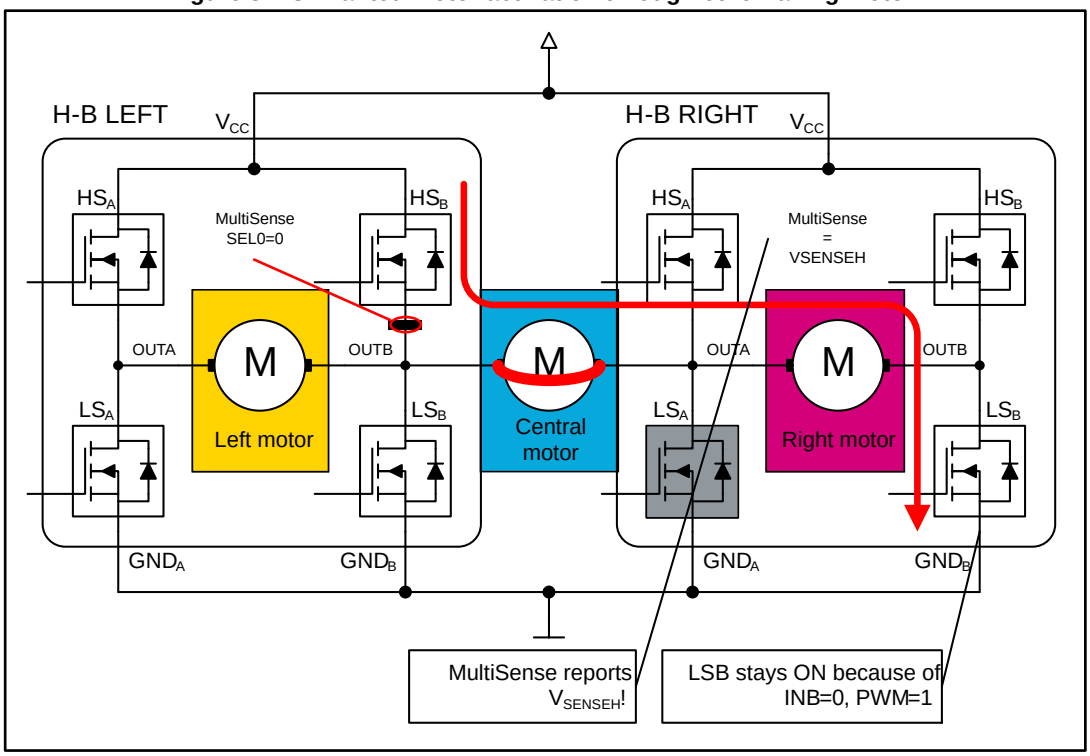
Right motor is braked to GND.

Figure 81: Motor failure possible scenario



If one of the low side protections on H-B RIGHT is activated (exceeding LS current shutdown threshold or overtemperature shutdown) by, for instance, a hard short-circuit between the terminals of the central motor, the low side on H-B RIGHT stays ON (because the PWM is high) and so the Right motor will be activated as it is in series with the Central motor.

Figure 82: Unwanted motor activation through other failing motor



To prevent the unwanted activation of the right motor:

1. Read V_{SENSE} with SEL0 =H on H-B RIGHT (checking if any failure occurs on the low side which is activated together with the high side of the H-B LEFT)
2. As soon as V_{SENSEH} is detected, set the PWM of the faulty bridge from high to low immediately.

This sequence will prevent any motion of the motor in standby.

7 Revision history

Table 26: Document revision history

Date	Version	Changes
03-Nov-2017	1	Initial release.

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